## EE5: Is an Open-source Hardware Revolution on the Horizon?

**Panelists:**
- Rob Aitken: Arm, San Jose, USA
- Elad Alon: UCB and Blue Cheetah Analog Design, Berkeley, USA
- Brucek Khailany: NVIDIA, Austin, USA
- Sailesh Kottapalli: Intel, Santa Clara, USA
- Shichin Ouyang: MediaTek, San Jose, USA
- David Patterson: UCB and Google, Berkeley and Mountain View, USA
- Davide Rossi: UNIBO, Bologna, Italy

**Moderator:**
- Denis Daly: Omni Design Technologies, Boston, USA

**Organizers:**
- Naveen Verma: Princeton University, Princeton, USA
- Tanay Karnik: Intel, Hillsboro, USA
- Kush Gulati: Omni Design Technologies, Milpitas, USA
- Sudip Shekhar: UBC, Vancouver, Canada
- Rabia Yazicigil: Boston University, Boston, USA
## Agenda

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<td>8:05-8:10</td>
<td>Panel Introduction</td>
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<td>Open Discussion</td>
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<td>Questions from Audience</td>
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<td>Short Debates with Voting</td>
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Questions for the Panelists? Please email isscc2020.ee5@gmail.com
Revolution: A forcible overthrow of a government or social order, in favor of a new system. A dramatic and wide-reaching change in the way something works or is organized or in people's ideas about it.
Open Source has Revolutionized the Software Industry
Software Companies Have Embraced the Open Source Movement

In 2018 Microsoft had >4500 employees actively pushing code to repositories on GitHub. Google and Red Hat had >2000 employees active on GitHub, pushing code to ~1,100 top repositories.
Fruits of the Revolution

• Allow companies/individuals to focus effort and money on differentiation rather than the commodities

• Faster execution with fewer people

• More sophisticated products

• Virtuous cycle which feeds itself
Is a similar Open-Source Hardware Revolution on the Horizon?

Let us focus on open-source circuit designs and EDA software for the semiconductor industry

Not focus on FABs, or system level open-source hardware (e.g. Open Compute Project)
What Would Be Impact of An Open-Source Hardware Revolution?

- Democratize IC development
- Overcome exponentially increasing cost of advanced nodes
- Enable more complex systems
- Encourage more entrepreneurs and smaller companies

... Source: IBS
Open-Source Hardware Ongoing Efforts

**Design Flows**

- CHISEL
- KiCad
- OpenROAD
- VPR
- BAG
  (Berkeley Analog Generator)

**Verification**

- Xyce
- Verilator
- POSH
- UPScale

**IP Cores & Instruction Sets**

- RISC-V
- CORE-V
- SweRV Core

**Organizations**

- CHIPS Alliance
- OpenHW

**Intel Joins CHIPS Alliance, Contributes Advanced Interface Bus, January 22, 2020**

Open DSA (Freescale, Xilinx, ...)

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Open Source Hardware: Roadblocks (and some questions)

- **Culture**
  - *Is the industry culture open source hardware back?*
  - *Why can’t Universities publicly release design databases?*
- **Entrrenched business models**
  - *How to encourage both large and small companies to embrace OSH and contribute to it?*
- **Insufficient scale**
  - *Is the industry large enough to get achieve OSH critical mass?*
- **Intellectual property**
  - *How to avoid patent lawsuits?*
- **Unclear business models**
  - *Does Open Source Hardware need a RedHat?*
Panelists

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San Jose, USA

Elad Alon  
UCB and Blue Cheetah Analog Design  
Berkeley, USA

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Bologna, Italy

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Avoiding the design graveyard

“I put it on GitHub” != Open Hardware

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Example Hardware IP Ecosystem

- Specs
- Governance
- User
- Implementation Effort
- Chips
- Design Effort
- Maintenance Effort

Openness measures:
- Type of governance
- Visibility into IP Pool
- Who can/does contribute
Open Source A/MS Hardware

Elad Alon

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Goals and Challenges

• Main potential benefit of open source is **re-use**
  • For A/MS specifically, you most likely won’t be able to put the actual circuits you built into the open source (PDK not open)

• Even if the PDK is available, is a repo with schematics, layout, and even testbenches really enough to enable reuse?
  • A/MS circuits are much more sensitive to environment / integration concerns – what happens when something goes wrong?

• What if everything works, but you want to add a customization, need the circuit in a different process, ... ?
Prognostication

• For open-source (A/MS) hardware reuse to succeed, we will need:
  (1) Organizations providing support and maintenance (a la RedHat)
  (2) A/MS designers to capture their methodologies rather than the results of them

• Open-source BAG framework can enable both (1) and (2)
  • Allows design procedure as well as layout strategy to be captured as process-portable executable generators
  • Open-sourced BAG-based generators have been used to produce instances in a wide variety of FinFET, bulk, and SOI processes
ISSCC 2020 PANEL: OPEN-SOURCE HARDWARE

Brucek Khailany, Director of Research - ASIC & VLSI
February 18, 2020
OPEN SOURCE HARDWARE: THE GOOD

Trend: Exciting progress in open-source digital IP, tools & flows!

Open-Source IP (some examples)

- RISC-V Cores: Rocketchip, BOOM, Ariane, etc...
- HLS LIBS
- MatchLib
- NVDLA

Open-Source Tools & Flows (some examples)

- VERILATOR
- Yosys
- CHISEL
- OpenROAD
- DREAMPlace

Value Propositions

Researchers: Improve research productivity, reproducible results

Commercial contributors: Develop SW/HW platforms connected to business goals

Commercial users: Leverage ecosystems

Value Propositions

Researchers: Improve research productivity, reproducible results

Commercial contributors: Enable collaborations with researchers, community

Commercial users: Can fill gaps in commercial tools, support customization

Position: Open source - great for creating extensible digital IP platforms, research IP & tools!
# OPEN SOURCE HARDWARE: THE BAD

## The Bad: Many Challenges Remain

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<th>Level of abstraction</th>
<th>Business models</th>
<th>Quality</th>
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<td>• Are user bases large enough to sustain open-source models?</td>
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OPEN SOURCE HARDWARE: THE BAD, ... AND THE UGLY

The Bad: Many Challenges Remain

Level of abstraction
• RTL works fine for digital
• Analog / mixed-signal is too process-dependent

Business models
• Are user bases large enough to sustain open-source models?
• Will new HW-specific business models need to be invented?

Quality
• Verification already dominates
• Only useful if open-source IP reduces verification effort

The Ugly: SoC Economics

Open source digital IP can lower the IP licensing cost of SoCs built from commodity IP, however:

• Most of the value in our industry is in large design teams building highly complex processors/SoCs
  • Customization and HW/SW platforms, not commodity IP, adds value
  • Open-source IP can have value here in making design teams more productive

• Design NRE costs other than IP licensing still dominate
  • Tapeout + productization NRE: tens of millions of $$
  • >100-person engineering team (Hardware + Software) * 2 years: >$50M
    • 10-50x that for really complex high-volume chips!
  • CAD tools + IT infrastructure: Millions of $$
  • Replacing proprietary IP license costs with open-source IP licenses will only reduce these costs by ~1%-20%

Position: Open source won’t change these economics much, so it won’t enable a revolution
Open Source in not the same for HW and SW...

- Broad success of HW requires good architecture abstraction.
  - Most of general purpose architectures are covered by intellectual property rights that need to be resolved
- There is a good opportunity for open source RTL with new architectures
  - Embedded controllers
  - Application specific appliances
  - IO controllers for Industry standard Ios
- Systems on Chip with advance packaging will enable rich mix and match
  - Open source HW does not need to address the full SoC
- HW is very different that SW
  - Higher cost barrier to functional correctness – inherently leads to licensing or services.
  - HW gets hardened to specific foundry and each requires very different circuit and layout optimizations.
Open Source Hardware (OSH)

- **Open Source** → a “development methodology”
- **Benefits**: Transparency/Lower-Cost/Customization…
- **Challenges** to deliver commercially successful **physical** end-products: “Cost justification” “Well-controlled process” “Sizeable qualified Community (higher technical barriers)”…
- **Workable model**: An organization supported by committed stakeholders, with sound business models for funding, and executed under well-defined regulation/supervision
- **Examples**: Open source ISA and IP (design source codes)
OSH – from an IC design house’s viewpoint

What we have seen:
• Exponentially increasing IC development & manufacturing cost
• Consolidation in IP/EDA/Foundry
• Demand for differentiation (i.e., customization)
• Time To Market (Lego-like HW)
• Resource/$$ Optimization (HW talent pool gap)
• More ISA & IP have been open (MIPS, ARM, etc...). Some failed, some WIP....

We embrace OSH with cautious optimism
Open Source Hardware

David Patterson
Google and UC Berkeley
# Need Free & Open Specification To Have Free & Open Source Designs

## Specifications

### Designs

- **Free & Open Spec (RISC-V)**
- **Licensable Spec (ARM)**
- **Closed Spec (x86)**

### Free & Open Designs

- “Open Source”

### Licensable Designs

- ~$5M + 4%

### Closed Designs

- ~$25M

## Products

- Based on Free & Open Licensed Closed
- Based on Licensed or Closed
- Based on Closed Designs
NRE for Custom chip (no processor)

- Today $10-$20 in NRE for production chip
- Academic paper with data from 2016*

NRE for Custom chip (simple processor)

- Today $10-$20 in NRE for production chip
- Industry source for 2019 data: “For a fixed function simple ASIC today, % distribution is OK, but for complex SOCs Labor and IP % would be much higher & mask would be smaller (even for 16 nm)”
The “PULP” Case

Academic project started in 2013, between University of Bologna and ETH Zürich

Research goal:
- Parallel Computing Platform for IoT Nodes
- PULP = Parallel Ultra Low Power

Open Source Approach:
- Start from a clean slate
- No forced to be compatible with legacy systems
- No dependencies with commercial IP
Lesson Learned + Perspectives

**PULP Open-Source Success**
- 25+ Companies
- 30+ Universities

**Why they like PULP**
- System Verilog (easily) Customizable Design
- Permissive Open Source License (Solderpad)
- Silicon proven IPs (25+ tape-outs)

**Areas of Improvement**
- Simple is Better (e.g. *PULPino*)
- Professional Verification
- Professional Documentation