PREAMBLE

The Session Overviews to follow serve to capture the context, highlights, and potential impact, of the papers to be presented in each Session at ISSCC 2015 in February in San Francisco.

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FOOTNOTE

- From ISSCC’s point of view, the phraseology included in the box below captures what we at ISSCC would like your readership to know about this, the 62nd appearance of ISSCC, on February 22nd to the 26th, 2015, in San Francisco.

This and other related topics will be discussed at length at ISSCC 2015, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 22-26, 2015, at the San Francisco Marriott Marquis Hotel.

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The material presented here is preliminary.
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INDICATORS – HISTORICAL TRENDS IN TECHNICAL THEMES

ANALOG SYSTEMS

ANALOG SUBCOMMITTEE

DATA CONVERTERS SUBCOMMITTEE
The efficient control, storage, and distribution of energy are worldwide challenges, and are increasingly important areas of analog circuit research. While the manipulation and storage of information is efficiently performed digitally, the conversion and storage of energy is fundamentally performed with analog systems. Therefore, the key technologies for power management are predominantly analog. For example, there is much interest in wireless power transmission for battery charging applications, ranging from mobile handsets to medical implants: increased performance in wireless power transmission is enabling more efficient power delivery over longer distances. There is also an explosion of technologies that allow energy to be collected from the environment via photovoltaic, piezoelectric, or thermoelectric transducers, with a trend toward the use of multiple sources at the same time. A significant focus here is on analog circuits that are able to harvest sub-microwatt power levels from multiple energy sources at tens of millivolts, to provide autonomy for remote sensors, or to supplement conventional battery supplies in mobile devices. To achieve this, the attendant analog circuits have to consume extremely low power, so that some energy is left over to charge a battery or supercapacitor. Similarly, the power consumption of analog instrumentation amplifiers, oscillators, and audio power amplifiers is being scaled down to meet the demands of these low-power systems. Fast power-up and -down is also desired from these circuits to permit high energy-efficiency during intermittent operation. Together, these technologies will lead to devices powered indefinitely from sustainable sources, opening the door to internet of things, ubiquitous sensing, environmental monitoring, and medical applications.

Analog circuits also serve as bridges between the digital world and the analog real world. Just like actual bridges, analog circuits are often bottlenecks and their design is critical to overall performance, efficiency, and robustness. Nevertheless, since digital circuits, such as microprocessors, drive the market, semiconductor technology has been optimized relentlessly over the past 40 years to reduce their size, cost, and power consumption. Analog circuitry has proven increasingly difficult to implement using these modern IC technologies. For example, as the size of transistors has decreased, the range of analog voltages they can handle as well as their analog performance have decreased, while the variation observed in the analog parameters has increased.

These aspects of semiconductor technology explain two key divergent trends in analog circuits. One trend is to forgo the latest digital IC manufacturing technologies, instead fabricating analog circuits in older technologies, which may be augmented to accommodate the high voltages demanded by increasing markets in medical, automotive, industrial, and high-efficiency lighting applications. Other applications dictate full integration of analog and digital circuits together in the most modern digital semiconductor processes, including FinFET and FDSOI technologies. For example, microprocessors with multiple cores can reduce their overall power consumption by dynamically scaling operating voltage and frequency in response to time-varying computational demands. For this purpose, DC-DC voltage converters can be embedded alongside the digital circuitry, driving research into the delivery of locally-regulated power supplies with increasing efficiency, decreasing die area, and increasing output power, but without requiring external components. These trends are captured by movement towards the top-right in the plot below with a concurrent increase of the output power level.
Comparison of Integrated Switched-Capacitor Power Converters from ISSCC papers showing Peak Efficiency vs Power Density and Output Power. Recent advances achieve much higher power density and output power without sacrificing efficiency (see the top right quadrant).
Data Converters – 2015 Trends

Subcommittee Chair: Boris Murmann, Stanford University, Stanford, CA

Data converters serve as key building blocks in virtually all electronic systems, and serve to bridge the analog physical world to the digital circuitry prevalent in modern integrated circuits. Key metrics such as linearity, bandwidth, and power efficiency continue to be the dominant drivers for innovation, as evidenced by the data converters presented at ISSCC 2015. Also, for the first time, we see a converter in 14nm FinFET technology. This design leverages the integration density of this technology to realize a process-voltage-temperature (PVT) tolerant Time-to-Digital Converter using $2^{14}$ delay elements.

Figure 1 below is a survey of ADC power efficiency expressed as power dissipated relative to the effective Nyquist rate ($P/f_{\text{Nyq}}$), and as a function of signal-to-noise and distortion ratio (SNDR). For low-to-medium-resolution converters, energy is primarily expended to quantize the signal and the overall efficiency of this operation is typically measured by the energy consumed per conversion and quantization step. The dashed trend-line represents a benchmark of 5fJ/conversion-step. Higher-resolution converters face the additional burden of overcoming circuit noise, necessitating a different benchmark proportional to the square of signal-to-noise ratio, represented by the solid line. Contributions at ISSCC 2015 are highlighted by the colored squares representing various converter architectures, and contributions from previous years are marked by smaller markers. Delta-Sigma, pipeline and SAR ADCs at various SNDR design points continue to push the limits of energy efficiency. (Note that a lower $P/f_{\text{Nyq}}$ metric represents a more efficient circuit on this chart.)

Figure 2 shows energy per conversion-step vs. the Nyquist sampling rate. This figure elucidates the difficulty of maintaining good efficiency at higher speeds of operation. Nevertheless, advances in circuit innovations embodied in leading-edge technologies have resulted in new benchmarks in energy efficiency across the entire spectrum of conversion rates.

Figure 3 plots achieved bandwidth as a function of SNDR. Sampling jitter or aperture errors make the combination of high resolution and high bandwidth a particularly difficult task. Nonetheless, in 2015, we see many examples achieving excellent results in this metric across a wide range of SNDR and bandwidths utilizing several different converter architectures.
Figure 1: ADC power efficiency ($P_f/s_{nyq}$) as a function of SNDR.

Figure 2: Energy per conversion-step vs. the Nyquist sampling rate.
Figure 3: Bandwidth vs. SNDR
INDICATORS – HISTORICAL TRENDS IN TECHNICAL THEMES
Communication Systems
RF Subcommittee - Wireless Subcommittee
Wireline Subcommittee
RF Subcommittee – 2015 Trends

Subcommittee Chair: Andreia Cathelin, STMicroelectronics, Crolles, France

Introduction
This year has shown increased innovation, integration, and technical maturity across the radio frequency (RF) bands from a few GHz to beyond 300GHz. This includes wireless communication which has made our world a smaller place by enabling us to share ideas and concerns regardless of our geographical location. This document outlines such emerging RF trends that will be covered at the 2015 ISSCC conference. Papers showcase some of the recent advances in RF transmitter and receiver building blocks, with an ongoing drive towards higher output power with better energy efficiency, lower noise and increasing levels of integration. This trend can be seen in all areas of RF design, from cellular and wireless sensors up to mm-Wave/THz sources.

Energy efficiency: There is an increasing demand for energy efficient and very small wireless device solutions for different applications such as IoT, wearable and wireless sensors. The trend is toward highly integrated low-power RF systems. Very low power techniques like receiver-based FLL, wake-up radio, extreme low-duty-cycle regimes and RF energy harvesting have been demonstrated this year.

RF Transmitters and Receivers: RF techniques for transceivers have made significant progress to enable energy and cost-efficient wireless communication systems. For cellular RF, a new class of PA is proposed for high linearity and low voltage stress. In addition, a silicon-based duplexer breaking the +70 dBm IIP3 barrier and a hybrid supply modulator that enhances the dynamic range of envelope-tracking (ET) are realized. For wideband radios spanning across a few GHz, an inductorless receiver with as low as 2dB NF and a Class-AB PA achieving near 30% PAE with >22 dBm P_{sat} are presented. It is observed that utilization of digitally-intensive PA design techniques and body bias in SOI process technology for mm-Wave building blocks have grown significantly. At the same time, the operating frequency bandwidth coverage is also broadened.

Power delivery: There is a continued trend in increasing the output power by means of power combining techniques with improved efficiency, trying to circumvent the low breakdown voltages of nanoscale CMOS. Implementing RF PAs for 3G/4G standards are in particular challenging due to the amplification of signals with high peak-to-average-ratio. The trend is to reach a high degree of linearity with novel linearization techniques using active feedback without pre-distortion for LTE signals. Wideband power amplifiers are further needed to reach higher data-rates. This demands output matching networks that can provide an optimum load impedance over at a larger fractional RF bandwidth. The conference will show a first implementation of PAs supporting modulations such as 256QAM with a PAE reaching 28% over an octave of bandwidth. There is also a continued interest in improving envelope tracking by modulating the supply voltage of power amplifiers to further increase the battery lifetime in mobile LTE applications. Techniques that can enhance the dynamic range of envelope tracking with adaptive control of both the PA supply voltage and the bias currents achieve record PAE performance with lowest power dissipation.

New PA design methodologies presented at this year’s conference indicate that future PA architectures may have to combine multiple techniques to further improve the performance of both CMOS and SiGe amplifiers. For instance, different modes of operation such as Class-G are combined with Doherty to enhance the efficiency without mitigating RF bandwidth at around 3.7GHz. Such approaches achieve substantial efficiency enhancements at power back-off. The combination of multiple design techniques also shows first PA implementations at mm-Wave frequencies that have the potential to soon bridge the 1-Watt barrier with good PAE efficiency. This is enabled with novel dynamic load-line modulation techniques using variable impedance transmission lines. A digital Class-E architecture for instance has shown up to 29dBm at 46GHz. Another avenue towards efficient linear power amplification is to leverage advanced technologies such as 28nm CMOS FD-SOI using body biasing. This extra biasing flexibility allows the combination of parallel transistors to operate in different classes by adjusting their threshold voltage individually. First 60GHz WiGig implementations reach 21% PAE at 18.2dBm at P_{1dB}. The trend to simultaneously optimize power and efficiency is indicated in Figure 1 for mm-Wave PAs implemented in CMOS.
**Frequency generation**: Frequency generation circuits are ubiquitous building blocks. The race to reduce phase noise, chip area, and power consumption for synthesizers and VCOs is never ending. Utilizing circuit techniques to suppress the impact of flicker noise on phase noise, as well as employing a capacitance scaling technique to decrease PLL filter size are becoming popular. Very low phase noise is achieved and the VCO Figure-of-Merit (FOM) has reached a new record. The trend towards better performing VCOs is shown in Figure 2, where the VCOs FOM versus oscillation frequency is continuously improving. With an attempt to remove the bulky quartz crystal, a highly stable thin-film-based reference frequency generator is reported, attaining a stability of ±3 ppm from 0 to 90°C. At the THz frontier a phase-locked-based transmitter array has been demonstrated with sufficiently high output power beyond 300GHz, enabling numerous practical terahertz applications that require coherent radiation. The output power versus frequency for the trend in mm-Wave and sub-mm-Wave sources is given in Figure 3.

![Figure 1: PAE (%) vs. output power for recent submicron mm-Wave CMOS PAs](image-url)
Figure 2: Oscillator phase-noise FOM at 20MHz offset frequency versus oscillation frequency

Figure 3: Output power versus frequency for mm-Wave and sub-mm-Wave sources
Wireless – 2015 Trends

Subcommittee Chair: Aarno Pärssinen, Broadcom, Finland

The vision for Wireless Sensor Networks (WSN) and the Internet of Things (IoT) continues towards more mature integration strategy. The commercial landscape is focusing these technologies towards Bluetooth Low Energy (BLE), while still maintaining flexibility by having the ability to function as multimode radios. This conference features some of the first published comprehensively integrated wireless sensor nodes, including MCU, power management, digital baseband modem and wireless transceivers. The key aspect and challenge of these wireless radios continues to be the ability to function at the lowest power possible, while being robust to the presence of other wireless signals. A prominent use case of most of the Wireless Sensor Network nodes is the transmit operation. Therefore, transmit power efficiency is a key metric that determines the evolution of these sensor nodes in terms of power consumption. A development trend in wireless sensor nodes for transmit power efficiency is shown in Figure 1. Similarly, Figure 2 shows that the receiver sensitivity as a function of power consumption in complete SoC’s has almost reached the levels of a stand-alone wireless transceiver.

While exponential increase in data rate of cellular devices is still ongoing, a different vector that is also important is the level of integration in these SoC’s. The trend in these integration strategies is shown in Figure 3, where the progress has been to transition from BiCMOS to CMOS to baseband modem integration and finally this year to 3G power amplifier integration on the same die. PA integration as well as elimination of the front-end SAW filter, as is shown in another paper in this year’s conference significantly advance the trend of BOM reduction and simplification of the overall system complexity.
Figure 1: Ultra-Low Power 2.4GHz Wireless Transmit Efficiency Trends. Arrow shows desired trends. All symbols except red squares represent ISSCC papers. The ISSCC 2015 paper numbers are indicated next to the red circles.

Figure 2: Ultra-Low-Power 2.4GHz Wireless Receiver Sensitivity Trends. Sensitivity is normalized to bandwidth at 2.4GHz carrier. Lines represent constant performance. The triangle is transceiver only and red dots and squares represent full SOCs.
Figure 3: Integration Trends in Cellular Wireless
Over the past decade, wireline I/O has been instrumental in enabling the incredible scaling of computer systems, ranging from handheld electronics to supercomputers. During this time, aggregate I/O bandwidth requirements have increased at a rate of approximately 2 to 3× every 2 years. Demand for bandwidth is driven by applications including memory, graphics, chip-to-chip fabric, backplane, rack-to-rack, and LAN. In part, this increase in bandwidth is enabled by expanding the number of I/O pins per component. As a result, I/O circuitry consumes an increasing amount of area and power on today’s chips. Increasing bandwidth has also been enabled by rapidly accelerating the per-pin data rate. Figure 1 shows that per-pin data rate has approximately doubled every four years across a variety of diverse I/O standards ranging from DDR to graphics to high-speed Ethernet. Figure 2 shows that the data rates for published transceivers have kept pace with these standards, enabled in part by process technology scaling. However, continuing along this rather amazing trend for I/O scaling will require more than just transistor scaling. Significant advances in both energy efficiency and signal integrity must be made to enable the next generation of low-power and high-performance computing systems.

Energy Efficiency and Interconnect Density:
Power consumption for I/O circuits is a first-order design constraint for systems ranging from cell phones to servers. As the pin count and per-pin data rate for I/Os has increased on a die, so has the percentage of total power that they consume. Technology scaling enables increased clock and data rates and offers some energy efficiency improvement, especially for digital components. Many recent advances have reduced power for high-speed link components through circuit innovation, including low-power RX equalization (DFE, CTLE), CMOS and resonant clocking, low-swing voltage-mode transmitters and links with low-latency power-saving states. Papers at ISSCC this year include the lowest reported long-range 25Gb/s transceiver achieving 11pJ/b [3.1], and a scaled-supply link that consumes only 0.29pJ/b by operating at 0.45V [3.8].

Simply increasing per-pin baseband data rates with existing circuit architectures and channels is not always a viable path given fixed system power limits. Figure 3 plots the energy efficiency (expressed in mW/Gb/s, which is equivalent to pJ/b) as a function of channel loss for recently reported transceivers. Looking at the most aggressive designs, the data indicates that the scaling factor between link power and signaling loss slightly less than unity—in particular, that 30dB in channel loss corresponds to a roughly 10× increase in pJ/b. In this year’s ISSCC, a fast 20ns on/off link is demonstrated that save power by dynamically gating the transceiver [3.7]. A multi-tone transceiver is also demonstrated that consumes only 1pJ/b by shaping the data spectrum to match the channel discontinuities [10.3].

Electrical Interconnect:
Some types of channels, especially those related to medium-distance electrical I/O like server backplanes, must support high data rates over high loss channels. For these links, the key to scaling has been improvements in equalization and clock/data recovery. Recent high-speed transceivers use a combination of fully adaptive equalization methods, including TX FIR, RX CTLE, DFE, as well as RX FIR and/or IIR FFEs. As a result, recent transceivers achieve data-rates above 20Gb/s with channels that have 30dB or more loss. This year’s ISSCC includes a paper that describes 35-to-33Gb/s transceivers operating over up to 40dB loss channel [3.1, 3.2, 3.3], and two transmitters that support both NRZ and PAM4 signaling up to 40Gb/s [3.4, 3.5].

Optical Interconnect:
As the bandwidth demand has accelerated for traditionally electrical wireline interconnects, optics has become an increasingly attractive alternative for interconnects within computing systems. Optical communications have clear benefits for high-speed and long-distance interconnects. Relative to electrical interconnects optics provides lower channel loss. Circuit design and packaging techniques that have traditionally been used for electrical wireline are being adapted to enable integrated optical with extremely low power. This has resulted in rapid progress in optical ICs for Ethernet, backplane and chip-to-chip optical communication. At ISSCC this year, several 20-to-25Gb/s optical transceivers and components will be presented with a focus on power efficiency and optics integration. One paper demonstrates a full transceiver that uses WDM to send multiple 20Gb/s data streams on the same optical fiber [22.5].
Concluding Remarks:
Continuing to aggressively scale I/O bandwidth is both essential for the industry and extremely challenging. Innovations that provide higher performance and lower power will continue to be made in order to sustain this trend. Advances in circuit architecture, interconnect topologies, and transistor scaling are together changing how I/O will be done over the next decade. The most exciting and most promising of these emerging technologies for wireline I/O will be highlighted at ISSCC 2015.

Figure 1: Per-pin data rate vs. Year for a variety of common I/O standards.

Figure 2: Data-rate vs. process node and year.
Figure 3: Transceiver power efficiency vs. channel loss.
Energy Efficient Digital – 2015 Trends

Subcommittee Chair: Stephen Kosonocky, AMD, Fort Collins, CO

Demand for ubiquitous mobile functionality to achieve enhanced productivity, a better social-networking experience, and improved multimedia quality, continues to drive innovation in systems-on-chip (SoC), which are also constrained by a need to improve battery life and reduce cost. While the performance of embedded application processors has increased to meet the rising demands of general-purpose computing, dedicated multimedia accelerators are necessary to provide dramatic improvements in performance and energy efficiency of emerging applications. At the other side of the spectrum, sensor nodes for the Internet-of-Things (IoT) require low energy wireless and sufficient computational capabilities.

Technology scaling continues to be exploited to deliver designs capable of operating at lower voltages, resulting in reduced energy per operation, as well as lowering the area required to implement specific functions. Processors unveiled at ISSCC 2015 are built in a variety of technology nodes, with best-in-class results accomplished with higher integration, and improved performance-per-watt. These are demonstrated in various process nodes ranging from 130nm to 14nm FinFET, as well as low power FD-SOI CMOS technologies.

Energy-efficiency techniques for microcontrollers
Semiconductor chips used for the Internet-of-things (IoT) and other embedded application areas demand energy-efficient active operation, while also requiring ultra-low power state retention to enable event-driven operation with fast wake-up. Typically an energy-efficient microcontroller unit (MCU) is used as the main processing element for local processing and system control these applications. Over time, the microcontroller energy efficiency, shown in Figure 1, has continuously improved through a combination of technology and design techniques, as illustrated in Figure 2.

![Fig. 1 Energy-efficiency evolution in commercial microcontrollers.](image)

Low-power silicon technology with embedded non-volatile memory enables more power-effective full state retention, while reduced supply and feature sizes cut active energy consumption. At the circuit level, the chase for energy efficiency drives innovation on adaptive and near-threshold operation, enabling further supply voltage reduction. A complete Cortex M0+ ARM core now can scale down to 850nW active power at 250mV, yet can also operate at 66MHz at 0.9V supply. Retention power is tackled by improved leakage reduction techniques, shadow latches in logic, and optimized SRAM design.
At the architecture level, smaller and smaller microcontrollers are enhanced with advanced integrated power management and variation mitigation. Dedicated accelerators are selectively powered up to improve the efficiency of important compute kernels, such as AES cryptography. The latest state-of-the-art focuses on dynamic scalability and efficient always-on peripherals, such as real time clocks and wake-up sensors, enabling nano-Watt operation from integrated energy harvesters.

**Rising complexity and functionality for application processors**

Figure 3 illustrates the major trends of smart phones and tablets relevant to energy-efficient digital circuits. In the late 1990s, a GSM phone contained a simple RISC processor running at 26MHz, supporting a primitive user interface. After a steady increase in clock frequency to roughly 300MHz in the early 2000s, there was a sudden spurt towards 1 GHz and beyond. Moreover, following trends in laptops and desktops, processor architectures have become much more advanced, and smart phones incorporate four and even eight-core 64b processors, now running up to 2.5GHz. Heterogeneity was recently adopted to further improve power efficiency. Overall, energy efficiency has become the main challenge in designing application processors, graphics processors, media processors (video, image, audio), and modems (cellular, WLAN, GPS, Bluetooth) for mobile platforms. For video and image processing, the trend has been towards dedicated, optimized hardware solutions. Some examples of new areas where dedicated processors are particularly needed include gesture-based user interfaces, recognition processors, augmented reality and computational imaging. For all digital circuits, the limited power budget leads to more fine-grained power management, various forms of adaptive voltage-frequency scaling, variable device threshold and biasing schemes, and elaborate thermal management strategies.

Figure 4 shows the evolution of bitrates for wired and wireless links over time. Interestingly, cellular links, wireless LAN, as well as short links show a consistent 10× increase in data rate every five years, with no sign of abating. With essentially constant power and thermal budgets, energy efficiency has become a central theme when designing digital circuits for mobile baseband processing. With benefits from pure CMOS scaling flattening, alternative approaches to improve energy efficiency and system throughputs are pursued, such as new standards, smarter algorithms, more efficient digital signal processors, highly-optimized accelerators, optimized hardware-software partitioning, power management techniques, as well as inter-system aggregation and heterogeneous networks.
Fig. 3 Application processor trends in smart phones.

Fig. 4 Wireless and wired datarates over time.
High-Performance Digital – 2015 Trends

Subcommittee Chair: Stefan Rusu, Intel, Santa Clara, CA

The relentless march of process technology brings more integration and energy-efficient performance to mainframes, enterprise and cloud servers. ISSCC 2015 features IBM’s high-frequency 8-core, 16-thread System z mainframe processor in 22nm SOI with 64MB of eDRAM L3 cache and 4MB/core eDRAM L2 cache. The SPARC M7 processor from Oracle implements 32 S4 cores, a 1.6TB/s bandwidth 64MB L3 Cache and a 0.5TB/s data bandwidth on-chip network (OCN) to deliver more than 3.0x throughput compared to its predecessor. 280 SerDes lanes support up to 18Gb/s line rate and 1TB/s total bandwidth. Intel’s next generation Xeon processor supports 18 dual-threaded 64b Haswell cores, 45MB L3 cache, 4 DDR4-2133MHz memory channels, 40 8GT/s PCIe lanes, and 60 9.6GT/s QPI lanes. It has 5.56B transistors in Intel’s 22nm tri-gate HKMG CMOS and achieves a 33% performance boost over previous generations.

The chip complexity chart below shows the trend in transistor integration on a single chip over the past two decades. While the 1 billion transistor integration threshold was achieved some years ago, we now commonly see processors incorporating more than 5B transistors on a die.
The maximum core clock frequency seems to have saturated in the range of 5-6GHz, primarily limited by thermal considerations. The nominal operating frequency of the power-limited processors this year is around 3.5GHz. Core counts per die are typically above 10, with increases appearing to slow in recent years. Cache size growth continues, with modern chips incorporating tens of MB on-die.
The trend towards digital phase-locked loops (PLL) and delay locked loops (DLL) to better exploit nanometer feature size scaling, and reduce power and area continues. Through use of highly innovative architectural and circuit design techniques, the features of these digital PLLs and DLLs have improved significantly over the recent past. Another new trend evident this year is towards fully digital PLLs being synthesizable and operated with non-LC oscillators. The diagram below shows the jitter performance vs. energy cost for PLLs and multiplying DLLs (MDLL).
Overall, digital processors continue to grow in complexity, core count and cache integration (see figures above). We observe that traditionally analog building blocks are being implemented using digital techniques to cope with variability and ease scaling to finer geometries.
MEMORY – 2015 Trends

Subcommittee Chair: Joo Sun Choi, Samsung Electronics, Hwasung, Korea

Mobile products are everyone’s companion and need to store and process ever increasing amounts of data. Progress is only possible by constant improvements in area, power and performance of volatile and non-volatile memories. FinFET technology is now mainstream for embedded SRAM and DRAM, and has facilitated continued scaling. Improvements in DRAM data rates support the increasing demands of greater data volumes. NAND Flash memories have moved from 2b/cell to 3b/cell and 3D multi-layer designs are now typical. Embedded Flash, which is essential to IoT and wearable applications, has moved to 28nm. STT-MRAM is the most mature of the emerging memories, although ReRAM is quickly catching up.

Some current state-of-the-art papers from ISSCC 2015 include:

- Two 14nm SRAM bitcells; 0.0500 m² (HDC) and 0.0588 m² (LVC) capable of achieving 1.5GHz operation at 0.6V
- A 14nm FinFET SOI eDRAM with a cell size of 0.01747µm² and 1ns access time
- 128Gb 3 b/cell 32 stacked WL layer 3D NAND Flash running at 1Gb/s I/O rate
- A low power 64Gb 2b/cell NAND flash manufactured in 15nm technology
- A 1.1V 10Gb/s/pin transceiver for DRAM interface suitable for use beyond LPDDR4
- A high-speed 1Mb STT-MRAM using 2T2MTJ cells achieves 3.3ns access time and a sub-20nm technology node
- A 28nm embedded SG_MONOS FLASH developed for automotive applications.

SRAM

Consumer and computing products in 2015, from smart watches to the cloud, depend on low-power and high-performance embedded SRAM. Challenges for SRAM include VMIN, leakage and dynamic power reduction. Last year saw the first introduction of 14nm/16nm technology. This year a 14nm SRAM using 2nd generation FinFET technology discloses the smallest SRAM bitcell ever reported at just 0.050µm². As the transistor feature size advances further below 20nm, device variation has made it very difficult to shrink the bit cell size at the desired 50% rate while maintaining or lowering VMIN between generations. Introduction of high-k metal-gate (45nm) and FinFET or fully-depleted SOI transistors (22nm) reduces the VTH mismatch and have enabled further device scaling. Design solutions such as read/write assist circuitry and variation-tolerant sensing schemes have been used to improve SRAM VMIN performance starting at 32nm and are now ubiquitous in high-density SRAM designs at 14/16nm. Dual-rail SRAM design emerges as an effective solution to enable dynamic voltage-frequency scaling (DVFS) by decoupling logic supply rails from SRAM arrays and thus allowing much wider operating window. The use of assist circuit techniques, FinFET transistors and dual-rail architectures is expected to extend the viability of using the high-density 6T SRAM bitcell beyond 14nm. It is important for SRAM to reduce both leakage and dynamic power, keeping products within the same power envelope at the next technology node. Last year we heard about the first FinFET based eDRAM at 22nm. This year a 14nm FinFET based eDRAM is discussed. eDRAM continues to show itself as a desirable way to provide memory scaling in high-performance CPU designs. Figure 1 shows the bit cell and VDD scaling trend of SRAM from major semiconductor manufacturers.
In order to reduce the bandwidth gap between main memory and processor performance, DRAM data-rates continue to increase at the memory interface with schemes such as DDR(x), LPDDR(x) and GDDR(x), as shown in Figure 1 – Bit Cell and $V_{DD}$ scaling trend of SRAM.
Figure 2. Currently, DDR4 and GDDR5 memory I/Os operate around 3Gb/s/pin and 7Gb/s/pin, respectively, which represent aggregate rates of 6GB/s and 28GB/s, respectively. A digital DLL with hybrid DCC using a 2-step duty-error extraction and 180° phase aligner for 2.67Gb/s/pin 16Gb DDR4 SDRAM with TSV’s is covered. Last year LPDDR4 SDRAM was introduced at 3.2Gbps/pin at 1.0V. This year, an interface suitable for use beyond LPDDR4 operating at 10Gb/s is demonstrated.
Figure 2 - DRAM Data Bandwidth Trends
NON-VOLATILE MEMORIES

In the past decade significant investment has been put into the emerging memories field to find an alternative to floating-gate based non-volatile memory. The emerging NVMs, such as phase-change memory (PRAM), ferroelectric RAM (FeRAM), magnetic spin-torque-transfer (STT-MRAM), and resistive memory (ReRAM), are showing potential to achieve high cycling capability and lower power per bit in read/write operations. Figure 3 highlights how 3b/cell (TLC) NAND Flash write throughput continues to improve and even though Figure 4 shows no increase in NAND Flash density over last year, these devices are built with finer dimensions or more sophisticated 3-dimensional vertical bit cells.

Figure 3 - Read/Write Bandwidth Comparison of Nonvolatile Memories
NAND FLASH MEMORY

NAND Flash memory continues to advance towards higher density and lower power, resulting in low-cost storage solutions that are replacing traditional hard-disk storage with solid-state disks (SSDs). SSDs with typical storage density of 240GB have become the mainstream. Despite the growing difficulties to further scale down planar cell technology, the latest 2D NAND Flash technology is scaled down to 15nm, achieving a low power 1.8V 64Gb device occupying only 75mm². It will be very interesting to see how far planar NANDs go down the scaling path. This year, 3D NAND is extended to 3b/cell and 32 stacked wordline (WL) layers, to satisfy the ever-growing demand for increased density requirements and lower manufacturing cost. As IoT becomes more of a reality, embedded Flash becomes a critical technology. This year a 28nm SG-MONOS embedded Flash for an automotive application is discussed. Figure 5 shows the observed trend in NAND Flash capacities presented at ISSCC over the past 20 years.
Figure 5 - NAND Flash Memory Trends

- 1 bit/cell (SLC)
- 2 bit/cell (MLC)
- 3 bit/cell (TLC)
- 4 bit/cell (16LC)

x 1.56 / year
INDICATORS – HISTORICAL TRENDS IN TECHNICAL THEMES

Innovative Topics

Imagers, MEMS, Medical Devices & Displays Subcommittee
Technology Directions Subcommittee
The CMOS-image-sensor business is one of the fastest-growing segments of the semiconductor industry. Key applications include cellphone cameras, digital still cameras, camcorders, security cameras, automotive cameras, digital-video cameras, wearable devices, and gaming.

The resolution and miniaturization races are ongoing but slowing down, and while the performance requirements stay constant, pixel size continues to scale down (see Figure 1). Images of over 40M pixels are commercially available, and sensors for large TV format (8K) have been reported. A column-parallel approach based on pipelined and multiple-sampling implementations has become standard for low-power, high-speed, low-noise camera and video applications. Backside illumination is now a mainstream technology for mobile imaging. Wafer stacking of the image array on a CMOS image signal processor is becoming more common.

The importance of digital signal processing technology in cameras continues to grow in order to mitigate sensor imperfections and noise, and to compensate for optical limitations. The level of sensor computation is increasing to thousands of operations-per-pixel, requiring high-performance and low-power digital signal processing solutions.

High Dynamic Range (HDR) is now well established in low-cost consumer imaging. While HDR combines multiple distinct images, new work is progressing with specialized architectures to extend the dynamic range in single exposures, and thus avoid movement artifacts.

As well, global shutters are being introduced to avoid movement artifacts. For precision scientific, medical applications, and consumer products, we now employ single-photon avalanche diode (SPAD) imager arrays. Deep-submicron CMOS SPADs will meet the requirements for high resolution, high accuracy time-to-digital converters (TDCs), and small-pitch imagers with better fill factor. Wafer stacking of the SPAD array on a CMOS image signal processor is an emerging trend.

The market share of CCD imagers continues to shrink and they are now relegated to minor applications. Top-end broadcast and top-end digital cameras have moved from CCD to CMOS sensors (see Figure 1).
Figure 1: Pixel size trends

Figure 2: Image sensor performance trends: sensitivity, full-well capacity and conversion gain vs. pixel size.
MEMS inertial sensors (accelerometer and gyroscopes) are key components used in a large variety of consumer products, where ultra-low power consumption is a key requirement. For automotive applications, reduced vibration sensitivity and high precision are additional requirements.

CMOS temperature sensors continue to improve, with new circuit techniques increasing accuracy and supporting wider applications. Strides in low-power architectures continue to eclipse previous results with record-setting efficiency that support battery-operated and mobile applications. Pure digital implementations are often used in thermal monitoring for large SoCs, which is an important application where small sensor area is a key feature.

Current sensors are becoming more integrated and precise. These devices detect the magnetic field around a wire or trace carrying a current, and they are used for instance in electrical motor drives, solar power, and battery charge applications.

Capacitive-to-digital converters are essential sensor interface components, where new circuit technologies result in increased accuracy, smaller die size, and reduced power consumption. Digital-centric implementations enable these improvements to be maintained in more advanced processes.

MEMS pressure sensors are getting smaller, and fully integrated systems have been reported.
There is an ever-increasing demand for higher-throughput life-science tools, e.g., cellular and molecular assays, coming from the field of precision and personalized medicine. Electronic platforms for genomics, proteomics, and cellular assays bring improved accuracy and throughput. For example, increased sensitivity has been successfully exploited for detection of chemical reactions through physical means, e.g., pH, charge, or impedance changes, in DNA sequencing.

For improved capability and quality, medical ultrasound is moving toward 3D imaging with large arrays. As these arrays increase in size, the number of connections to the front-end processing circuitry, and the amount of required signal processing are becoming bottlenecks. To resolve this congestion, MEMS transducers and CMOS technology increasingly allow transducer arrays and their signal processors to be mounted together.

Smart wearable sensors for medical applications will support continuous remote monitoring with data transmission to centralized analysis systems. These sensors will adapt their algorithms to match a specific user’s vital signs. Potentially, closed-loop control will allow therapy to be applied directly, for instance to suppress seizures or arrhythmias.

Medical imaging is an important field with a growing number of applications. One such example is positron emission tomography (PET), where solid-state implementations allow PET scanning to be carried out simultaneously with magnetic resonance imaging (MRI), which opens up new and improved cancer diagnostic methods. Another example is wide-field microscopy imaging, where higher resolution and shorter time gating are enabled by smaller pixel pitch, and faster detectors, respectively.
Touch- and gesture-sensing systems for large displays are in development. These will require extensions of capacitive-sensing technology beyond the present state of the art. Applications will require sensing hand gestures at a distance (30cm), and high-resolution touch for writing recognition. Hovering touch systems, and active as well as passive pen input systems (styluses) are emerging trends. Touch sensors simultaneously detecting position and pressure have been reported.

LCD panels with integrated touch sensing are being driven toward thinner and lower-cost single-chip solutions. Robust circuit technology that is immune to display-driver noise is a key design factor.

Higher-resolution and higher-definition displays are being developed for mobile applications. Displays with more than 500 pixels-per-inch (ppi) are now in production, for 6-inch and smaller displays. While low-temperature polysilicon (LTPS) technology seems to be superior to amorphous-silicon (a-Si), traditional a-Si TFT and oxide TFT technologies supported by compensating driver systems are being prepared to compete.

Plastic organic light-emitting diodes (OLEDs) are entering into commercial production for curved smartphones. These will give improved user experiences, being very thin, light, and unbreakable. They are also expected to find applications in wearable displays.
Technology Directions – 2015 Trends
“Innovative Systems”

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This year at ISSCC 2015 the theme is “SILICON SYSTEMS — SMALL CHIPS for BIG DATA”. System considerations are extremely important for circuit engineers. The system designer defines the performance parameters such as power, bandwidth, SNR or QoS, etc. that hardware has to comply to. The system designer also helps to jointly optimize all the building blocks of the entire system. The next level of innovation will come from the mutual understanding of how all parts of the system work together so that the design team can optimize across multiple layers. For this reason, ISSCC’s Technology Directions subcommittee is highlighting system aspects by providing two sessions that focus on innovative systems. These sessions will present papers from two types of systems that will continue to drive future innovations: Session 21 is on “Innovative Personalized Biomedical Systems” and Session 24 showcases “Secure, Efficient Circuits for IoT”.

Innovative Biomedical Systems
A breakthrough concept in biomedical electronics has been the development of "anytime and anywhere" human monitoring systems using wearable/implantable devices. It will enable improvements of the quality of life, such as self-health checks, remote medical examination, and constant monitoring for acute diseases.

Key technologies for such systems include:
(1) Small footprint devices and flexible electronics to enhance the comfort of wearable devices,
(2) High accuracy and low-power monitoring devices,
(3) Low-power communication systems for wireless operation.

To develop devices with a small footprint, highly integrated biomedical SoCs capable of sensor detection, diagnosis and wireless communication have been developed. Progress in the development of 3D-integrated electrodes and sensors with MEMS has also contributed to reduce the footprint. To monitor weak vital signs, such as electrocardiogram (ECG) and electroencephalogram (EEG), with a high degree of accuracy, there is clear progress in variation correction methodologies and techniques to compensate for artifacts due to the subject’s movements. Furthermore, state-of-the-art biomedical SOCs are capable of multimodal tele-monitoring of various bio-signals. To improve the device longevity, SOCs have evolved to contain a power-efficient dedicated processor and algorithms for diagnosis, ultra-low-power circuit blocks, low-power wireless circuits and energy-harvesting technologies. Furthermore, different communication standards are being developed to satisfy the low-power requirements of portable medical systems.

Another trend in technology directions is a move towards Lab-on-a-Chip or semiconductor systems for diagnosis and disease screening. Silicon solutions are being designed for portable systems to quickly and inexpensively diagnose illness from simple blood tests to imaging to spectroscopy. The trend of using emerging technologies such as MEMS or CMOS-CNT (carbon nanotube) arrays to solve medical problems will make it possible to bring traditionally expensive diagnosis tools to rural and remote areas where medical expertise is typically scarce.

In line with these trends, ISSCC 2015 Session 21 features 9 papers representing the latest technological innovations in bio-medical systems.

Ultra-Low-Power and Secure Systems for IoT Applications
In the past few decades, many new applications such as mobile devices and the Internet have driven the growth of high-performance computing systems. The next big applications will focus on the Internet of Things (IoT) that require secure systems with ultra-low power including autonomous sensors and big-data analysis platforms. Important trends and challenges of the future that need system innovation include:
(1) Counter measures for post-quantum cryptography,
(2) Efficient extraction of relevant context from autonomous sensors,
(3) Processors for big-data analysis.
To protect privacy and properties in the Internet-of-Things era, various technologies for post-quantum cryptography are being introduced as a counter measure for quantum computers, which will be available in the near future. With quantum computers, mathematically hard problems used to protect encryption keys turn into easy problems. Therefore, new algorithms such as lattice-based ring learning with errors (RLWE) is necessary. For extensive deployment of autonomous smart sensors, low-power architectures for context-aware sensors are being developed. For example, a hierarchical sensing architecture will turn on the minimum amount of sensor circuitry when it is waiting for data to come in, but will later turn on the full sensor after detecting the incoming data. In-sensor feature extraction is another trend to reduce power and performance requirements of host processors. To efficiently analyze massive data collected from various sensors, innovative computing architectures such as spin computing and machine-learning co-processors are also emerging.

New circuit technology is also needed to reach the power and performance requirements of autonomous sensors. One example is an ultra-low power ADC operating near sub-threshold voltage. A second example involves circuits for harvesting energy from thermal and light sources. Sub-threshold operation greatly improves energy efficiency of overall circuits at the expense of maximum operating speed, which is usually not a concern for IoT sensors. At ISSCC 2015, Session 24 includes three papers presenting innovative techniques on counter measures for post-quantum cryptography, ultra-low-power hierarchical sensing, and computing architectures for big data analysis.
Wide Bandgap Power Devices: GaN and SiC

Power electronics blocks are becoming ubiquitous and can be found in almost every electrical and electronic system from inverters that connect solar panels and wind turbines to the electric grid, to electric vehicles, industrial motors and laptop power adapters. For nearly 50 years, silicon chips have been the basis of power electronic circuits. However, as clean energy technologies and the electronics industry have advanced, silicon chips are reaching their limits in power conversion — resulting in too much wasted heat as well as higher energy consumption. The wide bandgap (WBG) semiconductors such as Gallium Nitride (GaN) and Silicon Carbide (SiC) have the potential to change this. As compared to silicon, WBG semiconductors operate at higher temperatures, frequencies and voltages — helping to eliminate a large portion of the power losses in electricity conversion.

Currently, GaN and SiC technologies, particularly for power devices, are becoming mature. For instance, high-voltage SiC power diodes are expanding their market by leaps and bounds due to their lower loss and higher speed. Furthermore, GaN power switches are being introduced in compact DC/DC converters and inverters for low-power applications due to their high-speed operation, which in turn, is leveraged to meet the demand for smaller system sizes.

As GaN power devices are expanding their application domain, supporting circuit blocks such as specialized integrated gate drivers, high-speed signal and power isolators, and high-frequency passive components that can fully exploit the speed performance of GaN power devices are becoming increasingly important.