ISSCC 2013
TRENDS
CONDITIONS OF PUBLICATION

PREAMBLE

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FOOTNOTE

• From ISSCC’s point of view, the phraseology included in the box below captures what we at ISSCC would like your readership to know about this, the 60th appearance of ISSCC, on February 17th to the 21th, 2013, in San Francisco.

This and other related topics will be discussed at length at ISSCC 2013, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 17-21, 2013, at the San Francisco Marriott Marquis Hotel.

ISSCC Press Kit Disclaimer
The material presented here is preliminary.
As of November 9, 2012, there is not enough information to guarantee its correctness.
Thus, it must be used with some caution.
The efficient control, storage, and distribution of energy are worldwide challenges, and are increasingly important areas of analog circuit research. While the manipulation and storage of information is efficiently performed digitally, the conversion and storage of energy must fundamentally be performed with analog systems. As a result, the key technologies for power management are predominantly analog. For example, there is much interest in wireless power transmission for battery charging applications, ranging from mobile handsets to medical implants, and increased efficiency in wireless power transmission is enabling faster charging over longer distances. There is also an explosion of technologies that permit energy to be collected from the environment via photovoltaic, piezoelectric, or thermoelectric transducers. A significant focus here is on analog circuits that are able to harvest sub-microwatt power levels from energy sources at 10’s of millivolts, to provide autonomy for remote sensors or to supplement conventional battery supplies in mobile devices. To achieve this, extremely low power must be consumed by the attendant analog circuits so that some energy is left over to charge a battery or supercapacitor. Similarly, the power consumption of analog instrumentation amplifiers, oscillators, and audio power amplifiers is being scaled down to meet the demands of these low power systems. Fast power-up and -down is also desired from these circuits to permit high energy-efficiency during intermittent operation. Together, these technologies will permit devices to be powered indefinitely from sustainable sources, opening the door to ubiquitous sensing, environmental monitoring, and medical applications.

Analog circuits also serve as bridges between the digital world and the analog real world. Just like the bridges in our roads, analog circuits are often bottlenecks and their design is critical to overall performance, efficiency, and robustness. Nevertheless, digital circuits such as microprocessors drive the market; so semiconductor technology has been optimized relentlessly over the last 40 years to reduce the size, cost, and power consumption of digital circuits. Analog circuitry has proven increasingly difficult to implement using these modern IC technologies. For example, as the size of transistors has decreased, the range of analog voltages they can handle has decreased and the variation observed in their analog performance has increased.

These aspects of semiconductor technology explain two key divergent trends in analog circuits. One trend is to forgo the latest digital IC manufacturing technologies, instead fabricating analog circuits in older technologies, which may be augmented to accommodate the high voltages demanded by increasing markets in medical, automotive, industrial and high-efficiency lighting applications. Other applications dictate full integration of analog and digital circuits together in our most modern digital semiconductor technologies. For example, microprocessors with multiple cores can reduce their overall power consumption by dynamically scaling operating voltage and frequency in response to time-varying computational demands. For this purpose, DC-DC voltage converters can be embedded alongside the digital circuitry, driving research into the delivery of locally regulated power supplies with high efficiency and low die area, but without recourse to external components. These trends are captured by movement towards the top-right in the plot below.
[Session 5: Audio and Power Converters, courtesy paper 5.4 ISSCC 2012]
Data Converters – 2013 Trends

**Subcommittee Chair: Boris Murmann, Stanford University, Stanford, CA**

Data converters serve as key building blocks in almost all known applications that bridge the analog physical world with the digital circuits that drive the functionality in modern integrated circuits. Key metrics such as signal-to-noise ratio, bandwidth, and power efficiency continue to be key drivers for innovation, as evidenced by the data converters presented at ISSCC 2013.

The first figure below shows energy efficiency expressed as power dissipated relative to the effective Nyquist sample rate ($P/f_{\text{Nyq}}$) and as a function of the ADC’s signal-to-noise ratio (SNDR). For low- to medium-resolution converters, energy is primarily expended to quantize the signal; the efficiency of this operation can be measured as the energy consumed per conversion step (the so-called Walden Figure of merit). The dotted trend line represents a benchmark of 10 fJ/conv-step. Higher-resolution converters face the additional burden of overcoming circuit noise, necessitating a different benchmark proportional to the square of the signal-to-noise ratio shown by the solid line. Contributions for 2013 are indicated by the colored dots representing various converter architectures with contributions from previous years denoted by the smaller dots. (Note here that a lower $P/f_{\text{Nyq}}$ metric represents a more efficient circuit.) Several new SAR-based converters at various SNDR design points continue to push the limits of energy efficiency and push into previously unchartered territory.

The second figure shows energy per conversion step vs. the effective sample rate. This figure elucidates the difficulties of high-speed operation for a given technology. Nevertheless, advances in circuit innovations embodied in leading-edge technologies have resulted in new benchmarks in energy efficiency across the spectrum of conversion rates.

The final chart shows achieved bandwidth as a function of SNDR. Sampling jitter or aperture errors make the combination of high resolution and high bandwidth a particularly difficult task. Nonetheless, in 2013, we see many examples that set new records in this metric utilizing several different converter architectures.
FoM (energy per conversion step) versus Nyquist-bandwidth for various converters

Bandwidth versus SNDR.
Demand for ubiquitous mobile functionality to achieve enhanced productivity, a better social-networking experience, and improved multimedia quality, continues to drive innovation in technologies that will deliver to these objectives in an energy and cost-efficient manner. While the performance of embedded processors has increased to meet the rising demands of general-purpose computations, dedicated multimedia accelerators provide dramatic improvements in performance and energy efficiency of specific applications. Energy harvesting is another area of growing importance, leading to technologies that leverage non-volatile logic-based SoC’s for applications that do not have a constant power source or handheld devices with very limited battery capacity.

Technology scaling continues to be exploited to deliver designs capable of operating at lower voltages, resulting in reduced energy per operation, as well as reducing the area required to implement specific functions. Processors unveiled at ISSCC 2013 are built on a variety of technology nodes, with best-in-class results accomplished along the axes of integration, performance/watt and functional integration, as well as a few industry-first implementations. These are demonstrated in various process nodes ranging from 0.13µm down to 28nm bulk, and SOI CMOS technologies.

Emerging medical applications require a significant reduction in the standby power over state-of-the-art commercial processors. This drives the exploration of new leakage-reduction techniques in both logic and on-chip memories, targeting orders of magnitude reduction in leakage currents. Fast wake-up time requirements drive the need for saving and restoring the processor state.

Figure 1 illustrates the main trends in feature phones and smart phones relevant to energy-efficient digital circuits. In the late 1990s, a GSM phone contained a simple RISC processor running at 26MHz, supporting a primitive user interface. After a steady increase in clock frequency to roughly 300 MHz in the early 2000s, there has been a sudden spurt towards 1 GHz and beyond. Moreover, following trends in laptops and desktops, processor architectures have become much more advanced, and recent smart phones incorporate dual and even quad-core processors, running up to 2GHz frequencies. Battery capacity, mostly driven by the required form factor, as well as thermal limits imply a power budget of roughly 3W for a smartphone. From this budget, also the power amplifier (for cellular communication) and the displays have to be powered. The available power budget for everything digital is in the range of 2W (peak) to 1W (sustained). As a result, energy efficiency has become the main challenge in designing application processors, graphics processors, media processors (video, image, audio), and modems (cellular, WLAN, GPS, Bluetooth). For video and image processing, the trend has been towards dedicated, optimized hardware solutions. Some new areas where dedicated processors are particularly needed include gesture-based user interfaces, and computational imaging, to name a few. For all digital circuits, the limited power budget leads to more fine-grained clock gating, various forms of (adaptive) voltage-frequency scaling, a variety of body-bias schemes, and elaborate power management strategies.

Figure 2 shows the evolution of bitrates for wired and wireless links over time. Interestingly, cellular links, wireless LAN, as well as short links consistently show a 10× increase every five years, with no sign of abating. With essentially constant power and thermal budgets, energy efficiency has become a central theme in designing application processors, graphics processors, media processors (video, image, audio), and modems (cellular, WLAN, GPS, Bluetooth). For video and image processing, the trend has been towards dedicated, optimized hardware solutions. Some new areas where dedicated processors are particularly needed include gesture-based user interfaces, and computational imaging, to name a few. For all digital circuits, the limited power budget leads to more fine-grained clock gating, various forms of (adaptive) voltage-frequency scaling, a variety of body-bias schemes, and elaborate power management strategies.
<table>
<thead>
<tr>
<th>Graphics</th>
<th>2D, 3D</th>
<th>OpenGL (ES1.1)</th>
<th>OpenGL/VG/Max (ES2.0)</th>
<th>AR (Augmented Reality)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Display</td>
<td>16b QVGA</td>
<td>VGA</td>
<td>Dual 24b WVGA @ 60fps</td>
<td>Dual 24b Stereo SXGA @ 60fps</td>
</tr>
<tr>
<td>Camera</td>
<td>1-2M</td>
<td>3M</td>
<td>5-8M</td>
<td>10M</td>
</tr>
<tr>
<td>Image/Video</td>
<td>JPEG, MPEG-4</td>
<td>H.264/AVC (VGA)</td>
<td>H.264/AVC (D1)</td>
<td>H.264/AVC (Full HD)</td>
</tr>
<tr>
<td>Audio</td>
<td>MP3</td>
<td>AAC</td>
<td>AAC Plus</td>
<td>WMA</td>
</tr>
<tr>
<td>Accelerator</td>
<td>DSP</td>
<td>FPU</td>
<td>SIMD Multi-core</td>
<td>Many-core</td>
</tr>
<tr>
<td>downlink [Mb/s]</td>
<td>EGPRS 0.4</td>
<td>UMTS 0.4-2</td>
<td>HSPA 1.8-7</td>
<td>HSPA+ 7-42</td>
</tr>
<tr>
<td>CPU [MIPS]</td>
<td>-300</td>
<td>300-500</td>
<td>500-800</td>
<td>800-2400</td>
</tr>
</tbody>
</table>


Application processor trends in smart phones.

Wireless and wired data rates over time.
The relentless march of process technology brings more integration and performance. IBM’s System z processor leads the charge at ISSCC 2013 clocking in at 5.7GHz and with 2.75B transistors.

The chip complexity chart below shows the trend in transistor integration on a single chip over the past two decades. While the 1 billion transistor integration mark was achieved some years ago, we now commonly see processors with beyond 2B transistors on a die.

Leveraging sophisticated strategies to lower leakage and manage voltage, variability and aging, has bolstered the continuing reduction in total power dissipation. This is helping rein in the increase in energy demands from PCs, servers, and similar systems. As power reduction becomes mandatory in every application, the trend towards maintaining near-constant clock frequencies also continues as shown below in frequency trends plot. This will yield solutions with less cost and cooling demands, resulting in greener products in the future.
Processors are choosing to trade off performance by lowering supply voltage. The performance loss of reduced voltage and clock frequency is compensated by further increased parallelism. Processors with more than 8 cores are now commonplace. This year at ISSCC 2013, a 24-core processor from Fudan University will be presented as noted in the core-count trend chart below.

In addition to the trend to integrate more cores on a single chip, multiple die within a single package are appearing. In ISSCC 2013, IBM will present a multi-chip module with six CPUs and two embedded DRAM cache chips. As well, dedicated co-processing units for graphics and communications are now commonly integrated on these complex systems-on-chip. Design of these SoCs requires broad collaboration across multiple disciplines including circuits, architecture, graphics, process technology, package, system design, energy efficiency and software. New performance and power-efficient computing techniques continue to be introduced at targeted, critical applications such as floating point and SIMD.
As technology continues to scale to finer dimensions, large caches are being integrated into microprocessor die. The chart below shows the general trend of large cache integration.

Methods to communicate within-die as well as cross-die are becoming increasingly important. This is being driven by two trends: (1) 3D integration continues to grow in interest and (2) intra-die communications become more challenging with process scaling due increases in delay per unit interconnect length. Work on bringing package-level inter-chip transport onto the die has been gaining in popularity and we see this trend continuing.

Another trend evident at ISSCC 2013 is the continued emergence of all-digital phase-locked loops and delay-locked loops to better exploit nanometer feature size scaling and reduce power and area costs. Due to the application of highly innovative architectural and circuit design techniques, the features of these “all-digital” PLLs and DLLs have improved significantly over the recent past. The diagram below shows the jitter performance vs. energy cost for PLLs and MDLLs.
Overall, digital processors continue to grow in complexity, while more circuits are implemented using digital techniques to cope with variability and ease scaling to finer geometries.
Subcommittee Chair: Roland Thewes, TU Berlin, Berlin, Germany

IMAGERS

Since 2010 there has been growth beyond expectations in the adoption of mobile devices, e.g., smart phones and tablets, which has called for larger volumes of CMOS image sensor chips to be produced. The resolution and miniaturization races are ongoing, and performance metrics are also becoming more stringent. In addition to the conventional pixel shrinkage, a “more than Moore” trend is increasingly evident. Resolutions of over 20Mpixels are commercially available for mobile devices employing enhanced small-size pixels. Thanks to the innovative readout and ADC architectures embedded at the column and chip levels, data rates approaching 50Gb/s and a noise floor below single electron have been demonstrated. In addition to the conventional applications, ultra-low-power vision sensors, 3D, high-speed, and multispectral imaging are the front-running emerging technologies.

Back-side Illumination (BSI) is now the mainstream technology for high-volume, high-performance mobile applications, 1.12μm BSI pixels are available, and the industry is potentially moving towards 0.9μm pixel pitch and below. Additional innovative technologies outside of the traditional scaling include advanced 3D stacking of a specialized image sensor layer on top of deep-submicron digital CMOS (65nm 1P7M) using through silicon vias (TSVs) and micro-bumps. The importance of digital-signal-processing technology in cameras continues to grow in order to mitigate sensor imperfections and noise, and to compensate for optical limitations. The level of sensor computation is increasing to thousands of operations-per-pixel, requiring high-performance and low-power digital-signal-processing solutions. In parallel with these efforts is a trend throughout the image sensor industry toward higher levels of integration to reduce system costs.

Ultra-low-power vision sensors are being reported in which more programmability and computation is performed at the pixel level in order to extract scene information such as object features and motion.

Lightfield/plenoptic commercial cameras, which have been available since 2010, are now gaining popularity and are being marketed for 3D imaging and/or all-in-focus 2D imaging. On-chip stereoscopic vision has been demonstrated through digital micro lenses (DML), paving the way to next-generation passive 3D imaging for mobile and entertainment applications, e.g. through gesture control user interfaces.

Significant R&D effort is being spent on active 3D imaging time-of-flight (TOF) applications to support requirements from autonomous driving, gaming, and industrial applications, addressing open challenges like background light immunity, higher spatial resolution, and longer distance range. Deep-submicron CMOS single-photon avalanche diodes (SPADs) have been developed by several groups using different technology nodes. They are now capable of meeting the requirements for high resolution, high timing accuracy by employing highly parallel time-to-digital-converters (TDCs) and small pixel pitch with better fill factor.

Ultra-high-speed image sensors for scientific imaging applications with up to 20Mfps acquisition speed have been demonstrated.

Multispectral imaging is gaining a lot of interest from the image sensor community: several research groups have demonstrated fully CMOS room-temperature THz image sensors, and a hybrid sensor capable of simultaneous visible, IR, and THz detection has been reported.

The share of CCDs continues to shrink in machine vision, compact DSC and security applications. Only for high-end digital cameras for astronomy and medical imaging do CCDs still maintain a significant market share.

Sensors & MEMS
MEMS inertial sensors are finding widespread use in consumer applications to provide enhanced user interfaces, localization, and image stabilization. Accelerometers and gyroscopes are being combined with 3D magnetic-field sensors to form nine-degree-of-freedom devices, and pressure sensors will eventually add a 10th degree. The power consumption of such devices is becoming sufficiently low for the sensor to be on all the time, enhancing indoor navigation. There have been further advances in heterogeneous integration of MEMS with interface circuits in supporting increased performance, larger sensor arrays, reduced noise sensitivity, reduced size, and lower costs.

To address the stringent requirements of automotive, industrial, mobile, and scientific application, MEMS inertial sensors, pressure sensors and microphones are becoming more robust against electromagnetic interference (EMI), packaging parasitics, process voltage temperature (PVT) variations, humidity, and vibration.

Sensor interfaces achieve increasingly high resolution and dynamic range while maintaining or improving power or energy efficiency. This is achieved through techniques such as zooming, non-uniform quantization, and compensation for baseline values.

New calibration approaches, such as voltage calibration, are being adopted for BJT-based temperature sensors to reduce cost. In addition to thermal management applications (prevention of overheating in microprocessors and SoCs), temperature sensors are also increasingly co-integrated with other sensors (e.g. humidity, pressure, and current sensors) and MEMS resonators for cross-sensitivity compensation. Alternative temperature-sensing concepts find their way into applications with specific requirements not easily addressed by BJTs: thermal diffusivity-based sensing for high-temperature applications; thermistor-based and Q-based concepts for in-situ temperature sensing of MEMS devices and for ultra-low-voltage operation.

MEMS oscillators continue to improve; phase noise is now low enough for demanding RF applications, 12kHz-to-20MHz integrated jitter is now below 0.5ps, and frequency accuracy is now better than 0.5ppm. Consumer applications are adopting new low-power and low-cost oscillators.

**Biomedical**
There have been continuous achievements in the area of ICs for neural and biopotential interfacing technologies. Spatial resolution of neural monitoring devices is being reduced utilizing the benefits of CMOS technology. IC providers are increasing their component offerings towards miniaturization of portable medical devices.

Telemedicine and remote-monitoring applications are expanding with support from IC manufacturing companies. The applications of such systems are not limited to services targeted for elderly or chronically ill patients; for example there are several technologies developed to enhance the way clinical trials are conducted by monitoring patient adherence and by improving data collection. Low power WiFi, and Bluetooth-low-energy is emerging as a standard wireless connection between portable communication services and wearable technology.

Smart biomolecular sensing is another major trend that marries solid-state and biochemical worlds together with the ultimate goal of enabling a more predictive and preventative medicine. With the help of the accuracy and parallelism enabled by CMOS technology, time, cost, and error rate of DNA sequencing may be significantly improved. Direct electronic readout may relax the need for complex biochemical assays. Similar trends are becoming increasingly evident in the space of proteomics and sample preparation.

Even for medical imaging, there is a trend from hospital imaging toward point-of-care and portable devices. A key example is in the space of portable high-resolution ultrasounds in which larger scientific imaging setups are being integrated onto the sensor by process technology (e.g. integrated spectral filters, CMUT). Another example is in the space of molecular imaging. The advent of silicon photomultipliers (SiPM) providing a solid-state alternative to PMTs enable the realization of PET scanners compatible with MRI, opening the way to new frontiers in the field of cancer diagnostics. More recently, SiPMs realized within deep-submicron CMOS technologies have allowed the integration at pixel- and chip-level of extra features, e.g. multiple timestamp extraction, allowing in perspective a dramatic reduction of the system cost.

**Displays**
The desire to put much higher-resolution and higher-definition displays into mobile applications is one of the display-technology trends, and it is now opening a Full HD smartphone era. 440ppi high-definition displays are expected, even for 5-inch display sizes. Low-temperature polysilicon (LTPS) technology seems to have more merits over a-Si TFT technology. But a-Si TFT and oxide TFT technologies supported by compensating driver systems are being prepared to compete with it. Very-large-size LCD TVs over 84 inches, and UD (3840×2160) resolution are now the leading entertainment systems. 55-inch AMOLED TVs with Full HD resolution are also opening new opportunities in consumer applications.

As touch-screen displays for mobile devices become increasingly thin, capacitive touch sensors move closer to the display. The resulting in-cell touch displays come with reduced signal levels due to increased parasitics, and increased interference from the display and switched-mode chargers. Noise immunity is improved by adopting noise filtering and new signal-modulation approaches.
We continue to see progressive scaling in embedded SRAM, DRAM, and floating-gate based Flash for very broad applications. However, due to the major scaling challenges in all mainstream memory technologies, we see a continued increase in the use of smart algorithms and error-correction techniques to compensate for increased device variability. In further response to these challenges, we see logic processes adopting FinFET devices along with read- and write-assist circuits in SRAMs. Emerging memory technologies are making steady progress towards product introductions, including PCRAM and ReRAM, while STT-MRAM is beginning to become a strong candidate for both standalone and embedded applications.

**SRAM**

Embedded SRAM continues to be a critical technology enabler for a wide range of applications from high performance computing to mobile applications. The key challenges for SRAM include $V_{\text{CCMIN}}$, leakage and dynamic power reduction while relentlessly following Moore’s law to shrink the area by $2^x$ for every technology generation. As the transistor feature size marches toward sub-30nm, device variation has made it very difficult to shrink the bit cell size at the $2^x$ rate while maintaining or lowering $V_{\text{CCMIN}}$ between generations. Starting at 45nm, the introduction of high-k metal-gate technology reduces the $V_t$ mismatch and enables further device scaling by significantly reducing the equivalent oxide thickness. Starting at 22nm and beyond, new transistors such as FinFETs and fully-depleted SOI are key to enabling the continuous scaling of bit cell area and low voltage performance. Design solutions such as read/write assist circuitry have been used to improve SRAM $V_{\text{CCMIN}}$ performance starting at 32nm. New SRAM bit cells with more than 6 transistors have also been proposed to minimize operating voltage. For example, 8T register file cells have been reported in recent products requiring low $V_{\text{CCMIN}}$. Dual-rail SRAM design emerges as an effective solution to enable dynamic voltage-frequency scaling (DVFS) by decoupling logic supply rails from SRAM arrays and thus allowing much wider operating window. It is important for SRAM to reduce both leakage and dynamic power, keeping products within the same power envelope at the next technology node. Sleep transistors, fine-grain clock gating and clock-less SRAM designs have been proposed to reduce leakage and dynamic power. Redundancy and ECC protection are also keys to ensure yield and reliability when embedded SRAM products go to production. Figure 1 shows the SRAM bit cell scaling trend on the left axis and the SRAM $V_{DD}$ scaling trend on the right axis, using data from major semiconductor manufacturers.
HIGH-SPEED I/O for DRAM

In order to reduce the bandwidth gap between main memory and processor frequencies, external data rates continue to increase as conventional high-speed wired interface schemes such as DDR(x) and GDDR(x) for DRAM evolve (Figure 2). Currently GDDR5 and DDR4 memory I/Os operate around 7Gb/s/pin and 3Gb/s/pin, respectively. To achieve higher speed data transfer rate, signal integrity techniques such as crosstalk, noise and skew cancellation, and speed enhancement techniques such as equalizer and pre-emphasis have been developed. These advanced techniques have pushed I/O speeds towards 10Gb/s/pin. Lower power consumption for data center and mobile applications is also pursued. A near-ground signaling method, termination impedance optimization, decision feedback equalizer, and clock-feathering slew rate control technologies have been demonstrated to reduce the power dissipation of memory interfaces significantly, while achieving high bandwidth.
In the past decade significant focus has been put on the emerging memories field to find a possible alternative to floating gate nonvolatile memory (NVM). The emerging NVMs, such as phase-change memory (PRAM), ferroelectric RAM (FeRAM), magnetic spin-torque-transfer RAM (STT-MRAM), and resistive memory (ReRAM), are showing potential to achieve high cycling capability and lower power per bit for both read and write operations. Some commercial applications, such as cellular phones, have recently started to use PRAM, demonstrating that reliability and cost competitiveness in emerging memories is becoming a reality. Fast write speed and low read-access time are being achieved in many of these emerging memories. At ISSCC 2013, a 32Gb ReRAM cross-point array is demonstrated in 24nm technology. Figures 3 and 4 provide a summary on the scaling trends for both bandwidth and density in emerging memories.
Figure 3: Read- and write-bandwidth comparison of nonvolatile memories.
NAND FLASH MEMORY

NAND Flash memory continues to advance towards higher density and lower power, resulting in low-cost storage solutions that are enabling the replacement of traditional hard-disk storage with solid-state disks (SSDs). Multiple bits per cell has proven to be effective in increasing the density. Figure 5 shows the observed trend in NAND Flash capacities presented at ISSCC over the past 18 years. With scaling, device variability and error rates increase, requiring system designers to develop sophisticated control algorithms to offset this trend. Some of these are implemented outside the NAND silicon in the system memory controller, especially ECC and data management methods, for improved overall reliability. Possible future scenarios include 3D stacked NAND vertical gates as a solution to further increase the NAND density.
Some current state-of-the-art papers from ISSCC 2013 include:

- [12.1] A 130.7mm² 2-Layer 32Gb ReRAM Memory Device in 24nm Technology
- [12.5] A 128Gb 3b/cell NAND Flash Design Using 20nm Planar Cell Technology
- [18.2] An SRAM Using Output Prediction to Reduce BL-Switching Activity and Statistically-Gated SA for up to 1.9× Reduction in Energy/Access
- A 45nm 6b/cell Charge-Trapping Flash Memory Using LDPC-Based ECC and Drift-Immune Soft-Sensing Engine
Introduction
This year has shown increased innovation, integration, and technical maturity across RF frequency bands. This document outlines emerging RF trends that will be covered at ISSCC 2013.

ISSCC 2013 authors will present an ongoing drive toward increasing levels of integration. This trend can be seen in all areas of RF design from mm-Wave, to cellular, to imaging, to wireless sensors. In mm-Wave designs, higher system complexity (front-end, synthesizer, and baseband) is increasingly being integrated onto a single die. In cellular, the push for integration has led to a strong trend of architectures allowing better linearity and co-existence of these multiple bands and standards. In a related trend, there has been much research the last few years into various ways to remove costly and bulky SAW filters and duplexers. Some of these research areas include highly linear blocker-tolerant receivers, mixer-first receivers, feedback blocker cancellation, feed-forward blocker cancellation, N-path filters, and electrical balance of hybrid transformers. Strong work continues in the effort to integrate CMOS PAs while delivering viable power/efficiency performance. Finally, a clear trend this year was a significant number of chips demonstrated in 65nm CMOS compared to other technology nodes. This observation was noted across all frequency ranges and circuit topologies. The chips presented at ISSCC 2013 confirm that RF devices will continue to see larger levels of integration at the chip- and package-level for years to come.

Over the past decade, the papers submitted to ISSCC have indicated clear trends in the continuing push to higher frequencies of operation in CMOS and BiCMOS. This trend has continued this year for oscillators, mm-Wave amplifiers, and PAs. An emerging trend is the increasing complexity of systems operating in the 60-to-200GHz range. The push to ever-higher frequencies is being pursued by both industry and academia for various applications. An important application is high-data-rate communication. With the low-GHz frequency spectrum already overcrowded, researchers are continuing to target frequencies above 60GHz. Two other applications for products operating in these frequency bands are imaging and radar. These frequencies are desirable for such products due to their high spatial resolution and enablement of small antenna dimensions, allowing efficient beam-forming arrays. Another continuing trend is the integration of mm-Wave antennas into silicon substrates.

The combination of these two trends (that is, increased integration and the push to higher frequencies) has enabled a new class of fully-integrated application-driven systems. With the availability of many RF and mm-Wave building blocks in CMOS and BiCMOS, fully integrated solutions for specific emerging domains are appearing, both in the RF and the mm-Wave frequency range. These systems are built on a foundation of circuit-block innovations that have been developed over the past few years. Single-chip radars in RF and mm-Wave frequencies with improved resolution, improved efficiency, showing increasing levels of integration are being demonstrated. Similarly, new systems are being developed for ultra-wideband radar and mm-Wave wireless sensing. Demonstrations in the biomedical field are clearly moving from simple electrical measurements towards real medical measurements in realistic environments using systems-in-package (SiP).

We now discuss these two trends supported with data from chips to be presented at ISSCC 2013.

Complexity and maturity in the mm-Wave and sub-mm-Wave ranges

The high cutoff frequency of bipolar transistors and highly downscaled MOS transistors enables the realization of circuits and systems operating in the mm-Wave range. In the last few years, high-data-rate communication in the 60GHz band and car radar around 77GHz have garnered much attention. While the integration level in these domains is already quite high, we see an improvement of the performance of the building blocks (e.g. output power of PAs, spectral purity and tuning range of VCOs).
The 100GHz barrier for the operating frequency of silicon circuits has been broken a few years ago. Whereas initially elementary building blocks like a VCO and an amplifier operating above 100GHz have been realized, we now witness the trend of increasing complexity in circuits operating above 100GHz. Meanwhile, the electrical performances at the building block level improve: the output power of mm-Wave and sub-mm-Wave sources and PAs increases (Figure 1, Figure 2) and VCOs can operate at ever-increasing frequencies with a higher tuning range.

**Co-existence and efficiency for cellular applications**

**RX and TX linearization:** in the past few years there has been increasing interest in techniques to improve the linearity of transmitters and receivers. Improved linearity in the receivers will ease the requirements on the RF filtering of out-of-band blockers that can be accomplished, for instance, by placing a programmable notch filter in the RF path. TX linearity improvements will benefit performance parameters such as error-vector magnitude (EVM), ACLR and spectral purity.

**Efficiency:** PA efficiency improvements demonstrated this year will directly impact the battery life in portable applications. These efficiency improvement techniques include analog and digital pre-distortion, dynamic biasing and envelope tracking.

**Digitally-assisted RF:** the trend towards digitally-assisted RF continues and is increasingly applied to mm-Wave chips. More digitally assisted calibration techniques are being demonstrated in order to improve the overall performance of the transceiver by reducing the impact of analog impairments at the system level. These techniques include: spur cancelation/reduction, IIP2 improvements, and digital pre-distortion.

**VCOs:** there is a continuing trend toward improvements in phase-noise figure-of-merit (FOM) and power consumption due to circuit techniques like Class-C and Class-D VCOs. Figure 3 shows trends in VCO FOM performance of some of the most significant VCOs published over the past decade. This year’s ISSCC shows clear contributions to this field.
Figure 1: PAE (%) vs. output power for recent submicron mm-Wave CMOS PAs.

Figure 2: Output power versus frequency for mm-wave and sub-mm-wave sources.
Figure 3: Phase-noise FOM at 20MHz offset frequency versus oscillation frequency.
Technology Directions – 2013 Trends

Subcommittee Chair: Hoi-Jun Yoo, KAIST, South Korea, Technology Directions

Large-Area Flexible Electronics

Technology directions in the field of large-area and low-temperature electronics focuses on lowering the cost-per-unit-area, instead of increasing the number of functions-per-unit-area that is accomplished in crystalline Si technology according to the well-known Moore’s law.

A clear breakthrough in research for large area electronics in the last decade has been the development of thin-film-transistor (TFT) processes with an extremely low temperature budget of (<150°C) enabling manufacturing of flexible and inexpensive substrates like plastic films and paper.

The materials used for these developments have for a long time been carbon-based organic molecules like pentacene with properties of p-type semiconductors. More recently, air-stable organic n-type semiconductors and amorphous metal oxides, which are also n-type semiconductors, have emerged. The most popular metal oxide semiconductor is amorphous Indium Gallium Zinc Oxide (IGZO), but variants exist (Zinc Oxide, Zinc Tin Oxide, and so on). The mobility of n- and p-type organic semiconductors has reached values exceeding 10 cm²/Vs, which is already at or exceeding the performance of amorphous silicon. Amorphous metal oxide transistors have typical charge carrier mobility of 10 to 20 cm²/Vs. Operational stability of all semiconductor materials has greatly improved, and should be sufficient to enable commercial applications, especially in combination with large-area compatible barrier layers to seal the transistor stack.

In the state-of-the-art p-type only, n-type only and complementary technologies are available. For the latter, all-organic implementations have been shown, but also hybrid solutions, featuring the integration of p-type organic with n-type oxide TFTs. Most TFTs are still manufactured with technologies from display-lines, using subtractive methods based on lithography. However there is a clear emphasis on the development of technologies that could provide higher production throughput, based on different technologies borrowed from the graphic printing world like screen and inkjet printing. The feature sizes and spread of characteristics of printed TFT technologies are still larger than those made by lithography, but there is clear progress in the field.

The prime application for these TFT families are backplanes for active-matrix displays, including in particular flexible displays. Organic TFTs are well-suited for electronic paper-type displays, whereas oxide TFTs are targeting OLED displays. Furthermore, these thin-film transistors on foil are well-suited for integration with temperature or chemical sensors, pressure-sensitive foils, photodiode arrays, antennas, sheets capable of distributing RF power to appliances, energy scavenging devices, and so on, which will lead to hybrid integrated systems on foil. Early demonstrations include smart labels, smart shop shelves, smart medical patches, etc. They are enabled by a continuous progress in the complexity of analog TFT circuits targeting the interface with sensors and actuators, to modulate, amplify and convert analog signals as well as progress in digital TFT circuits and non-volatile memory to process and store information.

In line with this trend, ISSCC 2013 features three papers representing the latest state-of-the-art of organic thin-film transistor circuits. A front-end amplifier array for EMG measurement is demonstrated for the first time with organic electronics in paper 6.4. Transistor mismatch and power consumption of the amplifier are reduced by 92% and 56%, respectively, by selecting and connecting the transistors trough a post-inkjet printing. Papers 6.5 and 6.6 present advances in analog-to-digital converters for sensing applications. Papers 6.5 demonstrates the first ADC that integrates on the same chips resistors and printed n and p-type transistors. The ADC achieves an SNDR of 19.6dB, SNR of 25.7dB and BW of 2Hz. In Papers 6.6, an ADC made only with p-type transistors is presented that has the highest linearity without calibration and that is 14 times smaller than previous works using the same technology.
Emerging Integrated Non-Volatile Memories and Processors

With continuing technology scaling, enabling advances in computation along with energy efficiency will become even more important. A new trend is towards integration of non-volatile memory with logic for ultra-fast power-down/power-up while keeping the state of the computation has been appearing at ISSCC 2013. These technologies will impact future mobile platforms and industrial applications, making mobile computing truly ubiquitous.

ISSCC 2013 features Paper 11.1 by MIT that presents a D-Flip-Flop with ferroelectric capacitor non-volatile storage, enabling logic pipelines to be suspended and power-cycled without losing the state. It demonstrates a save-restore energy budget of just 3.4 pJ/bit. Paper 11.2 by Tohoku University describes an MTJ-based logic-in-memory solution for parallel motion vector prediction accelerator implemented with cycle-based power gating, demonstrating 4X reduction in leakage power and 2X reduction in active power.
Data rates for modern wireless standards are increasing rapidly and this is evident from the trend of cellular standards (shown in Figure 1). The data rate has increased 100X over the last decade and another 10X is projected in the next five years. This trend is partly contributed by using more complex modulations (e.g. using OFDM – Orthogonal Frequency Division Multiplexing - for better spectral efficiency) at the cost of digital signal processing (DSP). In addition, the expansion of channel bandwidth is also an effective way to achieve the data rate increase. This is seen in the wireless connectivity chart (e.g. 802.11) shown in Figure 2. The channel bandwidths for the WLAN standards increase from the traditional 20MHz (802.11g) all the way to 2.16GHz (802.11ad). Because the available spectrum is limited in the low GHz range, for >1GHz channel bandwidth, the carrier frequency is moving from 2.4/5GHz (802.11a/b/g/n/ac) to 60GHz (802.11ad) in the mm-Wave range. With the available spectrum in the 60GHz range, data rates up to 6.76Gb/s can be achieved. Design at mm-Wave frequencies comes with significant challenges, with academic research oriented to the reduction of the power, while industry focuses on product-quality robustness and standards compliance. A new generation of chipsets, compliant with WiGig and 802.11ad, is ready for production.

Since spectrum is scarce, new carrier aggregation techniques are being developed that can combine available channels in a flexible way, e.g. combining non-contiguous channels, or even channels at different frequency bands. The new 802.11af standard aims to utilize “TV white space”, unused legacy analog TV frequency bands below 1GHz. This will first be implemented using a database of available channels per geographical location, but eventually high-sensitivity spectrum sensing will be used to confirm the availability of the spectrum. The possibility of opening up this large amount of spectrum generates radio challenges, e.g. highly linear transceivers that can cover a very wide frequency range and various channel bandwidths. As a consequence of high-linearity and wideband design requirements, distortion cancellation and tunable RF channel-selection techniques are very critical. Most transceivers in this category are adopting digital calibration and analog-feedback techniques to increase the linearity performance for a flexible and tunable front-end to cover a wide range of frequencies.

As wireless technology becomes cheaper, it can be deployed in many devices, including sensors for monitoring environmental conditions. Wireless Sensor Networks (WSNs) require ultra-low-power radio to increase battery life and minimize the battery size, or better yet, eliminate the battery altogether by using energy harvesting. To reduce the power consumption of the radio, the first approach is to use the radio only when it is requested. A “wake-up radio” that monitors the channel and alerts the “main” radio when communication is requested becomes one of the main building blocks of the WSN node. Once the radio is awake, power efficiency becomes the main target for both high- and low-data-rate communication. Another approach is to duty-cycle the radio operation, i.e. only use the radio for short communication bursts, which requires fast turn-on techniques. Such WSNs will enable electronics for sustainability.

Similar to the evolution in cellular, ultra-low-power radios are now becoming multistandard, covering for example Zigbee, BTLE, and IEEE 802.15.6. Multistandard implementation implies radio-block sharing, and standards management, including modulation, frequency, bandwidth, power output, sensitivity …, while maintaining the low power consumption, which is one of the key success factors of such devices. Another main concern is the price. These multistandard radios must have small silicon area circuits in low cost packaging.

NFC (Near Field Communication) is becoming more and more popular. This new secure data wireless transmission mode is now embedded in smart phones and will become a de-facto requirement in the next years.

Digital architectures implementing radio functions are very efficient in deep-nm CMOS. In the past years Digital-PLLs were developed in the radio front-ends. Now, new digital approaches are being deployed in transmitters, targeting more flexibility of the RF front-end that leverages CMOS scaling for reduced power dissipation and area, simplifying integration in large SOCs, and empowering the next generation of wireless communications.
Figure 1: Data Rate Trend of Cellular Standards

Figure 2: Data Rate Trend of Wireless Connectivity Standards (802.11x)
**Wireline – 2013 Trends**

**Subcommittee Chair: Daniel Friedman, IBM, Yorktown Heights, NY**

Over the past decade, wireline I/O has been instrumental in enabling the incredible scaling of computer systems, ranging from handheld electronics to supercomputers. During this time, aggregate I/O bandwidth requirements have increased at a rate of approximately 2-to-3× every 2 years. Demand for bandwidth is driven by applications including memory, graphics, chip-to-chip fabric, backplane, rack-to-rack, and LAN. In part, this increase in bandwidth is enabled by expanding the number of I/O pins per component. As a result, I/O circuitry consumes an increasing amount of area and power on today’s chips. Increasing bandwidth has also been enabled by rapidly accelerating the per-pin data rate. Figure 1 shows that per-pin data rate has approximately doubled every four years across a variety of diverse I/O standards ranging from DDR to graphics to high-speed Ethernet. Figure 2 shows that the data rates for published transceivers have kept pace with these standards, enabled in part by process technology scaling. However, continuing along this rather amazing trend for I/O scaling will require more than just transistor scaling. Significant advances in both energy efficiency and signal integrity must be made to enable the next generation of low-power and high-performance computing systems.

**Power Consumption and Energy Efficiency**

Power consumption for I/O circuits is a first-order design constraint for systems ranging from cell phones to servers. As the pin count and per-pin data rate for I/Os has increased on a die, so has the percentage of total power that they consume. Technology scaling enables increased clock and data rates and offers some energy efficiency improvement, especially for digital components. However, there is a strong correlation between the energy efficiency and the distortions introduced by the channel. Figure 3 plots the energy efficiency (expressed in mW/Gbps, which is equivalent to pJ/b) as a function of Nyquist loss for recently reported transceivers. These transceivers cover a wide variety of standards and process nodes. Based on these data points, the scaling factor between link power and signaling loss is approximately unity, meaning that required link power approximately doubles with every additional 6dB of channel loss. As a result, simply increasing per-pin data rates with existing circuit architectures and channels while scaling transistors is not a viable path given fixed system power limits. To address this issue, recent link research has focused on reducing power through both circuit and channel innovation. There have been a number of recent advances that reduce power through circuit innovation, including low-power RX equalization (DFE, CTLE), CMOS and resonant clocking, low-swing voltage-mode transmitters and links with low-latency power-saving states. Based on the relationship between channel loss and energy efficiency, power can also be reduced by changing the interconnect itself to either reduce the total loss or increase the interconnect density. Examples of this from ISSCC include stacked die TSVs and proximity interconnect, silicon interposers, on-package I/O, and low-loss flexible interconnect. Presentations at ISSCC 2013 move the state-of-the-art well below 1pJ/b for short-range links. A 20Gb/s chip-to-chip transceiver consuming just 540fJ/b employs single-ended ground-referenced signaling across high-density package interconnects [23.3]. Another demonstrates 1Tb/s aggregate bandwidth across low-loss flexible cabling consuming 2.6pJ/b [23.2].

**Electrical**

Some types of channels, especially those related to medium-distance electrical I/O like server backplanes, have to support high data rates along with high loss. Others, like DDR, must contend with increasing amounts of crosstalk in addition to channel loss. For these links, the key to scaling has been improvements in clock jitter and equalization. There are several recent examples of transceivers able to signal across 30 to 35dB of loss at Nyquist at data rates up to 28Gb/s. These transceivers use a combination of fully adaptive equalization methods, including TX FIR, RX CTLE, DFE, as well as RX FIR and/or IIR FFES. In some cases, equalization is being done in the digital domain after first converting the data signal using a 5-to-6b ADC. Although the energy efficiency for these systems tends to be lower than in conventional equalization approaches, they enable more complex and flexible equalization techniques as well as equalization power that may scale more gracefully. A number of CDR circuit techniques have also been developed for these high-loss transceivers, including digital CDRs that employ baud-rate sampling, oversampling, and even blind sampling techniques. Papers at this year’s conference represent the fastest link components reported to date, including a 66Gb/s 3-tap DFE consuming just 46mW.
without loop unrolling [2.2] and a 48Gb/s 88mW TX [2.6], both in standard 65nm CMOS. They also demonstrate significant advances in fully-integrated high-speed transceivers, including a 39.8-to-44.6Gb/s chipset in 40nm CMOS [2.3] and several 32Gb/s TX and RX equalizers compensating up to 40dB of channel loss [2.5, 2.7].

Optical

As the bandwidth demand for traditionally electrical wireline interconnects has accelerated, optics has become an increasingly attractive alternative for interconnects within computing systems. Optical communications have clear benefits for high-speed and long-distance interconnects. Relative to electrical interconnects, optics provides lower loss and potentially higher density through techniques like wavelength-division multiplexing. Optical components – including VCSELs, Mach-Zehnder Interferometers (MZI), optical ring modulators, and photodetectors – are simultaneously being developed for higher performance, lower power, and higher degrees of integration with standard CMOS processes. Circuit design techniques that have traditionally been used for electrical wireline are being adapted to enable integrated optical with extremely low power. This has resulted in rapid progress in optical ICs for Ethernet, backplane and chip-to-chip optical communication. ISSCC 2013 includes several examples of 25Gb/s optical transceivers, including an RX that consumes only 4.9pJ/b. The conference highlights significant advances in Si photonic integration, including a 20Gb/s driver and associated silicon photonic MZI [7.7] and a 2.5Gb/s driver and ring modulator designed and fabricated in a standard CMOS process [7.5].

Concluding Remark

Continuing to aggressively scale I/O bandwidth is both essential for the industry and extremely challenging. Innovations that provide higher performance and lower power will continue to be made in order to sustain this trend. Advances in circuit architecture, interconnect topologies, and transistor scaling are together changing how I/O will be done over the next decade. The most exciting and most promising of these emerging technologies for wireline I/O will be highlighted at ISSCC 2013.
Figure 2. Data Rate vs. Process Node and Year.

Figure 3. Transceiver Power Efficiency vs. Channel Loss.
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