ISSCC 2017
TRENDS
Conditions of Publication

PREAMBLE

The Trends to follow serve to capture the context, highlights, and potential impact, of the papers to be presented in each Session at ISSCC 2017 in February in San Francisco

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FOOTNOTE

- From ISSCC’s point of view, the phraseology included in the box below captures what we at ISSCC would like your readership to know about this, the 64th appearance of ISSCC, on February 5th to February the 9th, 2017, in San Francisco.

This and other related topics will be discussed at length at ISSCC 2017, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 5 - February 9, 2017, at the San Francisco Marriott Marquis Hotel.

ISSCC Press Kit Disclaimer

The material presented here is preliminary.

As of October 9, 2016, there is not enough information to guarantee its correctness.

Thus, it must be used with some caution.
The efficient control, storage, and distribution of energy are worldwide challenges, and are increasingly important areas of analog circuit research. While the manipulation and storage of information is efficiently performed digitally, the conversion and storage of energy is fundamentally performed with analog systems. Therefore, the key technologies for power management are predominantly analog. For example, there is much interest in wireless power transmission for battery charging applications, ranging from mobile handsets to medical implants: increased performance in wireless power transmission is enabling more efficient power delivery over longer distances. There is also an explosion of technologies that allow energy to be collected from the environment via photovoltaic, piezoelectric, or thermoelectric transducers, with a trend toward the use of multiple sources at the same time. A significant focus here is on analog circuits that are able to harvest sub-microwatt power levels from multiple energy sources at tens of millivolts, to provide autonomy for IoE devices, or to supplement conventional battery supplies in portable devices. To achieve this, the attendant analog circuits have to consume extremely low power, so that some energy is left over to charge a battery or super-capacitor. This trend is captured by movement towards the top-left in the plot shown in Fig. 1.

Fig. 1 – Comparison of Integrated Energy Harvesting Systems showing End-to-End Efficiency vs Quiescent Power
Similarly, the power consumption of analog instrumentation amplifiers, oscillators, and audio power amplifiers is being scaled down to meet the demands of these low-power systems. This trend is captured by movement towards the bottom-right in the plot shown in Fig. 2. Fast power-up and -down is also desired from these circuits to permit high energy-efficiency during intermittent operation. Together, these technologies will lead to devices powered indefinitely from sustainable sources, opening the door to internet of everything, ubiquitous sensing, environmental monitoring, and medical applications.

Analog circuits also serve as bridges between the digital world and the analog real world. Just like actual bridges, analog circuits are often bottlenecks and their design is critical to overall performance, efficiency, and robustness. Nevertheless, since digital circuits, such as microprocessors, drive the market, semiconductor technology has been optimized relentlessly over the past 40 years to reduce their size, cost, and power consumption. Analog circuitry has proven increasingly difficult to implement using these modern IC technologies. For example, as the size of transistors has decreased, the range of analog voltages they can handle as well as their analog performance have decreased, while the variation observed in the analog parameters has increased.

These aspects of semiconductor technology explain two key divergent trends in analog circuits. One trend is to forgo the latest digital IC manufacturing technologies, instead fabricating analog circuits in older technologies, which may be augmented to accommodate the high voltages demanded by increasing markets in medical, automotive, industrial, and high-efficiency lighting applications. Other applications dictate full integration of analog and digital circuits together in the most modern digital semiconductor processes. For example, microprocessors with multiple cores can reduce their overall power consumption by dynamically scaling operating voltage and frequency in response to time-varying computational demands. For this purpose, DC-DC voltage converters can be embedded alongside the digital circuitry, driving research into the delivery of locally-regulated power supplies with increasing efficiency, decreasing die area, and increasing power density. The latest advances are implemented in low cost standard CMOS technologies. These trends are captured by movement towards the top-right in the plot shown in Fig. 3.

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Fig. 2 – Comparison of Integrated 3-to-2000kHz Oscillators showing Power Normalized to Frequency vs Year
Fig. 3 – Comparison of Integrated Switched-Capacitor Power Converters showing Peak Efficiency vs Maximum Power Density
Data Converters – 2017 Trends

Subcommittee Chair: Un-Ku Moon, Oregon State University, Corvallis, OR

Data converters form the key link between the analog physical world and the world of digital computing and signal processing prevalent in modern electronics. The need to faithfully preserve the signal across domains continues to pressure data converters to deliver more bandwidth and greater linearity while continuing to increase power efficiency. The dominance of successive-approximation (SAR) techniques continues at ISSCC 2017 with their extension into pipelined architectures to set new metrics in resolution and conversion speed.

The three figures below represent traditional metrics to capture innovative progress in data converters. The first figure plots power dissipated relative to the effective Nyquist rate ($P/f_{\text{Nyq}}$), as a function of signal-to-noise and distortion ratio (SNDR), to give a measure of ADC power efficiency. For low-to-medium-resolution converters, energy is primarily expended to quantize the signal; thus the overall efficiency of this operation is typically measured by the energy consumed per conversion and quantization step. The dashed trend-line represents a benchmark of 5fJ/conversion-step. ISSCC 2017 heralds the first converter achieving this benchmark while simultaneously demonstrating nearly 80dB SNDR through the use of noise shaping and dynamic amplification techniques. Circuit noise becomes more significant with higher-resolution converters, necessitating a different benchmark proportional to the square of signal-to-noise ratio, represented by the solid line. Contributions at ISSCC 2017 are depicted by the colored legends representing various converter architectures; historical contributions are shown using smaller markers. (Note that a lower $P/f_{\text{Nyq}}$ metric represents a more efficient circuit on this chart.)

The second figure plots signal fidelity vs. the Nyquist sampling rate normalized to power consumption. Higher speeds of operation present additional challenges in maintaining accuracy in an energy-efficient manner. This year, pipelined SAR converters demonstrate gigahertz bandwidths while delivering the levels of accuracy and energy efficiency demanded by modern applications.

The final figure plots achieved bandwidth as a function of SNDR. Sampling jitter or aperture errors coupled with an increased noise bandwidth make achieving both high resolution and high bandwidth a particularly difficult task. Nonetheless, ISSCC 2017 presents multiple approaches demonstrating excellent results in this metric. A continuous-time noise-shaped pipeline joins interleaved converters based on SARs and pipelined SARs to advance the state-of-the-art across a wide range of SNDR and bandwidths.'
Figure 1: ADC power efficiency ($P/f_{\text{synq}}$) as a function of SNDR
Figure 2: Power normalized noise and distortion vs. the effective Nyquist sampling rate
Figure 3: Bandwidth vs. SNDR
RF Subcommittee – 2017 Trends

Subcommittee Chair: Piet Wambacq, imec, Belgium

Introduction

This year, ISSCC 2017 shows ongoing advancements in circuits and subsystems for various applications spanning a broad frequency range from below 1GHz to beyond 1THz. Innovation topics include circuits for RF and mm-wave frequency generation, efficient power-amplification techniques as well as building blocks for mm-wave and THz spectroscopy, imaging applications and broadband communication systems. This document highlights such trends that will emerge at the 2017 ISSCC conference. Papers showcase advances in voltage controlled oscillators, digitally-intensive mm-wave frequency synthesizers, linearized power amplifiers, and efficiency-improving envelope-tracking transmitter front-ends. RF building blocks demonstrate support for complex modulation schemes to enable increased data-rates. Advanced circuit and system techniques as well as antenna interface improvements enable broadband imagers and spectrometers at mm-wave/THz frequencies.

RF and mm-wave frequency generation: The trend is toward high-efficiency frequency generation, ultra-low-voltage frequency generation without compromising figure-of-merit (FOM), and the use of calibration and digital architectures targeting applications such as 5G and wireless LAN. The 2017 ISSCC presents a high-efficiency, high-power multiport radiating element at 114GHz in SiGe BiCMOS technology is demonstrated. An efficient calibration technique, applied to a 27GHz-to-31GHz injection-locking frequency multiplier with quadrature outputs, is introduced. In the area of frequency synthesizers, three papers at ISSCC 2017 highlight advancements in digital architectures: a 50GHz-to-66GHz PLL featuring low-noise and low spur levels by leveraging a high-speed TDC and intensive calibrations; two PLLs based on ring-oscillators, leveraging subsampling phase detection and FIR filtering, respectively, to achieve simultaneously low noise and compact area. An ultra-low voltage DCO in a 16nm FinFET technology with a 188dBc/Hz FOM is shown. As illustrated with a 2017 ISSCC ultra-low-voltage VCO identified in Figure 1, frequency generation with low phase-noise at low power becomes challenging and even more so at higher frequencies.

Efficient power amplification for broadband communications systems: Improving efficiency at the back-off power levels has become an active area of research to support spectrally efficient modulation schemes with high peak-to-average power ratios. Doherty-like power-amplifier topologies and envelope-tracking supply modulation are key enablers to improve the back-off efficiency of transmitters. Increasing signal bandwidths for applications such as carrier-aggregation LTE and WiFi 802.11ac poses challenges for supply modulation. A triple-band mm-wave PA with an offset-line-based transformer is discussed and demonstrates the enhancement of efficiency and bandwidth. A WLAN SoC with a fully-integrated envelope tracker is demonstrated for wideband modulation. A Class-G voltage-mode Doherty power amplifier is presented, which achieves high efficiency at various power backoff levels. The trend to simultaneously optimize power and efficiency is indicated in Figure 2. This year, at ISSCC 2017, wideband PAs achieve high linearity in addition to adequate P_{sat} and PAE for both cellular applications with excellent EVM and mm-wave frequencies over multiple bandwidths.

RX and TX Building Blocks: The 2017 ISSCC will highlight several advances in the state of the art in the RF, mm-wave, and THz domains. Antenna interface improvements include a circulator for TX/RX isolation, a digitally assisted CMOS front-end module, a polar PA with intrinsic nonlinearity compensation, electrical-balance-duplexer impedance detection, and radiator-embedded power combining. Wideband systems for spectroscopy achieve record bandwidths and parallel multitone generation. A 310-to-370GHz array embeds beam steering with independent frequency tuning. High data-rate communication is demonstrated with a 5m 130GHz 12.5Gb/s link and a 105Gb/s 300GHz transmitter with 6 carrier-aggregated 128-QAM channels.
Figure 1: LC Oscillator FoM versus frequency.

Figure 2: PAE (%) vs. output power for recent submicron CMOS PAs.
Wireless – 2017 Trends

Subcommittee Chair: Aarno Pärssinen, University of Oulu, Oulu, Finland

The insatiable need for big-data communication calls for transceivers with high throughput, achieved through higher digital modulation, carrier aggregation, MIMO with beam forming or beam steering, and interference detection and cancellation. As presented at ISSCC 2017, a variety of new techniques have been developed, such as a 5G transceiver employing dual polarized beam steering with a 32-phased array, a 128QAM 4-channel bonding transceiver, a MIMO receiver array with analog/RF spatial equalization and a wideband full-duplex cancellation transceiver, to help push to even higher data-rates.

As seen at ISSCC 2017, high-speed digital complex sampling schemes applied to transmitters, receivers, and fractional-N PLL’s allow RF to scale with digital in more advanced process nodes. Digital PAs replace the area-hungry inductors/transformers with high-speed digital processing circuits running at lower supply voltage. Various kinds of digital PAs such as switched capacitor, inverse Class-D/E and Class-F digital PAs are reported paving the way for a lower cost, miniaturized module. The FOM of all digital fractional-N spurious reduction PLLs continues to improve to enable higher SNR, higher data-rate, and ultimately better spectral efficiency.

At ISSCC 2017, in IoE space, ultra low power and highly integrated system solutions have emerged in various fields. A first sub-GHz ultra-narrow-band DBPSK/GFSK modulation RF transceiver for low-power wide-area networks is reported. In designing IoT devices, there is a well-known trade-off in sensitivity, output power, and blocker tolerance for lower cost and low power. Instead, a higher output power and better sensitivity Bluetooth low-energy transceiver with integrated RF bandpass filter saving overall power consumption is reported.

Figure 1 shows Ultra-Low-Power 2.4GHz and MICS-band Wireless Transmit-Efficiency trends, while Figure 2 shows Ultra-Low-Power 2.4GHz and MICS-band Wireless Receiver Sensitivity Trends. Because many different techniques are used to design the circuits, there is significant scatter in the graphs. However, in both cases, the arrows show the desired trend directions.

![Image of Figure 1: Ultra-Low-Power 2.4GHz and MICS-band Wireless Transmit-Efficiency Trends.](image)
Figure 2: Ultra-Low-Power 2.4GHz and MICS-band Wireless Receiver Sensitivity Trends.
Over the past decade, wireline I/O has been instrumental in enabling the incredible scaling of computer systems, ranging from handheld electronics to supercomputers. During this time, aggregate I/O bandwidth requirements have increased at a rate of approximately 2 to 3x every 2 years. Demand for bandwidth is driven by applications such as memory, graphics, chip-to-chip fabric, backplane, rack-to-rack, and LAN. In part, this demand has been met by expanding the number of I/O pins per component. As a result, I/O circuitry consumes an increasing amount of area and power on today’s chips. Increasing bandwidth has also been enabled by rapidly accelerating the per-pin data rate. Figure 1 shows that per-pin data rate has approximately doubled every four years across a variety of diverse I/O standards ranging from DDR, to graphics, to high-speed Ethernet. Figure 2 shows that the data rates for published transceivers have kept pace with these standards, enabled in part by process technology scaling. However, continuing along this rather amazing trend for I/O scaling will require more than simply transistor scaling. Significant advances in both energy efficiency and signal integrity must be made to enable the next generation of low-power and high-performance computing systems. Papers at ISSCC this year include a 64Gb/s NRZ optical receiver in 14nm CMOS, a 64Gb/s PAM-4 transmitter in 28nm CMOS, and a 100Gb/s coherent optical transceiver in 20nm CMOS featuring 4x64GS/s 8b ADCs and DACs.

Energy Efficiency and Interconnect Density:
Power consumption of I/O circuits is a first-order design constraint for systems ranging from cell phones to servers. As the pin count and per-pin data rate for I/Os have increased, so has the percentage of total power consumed by I/Os. Technology scaling enables increased clock and data rates and offers improved energy, especially for digital components. However, simply increasing per-pin baseband data rates with existing circuit architectures and channels is not always a viable path given fixed system power limits. Figure 3 plots the energy efficiency (expressed in mW/Gb/s, which is equivalent to pJ/b) as a function of channel loss for recently reported transceivers. Looking at the most aggressive designs, the data indicates that the scaling factor between link power and signaling loss is slightly less than unity—in particular, that 30dB channel loss corresponds to a roughly 10x increase in pJ/b. Many recent advances have reduced power for high-speed link components through circuit innovation, including low-power RX equalization (DFE, CTLE), CMOS and resonant clocking, low-swing voltage-mode transmitters and links with low-latency power-saving states. At ISSCC this year, Paper 6.4 demonstrates a 64Gb/s 4-tap FFE PAM-4 TX with 1.2Vppd swing that consumes only 2.3pJ/b. Paper 29.5 combines high signaling density with low power, demonstrating a braid clock signaling scheme over four balanced NRZ lines for interpanel interfaces.

Electrical Interconnect:
There is ever-growing demand for very high data rate communication across a wide variety of channels. Some types of channels, especially those related to medium-distance electrical I/O, such as server backplanes, must support high data rates over high-loss channels. For these links, the key to scaling has been improvements in equalization and clock/data recovery. Recent high-speed transceivers use a combination of fully adaptive equalization methods, including TX FIR, RX CTLE, DFE, as well as RX FIR and/or IIR FFEs. As a result, recent receivers achieve data rates above 28Gb/s across channels with up to 50db of loss. This year at ISSCC, we see examples of transceivers that are starting to extend the equalization range of 56Gb/s wireline communication. This year at ISSCC, Paper 6.2 describes a 60Gb/s NRZ transceiver that compensates 21dB loss at an energy efficiency of 4.8pJ/b. Paper 6.3 presents a 40-56Gb/s PAM-4 receiver with 10-tap direct feedback equalization.

Optical Interconnect:
As the bandwidth demand has accelerated and as electrical channel impairments become increasingly severe with the rise of per-lane data rates, optical interconnects have become an increasingly attractive alternative to traditional electrical wireline interconnects. Optical communication has clear benefits for high-speed and long-distance interconnects because it offers lower channel loss. Circuit design and packaging techniques that have traditionally been used for electrical wireline are being adapted to enable integrated optical links with extremely low power. This has resulted in rapid progress in optical ICs for Ethernet, backplane and chip-to-chip optical communication. At ISSCC this year, a 64Gb/s 1.4pJ/b optical receiver [Paper 29.1], a 40Gb/s PAM-4 transmitter based on a ring resonator optical DAC [Paper 29.3], and an ADC-and-DAC-based analog front-end for coherent optical transceivers [Paper 29.2] are presented.

Concluding Remarks:
Continuing to aggressively scale I/O bandwidth is both essential for the industry and extremely challenging. Innovations that provide higher performance and lower power will continue to be made in order to sustain this trend. Advances in circuit architecture, interconnect topologies, and transistor scaling are together changing how I/O will be done over the next decade. The most exciting and most promising of these emerging technologies for wireline I/O will be highlighted at ISSCC 2017.
Figure 1: Per-pin data rate vs. Year for a variety of common I/O standards.

Figure 2: Data-rate vs. process node and year.
Figure 3: Transceiver power efficiency vs. channel loss.
HISTORICAL TRENDS IN TECHNICAL THEMES

DIGITAL SYSTEMS

DIGITAL ARCHITECTURES & SYSTEMS SUBCOMMITTEE

DIGITAL CIRCUITS SUBCOMMITTEE
This year at ISSCC 2017, process scaling continues with the application of the 10nm node. Process scaling continues to enable integration of more transistors and reduces power consumption, but frequency scaling is slowing down. Thus, performance improvements are now being achieved primarily through architectural innovations.

One continued trend is towards increasing heterogeneity with application-specific CPUs, GPGPUs, and custom accelerators. Thus, computation is moving from general-purpose CPUs to more power-efficient cores to meet performance demands within limited power budgets. From the following graphs, the core numbers (Figure 1) and frequencies (Figure 2) are not growing significantly, but application-specific cores and accelerators represent a growing portion of die area. Heterogeneous computing that enables efficient collaboration among various cores is gaining in importance.

Figure 1. Core counts on processors published at ISSCC.
Using Increased Integration Density to Improve Application Energy Efficiency

The first 10nm chip is a mobile applications processor SoC, as the development cycle is shorter than for high-performance general-purpose CPUs. The new process node provides lower power (Figure 3) and higher performance-per-Watt, even though transistor speed has saturated. Advanced power management techniques – such as integrated voltage regulators, fast voltage-droop detection and mitigation, and adaptive voltage guard bands – are now crucially important to maximize the power efficiency or performance within a power/thermal budget. Continued area scaling allows increased core numbers for CPUs and GPUs, and also additional multimedia features, such as dual cameras, larger screen size, and VR features.
Figure 3. Application processor power trends.

Figure 4 shows application processor feature trends for smart phones. These CPUs are now running up to 2.8GHz, approaching laptop and desktop CPUs. Single-thread performance is improved by micro-architectural improvements and multi-thread performance by adding more cores and more efficient management of differently optimized cores. State-of-the-art incorporates up to ten cores with three distinct power/efficiency points. A new graphics API standard, Vulkan, will utilize multicores more efficiently. Virtual reality (VR) is one of the key drivers of the demand for the evolution of GPUs, displays and cameras. Small CPU sub-systems are being added for I/O and sensor-hub control to ensure low-power always-on functionality. Wireless bandwidth keeps evolving, reaching 1.6Gb/s bandwidth and heading toward 5G in the near future.

Figure 4. Application processor trends in smart phones.
Wired and wireless links continue to increase in bandwidth. As illustrated in Figure 5, a consistent 10× increase in datarate is seen every five years. The IoE revolution is bringing an explosion of demand for network bandwidth. Everything will be connected through wired and wireless networks, generating a tremendous amount of data to be processed/analyzed in the cloud. Correspondingly, IEEE 802.3 400Gb/s is being developed and LTE-A standard is extending to 1.6Gb/s bandwidth; 5G is targeting 10Gb/s-to-100Gb/s, comparable with current WiFi speeds which can enable real-time VR streaming.

[Diagram showing data rates over time]

Deep learning is on the rise, drastically shaking up the landscape of high-accuracy recognition applications, achieving near human performance in visual and acoustic recognition. Yet until now, the computational complexity of typical deep neural networks impedes their execution on resource-scarce mobile or wearable devices. This year, ISSCC 2017 shows strong growth in the area of deep learning processors, significantly improving computational energy efficiency up to multiple TOPS/W, bringing deep neural networks within reach of battery-operated devices. This development has been enabled through innovative memory organization, reduced bit-width computation, and approximate and error-tolerant datapath structures. Figure 6 illustrates the order of magnitude efficiency and throughput improvement to be presented at ISSCC 2017, compared to 2016’s state-of-the-art in deep-learning processors. Benefiting from this efficiency leap, several always-on sensing applications will be showcased. Hierarchical wake-up schemes, which gradually activate more and more complex neural networks and recognition algorithms, are exploited to enable always-on recognition at low average power consumption.
ISSCC 2017 features MediaTek’s 10nm FinFET mobile SoC with a tri-gear deca-core CPU complex running up to 2.8GHz. Logic blocks are integrated to aid software and hardware debug, while new circuit blocks improve system power budget management and reduction in supply droop. A new standard-cell approach is used to mitigate the MEOL performance penalty in the 10nm. IBM describes a 24-core microprocessor implemented in 14nm SOI FinFET technology using 17 metal layers. It features a redesigned core based on an execution slice microarchitecture, contains 8B transistors, and has 120MB of eDRAM L3 cache. STMicro presents an energy-efficient deep convolutional neural network (CNN) SoC implemented in a 28nm FDSOI process. The SoC integrates a host CPU, a 16 DSP array and a convolutional DNN accelerator fed by an on-chip reconfigurable network that reduces on-chip and off-chip memory traffic. It achieves a state-of-the-art efficiency of 2.9 TOPS/W and a peak performance of more than 676GOPS. MIT also presents a low-power standalone speech processor with a voice activity detection mechanism for wake-up, and a feed-forward DNN accelerator for speech recognition. It achieves 4.1× fewer word errors, 3.3× lower core power consumption and 12.7× lower memory bandwidth over the prior art.
Digital Circuits – 2017 Trends

Subcommittee Chair: Edith Beigne, CEA-LETI, Grenoble, France

Demand for higher performance across ubiquitous, connected and energy-constrained platforms ranging from Internet of Everything (IoE) to cloud data-centers continues to drive innovations in all CMOS digital circuit building blocks, with goals of improving energy-efficient performance, lowering cost and design effort, and enhancing security. Classic technology scaling has slowed and circuit design efforts are exploiting technology features, such as body biasing or passive-device advancements, to enable circuit innovation.

Energy Efficiency Techniques and Integrated Voltage Regulators

At ISSCC 2017, energy reduction remains a top priority as power density continues to increase. Voltage regulators, while traditionally being off-chip, are increasingly being integrated on-chip to reduce cost. Low-dropout (LDO) linear regulators, switched capacitor voltage regulators (SCVR), and now, buck voltage regulators are integrated in scaled process nodes to enable faster and fine-grain DVFS of individual functional blocks. The conversion efficiency and current density (Figure 1) of these integrated voltage regulators continues to improve. As well, variation mitigation has become a major trend in digital circuits in order to improve robustness and power efficiency across Process, Voltage and Temperature (PVT). Specific all-digital sensors and adaptive techniques are currently proposed to mitigate these effects on-chip.

![Figure 1 Integrated voltage regulators](image)

Scalable Digital PLLs for Low Jitter Applications

The trend of PLLs is to migrate from analog to digital to include more functionality, cope with variability, and ease scaling to finer geometries. Demand for low jitter PLLs is increasing. The use of more automated digital design flows (e.g. synthesizable and/or standard cells) dramatically reduces development costs but can degrade jitter, requiring new techniques to compensate. Figure 2 highlights metrics for PLLs and DPLLs published at ISSCC over the past 10 years.
Circuits for Hardware Security

With the increasing risk and cost of information theft, hardware-implemented security has become a common circuit element. Though at ISSCC 2017 focus on cryptographic implementation continues, cost-effective PUFs (Physically Unclonable Functions) are now a focus area, such as smart cards and consumer devices. TRNGs (True Random Number Generators) are leveraged to strengthen secret key generation in cryptographic applications. The figure below shows how energy/b has scaled for such structures in recent years at ISSCC, pursuing both low-energy and stable operation at the same time. Figure 3 illustrates the trends in energy consumption for security circuits over time published at ISSCC.
Figure 3. Energy-efficiency evolution in security circuits.
Memory – 2017 Trends

Subcommittee Chair: Leland Chang, IBM, Yorktown Heights, NY, Memory

The demand for high-density high-bandwidth and low-energy memory systems continues on all fronts from high-performance computing to SoC, wearables and IoE. In embedded memory, record bitcell size SRAM in 7nm operates at the MB level, and a 10nm dual-supply SRAM cache is optimized for power/performance. DRAM high-performance memory interface technologies are enhanced for GDDR5X, LPDDR4 and low-voltage LPDDR4X. STT-MRAM is introduced as a non-volatile memory system matching LPDDR2 interface at a competitive 4Gb size. In non-volatile memory space, a 40nm low-power eFlash and 10nm anti-fuse OTP are introduced for embedded applications, meanwhile 64 layer 3b/cell 3D NAND Flash provides 512Gb capacity.

Some current state-of-the-art papers from ISSCC 2017 include:

- Two sub-0.030µm² bitcells in 7nm CMOS are functional at 8Mb and 256Mb array levels.
- An 8Gb GDDR5 is shown to operate at 12Gb/s/pin using a PLL-generated 3GHz clock.
- An 8Gb LPDDR4X DRAM operating at 5Gb/s/pin and 0.6V I/O voltage for low-power high-speed memory access.
- 64 layer 3b/cell 3D NAND Flash at 512Gb with only 132mm² die area.
- A 10nm anti-fuse OTP bitcell that achieves reliable operation at the 32kb array level, operating at supplies as low as 0.525V.

SRAM:

For embedded high-speed applications, SRAM continues to be the memory of choice, from mobile to high-performance servers to IoE. This year, at ISSCC 2017, the latest 7nm FinFET technologies with the smallest bitcells achieved to date for SRAM – down to 0.027µm². Key industry benchmarks for 10nm SRAM and 14nm TCAMs are also presented. Fig.1 shows SRAM bit cell area and \( V_{\text{min}} \) scaling trend.

![Figure 1 – Bit cell and \( V_{\text{min}} \) scaling trend of SRAM.](image_url)
High-Bandwidth DRAM:

In order to maintain the optimal memory hierarchy ratio with respect to storage memory, DRAM continues to scale density, form factor, and bandwidth. This year, at ISCC 2017, benchmarks for the latest interface standards are presented, including GDDR5x for high-bandwidth, low-cost applications and LPDDR4x for low-power applications. Improvements are also demonstrated in very low standby power LPDDR4 DRAMs as well as next-generation transceivers based on time-based circuits and the MIPI C-PHY specification. In addition, a new L4 cache memory tier based on high-bandwidth, low-latency DRAM is shown. Figure 2 shows DRAM bandwidth scaling over the past decade.

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Figure 2 - DRAM data bandwidth trends.
Non-volatile Memories:

In the past decade, significant investment has been made in emerging memories field to find an alternative to floating-gate-based non-volatile memory. The emerging NVMs, such as phase-change memory (PRAM), ferroelectric RAM (FeRAM), magnetic spin-torque-transfer (STT-MRAM), and Resistive memory (RRAM), are showing potential to achieve high cycling capability and lower power per bit in read/write operations. Figure 3 highlights how 3b/cell (TLC) NAND Flash write throughput and a new STT-MRAM with LPDDR2 interface that continue to improve. Figure 4 shows a significant increase in NAND Flash capacity from 256Gb and 512Gb this year. Such high capacities are achieved through advancements in 3-dimensional vertical bit cell stacking technologies.

Figure 3 - Read/write bandwidth comparison of non-volatile memories.
NAND Flash Memory:

As seen at ISSCC 2017, NAND Flash memory continues to advance towards higher density and lower power, resulting in low-cost storage solutions that are replacing traditional hard-disk storage with solid-state disks (SSDs). 3D memory technology becomes a mainstream for NAND Flash memory for the first time in mass-production of semiconductor industries. This year, two 512Gb 3b/cell 3D NANDs with 64 stacked WL layers are reported, continuing the trend to satisfy the ever-growing demand for increased density requirements and lower manufacturing cost. Not only higher density, but also high performance over 45MB/s program throughput and 1GB/s read throughput with lower I/O voltage from 1.8V to 1.2V. Figure 5 shows the observed trend in NAND Flash capacities at ISSCC over the past 20 years.
Figure 5 - NAND Flash memory trends.
HISTORICAL TRENDS IN TECHNICAL THEMES

Innovative Topics

Imagers/MEMS/Medical/Displays Subcommittee

Technology Directions Subcommittee
Sensors are a key building block for the Internet of Everything. They collect the data and are an important part of the value chains that are enabling new services and fueling the need for more internet bandwidth. Increasingly, multiple sensors and their associated interface circuits are being combined on a single chip, or in a single package, allowing multi-parameter sensing and compensation for crosstalk. Digital-centric implementations of sensor interfaces enable these improvements to be maintained in more advanced processes.

MEMS inertial sensors (accelerometer and gyroscopes) are key components used in a wide variety of consumer products, where low power consumption is a key requirement. For automotive applications, reduced vibration sensitivity and drift, but also high precision and reliability, are additional requirements. In addition to consumer applications, with continuing improvements in accuracy, stability and cost, MEMS inertial sensors have emerged as strong contenders for high-performance navigation and positioning-related applications. MEMS microphones continue to improve (the signal-to-noise ratio and linearity), while reducing the size of the sensor.

CMOS temperature sensors continue to improve, with new circuit techniques increasing accuracy and energy-efficiency, supporting wider applications. The new temperature sensors are shown to have accurate calibration on both plastic and ceramic packages.

In an effort to enlarge the application area of touch user interfaces, aside from performance enhancements in noisy environments, natural handwriting with stylus is becoming important to support with a capacitive touch controller. Styluses are classified into two categories: passive and active. Energy-efficient high-SNR readout circuits are required to support a fine tip passive stylus. New touch sensing architectures are being investigated to integrate active stylus functions, such as buttons, pressure, and tilt sensors, with capacitive touch sensors.
IMMD – 2017 Trends (Medical)

Subcommittee Chair: Makoto Ikeda, University of Tokyo, Tokyo, Japan

As illustrated at ISSCC 2017, medical imaging is an important field with a growing number of applications. For improved capability and quality, medical ultrasound is moving toward 3D imaging with large arrays. As the number of transducer elements in arrays increases, the number of connections to the front-end circuitry is becoming a bottleneck. The same trend is obvious for the amount of signal processing needed. To resolve these congestions, MEMS transducers and CMOS technology increasingly allow transducer arrays and their signal processors to be mounted together for photoacoustic and volumetric imaging.

Sensors used for noninvasive monitoring of human body parameters, such as electrocardiogram (ECG), electroencephalogram (EEG), or bio-impedance are trending toward multimodal electrical/optical systems-on-chip (SoCs) to provide more holistic information about the state of health and consciousness of the subject. An interesting application for such an SoC is in accurate assessment of the depth of anesthesia in the operating room.

Both sensor and actuator systems for in-body implantable usage continue to evolve toward more robust and energy-efficient operation. New circuit concepts permit recording of weak biopotential signals in the presence of artifacts, paving the way toward autonomous, closed-loop systems that combine sensing, sense-making, and actuation as part of a single implantable device. This will allow therapy to be applied directly, for instance to suppress drug-resistant seizures without any involvement by the patient. Furthermore, technological approaches for wireless powering and bidirectional communication with these implantable devices continue to advance, with ultrasonic powering and communication gaining traction for deeply implanted devices.
IMMD – 2017 Trends (Imagers)

Subcommittee Chair: Makoto Ikeda, University of Tokyo, Tokyo, Japan

The CMOS-image-sensor business remains one of the fastest-growing segments of the semiconductor industry. Key applications include cellphone cameras, digital still cameras, camcorders, security cameras, automotive cameras, digital-video cameras, wearable devices, gaming and biomedical.

As seen at ISSCC 2017, the resolution and miniaturization races are ongoing but slowing down, and while the performance requirements stay constant, pixel size continues to scale down (see Figure 1). A column-parallel approach based on pipelined and multiple-sampling implementations has become standard for low-power, high-speed, low-noise camera and video applications. Wafer stacking of the image array on a CMOS image signal processor is becoming more common in mobile applications. A three-layer stacked CMOS image sensor with DRAM as a frame buffer has been reported for high-speed pixel readout. A high-speed vision chip with 3D-stacked column-parallel ADCs and 140GOPS programmable SIMD column-parallel PEs has been reported for spatio-temporal image processing.

The importance of digital signal processing technology in cameras continues to grow in order to mitigate sensor imperfections and noise, and to compensate for optical limitations. The level of sensor computation is increasing to thousands of operations-per-pixel, requiring high-performance and low-power digital signal processing solutions. A monolithic dynamic vision sensor supporting an event detection rate of 300M events per second has been reported.

High Dynamic Range (HDR) is now well established in low-cost consumer imaging. As well, global shutters are being introduced to avoid motion artifacts. A 2592×2054 imager with small pixels, low noise, wide dynamic range and global shutter has been demonstrated. Organic photoconductive film continues to make advances with electrically controllable IR sensitivity.

For precision scientific and medical applications, fluorescent lifetime imaging is extended to capture multiple exponential decays using 4-tap lock in pixel and shared pulse generator. Large pixels have been improved with increased conversion gain. A biochip with a fluorescence-based pixel array with an integrated excitation filter and on-chip heater is implemented for real-time amplicon-probe hybridization detection. We now employ single-photon avalanche diodes (SPAD) imager arrays. Deep-submicron CMOS SPADs will meet the requirements for high-resolution, high-accuracy time-to-digital converters (TDCs), and small-pitch imagers with better fill factor.

The market share of CCD imagers continues to shrink and they are now relegated to minor applications. Top-end broadcast and top-end digital cameras have moved from CCD to CMOS sensors (see Figure 1).
Figure 1: Pixel size trends (microns).
Technology Directions – 2017 Trends

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Technology innovations bring the promise of enabling completely new system functionalities or substantially greater efficiency of existing ones. It is significant that harnessing such innovations for the solution of real-world problems requires thinking about technologies in the context of systems. Thus, now, with a focus on IoE, trends in Technology Directions emphasize the embedding of functionality in the real world. In this process, there must be a novel emphasis on both form factor and power management.

Large-area Electronics: Large-area electronics provide transformational form factors for electronic systems. The ability to create systems that are thin, form fitting, and capable of spanning large areas enables the integration of rich functionality within the real world. While materials and devices for large-area electronics began emerging well over a decade ago, demonstrations of systems addressing practical applications of societal importance have reached notable sophistication only in the past few years. This has required overcoming challenges on two important fronts: (1) the substantially lower performance of the devices compared with silicon CMOS, the workhorse technology of today; and (2) the role of key application drivers, and the architectures required to enable these.

With regards to the performance of devices, the field of large-area electronics has seen an evolution from amorphous-silicon, to organic, to metal-oxide semiconductors. An important source of this evolution has been a coupling with trends in the flat-panel display industry, where the demand for larger and higher performance displays has driven innovations and engineering refinement in the materials and fabrication methods for large-area technologies. With the flat-panel-display industry moving from amorphous-silicon to metal-oxide semiconductors, large-area thin-film transistors (TFTs) have benefitted from over an order of magnitude enhancement in mobility, from 1cm^2/Vs to well over 10cm^2/Vs. As illustrated at ISSCC 2017, activities in Technology Directions have focused on harnessing these gains far more broadly in displays, towards diverse IoE applications. This has necessitated careful thinking of the applications and systems architectures.

With regards to systems architectures, though designers now have the benefit of higher performance TFTs for implementing the range of functions required, the performance remains well below that of silicon CMOS. This raises important questions about how and which functions to selectively delegate to the large-area domain. While previous efforts in the systems space focused on demonstrating various blocks, including instrumentation amplifiers, ADCs, microprocessors, power converters, etc., today much more directed principles for designing large-area systems have emerged. This has brought selective and concerted focus on specific blocks, functionalities, and subsystems. ISSCC 2017 captures state-of-the-art thinking and demonstrations along these lines.

For example, this year’s conference presents the first standard-compliant 13.56MHz NFC barcode tag in metal-oxide technology. This is enabled both by materials and processing enhancements at the TFT level and by careful circuit-level design. In another example, the conference presents clear progression in analog-to-digital converters, now achieving ENOB of 8b with input-signal bandwidth to 300Hz. This is enabled by an architecture for asynchronous delta-sigma modulation that eliminates high-rate input sampling and output bitstream transitions. In addition, the conference presents a new architecture for large-scale acquisition of distributed large-area sensors to a silicon-CMOS IC, using frequency-hopping injection-locked TFT oscillators. This is enabled by a resonant LC oscillator topology, which exploits the ability to create high-frequency high-spectral-purity oscillations by exploiting high-quality passives (inductors) that can be fabricated in large-area technologies.

Drivers for Gallium-Nitride (GaN) Transistors: With silicon power transistors hitting limits in efficiency, speed, and power handling, wide bandgap semiconductors, most notably GaN, have taken over in applications where silicon leaves off. The past few years have seen a progression, with GaN devices becoming broadly available commercially and deployed in many applications. With this, Technology Directions has seen corresponding advancement in architectures for silicon-CMOS topologies used to drive these devices. This year, ISSCC 2017 offers two solutions in this direction: one addresses the critical issue of reducing EMI noise due to switching high currents at high frequencies by adaptive-slope gate drive control; another focuses on efficiency and fast switching using an integrated capacitor to form a resonant LC gate-drive structure.

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