ISSCC 2010 TRENDS REPORT

ISSCC remains the pre-eminent forum for the discussion of the latest state-of-the-art integrated circuit solutions across a variety of application areas including:

- Microprocessors
- Imagers, MEMS, Medical, and Display Devices
- Memory
- Radio Frequency
- Wireless Communications
- Wireline Communications
- Data Converters

Over time, ISSCC has observed a number of trends in these application areas in terms of how technology has developed over time, and where it is headed in the both the near and long terms. This report serves as a summary of these trends, as seen by the industrial and academic experts that make up the International Technical Program Committee of the ISSCC.

MICROPROCESSORS

The advances in new materials, device architectures, and processing techniques, have enabled silicon manufacturing technology scaling into the 32 nanometer regime where the transistor channels are comprised of literally just a handful of atoms. The extreme scaled dimensions have enabled massive transistor-integration capacity on commercial silicon chips. The relentless pursuit of performance has driven the utilization of the available transistor capacity and prompted designers to integrate more functions in hardware that push the performance beyond the previously-assumed barriers.

Complexity: Figure 1 shows the trend for the number of transistors integrated in a single silicon chip over the last two decades. Recently, many products have been deployed successfully with more than a billion logic transistors (a staggering four orders of magnitude increase over the earliest microprocessors of the 1980s). It should be noted that the massive integration capacity has also enabled very large multi-megabyte on-die caches, exemplified most notably by IBM's whopping 32 megabytes of embedded DRAM cache on a POWER7™ processor chip.

Power Consumption: The pursuit of increased hardware-implemented functionality on a single die has hit the well known power wall, a barrier set by power-delivery and thermal limits. This event can easily be seen in **Figure 2,** where if anything, maximum power consumption is now exhibiting a downward trend driven by the cost burden of the cooling infrastructure. Achieving this power reduction requires innovative heat-removal solutions and sophisticated on-die power management.

Performance: The trend to lowering the power consumption implies constraining the growth of operating frequency to zero or below, as shown in **Figure 3**. As the usual frequency knob of increased performance is no longer available to architects and designers, the new trend is towards parallelism in the implementation. The best hardware approach to parallelism is to provide parallel execution paths in terms of multiple processor cores on a single chip, or multiple threads running on a single core. This trend of increasing performance through parallelization is well illustrated by **Figure 4** which shows a steady upward trend.

Dynamic Optimization: The combination of high transistor counts and low power (resulting in low operating voltages), along with scaled threshold voltages has incited variability and uncertainty in chips'

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performance and power consumption. Various dynamic variations, such as voltage, temperature, and aging, must be sensed, and the processor adapted to the continuously changing environment.

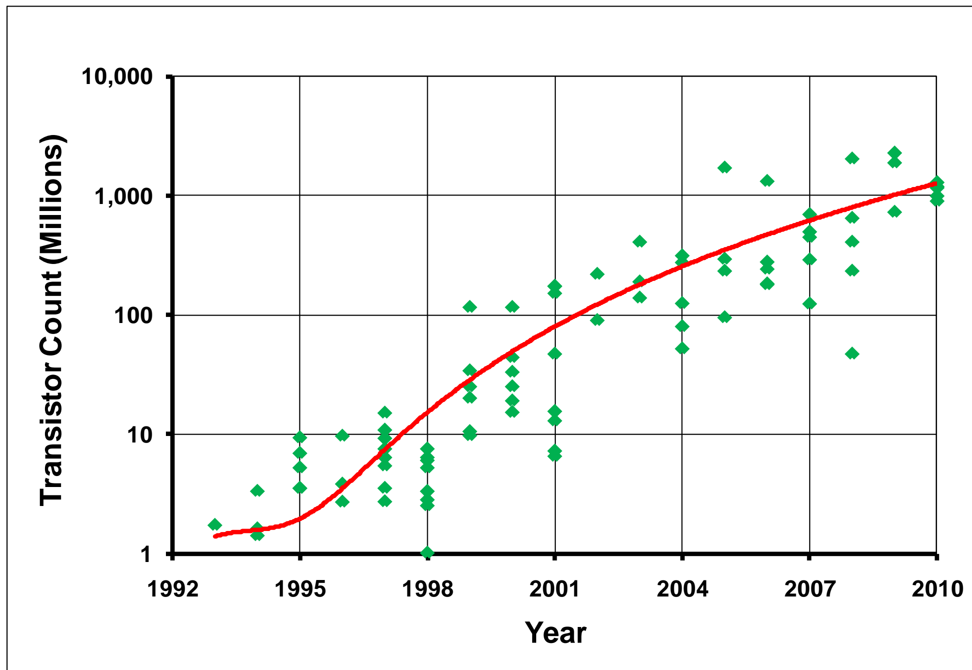

Figure 1. Microprocessor complexity (transistor count) over time

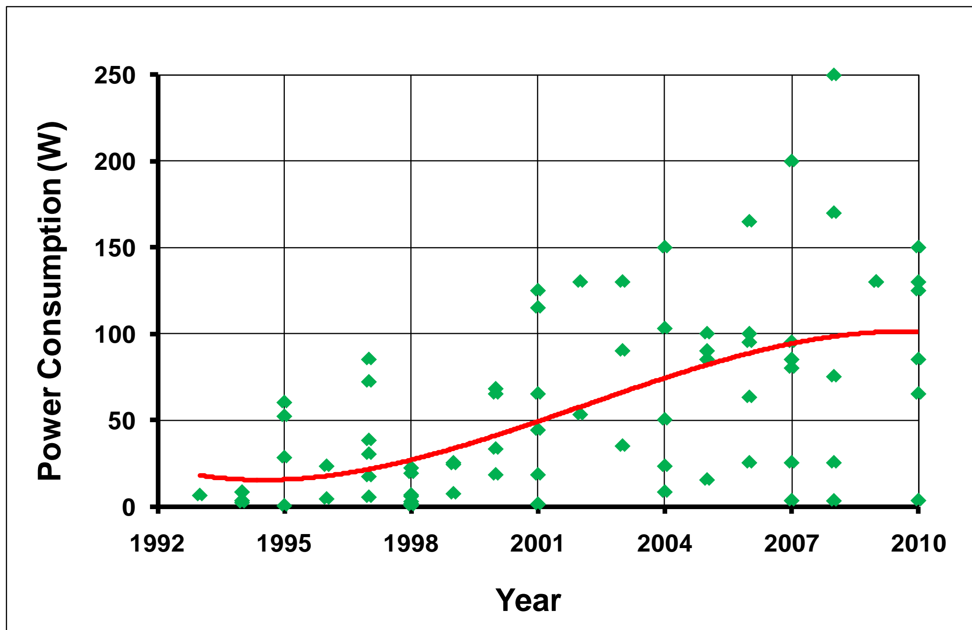

Figure 2. Microprocessor power consumption over time

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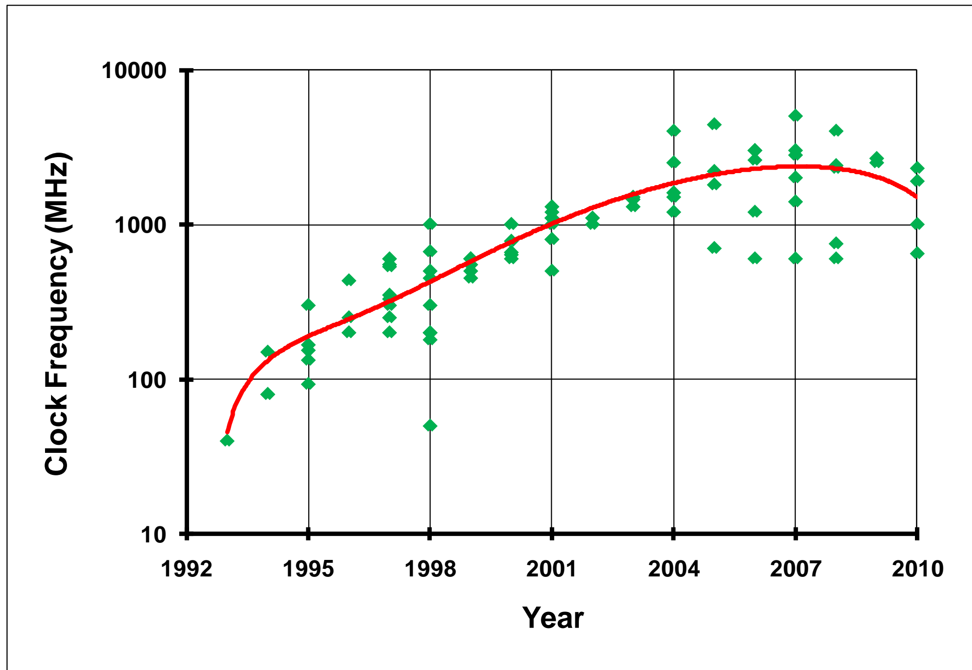

Figure 3. Microprocessor clock frequency over time

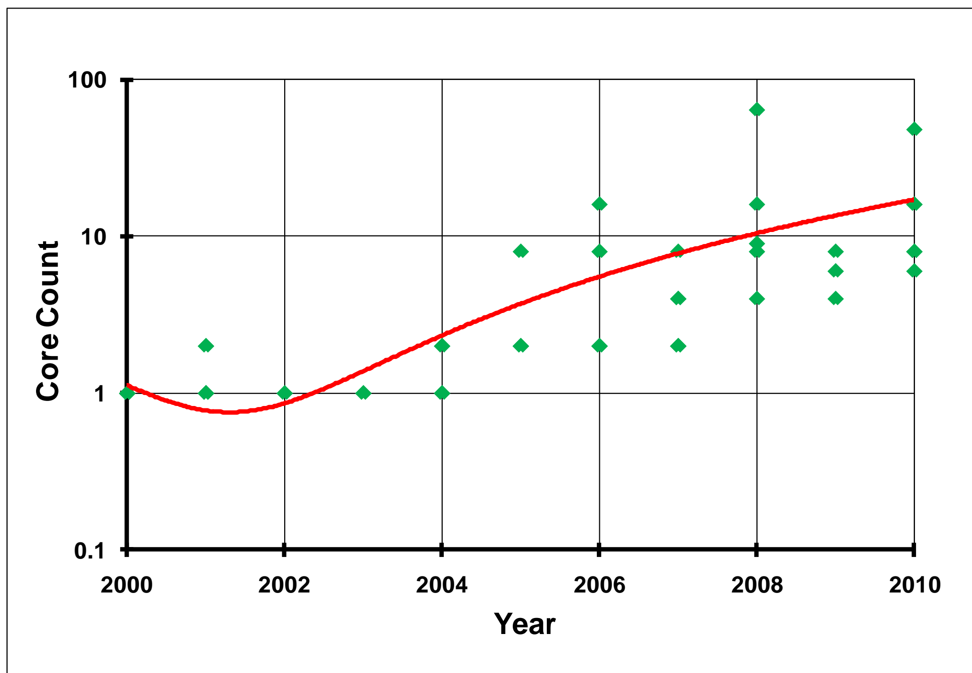

Figure 4. Microprocessor core count over time

SENSORS

Cost Reduction and Growth: Recent advances in design, technology, system integration, packaging of sensors together, and increased product volumes, have dramatically reduced the cost of sensors. Cell phones, game consoles, and other consumer products, now integrate multiple sensors such as accelerometers and gyroscopes in a single package, and have spurred-on significant innovation at the application level. The use of multiple sensors, their downscaling in size, and the ever higher levels of integration available, will lead to further growth in the sensor market.

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Temperature Sensors: Temperature sensors have evolved to lower power, lower cost, and eliminate the need for expensive calibration, without sacrificing sensor accuracy. Today, ultra-low power sensors with a power consumption of less than 1µW are achievable, as well as devices without trimming that deliver an accuracy of better than ±0.2°C over a wide temperature range.

DISPLAYS

OLED Displays: Organic LEDs (OLEDs) represents a revolutionary display technology that promises to displace LCDs. Currently it suffers from new-technology teething issues that have consequences such as the degradation of the image quality with use. Traditionally, straightforward solid-state circuits been used to drive conventional displays, but, now, new electronic methods of monitoring and adjusting the signal applied to the OLED can extend the uniformity and lifetime of the display.

LCD Backlights: Ongoing trends for LCDs include the drive towards larger, thinner, lower-power, and better quality displays. Structured LED backlights have provided benefits in all of these dimensions. In this technique, solid-state circuits are enabling LED backlight drivers to significantly increase the rate at which LED backlights can operate, and allow extended dynamic range by locally varying brightness. In particular, fast-moving sequences look better on screens that operate at higher frame rates.

Mobile Touch Screens: More and more mobile devices have touch screens, eliminating the need for a physical keyboard, allowing the display to fill almost the entire size of the device, and allowing simpler user interfaces. The increased adoption of touch screen technology has resulted in a new breed of IC that combines the display driver and touch-screen controller onto a single chip, delivering the required functionality in a more cost-efficient form factor.

MEDICAL

Evidence-based Medicine: The enormous pressure to demonstrate the effectiveness of medical treatments for outcome and cost-effectiveness will require new sensors and diagnostics for establishing quantitative metrics of success.

Cost Control: Medicine today is under enormous cost pressure. At the same time, technical trends in the semiconductor industry are being applied to the health-care field, helping to establish evidence for effective care, and to support the shift from reactive medicine to proactive care.

Bench-to-Bedside is Practical: Trends in bioelectrical-circuit engineering portend the likelihood that these technologies will transfer soon from “bench” to “bedside” -- moving analysis from the laboratory to the patient. The key enabling features being observed today include lower implant power, higher-complexity algorithm implementation for feature extraction, and faster telemetry for data dissemination and concurrent implant control. Applications of this technology are expanding to include heart-rate monitoring, implantable neural tags for research and chronic monitoring, and acute detection of electroencephelograms (EEG) for seizure monitoring and brain-state detection.

Power Management: A key trend in biomedical devices is enhanced power management. This is critical since the battery or other energy storage unit can dominate the size of the medical device. Inductive links are being prototyped that yield higher efficiency to provide greater flexibility for the supply of energy from external sources.

Complex Measurement Circuits for System Simplicity: Improvements in circuit instrumentation are transferring into the point-of-care arena. Novel measurement techniques, with a particular focus on complex impedance, are providing label-free methods that lower healthcare costs. Other emerging techniques include the combination of magnetic beads for sensing forces and molecular tagging. While these approaches currently do not match state-of-the-art approaches using optical techniques, improvements in sensitivity continue that might provide a disruptive point-of-care approach.

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IMAGE SENSORS

Markets and Growth: The CMOS image sensor business is still one of the fastest growing segments of the semiconductor industry due to cell phone cameras and other digital-imaging applications. The cell phone camera adoption rate is expected to be approximately 90% for 2009, and 3G mobile technology is accelerating the utilization of multiple cameras per cell phone. Other digital imaging markets include traditional digital still cameras (DSCs) and camcorders, as well as emerging markets such as web cameras, security cameras, automotive cameras, digital-cinema cameras, and gaming.

Issues to Address: Many barriers must be overcome in order to maintain market growth in the image sensor industry. These challenges include better image quality, higher sensitivity, higher-sensor resolution, lower cost, higher data-transfer rate, higher system-level integration, lower power consumption, and 3D imaging.

Technical Advances: The resolution and miniaturization races ongoing, and while the performance requirements stay constant, the pixel size continues to scale down. In 2009, CMOS image sensors with 1.4μm^2 pixels became available, and sensors with 1.1μm^2 pixels are expected to be available in 2011. New innovative technologies are constantly being developed in order to compete in this race. These technologies include advanced sub-100 nanometer CMOS image-sensor fabrication processes, backside illumination, digital optics, and wafer-level cameras. The importance of digital-signal-processing technology in cameras continues to grow in order to mitigate sensor imperfections and noise, and to compensate for optical limitations. The level of sensor computation is increasing to thousands of operations per pixel, requiring high-performance and low-power digital-signal-processing solutions. In parallel with these efforts is a trend throughout the image sensor industry toward higher levels of integration to reduce system costs.

Emerging Markets: The trends in emerging markets include lower-bandwidth communication for surveillance cameras, wider dynamic range and optical-communication functions for automotive cameras, faster read-out for digital-cinema cameras, and 3D imaging for gaming. These markets are placing ever increasing functionality and performance demands on today's image sensors, which are in turn delivering an exponential rate of growth in both complexity and performance to ensure they can keep pace.

MEMORY

Overall: Memory design has seen a number of trends over the years: process technology has steadily reduced its minimum feature size, a wide variety of techniques have been developed to improve packing-density, and a myriad of technology/circuit/system optimizations have been created to improve performance and reduce power dissipation. In addition, emerging technologies such as 3D chip stacking and new physical memory mechanisms are pushing the memory R&D frontier even-further forward. Some current state-of-the-are results include:

- 32nm 32Gb MLC NAND flash memory
- 8Gb/s-GDDR5 DRAM with 1Gb capacity
- 32nm SRAM using 7/8/10/12T cells for excellent margins in low-voltage low-power designs
- Revolutionary interface techniques (such as, 8Tb/s/1pJ/b inductive interfaces) developed to accommodate 3D integration
- Emerging memory technologies to realize non-volatile RAM: 45nm 1Gb PCRAM (Phase-Change Memory), FeRAM (Ferrolectric RAM), ReRAM (Resistive RAM), and MRAM (Magnetic RAM).

NAND Flash Memory: Significant developments in NAND flash memory over the past few years, resulting in high-density, low-power, and low-cost storage solutions that are enabling the replacement of traditional hard-disk storage with solid-state disks (SSDs). **Figure 5** shows the observed trend in NAND flash capacities presented at ISSCC in the past 12 years. Note that in 2010, the reduction in process feature sizes, coupled with advanced multi-level cell (MLC) techniques have yielded a 32Gb/chip capacity in a 32nm technology with 2b/cell operation. .

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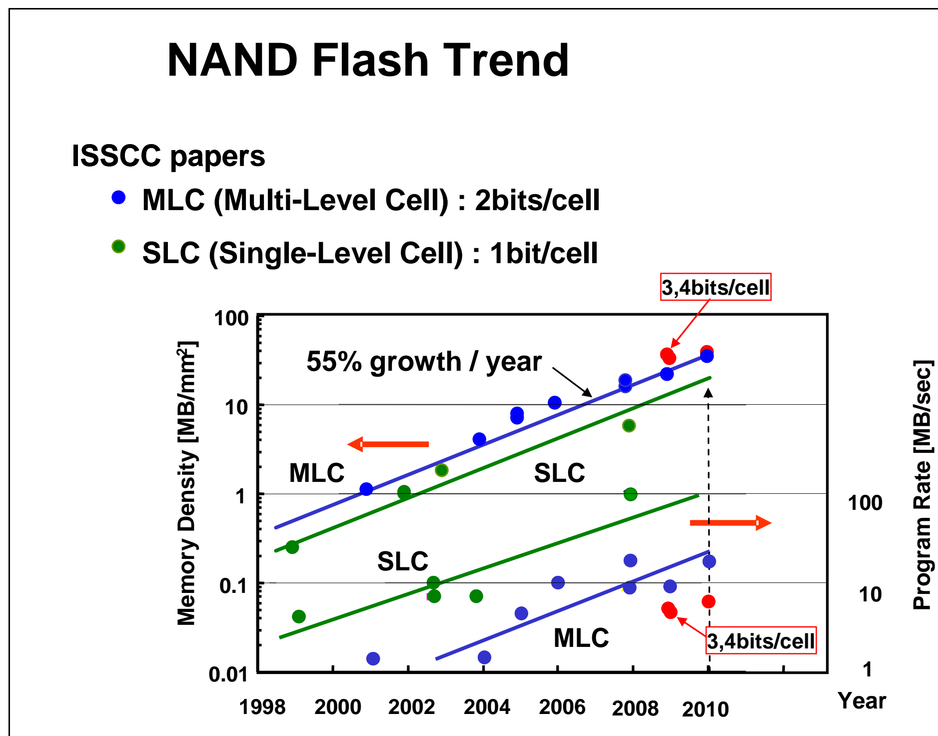

Figure 5. NAND Flash Memory Trends

Solid-State Disks (SSDs): SSD technology is beginning to take off as integration density and bit-cost reduction have made SSDs feasible replacements for conventional hard disk drives (HDDs) in niche applications where the higher costs are tolerable (such as, high-end ultra-portable laptops). Continued optimization of both density and cost will enable SSDs to become more price-competitive, increasing their adoption rate in more mainstream applications, and introducing new requirements for the SSD environment, such as:

- High-bandwidth NAND flash operations
- Optimized organization for SSD systems with 3D chip-stack structures
- Wireless interface schemes for 3D chip-stacks
- Defect control
- High-voltage power supplies for NAND flash memory cell operations

Interfaces: Unfortunately, the gap between memory-core frequency and external-data rate continues to increase as conventional high-speed wired interface schemes such as DDRx and GDDRx for DRAM and NAND flash memory continue to evolve (**Figure 6**). This leads to the need for a larger prefetch size, which is emerging as a major problem in modern memory systems. However, alternatives which accommodate high data rates through the use of wider or differential interfaces will face the problem of increased pin-counts, and enlarged silicon areas. Combined with 3D integration of memory and memory/logic in near-future commercial products, new interface technologies will yield more memory stacking, along with lower-power and higher-bandwidth interfaces. A recent experimental inductive coupling interface demonstration has achieved a 128 NAND chip stack for SSD use, with an 8Tb/s interface for a DRAM/GPU stack.

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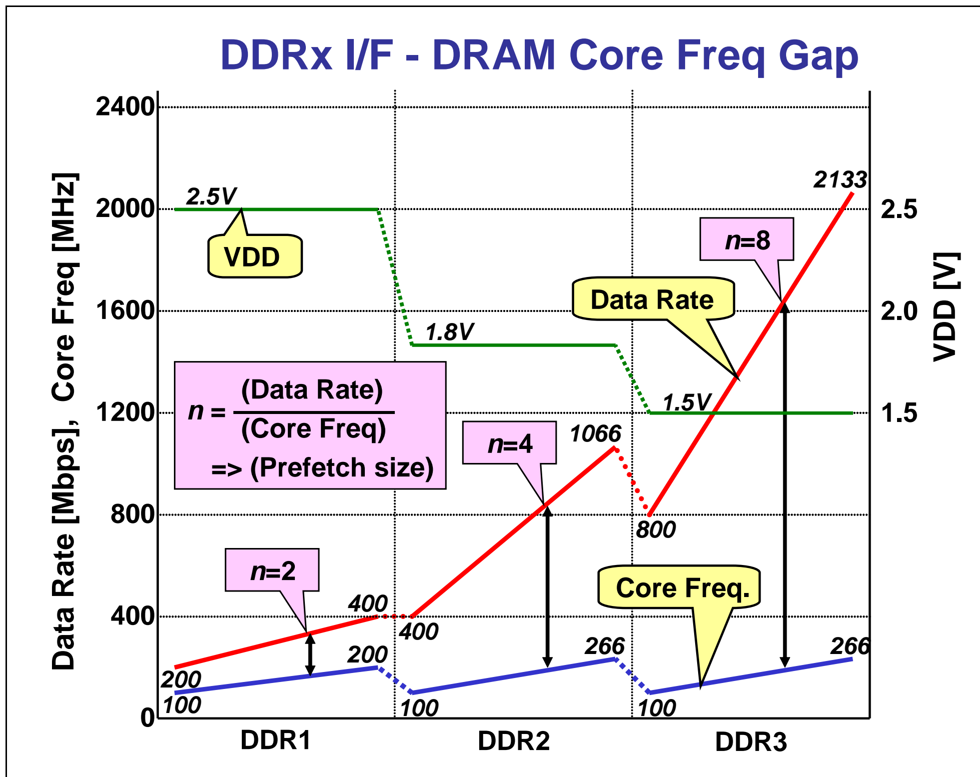

Figure 6. Memory Interface/Core Performance Comparison

Non-Volatile Memory (NVM): New breeds of non-volatile memory technologies aiming at persistent, non-volatile-RAM (NV-RAM) has evolved over time, with ISSCC faithfully tracking these developments over the years. New levels of ReRAM (Resistance RAM) integration and circuit design are presenting new opportunities for extending the memory technology spectrum, together with existing FeRAM/MRAM/PCRAM technologies, as shown in **Figure 7**. Commercial uses of these new breeds of NV-RAM have been very slow to appear because of the rapid reduction of per-bit costs of conventional flash memory technologies already in the market. However, these new technologies are sure to capture some specific markets for lower-power or zero stand-by system implementation in the coming age of green technology.

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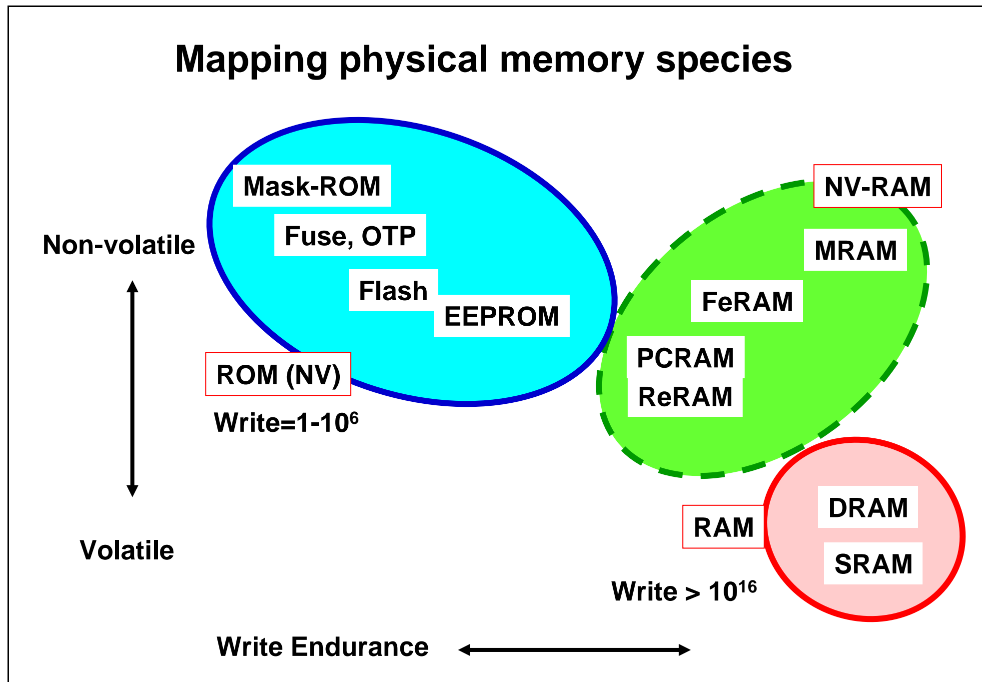

Figure 7. Comparison of NV-RAM Technologies

RADIO-FREQUENCY

Datacom Technologies: As communication needs increase in our ever technological society, there is an increasing need for higher and higher data-communication (datacom) rates. **Figure 8** projects the capabilities of wireless and wireline datacom technologies using current standards. Note that the graph indicates that millimeter-wave frequency bands (for example, 60GHz) provide a potentially-disruptive technology, enabling gigabit/s data rates over a short-range wireless link at speeds well over 1,000Mbits/s (1Gb/s) (for example, 802.15.3 shown below).

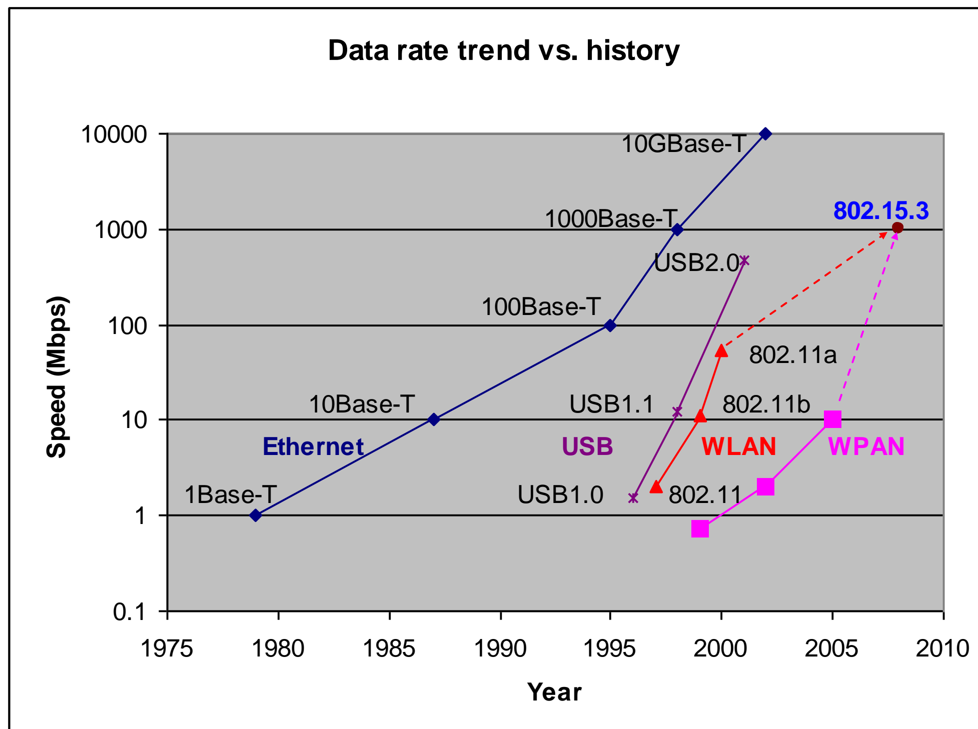

Figure 8. Data Rate Trend Chart

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mm-Wave Imaging: As silicon IC technology advances to higher and higher frequencies, millimeter-Wave (mm-Wave) and TerHertz (THz) technology is enabling fine resolution imaging for biomedical, logistics, and security applications. **Figure 9** shows two images (courtesy of TNO-FEL, the Netherlands), one optical and the other taken using a 94GHz radio imager, which indicate the ability for very-high-frequency radio imaging techniques to reveal a concealed weapon. This technology is now in widespread use throughout airports as part of the passenger security screening protocol.

Figure 9. mm-Wave Imaging Example

WIRELESS COMMUNICATIONS

Multi-Standard Solutions: Approximately four years ago, the first wireless LAN System-on-Chip (SoC) implementation was presented for a single- mode WLAN solution. Now, in just four short years, SoC solutions for WLAN have become multi-band and multi-standard, heralding a truly astonishing evolution! In the past three to four years, the celluar-handset world has evolved from simple radio transceivers to complete SoC solutions that include both the RF transceiver and baseband processor. Currently, 65nm CMOS SoCs are common place for these applications, with the expectation of 45nm CMOS solutions in the very near future. Unfortunately, the number of solutions in these areas is limited to a few companies who have the capabilities and can afford the access to advanced technologies; however, occasional disruptions occur when talented start-up companies with revolutionary ideas appear.

mm-Wave Technologies: Another emerging trend in the wireless area focuses on millimeter-wave radio transceivers, first in SiGe, and now in conventional nanoscale CMOS technologies. Recent wireless sessions at ISSCC have included university groups and companies who have introduced 60GHz high-speed short-range data links. There has also been an evolving trend toward the use of 65nm CMOS in low-cost 77GHz automotive radar solutions that enable these systems to move beyond high-end luxury vehicles to more economical market segments.

Wireless Sensors: Currently research activities in both academia and industry are focusing on all aspects of wireless sensor networks. Today's research efforts are exploring various circuit techniques and radio architectures to achieve the lowest possible power consumption, while enabling battery-less operation via energy scavenging from the surrounding environment. These new architectures encourage the highest

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level of integration in nanoscale CMOS, including the integration of antennas. Such combined efforts are slated to drive low-cost medical devices, inventory tracking, and new ways of interpersonal networking that will lead to ubiquitous wireless communications, continuing to improve (hopefully!) everyone's quality-of-life.

WIRELINE COMMUNICATIONS

General: New applications are emerging such as Internet multi-player gaming, network-based computing/data-storage, transaction-intensive Web 2.0 applications, and high-definition home-entertainment networks. The enabling technologies for these applications are OC-768 (40Gb/s) and 100G Ethernet, high-speed green serial links for data centers, and the deployment of gigabit passive optical networks (GPON), which will provide home-access data rates up to 10 Gb/s, and beyond, in the near future. PON technology reduces system cost by sharing fiber between multiple customers, but challenges transceiver designers by requiring burst-mode operation of amplifiers, and clock recovery with low latency at gigabit data rates. We expect continuing innovation in this area for the foreseeable future.

Data Rates: As shown in **Figure 10**, up to 100 Gb/s data rates are now readily available using CMOS chips. An entire high-definition movie can be transferred at this rate in less than a second. Achieving such high data rates with reasonable power consumption requires advanced energy-efficient clock-and-data recovery and equalization techniques to conquer transmission-channel impairments and speed limitations of low-cost CMOS. ISSCC 2010 showcased a large selection of techniques in various CMOS nodes down to 32 nm, with impressive sub-milliwatt power consumption per Gb/s metrics being achieved for a complete transceiver.

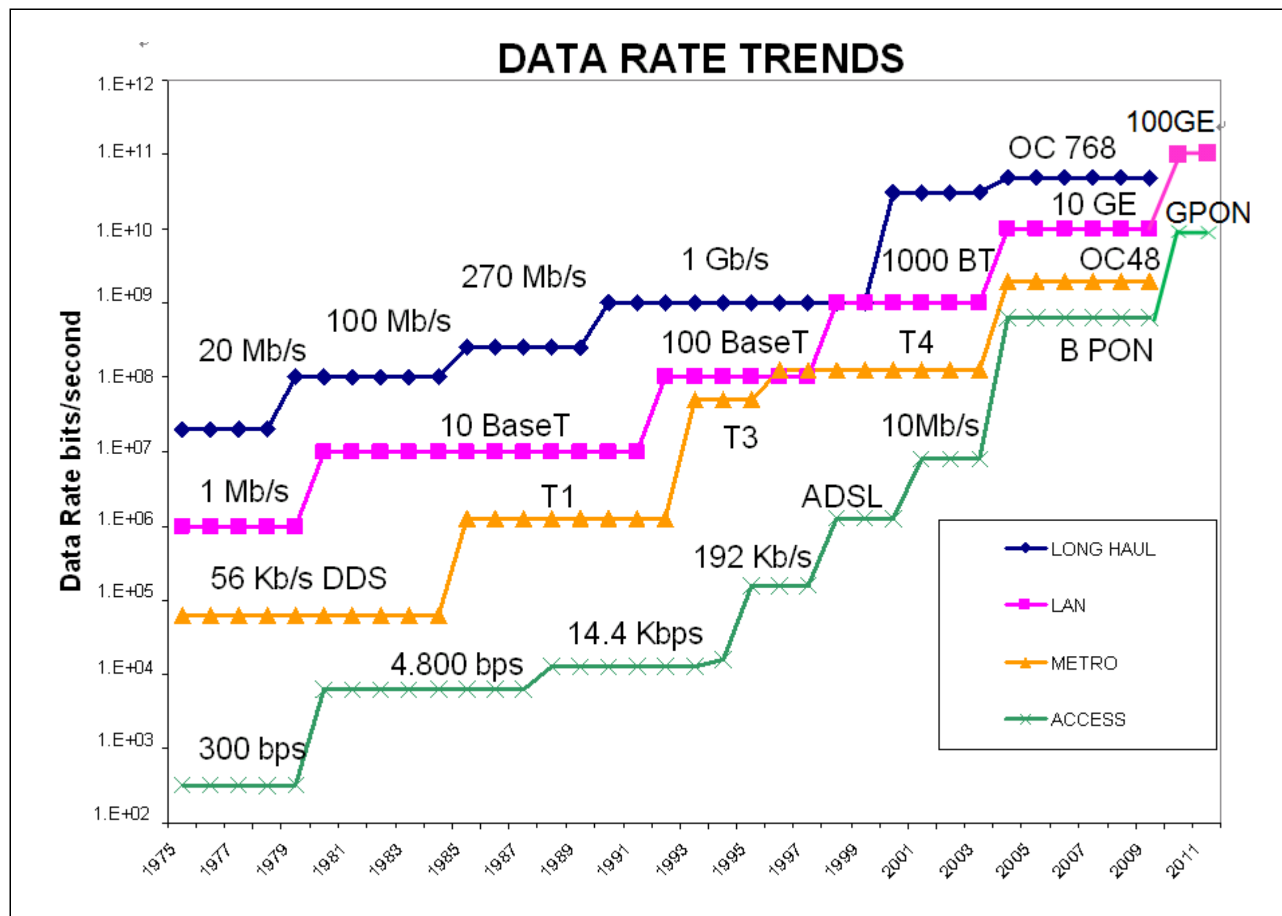

Figure 10. Wireline Data Rate Trends

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Data Converters

High Performance: The bandwidth (BW) and signal-to-noise-and-distortion-ratio (SNDR) are two key performance metrics for an Analog-to-Digital Converter (ADC). These two metrics are related by a fundamental trade-off which states that for a given bandwidth, an ADC cannot have a SNDR exceeding a theoretical maximum for a given level of jitter present in the ADC's sampling clock. The trade-off is illustrated in Figure 11 as two straight lines corresponding to $1000fs_{RMS}$ and $100fs_{RMS}$ jitter in the sampling clock.

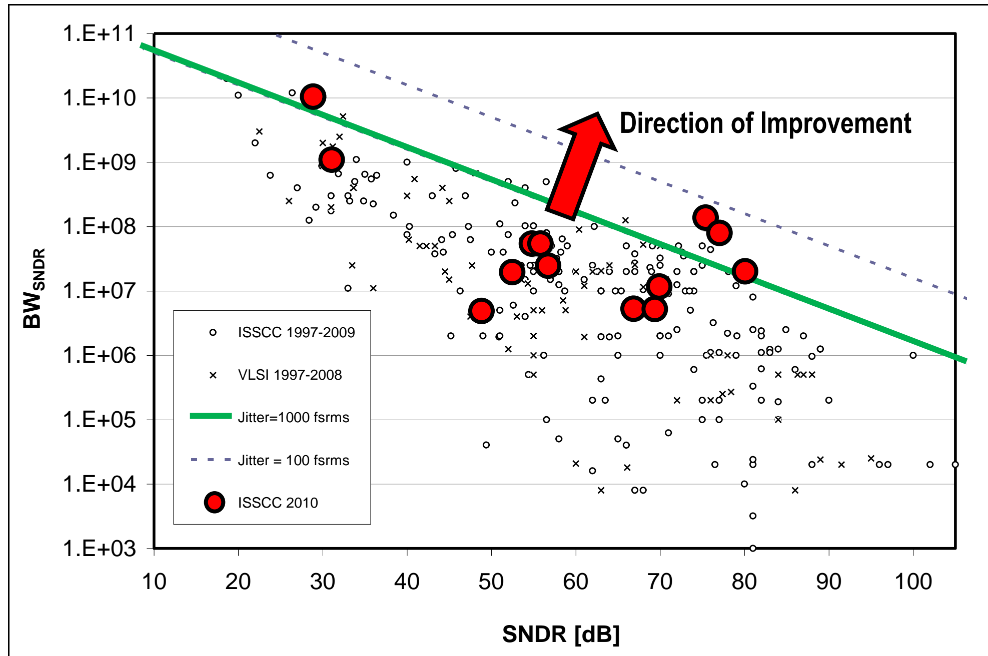

Figure 11. ADC Performance Metrics Trade-off

High Efficiency: A common method of benchmarking the power efficiency of an ADC is to measure the power it consumes per conversion step. Over the years, this figure has steadily improved in the work presented at ISSCC, and continues unabated in 2010. Once again a trade-off exists, this time between the efficiency of the conversion and its accuracy, as expressed by the SNDR. Increasing the SNDR for a given conversion rate typically demands increased power dissipation, thereby reducing the efficiency of the conversion. The trade-off is clearly illustrated in Figure 12 which depicts the reported efficiency of data converters presented at the VLSI Symposium and ISSCC versus their SNDR.

Figure 12 includes two lines plotting energy-per-conversion-step Figure-of-Merit (FOM) values of 100fJ/step and 10fJ/step. The progress in the state of the art in data converter design can be observed by the number of converters moving past these parametric limits to ever better FOMs.

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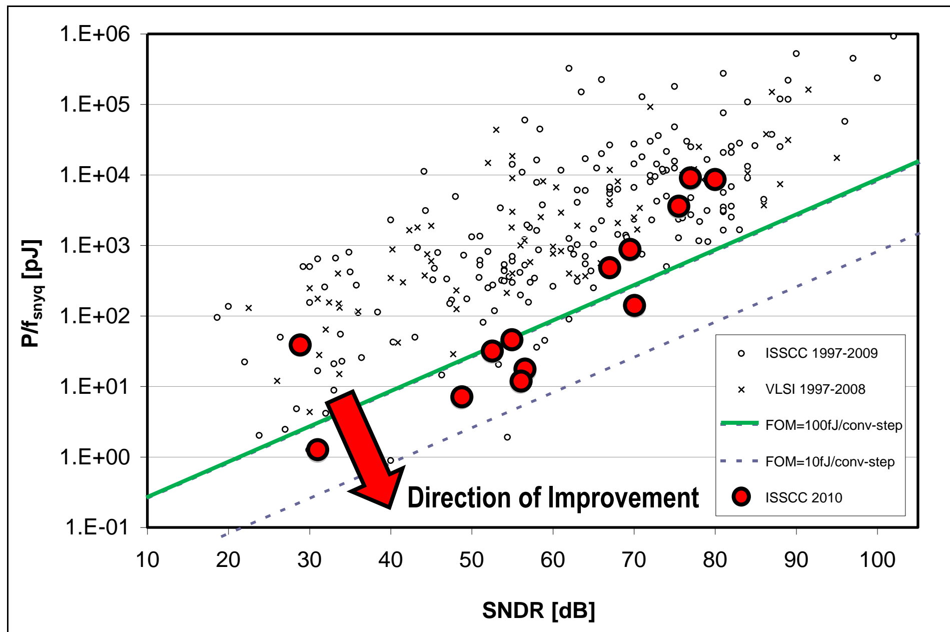

Figure 12. ADC Efficiency Metrics Trade-off

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