IEEE SOLID-STATE CIRCUITS SOCIETY

ADVANCE PROGRAM

2021 IEEE

INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE

FEBRUARY

13, 14, 15, 16, 17, 18, 19, 20, 21, 22

CONFERENCE THEME:

INTEGRATED INTELLIGENCE IS THE FUTURE OF SYSTEMS

NEW THIS YEAR!
Going Virtual

DRAFT 2 - 6 - 2021

12 TUTORIALS:

RF & mm-Wave PAs; Memory Subsystem for HPC/AI; Silicon Photonics; Measuring/Evaluating Security Level Circuits; Calibration Technologies in ADCs; DAC-Based WLn Transmitters; Design Accelerating DNNs; On-Chip Interconnects; Design Amplifier Stability; Fully Integrated Voltage Regulators; Ultra-Low-Power Receiver; Brain Computer Interfaces

SHORT COURSE:

Circuit Design in Advanced CMOS

6 FORUMS:

Energy Efficiency & Flexibility of ML Processors; Accuracy for DC & Analog Circuits; Silicon in the Fight Against Pandemics; Electronics for a Quantum World; System Architectures for 2.5D/3D/Chiplets; Optical/Electrical Transceivers

ISSCC VISION STATEMENT

The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and application to maintain technical currency, and to network with leading experts.

ISSCC 2021 ON-DEMAND CONTENT / RELEASE

ISSCC On-Demand Content	Release Date
Tutorials & Short Course	Friday, February 5, 5:00pm PST
Technical Papers	Friday, February 5, 5:00pm PST
Plenary Talks	Monday, February 15, 7:00am PST
Forums	Friday, February 12, 5:00pm PST

Recorded content available until March 31, 2021

CONFERENCE TECHNICAL HIGHLIGHTS

This year, ISSCC 2021 will be available only virtually.

See next page for Conference schedule details.

ISSCC 2021 CONFERENCE SCHEDULE

ISSCC 2021 Live Sessions • All Times are Pacific Standard Time

Education

ISSCC 2021 • Saturday, February 13th • Tutorials

7:00 am – T1: Fundamentals of RF and mm-Wave Power-Amplifier Designs	**7:20 am – T2:** Fundamentals of Memory Subsystem Design for HPC and AI	**7:40 am – T3:** Silicon Photonics – from Basics to ASICs
8:00 am – T4: Measuring and Evaluating the Security Level of Circuits	**8:20 am – T5:** Calibration Techniques in ADCs	**8:40 am – T6:** Basics of DAC-Based Wireline Transmitters
7:00 am – T7: Basic Design Approaches to Accelerating Deep Neural Networks	**7:20 am – T8:** On-Chip Interconnects: Basic Concepts, Designs, & Future Opportunities	**7:40 am – T9:** Designing Amplifiers for Stability
8:00 am – T10: Fundamentals of Fully Integrated Voltage Regulators	**8:20 am – T11:** Ultra-Low-Power Wireless-Receiver Design	**8:40 am – T12:** Brain Computer Interfaces: Fundamentals to Future Technologies

ISSCC 2021 • Sunday, February 14th • Short Course

7:05 am – SC1: Introduction to PLLs: Phase Noise, Modeling, and Key Wireless Design Considerations	**7:35 am – SC2:** PLL Architectures, Tradeoffs, and Key Application Considerations
8:05 am – SC3: Clocking, Clock Distribution, and Clock Management in Wireline/Wireless Subsystems	**8:35 am – SC4:** Processor Clock Generation, Distribution, and Clock Sensor/Management Loops

Innovations

ISSCC 2021 • Monday, February 15th

6:30 - 7:00 am • ISSCC 2021 Welcome Remarks

7:00 am **Plenary Paper 1.1:** Unleashing the Future of Innovation		**7:45 am** **Plenary Paper 1.2:** Adaptive Intelligence in the New Computing Era
8:30 am **Invited Session 2:** Highlighted Chip Releases: 5G and Radar Systems	**8:30 am** **Invited Session 3:** Highlighted Chip Releases: Modern Digital SoCs	**9:30 am** **Mentoring Session** (Open to all)

ISSCC 2021 • Tuesday, February 16th

7:00 am **Plenary Paper 1.3:** Working at the Intersection of Machine Learning, Signal Processing, Sensors, and Circuits			**7:45 am** **Plenary Paper 1.4:** There's More to the Picture Than Meets the Eye *(and in the future it will become only much more)*	
8:30 am **Session 4:** Processors	**8:30 am** **Session 5:** Analog Interfaces	**8:30 am** **Session 6:** High-Performance Receivers and Transmitters for Sub-6GHz Radios	**8:30 am** **Session 7:** Imagers and Range Sensors	**8:30 am** **Session 8:** Ultra-High-Speed Wireline

Break • Demo Videos • Author Interviews

9:30 - 10:30 am - Book Display

ISSCC 2021 • Wednesday, February 17th

7:00 am **Session 9:** ML Processors From Cloud to Edge	**7:00am** **Session 10:** Continuous-Time ADCs and DACs	**7:00am** **Session 11:** Advanced Wireline Links and Techniques	**7:00 am - Session 12:** Innovations in Low-Power and Secure IoT **7:45 am - Session 13:** Cryo-CMOS for Quantum Computing	**7:00am** **Session 14:** mm-Wave Transceivers for Communication and Radar
8:30 am - Session 15: Compute-in-Memory Processors for Deep Neural Networks **9:15 am - Session 16:** Computation in Memory	**8:30 am** **Session 17:** DC-DC Converters	**8:30 am - Session 18:** Biomedical Devices, Circuits, and Systems **9:15 am - Session 19:** Optical Systems for Emerging Applications	**8:30 am - Session 20:** High-Performance VCOs **9:15 am - Session 21:** UWB Systems and Wake-Up Receivers	**8:30 am - Session 22:** Terahertz for Communication and Sensing **9:15 am - Session 23:** THz Circuits and Front-Ends

Break • Demo Videos • Author Interviews

9:30 - 10:30 am - Book Display

ISSCC 2021 • Thursday, February 18th

7:00 am - Session 24: Advanced Embedded Memories **7:45 am - Session 25:** DRAM	**7:00 am** **Session 26:** RF Power-Amplifier and Front-End Techniques	**7:00 am** **Session 27:** Discrete-Time ADCs	**7:00 am** **Session 28:** Biomedical Systems	**7:00 am** **Session 29:** Digital Circuits for Computing, Clocking and Power Management
8:30 am - Session 30: Non-Volatile Memory **9:15 am - Session 31:** Analog Techniques	**8:30 am** **Session 32:** Frequency Synthesizers	**8:30 am** **Session 33:** High-Voltage, GaN and Wireless Power	**8:30 am** **Session 34:** Emerging Imaging Solutions	**8:30 am - Session 35:** Adaptive Digital Techniques for Variation Tolerant Systems **9:15 am - Session 36:** Hardware Security

Break • Demo Videos • Author Interviews

9:30 - 10:30 am - Book Display

ISSCC 2021 • Friday, February 19th • Special Events & Demos

7:00 am – Special Event: What Technologies Will Shape the Future of Computing?	**7:00 am – Special Event:** Going Remote: Challenges and Opportunities to Remote Learning, Work, and Collaboration	**7:00 am** **Demo Session 1**
8:15 am – Special Event: Favorite Circuit Design and Testing Mistakes of Starting Engineers	**8:15 am - Special Event:** ICs in PandemICs	**8:15 am** **Demo Session 2**

ISSCC 2021 • Saturday, February 20th • Special Events

7:00 am – Special Event: Making a Career Choice	**8:15 am – Special Event:** Student Research Preview

Exploration

ISSCC 2021 • Sunday, February 21st • Forums

7:00 am - F1: Striking the Balance Between Energy Efficiency & Flexibility: General-Purpose vs Special-Purpose ML Processors	**7:00 am - F2:** Pushing the Frontiers in Accuracy for Data Converters and Analog Circuits	**7:00 am - F3:** Silicon Technologies in the Fight Against Pandemics – from Point of Care to Computational Epidemiology

ISSCC 2021 • Monday, February 22nd • Forums

7:00 am - F4: Electronics for a Quantum World	**7:00 am - F5:** Enabling New System Architectures with 2.5D, 3D, and Chiplets	**7:00 am - F6:** Optical and Electrical Transceivers for 400GbE and Beyond

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Tutorials

There are a total of 12 tutorials this year on 12 different topics. Each tutorial, selected through a competitive process within each subcommittee of the ISSCC, presents the basic concepts and working principles of a single topic. These tutorials are intended for non-experts, graduate students and practicing engineers who wish to explore and understand a new topic.

Ali Sheikholeslami
ISSCC Education Chair

The presentations and the videos of all 12 tutorials (90 minutes each)
will be available online, on-demand, as of:
Friday, Feb. 5, 2021, 5:00pm, PST
until March 31, 2021.

Live Q&A sessions for the tutorials will be available on:
Feb. 13, 2021, 7:00am - 9:00am PST

20 minute live session = 5 minute summary + 10 minute Q&A + 5 minute break

The Q&A sessions will be recorded and made available after their live sessions.

Live Q&A - February 13, 7:00am PST

T1: Fundamentals of RF and mm-Wave Power-Amplifier Designs

Hua Wang, *Georgia Institute of Technology, Atlanta, GA*

This tutorial presents an overview of RF and mm-wave power-amplifier (PA) designs in silicon, focusing on the design fundamentals. First, the tutorial introduces PA performance metrics and their impact on wireless systems. Next, it presents the design basics of both PA active circuits and passive networks. The tutorial discusses popular PA classes, such as Class A, AB, B/C, E, F/F-1, and J. Finally, the tutorial concludes with several RF and mm-wave PA design examples.

Hua Wang is an associate professor at the School of Electrical and Computer Engineering at the Georgia Insitute of Technology and the director of the Georgia Tech Electronics and Micro-System (GEMS) lab. Prior to that, he worked at Intel Corporation and Skyworks Solutions. He received his M.S. and Ph.D. degrees in electrical engineering from the California Institute of Technology, Pasadena, in 2007 and 2009, respectively.

Dr. Wang is interested in innovative analog, mixed-signal, RF, and mm-wave integrated circuits and hybrid systems for wireless communication, sensing, and bioelectronics applications. He has authored or co-authored over 170 peer-reviewed journal and conference papers.

Dr. Wang received the DARPA Director's Fellowship Award in 2020, the DARPA Young Faculty Award in 2018, the NSF CAREER Award in 2015, the Qualcomm Faculty Award 2020, and the IEEE MTT-S Outstanding Young Engineer Award in 2017. His GEMS research group has won multiple academic awards and best paper awards, including the 2019 Marconi Society Paul Baran Young Scholar, the IEEE RFIC Best Student Paper Awards (2014, 2016, and 2018), the IEEE CICC Outstanding Student Paper Awards (2015, 2018, and 2019), the IEEE CICC Best Conference Paper Award (2017).

Live Q&A - February 13, 7:20am PST

T2: Fundamentals of Memory Subsystem Design for HPC and AI

Kyu-Hyoun (KH) Kim, *IBM T. J. Watson, Yorktown Heights, NY*

This tutorial will help the audience understand memory subsystem design choices for various applications and systems: including technology, hierarchy, architecture, interface and packaging. The talk will begin with an overview of basics of memory subsystems including memory interfaces (device and module interfaces), controllers, subsystem architectures and RAS & ECC. The tutorial will then move on to explore memory subsystem design optimizations for HPC and AI applications.

Kyu-Hyoun (KH) Kim received his Ph.D. degree in EE from KAIST in 1997. In 1998, he joined Samsung Electronics and led the I/O circuit design team for DDR1/DDR2/DDR3 SDRAM and graphic memories.

He joined IBM T. J. Watson in 2006, and led memory subsystem development for IBM's HPC systems: including BlueGene and Exascale systems. He is now in charge of exploratory AI hardware.

He represents IBM in JEDEC for memory standardization. He received the JEDEC Technical Recognition Award in 2011 and an Award of Excellence in 2019.

Dr. Kim has presented eight papers at the International Solid-State Circuits Conference (ISSCC) as a first author between 1996 and 2009. He received the ISSCC Takuo Sugano Outstanding Paper Award in 2007. He holds 168 U.S. patents.

Live Q&A - February 13, 7:40am PST

T3: Silicon Photonics – from Basics to ASICs

Sudip Shekhar, *University of British Columbia, Vancouver, Canada*

The impact of silicon photonics is expected to grow exponentially in the next decade, driven by the demand for routing, switching, sensing, and computing massive amounts of data.

In this tutorial, the basics of silicon photonic devices will be first presented briefly. Then state-of-the-art examples of silicon photonics and CMOS circuits will be described for high-speed intensity-modulation and coherent links, router-switches, biomedical sensing, and compute accelerators.

Sudip Shekhar received his B.Tech. degree from the Indian Institute of Technology, Kharagpur, and the Ph.D. degree from the University of Washington, Seattle, in 2003 and 2008, respectively.

From 2008 to 2013, he was with the Circuits Research Laboratory, Intel Corporation, Hillsboro, OR, USA, where he worked on high-speed I/O architectures. He is currently an Associate Professor of Electrical and Computer Engineering with the University of British Columbia. His research interests include circuits for high-speed electrical and optical I/O interfaces, frequency synthesizers, and wireless transceivers.

Dr. Shekhar was a recipient of the IEEE Transactions on Circuit and Systems Darlington Best Paper Award in 2010 and a co-recipient of the IEEE Radio-Frequency IC Symposium Best Student Paper Award in 2015.

Live Q&A - February 13, 8:00am PST

T4: Measuring and Evaluating the Security Level of Circuits

Ingrid Verbauwhede, *KU Leuven, Leuven, Belgium*

When we design for low power, we estimate the power consumption at design time and measure it after fabrication and before we submit it to ISSCC. The same must be done with the security evaluation of a circuit: it should be estimated at design time, and measured after fabrication. It is however difficult to measure security. Therefore, in this tutorial, we plan to show how to perform the security evaluation for different classes of circuits: true random number generators, physically unclonable functions and side-channel evaluation of cryptographic implementations.

When designing a true random number generator, statistical tests on the output data are not sufficient: important in this context are the NIST standards SP800-90B and the German BSI AIS20/31 standards to evaluate true randomness. In the context of physically unclonable functions, established standards do not exist yet: here it is important to evaluate how much is the total cost to generate a full-entropy key. When evaluating the resistance to side-channel and fault attacks, it is important to describe the set-up of the experiments. If not, the only conclusion one can make is that the circuit resists an evaluation with the given set-up.

Dr. Ir. Ingrid Verbauwhede is a Professor in the COSIC research group of the Electrical Engineering Department of the KU Leuven. She is also adjunct professor at the University of California, Los Angeles. She received her PhD degree from the KU Leuven and was a post-doctoral researcher at UC Berkeley. At COSIC, she leads the secure embedded systems and hardware group. She is a Member of IACR and a Fellow of the IEEE. She was elected as member of the Royal Flemish Academy of Belgium for Science and the Arts in 2011. She is a recipient of an ERC Advanced Grant in 2016 and received the IEEE 2017 Computer Society Technical Achievement Award.

She is a pioneer in the field of efficient and secure implementations of cryptographic algorithms on many different platforms: ASIC, FPGA, embedded, cloud. With her research she bridges the gaps between electronics, the mathematics of cryptography and the security of trusted computing, including physically unclonable functions and true random number generators. Her group owns and operates an advanced electronic security evaluation lab. She is the author and co-author of more than 300 publications in conferences, journals, book chapters and books.

Live Q&A - February 13, 8:20am PST

T5: Calibration Techniques in ADCs

Ahmed Ali, *Analog Devices, Greensboro, NC*

Digitally assisted ADCs have become mainstream. Fine geometry processes and the insatiable need for higher resolution ADCs at higher sample rates have made sophisticated digital assistance a necessity. In this tutorial, we cover some of the advanced calibration techniques for high-speed and high-resolution ADCs. These include techniques to correct for inter-stage gain and settling errors, amplifier non-linearity, memory, DAC and reference errors. The tutorial will discuss the advantages and limitations of the different approaches, some of the practical considerations, and some state-of-the-art examples.

Ahmed M. A. Ali received the Ph.D. degree in electrical engineering from the University of Pennsylvania. He is a Fellow at Analog Devices, where he has led the design and development of several industry and world firsts in the high-speed data converter field. Before Analog Devices, he was with Texas Instruments and an Adjunct Assistant Professor at the University of Pennsylvania. He is an Associate Editor of the IEEE Transactions on Circuits and Systems I and was an SSCS Distinguished Lecturer. He is the author of the book: “High Speed Data Converters”, by the Institution of Engineering & Technology (IET).

Live Q&A - February 13, 8:40am PST

T6: Basics of DAC-Based Wireline Transmitters

Friedel Gerfers, *Technische Universität Berlin, Berlin, Germany*

This tutorial presents a practical overview of current-mode and voltage-mode DAC drivers, focusing on the fundamentals, accuracy challenges and design solutions.

First, the tutorial explains transmitter specifications for swing, jitter, equalization and linearity, while also introducing DAC performance metrics and discussing their overall impact on wireline systems.

Next, the current-mode and voltage-mode DAC architectures are introduced while highlighting the pros and cons of each. High-speed design challenges, bandwidth and non-linearity trade-offs are reviewed. PVT and mismatch effects, swing enhancements and calibration techniques are introduced.

The tutorial concludes with several DAC design examples utilizing deep submicron CMOS technologies reaching up to 56Gbaud/s.

Friedel Gerfers is a full professor in the Computer Engineering and Microelectronics Department at the Technische Universität Berlin, Germany and holds the Einstein-Professorship for Mixed-Signal Circuit Design.

He received the Dr.-Ing. degree from the Albert-Ludwigs-University Freiburg, Germany, in 2005.

Thanks to his entrepreneurial spirit, he co-founded two the technology start-ups in 2009 and 2018: NiederRhein Technologies, in Mountain View, USA and IC4X GmbH, in Berlin, Germany, which specialize in the development of high-performance analog and mixed-signal circuits and systems.

Prof. Gerfers is an author of the book “Continuous-Time Sigma-Delta A/D conversion, Fundamentals, Error Correction and Robust Implementations”.

Live Q&A - February 13, 7:00am PST

T7: Basic Design Approaches to Accelerating Deep Neural Networks

Rangharajan Venkatesan, *NVIDIA, Sunnyvale, CA*

Deep neural networks are used across a wide range of applications. Custom hardware optimizations for this field offer significant performance and power advantages compared to general-purpose processors. However, achieving high TOPS/W and/or TOPS/mm^2 along with the requirements for scalability and programmability is a challenging task.

This tutorial presents various design approaches to strike the right balance between efficiency, scalability, and flexibility across different neural networks and towards new models. It presents a survey of (i) different circuits and architecture techniques to design efficient compute units, memory hierarchies, and interconnect topologies, (ii) compiler approaches to effectively tile computations, and (iii) neural network optimizations for efficient execution on the target hardware.

Rangharajan Venkatesan is a Senior Research Scientist at NVIDIA. He received his B.Tech. degree in Electronics and Communication Engineering from the Indian Institute of Technology, Roorkee in 2009 and his Ph.D. degree in Electrical and Computer Engineering from Purdue University in 2014. His research interests include machine learning accelerators, high-level synthesis, spintronic memories, and SoC design methodologies. Dr. Venkatesan’s paper on scalable deep-learning accelerator design received the Best Paper Award at the International Symposium on Microarchitecture (MICRO), 2019. His work on spintronic memory design was recognized with the Best Paper Award at the International Symposium on Low Power Electronics and Design (ISLPED), 2012 and a Best Paper nomination at the Design, Automation and Test Conference and Exhibition (DATE) in Europe, 2017. Dr. Venkatesan’s work on FinFET-based SRAM also received a Best paper nomination at the Design, Automation and Test Conference and Exhibition (DATE) in Europe, 2015. Dr. Venkatesan has been a member of the technical program committees of several leading IEEE conferences including the International Solid-State Circuits Conference (ISSCC), the International Symposium on Microarchitecture (MICRO), the Design Automation Conference (DAC), and the International Symposium on Low Power Electronics and Design (ISLPED).

Live Q&A - February 13, 7:20am PST

T8: On-Chip Interconnects: Basic Concepts, Designs, & Future Opportunities

Yvain Thonnart, *CEA-List, Grenoble, France*

On-chip communication impacts the performance, energy efficiency, and area of systems-on-chip, multi-processors and highly parallel accelerators. This tutorial introduces a range of design options for on-chip interconnects. It presents routing schemes and mapping of different protocol families, flow-control and arbitration, synchronization strategies across clock domains, and fully asynchronous circuits. Finally, it introduces the potential of 3D-chip integration for on-chip communication.

Yvain Thonnart graduated from the Ecole Polytechnique and received the MS degree in 2005 from Telecom ParisTech, France. In 2005, He joined the Technological Research Division of CEA, the French Alternative Energies and Atomic Energy Commission, within CEA-Leti until 2019, then within CEA-List. He is now senior expert on communication & synchronization in systems-on-chip, and scientific advisor for the mixed-signal lab. His main research interests include asynchronous logic, networks-on-chip, physical implementation, emerging technologies integration, and interposers. He has contributed to and led several digital circuits projects, and co-authored more than 60 technical papers and 10 patents.

Live Q&A - February 13, 7:40am PST

T9: Designing Amplifiers for Stability

Viola Schaffer, *Texas Instruments, Freising, Germany*

Most amplifier designers spend at least as much or more effort assuring stability under all operating conditions with proper frequency compensation than on other amplifier features. This tutorial will revisit the basics of frequency compensation such as Miller, parallel, nested-Miller and feed-forward compensation and compare them in terms of power efficiency and load-drive capabilities. We will look into the loading effects of subsequent stages, common design traps and round up with a case study of recently published amplifiers.

Viola Schäffer was born in Szeged, Hungary in 1974. She received the M.S. degree in electrical engineering from the University of Arizona, Tucson in 1999.

She joined Texas Instruments Incorporated (formerly Burr-Brown Corporation) in 1998 and has been working as an analog IC design engineer/manager at various locations including Tucson, Arizona, as well as Erlangen and Freising in Germany. She was elected Distinguished Member Technical Staff in 2018. Her work focuses on precision signal conditioning including instrumentation and programmable-gain amplifiers, power amplifiers, industrial drivers as well as magnetic-based current sensors. She holds 17 patents related to this work with several applications pending.

Live Q&A - February 13, 8:00am PST

T10: Fundamentals of Fully Integrated Voltage Regulators

Yan Lu, *University of Macau, Macao, China*

Fully integrated voltage regulators (FIVRs) enable fast dynamic voltage and frequency scaling for energy-efficient high-performance digital systems. This tutorial will cover the fundamentals of low-dropout regulators (LDOs), as well as switched-capacitor (SC) and inductor-based DC-DC converters. Emphasis will be put on design considerations of analog/digital/mixed control, PID control for FIVR, resonant SC, and hybrid DC-DC converters. Last but not least, we will have a brief review of distributed FIVR designs.

Yan Lu received his B.E. and M.Sc. degrees in Microelectronics from South China University of Technology, and his Ph.D. degree in Electronic and Computer Engineering from the Hong Kong University of Science and Technology (HKUST). Since 2014, he has been with the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, where he is now an Associate Professor.

His research interests include fully integrated voltage regulators, DC-DC converters, and wireless power transfer. He is a recipient/co-recipient of the IEEE SSCS Pre-Doctoral Achievement Award, the IEEE CAS Society Outstanding Young Author Award, and the ISSCC 2017 Takuo Sugano Award for Outstanding Far-East Paper. He is currently a member of the Technical Program Committee of ISSCC and CICC.

Live Q&A - February 13, 8:20am PST

T11: Ultra-Low-Power Wireless-Receiver Design

David D. Wentzloff, *University of Michigan, Ann Arbor, MI*

Pervasive-computing and new wireless-sensing applications have re-energized the need for ultra-low-power (ULP) radios and wakeup receivers (WuR). These are used to improve the efficiency of wireless networks in multiple ways. This talk covers recent trends in ULP wireless receiver design, ULP receiver implementations, and design tradeoffs with examples of common ULP receiver architectures as well as examples of how industry wireless standards are adopting signaling to support ULP receivers.

David Wentzloff received a BS in Electrical Engineering from the University of Michigan, and a Ph.D. in Electrical Engineering from MIT. Since 2007, he has been with the University of Michigan, where he is currently an Associate Professor of Electrical Engineering and Computer Science. His research focuses on RF integrated circuits, with an emphasis on ultra-low-power design. In 2012, he co-founded Everactive; a fabless semiconductor company developing ultra-low-power wireless SoCs, where he is currently a co-CTO.

Live Q&A - February 13, 8:40am PST

T12: Brain Computer Interfaces: Fundamentals to Future Technologies

Rikky Muller, *University of California, Berkeley, CA*

Fueled by recent major investments, brain computer interfaces (BCIs) stand to revolutionize the treatment of neurological conditions, and in the future, the human experience. This tutorial will highlight key challenges in the realization of implantable BCIs such as closed-loop operation, miniaturization, and scale. We will start by covering fundamental circuit building blocks and their interactions with electrodes, signals, and tissues. We will then go through an example of how to minimize the volume of a wireless implant.

Rikky Muller is an Assistant Professor of Electrical Engineering and Computer Sciences at UC Berkeley where she holds the S. Shankar Sastry Professorship in Emerging Technologies. She is a Co-director of the Berkeley Wireless Research Center (BWRC), a Core Member of the Center for Neural Engineering and Prostheses and an Investigator at the Chan-Zuckerberg Biohub. Her research group focuses on emerging implantable and wearable medical devices and in developing low-power, wireless microelectronic and integrated systems for neurological applications. Prof. Muller was also the Co-founder of Cortera Neurotechnologies, a medical device company focused on closed-loop deep brain stimulation technology that was founded in 2013 and acquired in 2019.

Short Course: PLLs, Clocking, and Clock Distribution

On Demand Content will be available on
Friday, February 5, 2021, 5:00PM PST

Live Session: Q&A and Discussion:
Sunday, February 14, 7:00-9:00 AM PST

30 minute live session = 10 minute summary + 15 minute Q&A + 5 minute break

Q&A Time:	Topic:
7:00 AM	Introduction by Chair, **Daniel Friedman** *IBM Thomas J. Watson Research Center, Yorktown Heights, NY*
7:05 AM	**Introduction to PLLs: Phase Noise, Modeling, and Key Wireless Design Considerations** **Behzad Razavi,** *University of California, Los Angeles, CA*
7:35 AM	**PLL Architectures, Tradeoffs, and Key Application Considerations** **Woogeun Rhee,** *Tsinghua University, Beijing, China*
8:05 AM	**Clocking, Clock Distribution, and Clock Management in Wireline/Wireless Subsystems** **Mozhgan Mansuri,** *Intel, Hillsboro, OR*
8:35 AM	**Processor Clock Generation, Distribution, and Clock Sensor/Management Loops** **Phillip Restle,** *IBM Thomas J. Watson Research Center, Yorktown Heights, NY*

Introduction

High performance phase-locked loops are critical enabling elements for an extraordinary range of applications. Wireless applications demand low noise, frequency agility, and support for advanced power management. Wireline applications demand exceptional noise performance at very high operating frequencies. Data converters also demand very high performance clocks to achieve performance targets. Processors and SoCs demand flexible, highly responsive clock subsystems. And once the clock is generated, the challenge of distributing it to target sub-blocks without losing the performance the PLL designer worked so hard to achieve remains. This short course will therefore cover topics in frequency synthesis as well as clock distribution and management. The first presentation will describe the fundamentals of PLL architecture and modeling and key design considerations for wireless applications. The second presentation will present a range of architectural choices, including digital and hybrid PLL fundamentals, along with design examples focused on key application considerations. The third presentation will describe approaches for implementing clock subsystems in wired and wireless communication examples. Finally, the fourth presentation will explore clock distribution and management techniques for large-scale processor or ASIC designs.

Live Q&A - February 14, 7:05am PST

SC1: Introduction to PLLs: Phase Noise, Modeling, and Key Wireless Design Considerations

Behzad Razavi, *University of California, Los Angeles, CA*

This presentation deals with PLL fundamentals and their role in wireless systems. Following a brief overview of basic PLL operation, we study its imperfections and their impact on the performance. This culminates in the study of phase noise and its formulation in PLLs. We then introduce modeling methods for fast and relatively accurate PLL simulation. Finally, we study specific issues related to RF synthesis and look at the new trends in synthesis design.

Behzad Razavi is professor of Electrical and Computer Engineering at UCLA. He has published eight books and 200 papers. He has received eight IEEE Best Paper awards and five teaching and education awards.

Live Q&A - February 14, 7:35am PST

SC2: PLL Architectures, Tradeoffs, and Key Application Considerations

Woogeun Rhee, *Tsinghua University, Beijing, China*

A phase-locked loop (PLL) is a key building block in both wireless and wireline communications. For wireless systems, the ΔΣ PLL-based synthesizer plays a critical role in modern transceivers not only as a local oscillator but also as a phase modulator with direct digital modulation. As to wireline systems, low-jitter clock generation and versatile clock-and-data recovery circuits are critical in high data-rate I/O links. However, diversified PLL architectures with different tradeoffs make it difficult for circuit designers to choose the right design solution for various applications. This presentation discusses PLL architectures and application aspects with key design tradeoffs.

Woogeun Rhee received the B.S. degree from Seoul National University, Seoul, Korea, the M.S. degree from the University of California, Los Angeles, and the Ph.D. degree from the University of Illinois, Urbana-Champaign. From 1997 to 2001, he was with Conexant Systems, Newport Beach, CA, where he developed low-power low-cost fractional-N synthesizer products. From 2001 to 2006, he was with IBM Thomas J. Watson Research Center, Yorktown Heights, NY and worked on clocking area for high-speed I/O serial links, including low-jitter phase-locked-loops, clock-and-data recovery circuits, and on-chip testability circuits. In 2006, he joined the faculty at the Institute of Microelectronics, Tsinghua University, Beijing, China and is currently a Professor. He has published 150 IEEE papers and holds 24 U.S. patents. He was the recipient of the IBM Faculty Award.

Live Q&A - February 14, 8:05am PST

SC3: Clocking, Clock Distribution, and Clock Management in Wireline/Wireless Subsystems

Mozhgan Mansuri, *Intel, Hillsboro, OR*

The performance of high-speed wireline and wireless subsystems highly depends on their clock quality. As data rates continue to scale aggressively, practical understanding of clocking design tradeoffs to optimize system power and area while achieving target bandwidth is crucial. In this short course, different aspects of clocking from circuit implementation to system architecture are discussed to provide insight into challenges and design choices for an optimum clocking solution. Clock generation techniques such as phase-locked loops (PLLs), delay-locked loops (DLLs) and injection-locked oscillators (ILOs) are also discussed. The design tradeoffs among various clock distribution techniques are presented. Clock recovery architectures and their impact on overall system performance are explained. To mitigate process variation, variation-tolerant circuits and clock calibration techniques are required. Energy-efficient clocking solutions can be achieved by active power minimization, amortization and aggressive power management methods. Examples of state-of-the-art clocking circuit and architecture solutions are presented.

Mozhgan Mansuri received the B.S. and M.S. degrees in electronics engineering from Sharif University of Technology, Tehran, Iran, in 1995 and 1997, respectively, and the Ph.D. degree in electrical engineering from the University of California, Los Angeles, in 2003.

She joined Intel in 2003, where she is a Principal Engineer and leads the Discrete Photonics Signaling Research team in the PHY Research Lab, Intel Labs, in Hillsboro, Oregon. Her research interests include low-power, low-jitter clock synthesis/recovery circuits (PLLs and DLLs), variation-tolerant circuits and high-speed, low-power optical/electrical and memory I/O links.

Dr. Mansuri is the recipient of the 2015 Journal of Solid-State Circuits Best Paper Award and 2010 Transactions on Circuits and Systems Darlington Best Paper Award.

Live Q&A - February 14, 8:35am PST

SC4: Processor Clock Generation, Distribution, and Clock Sensor/Management Loops

Phillip Restle, *IBM Thomas J. Watson Research Center, Yorktown Heights, NY*

This discussion of processor global clocking starts with on-chip transmission-line effects, and the design and tuning of standard trees, including power, clock gating, and useful skew. Most high-performance processors use more specialized methods including clock spines and meshes, which require special timing methods, but can have significant advantages with respect to skew, robustness, and design closure. The design of resonant meshes with mode-changing capabilities are discussed. The final topic is clock sensors and control loops to improve power and performance including useful jitter.

Phillip J. Restle received a Ph.D. degree in Physics from the University of Illinois, Urbana, IL, in 1986. He is a Distinguished Research Staff Member with the IBM T. J. Watson Research Center, Yorktown Heights, NY. He has contributed to all recent zSeries and POWER processors. His interests include clock distribution networks, power-supply noise mitigation, and technical visualization. He has co-authored 75 papers and holds 45 patents. Dr. Restle was a recipient of three IBM Corporate Awards for clock distribution and resonant clocking and two best paper awards.

Plenary Session — Invited Papers

Session Chair:
Kevin Zhang, *Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan*
ISSCC Conference Chair

Session Co-Chair:
Makoto Ikeda, *University of Tokyo, Tokyo, Japan*
ISSCC International Technical Program Chair

The plenary presentations will be played according to the following program, and will be available online, on-demand until March 31, 2021.

6:30 AM
FORMAL OPENING OF THE CONFERENCE

7:00 AM

1.1 Unleashing the Future of Innovation

Mark Liu, *Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan*

The foundry business model, pioneered by TSMC more than three decades ago, brought a sea change to technology innovation and how integrated circuits (ICs) and systems are designed and manufactured. Access to semiconductor technology is no longer limited to large corporations that invest billions of dollars to build a fabrication plant. The foundry model has democratized IC innovation, making it available to all visionaries and innovators. Today, an open innovation platform that connects innovators with semiconductor-technology providers is a vital link in the global supply chain. Our industry has already begun to look beyond just engineering individual chips manufactured on wafers, and have moved to integrate individual chips into systems. System performance and energy efficiency will continue to advance at historical rates, driven by innovations from many aspects, including materials, device and integration technology, circuit design, architecture, and systems. User applications drives design choices, and design choices are enabled by technology advancements. Advances in an open innovation ecosystem will further lower the entry barriers and unleash the future of innovation!

7:45 AM

1.2 Adaptive Intelligence in the New Computing Era

Victor Peng, Xilinx, San Jose, CA

We are in a new computing era where hundreds of billions of intelligent devices are being connected and deployed in the cloud, at the edge, and endpoints, that generate, transport, process, and store Zettabytes of unstructured data. Developing products for this new era will require platforms that are not only intelligent with embedded AI, but also adaptive to enable rapid innovation and adaptation for optimizing changing workloads and market needs, both before and after deployment. Adaptive intelligence will be pervasive in all aspects of data generation, transport, storage, and processing. Infrastructure that is massively scaled out and connected is better optimized and more resilient to change when constructed with adaptive computing platforms. This paper will describe the trends driving this new computing paradigm, including the ability for technology scale-up, scale-out, and scale-down, and explain how adaptive platforms are enabling these trends. We will show real use-cases where adaptive intelligent platforms are helping usher in this new computing era!

Highlighted Chip Releases: 5G and Radar Systems

Session Chair: ***Theodoros Georgantas,*** *Broadcom, Alimos, Greece*
Session Co-Chair: ***Yves Baeyens,*** *Nokia - Bell Labs, Murray Hill, NJ*
Session Moderator: ***Alice Wang,*** *Everactive, Plano, TX*

On Demand Content will be available on Friday, February 5, 2021, 5:00PM PST
Live Session: Recap and Q&A will be scheduled according to the following program.
Both On-demand content and recorded live Q&A content will be available until March 31, 2021.

8:30 AM

2.1 mm-Wave 5G Radios: Baseband to Waves

A. Khalil[1], I. Eshrah[1], A. Elsherief[1], A. Mehana[1], M. Abdalla[1], M. Mobarak[1], J. Kilpatrick[2], B. Hall[2], A. Ashry[1], H. Fahmy[1], S. Salim[1], R. Kernan[2], B. Herdeg[2], G. Sapia[2], M. El-Nozahi[1], M. Weheiba[1], M. D'Amato[2], C. Bautista[2], K. Chatzopoulos[2], A. Ghoniem[1], Y. Mosa[1], D. Roll[2], K. Ok[2]

[1]Analog Devices, Cairo, Egypt
[2]Analog Devices, Chelmsford

DS1

8:35 AM

2.2 High-Performance and Small Form-Factor mm-Wave CMOS Radars for Automotive and Industrial Sensing in 76-to-81GHz and 57-to-64GHz Bands

K. Dandu[1], S. Samala[1], K. Bhatia[1], M. Moallem[1], K. Subburaj[2], Z. Ahmad[1], D. Breen[1], S. Jang[1], T. Davis[1], M. Singh[1], S. Ram[2], V. Dudhia[2], M. DeWilde[1], D. Shetty[2], J. Samuel[2], Z. Parkar[2], C. Chi[1], P. Loya[1], Z. Crawford[1], J. Herrington[1], R. Kulak[1], A. Daga[2], R. Raavi[2], R. Teja[2], R. Veettil[2], D. Khemraj[1], I. Prathapan[2], P. Narayanan[2], N. Narayanan[2], S. Anandwade[2], J. Singh[2], V. Srinivasan[1], N. Nayak[1], K. Ramasubramanian[2], B. Ginsburg[1], V. Rentala[1]

[1]Texas Instruments, Dallas, TX
[2]Texas Instruments, Bangalore, India

DS1

8:40 AM

2.3 SOLI: A Tiny Device for a New Human-Machine Interface

S. Trotta[1], D. Weber[2], R. W. Jungmaier[1], A. Baheti[1], J. Lien[2], D. Noppeney[1], M. Tabesh[2], C. Rumpler[1], M. Aichner[3], S. Albel [3], J. S. Bal[4], I. Poupyrev[2]

[1]Infineon Technologies, Neubiberg, Germany
[2]Google, Mountain View, CA
[3]Infineon Technologies, Villach, Austria
[4]Infineon Technologies, Milpitas, CA

8:45 AM

Session 2 Authors – 30 Minute Live Q&A

Highlighted Chip Releases: Modern Digital SoCs

Session Chair: ***Thomas Burd,*** *Advanced Micro Devices, Santa Clara, CA*
Session Co-Chair: ***Rangharajan Venkatesan,*** *Nvidia, Sunnyvale, CA*
Session Moderator: ***Dennis Sylvester,*** *University of Michigan, Ann Arbor, MI*

On Demand Content will be available on Friday, February 5, 2021, 5:00PM PST
Live Session: Recap and Q&A will be scheduled according to the following program.
Both On-demand content and recorded live Q&A content will be available until March 31, 2021.

8:30 AM

3.1 XBOX Series X: A Next-Generation Gaming Console SoC

P. Paternoster[1], A. Maki[2], A. Hernandez[2], M. Grossman[1], M. Lau[1], D. Sutherland[2], A. Mathad[3]

[1]Microsoft, Sunnyvale, CA
[2]Microsoft, Redmond, WA
[3]AMD, Austin, TX

8:35 AM

3.2 The A100 Datacenter GPU and Ampere Architecture

J. Choquette, E. Lee, R. Krashinsky, V. Balan, B. Khailany

Nvidia, Santa Clara, CA

8:40 AM

3.3 Kunlun: A 14nm High-Performance AI Processor for Diversified Workloads

J. Ouyang, X. Du, Y. Ma, J. Liu

Baidu, Beijing, China

8:45 AM

Session 3 Authors – 30 Minute Live Q&A

Monday February 15th, 9:30 am -10:30am PST.

SSCS Women in Circuits & Young Professionals

SSCS Women in Circuits and Young Professionals are hosting virtual mentoring sessions. After a short kickoff from a renown engineer in our field, you will be able to choose to join a breakout room with mentors who will speak on a variety of topics. For more details, see http://isscc.org/program-2/evening-events/

Plenary Session — Invited Papers

Session Chair:
Kevin Zhang, *Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan*
ISSCC Conference Chair

Session Co-Chair:
Makoto Ikeda, *University of Tokyo, Tokyo, Japan*
ISSCC International Technical Program Chair

The plenary presentations will be played according to the following program, and will be available online, on-demand until March 31, 2021.

7:00 AM

1.3 Working at the Intersection of Machine Learning, Signal Processing, Sensors, and Circuits

Dina Katabi, *Massachusetts Institute of Technology, Cambridge, MA*

The past few decades have witnessed major advances in wireless devices and sensors. We argue however that future innovations require novel designs that transcend the traditional boundaries between computer science and electrical engineering, and deliver software and hardware systems, where neural networks can directly interpret radio signals. We show that such a design delivers a form of x-ray vision, introducing a new class of sensors that can see through walls and occlusions. Unlike cameras which sense the visible light, the new sensors leverage that radio signals traverse walls and occlusions and reflect off objects and people. The sensing devices have embedded neural networks that interpret radio reflections to see people through walls and detect their actions. Our devices can also infer people's emotions (for example, sad, happy, angry) even if the emotion does not show on one's face! These sensors can also monitor breathing, heart rate, sleep, gait, and falls, without wearable devices or body contact, enabling a new generation of contactless health and wellness monitors.

7:45 AM

1.4 There's More to the Picture Than Meets the Eye *(and in the future it will become only much more)*

Albert J. P. Theuwissen, Delft University of Technology & Harvest Imaging

Over the last five decades, solid-state imaging has gone through a difficult "childhood", changing technology during its "adolescence", and finally growing up to become a mature, "adult" that can compete with the human visual system when it comes to image quality. State-of-the-art mobile devices enjoyed by consumers, rely on a multi-disciplinary mixture of analog electronics, digital circuits, mixed-signal design, optical know-how, device physics, semiconductor technology, and algorithm development. As a result, CMOS image sensors utilized in today's mobile phones come close to perfection as far as imaging characteristics are concerned. However, this does not mean that further developments in the field are no longer necessary. On the contrary, new technologies and new materials are opening up new dimensions and new applications which complement the classical imaging functionality of sensors. This trend will ultimately convert the image sensor landscape from image capturing to smart vision. Consequently, the future of solid-state imaging will not only revolve around the shooting of beautiful images, as the market driver will no longer be limited only to mobile phones.

Processors

Session Chair: ***Sanu Mathew,*** *Intel, Hillsboro, OR*

Session Co-Chair: ***Shidhartha Das,*** *Arm, Cambridge, United Kingdom*

Session Moderator: ***Hugh Mair,*** *MediaTek, Austin, TX*

On Demand Content will be available on Friday, February 5, 2021, 5:00PM PST
Live Session: Recap and Q&A will be scheduled according to the following program.
Both On-demand content and recorded live Q&A content will be available until March 31, 2021.

8:30 AM

4.1 A 7nm 5G Mobile SoC Featuring a 3.0GHz Tri-Gear Application Processor Subsystem

H. Chen[1], R. Lagerquist[1], A. Nayak[1], H. Mair[1], G. Manoharan[1], E. Wang[2], G. Gammie[1], E. Ho[1], A. Rajagopalan[1], L-K. Yong[1], R. Madhavaram[1], M. Jagota[1], C-J. Chung[1], S. Maruthi[1], J. Wiedemeier[1], T. Chen[1], H. Hsieh[2], D. Dia[2], A. Sikiligiri[1], M. Rahman[1], B. Chen[2], C. Lin[2], V. Lin[2], E. Chiang[2], C-Y. Wu[2], P-Y. Hsu[2], J. Tsai[2], W. Wu[2], A. Thippana[1], S. Huang[2], [1]MediaTek, Austin, TX; [2]MediaTek, Hsinchu, Taiwan

8:38 AM

4.2 A 12nm Autonomous-Driving Processor with 60.4TOPS, 13.8TOPS/W CNN Executed by Task-Separated ASIL D Control

K. Matsubara[1], L. Hanno[1], M. Kimura[2], A. Nakamura[1], M. Koike[1], K. Terashima[1], S. Morikawa[1], Y. Hotta[1], T. Irita[1], S. Mochizuki[1], H. Hamasaki[1], T. Kamei[1], [1]Renesas Electronics, Kodaira, Japan; [2]Renesas Electronics, Dusseldorf, Germany

8:46 AM

4.3 An Eight-Core 1.44GHz RISC-V Vector Machine in 16nm FinFET

C. Schmidt, J. Wright*, Z. Wang, E. Chang, A. Ou, W. Bae, S. Huang, A. Flynn, B. Richards, K. Asanović, E. Alon, B. Nikolić*, University of California, Berkeley, CA
*Equally-Credited Authors (ECAs)

8:54 AM

4.4 A 1.3TOPS/W @ 32GOPS Fully Integrated 10-Core SoC for IoT End-Nodes with 1.7μW Cognitive Wake-Up From MRAM-Based State-Retentive Sleep Mode

D. Rossi[1], F. Conti[1], M. Eggiman[2], S. Mach[2], A. Di Mauro[2], M. Guermandi[1,3], G. Tagliavini[1], A. Pullini[2,3], I. Loi[3], J. Chen[1,3], E. Flamand[2,3], L. Benini[1,2], [1]University of Bologna, Bologna, Italy
[2]ETH Zurich, Zurich, Switzerland; [3]Greenwaves Technologies, Grenoble, France

DS1

9:02 AM

4.5 BioAIP: A Reconfigurable Biomedical AI Processor with Adaptive Learning for Versatile Intelligent Health Monitoring

J. Liu, Z. Zhu, Y. Zhou, N. Wang, G. Dai, Q. Liu, J. Xiao, Y. Xie, Z. Zhong, H. Liu, L. Chang, J. Zhou
University of Electronic Science and Technology of China, Chengdu, China

DS1

9:10 AM

4.6 A 144Kb Annealing System Composed of 9×16Kb Annealing Processor Chips with Scalable Chip-to-Chip Connections for Large-Scale Combinatorial Optimization Problems

T. Takemoto[1], K. Yamamoto[2], C. Yoshimura[2], M. Hayashi[2], M. Tada[3], H. Saito[4], M. Mashimo[2], M. Yamaoka[2]
[1]Hitachi, Sapporo, Japan; [2]Hitachi, Tokyo, Japan; [3]TOPPAN Technical Design Center Co., LTD., Sapporo, Japan
[4]Total Design Service Co,LTD, Sapporo, Japan

9:18 AM

4.7 A 91mW 90fps Super-Resolution Processor for Full HD Images

H-Y. Shen, Y-C. Lee, T-W. Tong, C-H. Yang, National Taiwan University, Taipei, Taiwan

9:26 AM

4.8 An Area and Energy Efficient 0.12nJ/Pixel 8K 30fps AV1 Video Decoder in 5nm CMOS Process

T. S. Kim, S. Lee, K. Lee, S. Shin, S. Jun, Y. Lee, S. Lee, H. Kang, C. Yim, Y. Lim, E. Moon, S. Lim, K. Jeong, I. Kang, Samsung Electronics, Hwaseong, Korea

Analog Interfaces

Session Chair: ***Jens Anders,*** *University of Stuttgart, Stuttgart, Germany*
Session Co-Chair: ***Taeik Kim,*** *Samsung Electronics, Hwaseong, Korea*
Session Moderator: ***David Blaauw,*** *University of Michigan, MI*

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Live Session: Recap and Q&A will be scheduled according to the following program.
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DS2

8:30 AM

5.1 A 1.5µW 0.135pJ•%RH² CMOS Humidity Sensor Using Adaptive Range-Shift Zoom CDC and Power-Aware Floating Inverter Amplifier Array

H. Li[1], Z. Tan[2], Y. Bao[3], H. Xiao[3], H. Zhang[1], K. Du[1], Y. Zhang[1], L. Ye[1,3], R. Huang[1]
[1]Peking University, Beijing, China; [2]Zhejiang University, Hangzhou, China
[3]Advanced Institute of Information Technology of Peking University, Hangzhou, China

8:38 AM

5.2 Capacitance-to-Digital Converter for Operation Under Uncertain Harvested Voltage down to 0.3V with No Trimming, Reference and Voltage Regulation

O. Aiello[1], P. Crovetti[2], M. Alioto[1], [1]National University of Singapore, Singapore, Singapore; [2]Politecnico di Torino, Torino, Italy

8:46 AM

5.3 A Highly Digital 2210µm² Resistor-Based Temperature Sensor with a 1-Point Trimmed Inaccuracy of ±1.3°C (3σ) from -55°C to 125°C in 65nm CMOS

J. A. Angevare[1], Y. Chae[2], K. A. A. Makinwa[1]
[1]Delft University of Technology, Delft, The Netherlands; [2]Yonsei University, Seoul, Korea

8:54 AM

5.4 A Hybrid Thermal-Diffusivity/Resistor-Based Temperature Sensor with a Self-Calibrated Inaccuracy of ±0.25°C (3σ) from –55°C to 125°C

S. Pan, J. A. Angevare, K. A. A. Makinwa, Delft University of Technology, Delft, The Netherlands

9:02 AM

5.5 A 770 kS/s Duty-Cycled Integrated-Fluxgate Magnetometer for Contactless Current Sensing

P. Garcha[1,2], V. Schaffer[3], B. Haroun[1], S. Ramaswamy[1], J. Wieser[4], J. Lang[2], A. Chandrakasan[2]
[1]Kilby Labs, Texas Instruments, Dallas, TX; [2]Massachusetts Institute of Technology, Cambridge, MA
[3]Texas Instruments, Freising, Germany; [4]Kilby Labs, Texas Instruments, Santa Clara, CA

9:10 AM

5.6 A 25A Hybrid Magnetic Current Sensor with 64mA Resolution, 1.8MHz Bandwidth, and a Gain Drift Compensation Scheme

A. Jouyaeian[1], Q. Fan[1], M. Motz[2], U. Ausserlechner[2], K. A. A. Makinwa[1]
[1]Delft University of Technology, Delft, The Netherlands; [2]Infineon Technologies, Villach, Austria

9:18 AM

5.7 A MEMS Coriolis Mass Flow Sensor with 300µg/h/√Hz Resolution and ±0.8mg/h Zero Stability

A. C. de Oliveira[1], J. Groenesteijn[2], R. J. Wiegerink[3], K. A. A. Makinwa[1]
[1]Delft University of Technology, Delft, The Netherlands; [2]Bronkhorst BV, Ruurlo, The Netherlands
[3]University of Twente, Enschede, The Netherlands

9:26 AM

5.8 A 5V Dynamic Class-C Paralleled Single-Stage Amplifier with Near-Zero Dead-Zone Control and Current-Redistributive Rail-to-Rail G_m-Boosting Technique

S-T. Koh, J-H. Lee, G-G. Kang, H. Han, H-S. Kim, KAIST, Daejeon, Korea

High-Performance Receivers and Transmitters for Sub-6GHz Radios

Session Chair: ***Yiwu Tang,*** *Qualcomm Technologies, San Diego, CA*
Session Co-Chair: ***Yuan-Hung Chung,*** *MediaTek, Hsinchu, Taiwan*
Session Moderator: Sudhakar Pamarti, *University of California, Los Angeles, CA*

On Demand Content will be available on Friday, February 5, 2021, 5:00PM PST
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8:30 AM

6.1 A Low-Power and Low-Cost 14nm FinFET RFIC Supporting Legacy Cellular and 5G FR1

J. Lee, B. Kang, S. Joo, S. Lee, J. Lee, S. Kang, I. Jo, S. Ahn, J. Lee, J. Bae, W. Ko, W. Jung, S. Lee, S. Lee, E. Park, S. Lee, J. Woo, J. Lee, Y. Lee, K. Lee, J. Lee, T. B. Cho, I. Kang
Samsung Electronics, Hwaseong, Korea

8:38 AM

6.2 A 4-Way Doherty Digital Transmitter Featuring 50%-LO Signed IQ Interleave Upconversion with more than 27dBm Peak Power and 40% Drain Efficiency at 10dB Power Back-Off Operating in the 5GHz Band

M. Beikmirza[1], Y. Shen[1,2], M. Mehrpoo[1,3], M. Hashemi[1,4], D. Mul[1], L. C. N. de Vreede[1], M. S. Alavi[1]
[1]Delft University of Technology, Delft, The Netherlands; [2]now with imec-Netherlands, Eindhoven, The Netherlands
[3]now with Broadcom-Netherlands, Bunnik, The Netherlands; [4]now with ItoM, Eindhoven, The Netherlands

8:46 AM

6.3 A 0.9V Dual-Channel Filtering-by-Aliasing Receiver Front-End Achieving +35dBm IIP_3 and <–81dBm LO Leakage Supporting Intra- and Inter-Band Carrier Aggregation

S. Bu, S. Pamarti
University of California, Los Angeles, CA

8:54 AM

6.4 A 1-to-3GHz Co-Channel Blocker Resistant, Spatially and Spectrally Passive MIMO Receiver in 65nm CMOS with +6dBm In-Band/In-Notch B_{1dB}

J. Poojary, R. Harjani
University of Minnesota, Minneapolis, MN

9:02 AM

6.5 A 3dB-NF 160MHz-RF-BW Blocker-Tolerant Receiver with Third-Order Filtering for 5G NR Applications

M. A. Montazerolghaem[1], S. Pires[2], L. de Vreede[1], M. Babaie[1]
[1]Delft University of Technology, Delft, The Netherlands
[2]Ampleon, Nijmegen, The Netherlands

DS1 **9:10 AM**

6.6 Full-Duplex Receiver with Wideband Multi-Domain FIR Cancellation Based on Stacked-Capacitor, N-Path Switched-Capacitor Delay Lines Achieving >54dB SIC Across 80MHz BW and >15dBm TX Power-Handling

A. Nagulu[*1], S. Garikapati*[*1], M. Essawy[2], I. Kadota[1], T. Chen[1], A. Natarajan[2], G. Zussman[1], H. Krishnaswamy[1]*
[1]Columbia University, New York, NY
[2]Oregon State University, Corvallis, OR
*Equally-Credited Authors (ECAs)

9:18 AM

6.7 A 1.75dB-NF 25mW 5GHz Transformer-Based Noise-Cancelling CMOS Receiver Front-End

K. Yang[1], C. C. Boon[1], G. Feng[2], C. Li[1], Z. Liu[1], T. Guo[1], X. Yi[3], Y. Dong[1], A. Zhou[1], X. Wang[1]
[1]Nanyang Technological University, Singapore, Singapore
[2]South China University of Technology, Guangzhou, China
[3]Massachusetts Institute of Technology, Cambridge, MA

Imagers and Range Sensors

Session Chair: ***Vyshnavi Suntharalingam,*** *MIT Lincoln Laboratory, Lexington, MA*

Session Co-Chair: ***Calvin Yi-Ping Chao,*** *TSMC, Hsinchu, Taiwan*

Session Moderator: ***Bruce Rae,*** *ST Microelectronics, Edinburgh, United Kingdom*

On Demand Content will be available on Friday, February 5, 2021, 5:00PM PST
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DS1

8:30 AM

7.1 A 4-tap 3.5µm 1.2Mpixel Indirect Time-of-Flight CMOS Image Sensor with Peak Current Mitigation and Multi-User Interference Cancellation

M-S. Keel, D. Kim, Y. Kim, M. Bae, M. Ki, B. Chung, S. Son, H. Lee, H. Jo, S-C. Shin, S. Hong, J. An, Y. Kwon, S. Seo, S. Cho, Y. Kim, Y-G. Jin, Y. Oh, Y. Kim, J. Ahn, K. Koh, Y. Park, Samsung Electronics, Hwaseong, Korea

8:38 AM

7.2 A 48×40 13.5mm Depth Resolution Flash LiDAR Sensor with In-Pixel Zoom Histogramming Time-to-Digital Converter

B. Kim[1], S. Park[1], J-H. Chun[2,3], J. Choi[2,3], S-J. Kim[1]

[1]Ulsan National Institute of Science and Technology, Ulsan, Korea; [2]Sungkyunkwan University, Suwon, Korea; [3]SolidVue, Suwon, Korea

DS1

8:46 AM

7.3 A 189×600Back-Illuminated Stacked SPAD Direct Time-of-Flight Depth Sensor for AutomotiveLiDAR Systems

O. Kumagai[1], J. Ohmachi[1], M. Matsumura[1], S. Yagi[1], K. Tayu[1], K. Amagawa[2], T. Matsukawa[1], O. Ozawa[1], D. Hirono[1], Y. Shinozuka[1], R. Homma[1], K. Mahara[2], T. Ohyama[1], Y. Morita[1], S. Shimada[1], T. Ueno[3], A. Matsumoto[1], Y. Otake[1], T. Wakano[1], T. Izawa[1]

[1]Sony Semiconductor Solutions, Atsugi, Japan; [2]Sony LSI Design, Atsugi, Japan; [3]Sony Depthsensing Solutions, Brussels, Belgium

8:54 AM

7.4 A 256×128 3D-Stacked (45nm) SPAD FLASH LiDAR with 7-Level Coincidence Detection and Progressive Gating for 100m Range and 10klux Background Light

P. Padmanabhan[1], C. Zhang[2], M. Cazzaniga[3], B. Efe[1], A. R. Ximenes[4], M-J. Lee[5], E. Charbon[1]

[1]EPFL, Neuchâtel, Switzerland; [2]ADAPS Photonics, Shenzhen, China; [3]Intuitive Surgical, Aubonne, Switzerland
[4]Facebook, Redmond, WA; [5]Korea Institute of Science and Technology, Seoul, Korea

9:02 AM

7.5 A 250fps 124dB Dynamic-Range SPAD Image Sensor Stacked with Pixel-Parallel Photon Counter Employing Sub-Frame Extrapolating Architecture for Motion Artifact Suppression

J. Ogi[1], T. Takatsuka[1], K. Hizu[1], Y. Inaoka[1], H. Zhu[1], Y. Tochigi[1], Y. Tashiro[1], F. Sano[1], Y. Murakawa[2], M. Nakamura[2], Y. Oike[1]

[1]Sony Semiconductor Solutions, Kanagawa, Japan; [2]Sony Semiconductor Manufacturing, Nagasaki, Japan

9:10 AM

7.6 A High-Speed Back-Illuminated Stacked CMOS Image Sensor with Column-Parallel kT/C-Cancelling S&H and Delta-Sigma ADC

C. Okada[1], K. Uemura[1], L. Hung[1], K. Matsuura[1], T. Moue[1], D. Yamazaki[1], K. Kodama[1], M. Okano[1], T. Morikawa[1], K. Yamashita[1], O. Oka[2], I. Shvartz[3], G. Zeituni[3], A. Benshem[3], N. Eshel[3], Y. Inada[1]

[1]Sony Semiconductor Solutions, Kanagawa, Japan; [2]Sony Semiconductor Manufacturing, Kumamoto, Japan
[3]Sony Electronics, Ra'anana, Israel

DS1

9:18 AM

7.7 A 0.2-to-3.6TOPS/W Programmable Convolutional Imager SoC with In-Sensor Current-Domain Ternary-Weighted MAC Operations for Feature Extraction and Region-of-Interest Detection

M. Lefebvre, L. Moreau, R. Dekimpe, D. Bol

Université catholique de Louvain, Louvain-la-Neuve, Belgium

DS1

9:26 AM

7.8 A 1-inch 17Mpixel 1000fps Block-Controlled Coded-Exposure Back-Illuminated Stacked CMOS Image Sensor for Computational Imaging and Adaptive Dynamic Range Control

T. Hirata, H. Murata, H. Matsuda, Y. Tezuka, S. Tsunai

Nikon, Tokyo, Japan

9:30 AM

7.9 1/2.74-inch 32Mpixel-Prototype CMOS Image Sensor with 0.64µm Unit Pixels Separated by Full-Depth Deep-Trench Isolation

J. Park, S. Park, K. Cho, T. Lee, C. Lee, D. Kim, B. Lee, S. Kim, H-C. Ji, D. Im, H. Park, J. Kim, J. Cha, T. Kim, I-S. Joe, S. Hong, C. Chang, J. Kim, W. Shim, T. Kim, J. Lee, D. Park, E. Kim, H. Park, J. Lee, Y. Kim, J. Ahn, Y. Hong, C. Jun, H. Kim, C-R. Moon, H-K. Kang

Samsung Electronics, Hwaseong, Korea

Ultra-High-Speed Wireline

Session Chair: ***Yohan Frans,*** *Xilinx, San Jose, CA*

Session Co-Chair: ***Patrick Yue,*** *Hong Kong University of Science and Technology, Clear Water Bay, Hong Kong*

Session Moderator: ***Thomas Toifl,*** *Cisco Systems, Wallisellen, Switzerland*

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DS1

8:30 AM

8.1 A 224Gb/s DAC-Based PAM-4 Transmitter with 8-Tap FFE in 10nm CMOS

J. Kim[1], S. Kundu*[1], A. Balankutty[1], M. Beach[2], B. C. Kim[1], S. Kim[1], Y. Liu[1], S. K. Murthy[1], P. Wali[1], K. Yu[1], H. S. Kim[1], C-C. Liu[1], D. Shin[1], A. Cohen[3], Y. Fan[1], F. O'Mahony[1]*
[1]Intel, Hillsboro, OR; [2]Foundation Devices, Boston, MA; [3]Intel, Jerusalem, Israel; *Equally-Credited Authors (ECAs)

8:38 AM

8.2 An Output-Bandwidth-Optimized 200Gb/s PAM-4 100Gb/s NRZ Transmitter with 5-Tap FFE in 28nm CMOS

M. Choi[1], Z. Wang*[1], K. Lee[1], K. Park[1], Z. Liu[1], A. Biswas[1], J. Han[2], E. Alon[1]*
[1]University of California, Berkeley, CA; [2]Hanyang University, Seoul, Korea; *Equally-Credited Authors (ECAs)

DS1

8:46 AM

8.3 An 8b DAC-Based SST TX Using Metal Gate Resistors with 1.4pJ/b Efficiency at 112Gb/s PAM-4 and 8-Tap FFE in 7nm CMOS

M. A. Kossel[1], V. Khatri[1,4], M. Braendli[1], P. A. Francese[1], T. Morf[1], S. A. Yonar[1], M. Prathapan[1], E. J. Lukes[2], R. A. Richetta[2], C. Cox[3]
[1]IBM Research, Rüschlikon, Switzerland; [2]IBM Systems and Technology, Rochester, MN; [3]IBM Systems and Technology, Durham, NC
[4]now with Samsung Semiconductor India Research, Bangalore

8:54 AM

8.4 A 116Gb/s DSP-Based Wireline Transceiver in 7nm CMOS Achieving 6pJ/b at 45dB Loss in PAM-4/Duo-PAM-4 and 52dB in PAM-2

M-A. LaCroix, E. Chong, W. Shen, E. Nir, F. A. Musa, H. Mei, M-M. Mohsenpour, S. Lebedev, B. Zamanlooy, C. Carvalho, Q. Xin, D. Petrov, H. Wong, H. Ho, Y. Xu, S. N. Shahi, P. Krotnev, C. Feist, H. Huang, D. Tonietto
Huawei Technologies, Ottawa, Canada

DS1

9:02 AM

8.5 A Scalable Adaptive ADC/DSP-Based 1.25-to-56Gbps/112Gbps High-Speed Transceiver Architecture Using Decision-Directed MMSE CDR in 16nm and 7nm

D. Xu[1], Y. Kou*[1], P. Lai*[1], Z. Cheng[1], T. Y. Cheung[2], L. Moser[1], Y. Zhang[1], X. Liu[1], M. P. Lam[1], H. Jia[2,3], Q. Pan[2,4], W. H. Szeto[2], C. F. Tang[2], K. F. Mak[2], K. Sarfraz[2], T. Zhu[1], M. Kwan[1], E. Y. L. Au[1], C. Conroy[1], K. K. Chan[1]*
[1]eTopus Technology, San Jose, CA; [2]eTopus Technology, Hong Kong, China; [3]now with Tsinghua University, Beijing, China
[4]now with Southern University of Science and Technology, Shenzhen, China; *Equally-Credited Authors (ECAs)

9:10 AM

8.6 A Highly Reconfigurable 40-97GS/s DAC and ADC with 40GHz AFE Bandwidth and Sub-35fJ/conv-step for 400Gb/s Coherent Optical Applications in 7nm FinFET

R. L. Nguyen[1], A. M. Castrillon[2], A. Fan[1], A. Mellati[1], B. T. Reyes[2], C. Abidin[1], E. Olsen[1], F. Ahmad[1], G. Hatcher[1], J. Chana[3], L. Biolato[2], L. Tse[4], L. Wang[1], L. Wang[4], M. Azarmnia[1], M. Davoodi[1], N. Campos[2], N. Fan[1], P. Prabha[1], Q. Lu[1], S. Cyrusian[1], S. Dallaire[5], S. Ho[3], S. Jantzi[1], T. Dusatko[3], W. Elsharkasy[1]
[1]Inphi, Irvine, CA; [2]Inphi, Cordoba, Argentina; [3]Inphi, Vancouver, Canada; [4]Inphi, San Jose, CA; [5]Inphi, Ottawa, Canada

9:18 AM

8.7 A 112Gb/s ADC-DSP-Based PAM-4 Transceiver for Long-Reach Applications with >40dB Channel Loss in 7nm FinFET

P. Mishra[1], A. Tan[1], B. Helal[1], C. Ho[1], C. Loi[1], J. Riani[1], J. Sun[2], K. Mistry[3], K. Raviprakash[1], L. Tse[1], M. Davoodi[4], M. Takefman[3], N. Fan[4], P. Prabha[4], Q. Liu[2], Q. Wang[1], R. Nagulapalli[5], S. Cyrusian[4], S. Jantzi[4], S. Scouten[3], T. Dusatko[6], T. Setya[3], V. Giridharan[1], V. Gurumoorthy[1], V. Karam[3], W. Liew[2], Y. Liao[1], Y. Ou[1]
[1]Inphi, San Jose, CA; [2]Inphi, Singapore, Singapore; [3]Inphi, Ottawa, Canada; [4]Inphi, Irvine, CA; [5]Inphi, Northants, United Kingdom
[6]Inphi, Burnaby, Canada

9:26 AM

8.8 A 112Gb/s PAM-4 Low-Power 9-Tap Sliding-Block DFE in a 7nm FinFET Wireline Receiver

J. Bailey[1], H. Shakiba[1], E. Nir[2], G. Marderfeld[2], P. Krotnev[2], M-A. LaCroix[2], D. Cassan[1]
[1]Huawei Technologies, Toronto, Canada; [2]Huawei Technologies, Ottawa, Canada

ML Processors From Cloud to Edge

Session Chair: ***SukHwan Lim,*** *Samsung, Hwaseong, Gyeonggi, Korea*
Session Co-Chair: ***Luca Benini,*** *ETH Zurich, Zurich, Switzerland*
Session Moderator: ***Vivienne Sze,*** *MIT, Cambridge, MA*

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7:00 AM

9.1 A 7nm 4-Core AI Chip with 25.6TFLOPS Hybrid FP8 Training, 102.4TOPS INT4 Inference and Workload-Aware Throttling

A. Agrawal[1], S. K. Lee[1], J. Silberman[1], M. Ziegler[1], M. Kang[1,8], S. Venkataramani[1], N. Cao[1], B. Fleischer[1], M. Guillorn[1], M. Cohen[1], S. Mueller[2], J. Oh[1,9], M. Lutz[1], J. Jung[1], S. Koswatta[1], C. Zhou[1], V. Zalani[1], J. Bonanno[3], R. Casatuta[4], C-Y. Chen[1], J. Choi[5], H. Haynie[6], A. Herbert[1], R. Jain[1], M. Kar[1], K-H. Kim[1], Y. Li[1], Z. Ren[1], S. Rider[6], M. Schaal[1], K. Schelm[2], M. Scheuermann[1], X. Sun[1], H. Tran[1], N. Wang[1], W. Wang[1], X. Zhang[1], V. Shah[7], B. Curran[6], V. Srinivasan[1], P-F. Lu[1], S. Shukla[1], L. Chang[1], K. Gopalakrishnan[1]
[1]IBM Research, Yorktown Heights, NY; [2]IBM, Boeblingen, Germany; [3]IBM, Austin, TX; [4]IBM, Hopewell Junction, NY
[5]Hanyang University, Seoul, Korea; [6]IBM, Poughkeepsie, NY; [7]IBM, Hursley, United Kingdom
[8]now with University of California, San Diego, La Jolla, CA; [9]now with Rebellions, Seoul, Korea

7:08 AM

9.2 A 28nm 12.1TOPS/W Dual-Mode CNN Processor Using Effective-Weight-Based Convolution and Error-Compensation-Based Prediction

H. Mo[1], W. Zhu[1], W. Hu[1], G. Wang[1], Q. Li[2], A. Li[1], S. Yin[1], S. Wei[1], L. Liu[1]
[1]Institute of Microelectronics of Tsinghua University, Beijing, China; [2]Intel, Beijing, China

DS2

7:16 AM

9.3 A 40nm 4.81TFLOPS/W 8b Floating-Point Training Processor for Non-Sparse Neural Networks Using Shared Exponent Bias and 24-Way Fused Multiply-Add Tree

J. Park, S. Lee*, D. Jeon*, Seoul National University, Seoul, Korea; *Equally-Credited Authors (ECAs)

7:24 AM

9.4 PIU: A 248GOPS/W Stream-Based Processor for Irregular Probabilistic Inference Networks Using Precision-Scalable Posit Arithmetic in 28nm

N. Shah, L. I. Galindez Olascoaga, S. Zhao, W. Meert, M. Verhelst, KU Leuven - MICAS, Leuven, Belgium

7:32 AM

9.5 A 6K-MAC Feature-Map-Sparsity-Aware Neural Processing Unit in 5nm Flagship Mobile SoC

J-S. Park[1], J-W. Jang[2], H. Lee[1], D. Lee[1], S. Lee[2], H. Jung[2], S. Lee[2], S. Kwon[1], K. Jeong[1], J-H. Song[2], S. Lim[1], I. Kang[1]
[1]Samsung Electronics, Hwaseong, Korea; [2]Samsung Advanced Institute of Technology, Suwon, Korea

DS2

7:36 AM

9.6 A 1/2.3inch 12.3Mpixel with On-Chip 4.97TOPS/W CNN Processor Back-Illuminated Stacked CMOS Image Sensor

R. Eki[1], S. Yamada[2], H. Ozawa[1], H. Kai[1], K. Okuike[2], H. Gowtham[2], H. Nakanishi[2], E. Almog[3], Y. Livne[3], G. Yuval[3], E. Zyss[3], T. Izawa[2]
[1]Sony Semiconductor Solutions, Tokyo, Japan; [2]Sony Semiconductor Solutions, Atsugi, Japan
[3]Sony Semiconductor Israel, Hod-Hasharon, Israel

DS1

7:40 AM

9.7 A 184μW Real-Time Hand-Gesture Recognition System with Hybrid Tiny Classifiers for Smart Wearable Devices

Y. Lu[1], V. L. Le[2], T-H. Kim[1]
[1]Nanyang Technological University, Singapore, Singapore; [2]Nations Innovation Technologies, Singapore, Singapore

7:48 AM

9.8 A 25mm² SoC for IoT Devices with 18ms Noise-Robust Speech-to-Text Latency via Bayesian Speech Denoising and Attention-Based Sequence-to-Sequence DNN Speech Recognition in 16nm FinFET

T. Tambe[1], E-Y. Yang[1], G. G. Ko[1], Y. Chai[1], C. Hooper[1], M. Donato[2], P. N. Whatmough[1,3], A. M. Rush[4], D. Brooks[1], G-Y. Wei[1]
[1]Harvard University, Cambridge, MA; [2]Tufts University, Medford, MA; [3]ARM, Boston, MA; [4]Cornell University, New York, NY

DS1

7:56 AM

9.9 A Background-Noise and Process-Variation-Tolerant 109nW Acoustic Feature Extractor Based on Spike-Domain Divisive-Energy Normalization for an Always-On Keyword Spotting Device

D. Wang, S. J. Kim, M. Yang, A. A. Lazar, M. Seok, Columbia University, New York, NY

Continuous-Time ADCs and DACs

Session Chair: ***Seyfi Bazarjani,*** *Qualcomm Technologies, San Diego, CA*
Session Co-Chair: ***Jongwoo Lee,*** *Samsung Electronics, Hwaseong, Korea*
Session Moderator: *Marco Corsi, Texas Instruments, Parker, TX*

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DS1

7:00 AM

10.1 A 116µW 104.4dB-DR 100.6dB-SNDR CT ΔΣ Audio ADC Using Tri-Level Current-Steering DAC with Gate-Leakage Compensated Off-Transistor-Based Bias Noise Filter

C. Lo, J. Lee, Y. Lim, Y. Yoon, H. Hwang, J. Lee, M. Choi, M. Lee, S. Oh, J. Lee, Samsung Electronics, Hwaseong, Korea

7:08 AM

10.2 A 139µW 104.8dB-DR 24kHz-BW CTΔΣM with Chopped AC-Coupled OTA-Stacking and FIR DACs

S. Mondal[1,2], O. Ghadami[1], D. A. Hall[1]
[1]University of California, San Diego, La Jolla, CA
[2]now with Apple, San Diego, CA

7:16 AM

10.3 A 100MHz-BW 68dB-SNDR Tuning-Free Hybrid-Loop DSM with an Interleaved Bandpass Noise-Shaping SAR Quantizer

L. Jie, H-W. Chen, B. Zheng, M. P. Flynn, University of Michigan, Ann Arbor, MI

7:24 AM

10.4 A 3.7mW 12.5MHz 81dB-SNDR 4th-Order CTDSM with Single-OTA and 2nd-Order NS-SAR

W. Shi[1], J. Liu[2], A. Mukherjee[1], X. Yang[1], X. Tang[1], L. Shen[1], W. Zhao[1], N. Sun[1,2]
[1]University of Texas, Austin, TX
[2]Tsinghua University, Beijing, China

7:32 AM

10.5 A 12b 600MS/s Pipelined SAR and 2×-Interleaved Incremental Delta-Sigma ADC with Source-Follower-Based Residue-Transfer Scheme in 7nm FinFET

S. Baek, I. Jang, M. Choi, H. Roh, W. Lim, Y. Cho, J. Shin, Samsung Electronics, Hwasung, Korea

DS1

7:40 AM

10.6 A 12b 16GS/s RF-Sampling Capacitive DAC for Multi-Band Soft-Radio Base-Station Applications with On-Chip Transmission-Line Matching Network in 16nm FinFET

D. Gruber[1], M. Clara*[2], R. Sanchez[3], Y-S. Wang[4], C. Duller[1], G. Rauter[1], P. Torta[1], K. Azadet[2]*
[1]Intel, Villach, Austria
[2]Intel, Santa Clara, CA
[3]Intel, Madrid, Spain
[4]Intel, Hillsboro, OR
*Equally-Credited Authors (ECAs)

7:48 AM

10.7 A 64GS/s 4×-Interpolated 1b Semi-Digital FIR DAC for Wideband Calibration and BIST of RF-Sampling A/D Converters

M. Clara[1], D. Gruber*[2], A. Molina[3], M. Camponeschi[2], Y-S. Wang[4], C. Lindholm[2], H. Shin[5], R. Sanchez[3], C. Duller[2], P. Torta[2], K. Azadet[1]*
[1]Intel, Santa Clara, CA
[2]Intel, Villach, Austria
[3]Intel, Madrid, Spain
[4]Intel, Hillsboro, OR
[5]now with Apple, Cupertino, CA
*Equally-Credited Authors (ECAs)

Advanced Wireline Links and Techniques

Session Chair: ***Mike Shuo-Wei Chen,*** *University of Southern California, Los Angeles, CA*
Session Co-Chair: ***Wei-Zen Chen,*** *National Chiao Tung University, Hsinchu, Taiwan*
Session Moderator: ***Amir Amirkhany,*** *Samsung Electronics, San Jose, CA*

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7:00 AM

11.1 A 1.7pJ/b 112Gb/s XSR Transceiver for Intra-Package Communication in 7nm FinFET Technology

R. Yousry[*1], *E. Chen*[*1], *Y-M. Ying*[1], *M. Abdullatif*[1], *M. Elbadry*[1], *A. ElShater*[1], *T-B. Liu*[2], *J. Lee*[1], *D. Ramachandran*[1], *K. Wang*[2], *C-H. Weng*[2], *M-L. Wu*[2], *T. Ali*[1]
[1]MediaTek, Irvine, CA; [2]MediaTek, Hsinchu, Taiwan; *Equally-Credited Authors (ECAs)

7:08 AM

11.2 A 26.5625-to-106.25Gb/s XSR SerDes with 1.55pJ/b Efficiency in 7nm CMOS

R. Shivnaraine[1], *M. van Ierssel*[1], *K. Farzan*[1], *D. Diclemente*[1], *G. Ng*[1], *N. Wang*[2], *J. Musayev*[1], *G. Dutta*[1], *M. Shibata*[1], *A. Moradi*[1], *H. Vahedi*[1], *M. Farzad*[1], *P. Kainth*[1], *M. Yu*[1], *N. Nguyen*[2], *J. Pham*[1], *A. McLaren*[1]
[1]Rambus, Toronto, Canada; [2]Rambus, San Jose, CA

DS2 **7:16 AM**

11.3 A 480Gb/s/mm 1.7pJ/b Short-Reach Wireline Transceiver Using Single-Ended NRZ for Die-to-Die Applications

K. McCollough, S. D. Huss, J. Vandersand, R. Smith, C. Moscone, Q. O. Farooq, Cadence, Cary, NC

DS2 **7:20 AM**

11.4 A High-Accuracy Multi-Phase Injection-Locked 8-Phase 7GHz Clock Generator in 65nm with 7b Phase Interpolators for High-Speed Data Links

Z. Wang, *Y. Zhang*, *Y. Onizuka, P. R. Kinget*, Columbia University, New York, NY; *Equally-Credited Authors (ECAs)

7:24 AM

11.5 A 23.9-to-29.4GHz Digital LC-PLL with a Coupled Frequency Doubler for Wireline Applications in 10nm FinFET

D. Shin, H. S. Kim, C-C. Liu, P. Wali, S. K. Murthy, Y. Fan, Intel, Hillsboro, OR

7:32 AM

11.6 A 100Gb/s -8.3dBm-Sensitivity PAM-4 Optical Receiver with Integrated TIA, FFE and Direct-Feedback DFE in 28nm CMOS

H. Li, J. Sharma, C-M. Hsu, G. Balamurugan, J. Jaussi, Intel, Hillsboro, OR

7:40 AM

11.7 A 56Gb/s 50mW NRZ Receiver in 28nm CMOS

A. Atharav, B. Razavi, University of California, Los Angeles, CA

7:48 AM

11.8 An Echo-Cancelling Front-End for 112Gb/s PAM-4 Simultaneous Bidirectional Signaling in 14nm CMOS

R. Farjadrad[1], *K. Kaviani*[1], *D. Nguyen*[1], *M. Brown*[1], *G. Geelen*[2], *C. Bastiaansen*[2], *N. Rao*[1], *V. Popuri*[1], *G. Shen*[1], *H. Khatibi*[1], *S. Dey*[3], *A. Chatterjee*[3], *D. Shen*[1], *P. Zijlstra*[2], *H. Gunnink*[2], *K. Zhang*[1], *V. Penumuchu*[1], *O. Weiss*[1], *E. Paulus*[2], *J. Briaire*[2]
[1]Marvell, Santa Clara, CA; [2]Marvell, Eindhoven, The Netherlands; [3]Marvell, Bangalore, India

7:56 AM

11.9 A 105Gb/s Dielectric-Waveguide Link in 130nm BiCMOS Using Channelized 220-to-335GHz Signal and Integrated Waveguide Coupler

J. W. Holloway[1,2], *G. C. Dogiamis* [3], *R. Han*[1]
[1]Massachusetts Institute of Technology, Cambridge, MA; [2]Raytheon, Tewksbury, MA; [3]Intel, Chandler, AZ

Innovations in Low-Power and Secure IoT

Session Chair: ***Sriram Vangal,*** *Intel, Hillsboro, OR*

Session Co-Chair: ***Long Yan,*** *Samsung Electronics, Hwaseong, Korea*

Session Moderator: ***Frederic Gianesello,*** *STMicroelectronics, Crolles, France*

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7:00 AM

12.1 A 148nW General-Purpose Event-Driven Intelligent Wake-Up Chip for AIoT Devices Using Asynchronous Spike-Based Feature Extractor and Convolutional Neural Network

Z. Wang[1], L. Ye[1,2], Y. Liu[1], P. Zhou[2], Z. Tan[3], H. Fan[2], Y. Zhang[1], J. Ru[4], Y. Wang[1], R. Huang[1]
[1]Peking University, Beijing, China
[2]Advanced Institute of Information Technology of Peking University, Hangzhou, China
[3]Zhejiang University, Hangzhou, China
[4]XINYI Information Technology, Shanghai, China

DS2

7:08 AM

12.2 Improving the Range of WiFi Backscatter Via a Passive Retro-Reflective Single-Side-Band-Modulating MIMO Array and Non-Absorbing Termination

M. Meng[1], M. Dunna[1], H. Yu[1], S. Kuo[1], P-H. P. Wang[1,2], D. Bharadia[1], P. P. Mercier[1]
[1]University of California San Diego, La Jolla, CA
[2]Broadcom, San Diego, CA

7:16 AM

12.3 Exploring PUF-Controlled PA Spectral Regrowth for Physical-Layer Identification of IoT Nodes

Q. Zhou, Y. He*, K. Yang, T. Chi*
Rice University, Houston, TX
*Equally-Credited Authors (ECAs)

Cryo-CMOS for Quantum Computing

Session Chair: ***Denis Daly,*** *Apple, Cambridge, MA*

Session Co-Chair: ***Shawn Hsu,*** *National Tsing Hua University, Hsinchu, Taiwan*

Session Moderator: ***Edoardo Charbon,*** *EPFL, Neuchâtel, Switzerland*

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7:45 AM

13.1 A Fully Integrated Cryo-CMOS SoC for Qubit Control in Quantum Computers Capable of State Manipulation, Readout and High-Speed Gate Pulsing of Spin Qubits in Intel 22nm FFL FinFET Technology

J-S. Park[1], S. Subramanian[1], L. Lampert[1], T. Mladenov[1], I. Klotchkov[1], D. J. Kurian[2], E. Juarez-Hernandez[3], B. Perez-Esparza[3], S. R. Kale[1], A. B. K. T.[4], S. Premaratne[1], T. Watson[1], S. Suzuki[1], M. Rahman[1], J. B. Timbadiya[2], S. Soni[2], S. Pellerano[1]
[1]Intel, Hillsboro, OR
[2]Intel, Bangalore, India
[3]Intel, Guadalajara, Mexico
[4]Intel, Santa Clara, CA

7:53 AM

13.2 A Fully-Integrated 40-nm 5-6.5 GHz Cryo-CMOS System-on-Chip with I/Q Receiver and Frequency Synthesizer for Scalable Multiplexed Readout of Quantum Dots

A. Ruffino[*1], Y. Peng*[*1], T.-Y. Yang[2], J. Michniewicz[3], M. F. Gonzalez-Zalba[2,4], E. Charbon[1]*
[1]EPFL, Neuchâtel, Switzerland
[2]Hitachi, Cambridge, United Kingdom
[3]University of Cambridge, Cambridge, United Kingdom
[4]Quantum Motion Technologies, Leeds, United Kingdom
*Equally-Credited Authors (ECAs)

DS2

8:01 AM

13.3 A 6-to-8GHz 0.17mW/Qubit Cryo-CMOS Receiver for Multiple Spin Qubit Readout in 40nm CMOS Technology

B. Prabowo[1,2], G. Zheng[1,2], M. Mehrpoo[1,3], B. Patra[1,2], P. Harvey-Collard[1,2], J. Dijkema[1,2], A. Sammak[4], G. Scappucci[1,2], E. Charbon[1,2,5], F. Sebastiano[1,2], L. M. K. Vandersypen[1,2], M. Babaie[1,2]
[1]Delft University of Technology, Delft, The Netherlands
[2]QuTech, Delft, The Netherlands
[3]now with Broadcom Netherlands, Bunnik, The Netherlands
[4]TNO, Delft, The Netherlands
[5]EPFL, Neuchatel, Switzerland

8:09 AM

13.4 A 1GS/s 6-to-8b 0.5mW/Qubit Cryo-CMOS SAR ADC for Quantum Computing in 40nm CMOS

G. Kiene[1,2], A. Catania[3], R. Overwater[1,2], P. Bruschi[3], E. Charbon[1,2,4], M. Babaie[1,2], F. Sebastiano[1,2]
[1]Delft University of Technology, Delft, The Netherlands
[2]QuTech, Delft, The Netherlands
[3]University of Pisa, Pisa, Italy
[4]EPFL, Neuchatel, Switzerland

mm-Wave Transceivers for Communication and Radar

Session Chair: ***Bodhisatwa Sadhu,*** *IBM T. J. Watson Research Center, Yorktown Heights, NY*

Session Co-Chair: ***Matteo Bassi,*** *Infineon Technologies AG, Villach, Austria*

Session Moderator: ***Vito Giannini,*** *Uhnder, Austin, TX*

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7:00 AM

14.1 A 71-to-86GHz Packaged 16-Element by 16-Beam Multi-User Beamforming Integrated Receiver in 28nm CMOS

E. Naviasky, L. Iotti, G. LaCaille, B. Nikolić, E. Alon, A. Niknejad, University of California, Berkeley, CA

7:08 AM

14.2 An Early Fusion Complementary RADAR-LiDAR TRX in 65nm CMOS Supporting Gear-Shifting Sub-cm Resolution for Smart Sensing and Imaging

L. Lou[1], K. Tang[1], Z. Fang[1], Y. Wang[2], B. Chen[1], T. Guo[1], X. Feng[1], S. Liu[1], W. Wang[1], Y. Zheng[1]
[1]Nanyang Technological University, Singapore, Singapore; [2]Singapore University of Technology and Design, Singapore, Singapore

7:16 AM

14.3 A 26GHz Full-Duplex Circulator Receiver with 53dB/400MHz (40dB/800MHz) Self-Interference Cancellation for mm-Wave Repeaters

R. Garg, S. Jain, P. Dania, A. Natarajan, Oregon State University, Corvallis, OR

7:24 AM

14.4 A 24-to-30GHz Double-Quadrature Direct-Upconversion Transmitter with Mutual-Coupling-Resilient Series-Doherty Balanced PA for 5G MIMO Arrays

M. Pashaeifar, L. C. de Vreede, M. S. Alavi, Delft University of Technology, Delft, The Netherlands

7:32 AM

14.5 A 1V W-Band Bidirectional Transceiver Front-End with <1dB T/R Switch Loss, <1°/dB Phase/Gain Resolution and 12.3% TX PAE at 15.1dBm Output Power in 65nm CMOS Technology

W. Zhu, J. Wang, R. Wang, Y. Wang, Institute of Microelectronics of Tsinghua University, Beijing, China

7:40 AM

14.6 A 76-to-81GHz 2×8 FMCW MIMO Radar Transceiver with Fast Chirp Generation and Multi-Feed Antenna-in-Package Array

Z. Duan[1], B. Wu[1], C. Zhu[1], Y. Wang[1], W. Jin[1], Y. Liu[1], Y. Wu[2], T. Zhang[2], M. Liu[1], B. Dou[1], B. Liao[1], W. Lv[1], D. Pan[3], Y. Li[3], C. Wang[3], Y. Dai[1], P. Li[1], H. Gao[4,5]
[1]East China Research Institute of Electronic Engineering, Hefei, China; [2]Southwest Integrated Circuit Design, Chongqing, China
[3]University of Science and Technology of China, Hefei, China; [4]Silicon Austria Labs, Linz, Austria
[5]Eindhoven University of Technology, Eindhoven, The Netherlands

7:48 AM

14.7 An Adaptive Analog Temperature-Healing Low-Power 17.7-to-19.2GHz RX Front-End with ±0.005dB/°C Gain Variation, <1.6dB NF Variation, and <2.2dB IP_{1dB} Variation across -15 to 85°C for Phased-Array Receiver

M. Li[*1], N. Li*[*1], H. Gao*[*1], S. Wang*[*1], Z. Zhang[1], P. Chen[1], N. Wei[1], Q. J. Gu[2], C. Song[1], Z. Xu[1]*
[1]Zhejiang University, Zhoushan, China; [2]University of California, Davis, CA
*Equally-Credited Authors (ECAs)

7:56 AM

14.8 A Fully Integrated 62-to-69GHz Crystal-Less Transceiver with 12 Channels Tuned by a Transmission-Line-Referenced FLL in 0.13µm BiCMOS

J. Im, H. Kim, O. Abdelatty, D. D. Wentzloff, University of Michigan, Ann Arbor, MI

Compute-in-Memory Processors for Deep Neural Networks

Session Chair: ***Jun Deguchi,*** *Kioxia Corporation, Kawasaki, Japan*
Session Co-Chair: ***Yongpan Liu,*** Tsinghua University, Beijing, China
Session Moderator: ***Yan Li,*** *Western Digital, Milpitas, CA*

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8:30 AM

15.1 A Programmable Neural-Network Inference Accelerator Based on Scalable In-Memory Computing

H. Jia, M. Ozatay, Y. Tang*, H. Valavi*, R. Pathak*, J. Lee, N. Verma*
Princeton University, Princeton, NJ
*Equally-Credited Authors (ECAs)

8:38 AM

15.2 A 2.75-to-75.9TOPS/W Computing-in-Memory NN Processor Supporting Set-Associate Block-Wise Zero Skipping and Ping-Pong CIM with Simultaneous Computation and Weight Updating

J. Yue[1,2], X. Feng[1], Y. He[1], Y. Huang[1], Y. Wang[2], Z. Yuan[1], M. Zhan[1], J. Liu[1], J-W. Su[3], Y-L. Chung[3], P-C. Wu[3], L-Y. Hung[3], M-F. Chang[3], N. Sun[1], X. Li[1], H. Yang[1], Y. Liu[1]
[1]Tsinghua University, Beijing, China
[2]Pi2star Technology, Beijing, China
[3]National Tsing Hua University, Hsinchu, Taiwan

8:46 AM

15.3 A 65nm 3T Dynamic Analog RAM-Based Computing-in-Memory Macro and CNN Accelerator with Retention Enhancement, Adaptive Analog Sparsity and 44TOPS/W System Energy Efficiency

Z. Chen, X. Chen, J. Gu
Northwestern University, Evanston, IL

8:54 AM

15.4 A 5.99-to-691.1TOPS/W Tensor-Train In-Memory-Computing Processor Using Bit-Level-Sparsity-Based Optimization and Variable-Precision Quantization

R. Guo[1], Z. Yue[1], X. Si[2], T. Hu[1], H. Li[1], L. Tang[1], Y. Wang[1], L. Liu[1], M-F. Chang[3], Q. Li[2], S. Wei[1], S. Yin[1]
[1]Tsinghua University, Beijing, China
[2]University of Electronic Science and Technology of China, Chengdu, China
[3]National Tsing Hua University, Hsinchu, Taiwan

Computation in Memory

Session Chair: ***Meng-Fan Chang,*** National Tsing Hua University, Hsinchu, Taiwan

Session Co-Chair: ***Ru Huang,*** *Peking University, Beijing, China*

Session Moderator: ***Seung-Jun Bae,*** *Samsung, Hwaseong, Korea*

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9:15 AM

16.1 A 22nm 4Mb 8b-Precision ReRAM Computing-in-Memory Macro with 11.91 to 195.7TOPS/W for Tiny AI Edge Devices

C-X. Xue[1], J-M. Hung*[1], H-Y. Kao[1], Y-H. Huang[1], S-P. Huang[1], F-C. Chang[1], P. Chen[1], T-W. Liu[1], C-J. Jhang[1], C-I. Su[2], W-S. Khwa[2], C-C. Lo[1], R-S. Liu[1], C-C. Hsieh[1], K-T. Tang[1], Y-D. Chih[2], T-Y. J. Chang[2], M-F. Chang[1,2]*

[1]National Tsing Hua University, Hsinchu, Taiwan
[2]TSMC, Hsinchu, Taiwan
*Equally-Credited Authors (ECAs)

9:23 AM

16.2 eDRAM-CIM: Compute-In-Memory Design with Reconfigurable Embedded-Dynamic-Memory Array Realizing Adaptive Data Converters and Charge-Domain Computing

S. Xie[1], C. Ni[1], A. Sayal[1], P. Jain[2], F. Hamzaoglu[2], J. P. Kulkarni[1]

[1]University of Texas, Austin, TX
[2]Intel, Hillsboro, OR

9:31 AM

16.3 A 28nm 384kb 6T-SRAM Computation-in-Memory Macro with 8b of Precision for AI Edge Chips

J-W. Su[1,2], Y-C. Chou*[1], R. Liu[1], T-W. Liu[1], P-J. Lu[1], P-C. Wu[1], Y-L. Chung[1], L-Y. Hung[1], J-S. Ren[1], T. Pan[1], S-H. Li[2], S-C. Chang[2], S-S. Sheu[2], W-C. Lo[2], C-I. Wu[2], X. Si[1], C-C. Lo[1], R-S. Liu[1], C-C. Hsieh[1], K-T. Tang[1], M-F. Chang[1,3]*

[1]National Tsing Hua University, Hsinchu, Taiwan
[2]Industrial Technology Research Institute, Hsinchu, Taiwan
[3]TSMC, Hsinchu, Taiwan
*Equally-Credited Authors (ECAs)

9:39 AM

16.4 An 89TOPS/W and 16.3TOPS/mm² All-Digital SRAM-Based Full-Precision Compute-In Memory Macro in 22nm for Machine-Learning Edge Applications

Y-D. Chih, P-H. Lee, H. Fujiwara, Y-C. Shih, C-F. Lee, R. Naous, Y-L. Chen, C-P. Lo, C-H. Lu, H. Mori, W-C. Zhao, D. Sun, M. E. Sinangil, Y-H. Chen, T-L. Chou, K. Akarvardar, H-J. Liao, Y. Wang, M-F. Chang, T-Y. J. Chang

TSMC, Hsinchu, Taiwan

DC-DC Converters

Session Chair: ***Li Geng,*** *Xi'an Jiaotong University, Xi'an, China*
Session Co-Chair: ***Harish Krishnamurthy,*** *Intel, Beaverton, OR*
Session Moderator: ***Gaël Pillonnet,*** *CEA-Léti, Grenoble, France*

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DS1 **8:30 AM**

17.1 A Two-Stage Cascaded Hybrid Switched-Capacitor DC-DC Converter with 96.9% Peak Efficiency Tolerating 0.6V/µs Input Slew Rate During Startup
Z. Xia, J. Stauth, Dartmouth College, Hanover, NH

DS1 **8:38 AM**

17.2 A Masterless Fault-Tolerant Hybrid Dickson Converter with 95.3% Peak Efficiency 20V-to-60V Input and 3.3V Output for 48V Multi-Phase Automotive Applications
M. Ashourloo[1], V. R. Namburi[1], G. Villar Piqué[2], J. Pigott[3], H. J. Bergveld[2], A. El Sherif[3], O. Trescases[1]
[1]University of Toronto, Toronto, Canada; [2]NXP Semiconductors, Eindhoven, The Netherlands
[3]NXP Semiconductors, Chandler, AZ

DS1 **8:46 AM**

17.3 A 1.25GHz Fully Integrated DC-DC Converter Using Electromagnetically Coupled Class-D LC Oscillators
A. Novello[1], G. Atzeni[1], G. Cristiano[1], M. Coustans[2], T. Jang[1]
[1]ETH Zurich, Zurich, Switzerland; [2]STMicroelectronics, Plan-les-Ouates, Switzerland

8:50 AM

17.4 Peak-Current-Controlled Ganged Integrated High-Frequency Buck Voltage Regulators in 22nm CMOS for Robust Cross-Tile Current Sharing
N. Desai[1], H. K. Krishnamurthy[1], K. Ahmed[1], S. Weng[1], S. Kim[1], X. Liu[1], H. T. Do[2], K. Radhakrishnan[2], K. Ravichandran[1], J. W. Tschanz[1], V. De[1]
[1]Intel, Hillsboro, OR; [2]Intel, Chandler, AZ

8:58 AM

17.5 A 98.2%-Efficiency Reciprocal Direct Charge Recycling Inductor-First DC-DC Converter
A. Abdulslam, P. P. Mercier, University of California, San Diego, La Jolla, CA

9:06 AM

17.6 A Reconfigurable DC-DC Converter for Maximum TEG Energy Harvesting in a Battery-Powered Wireless Sensor Node
Y-S. Noh, J-I. Seo, W-J. Choi, J-H. Kim, H. V. Phuoc, H-S. Kim, S-G. Lee, KAIST, Daejeon, Korea

9:10 AM

17.7 A 0.03mV/mA Low Crosstalk and 185nA Ultra-Low Quiescent Single-Inductor Multiple-Output Converter Assisted by 5-Input Operational Amplifier for 94.3% Peak Efficiency and 3.0W Driving Capability
T-H. Yang[1], Y-H. Wen[1], Y-J. Ouyang[1], C-K. Chiu[1], B-K. Wu[1], K-H. Chen[1], Y-H. Lin[2], S-R. Lin[2], T-Y. Tsai[2]
[1]National Chiao Tung University, Hsinchu, Taiwan; [2]Realtek Semiconductor, Hsinchu, Taiwan

9:18 AM

17.8 A 90.5%-Efficiency 28.7µV_{RMS}-Noise Bipolar-Output High-Step-Up SC DC-DC Converter with Energy-Recycled Regulation and Post-Filtering for ±15V TFT-Based LAE Sensors
M-W. Ko, H. Han, H-S. Kim, KAIST, Daejeon, Korea

9:26 AM

17.9 A High Conversion Ratio and 97.4% Peak-Efficiency 3-Switch Boost Converter with Duty-Dependent Charge Topology for 1.2A High Driving Current and 20% Reduction of Inductor DC Current in MiniLED Applications
Y-A. Lin[1], S-Y. Li[1], Z-L. Huang[1], C-S. Huang[1], C-H. Liang[1], K-S. Chang[1], K-C. Chung[1], K-H. Chen[1], Y-H. Lin[2], S-R. Lin[2], T-Y. Tsai[2]
[1]National Chiao Tung University, Hsinchu, Taiwan; [2]Realtek Semiconductor, Hsinchu, Taiwan

Biomedical Devices, Circuits, and Systems

Session Chair: ***Rabia Tugce Yazicigil,*** *Boston University, Boston, MA*

Session Co-Chair: ***Milin Zhang,*** *Tsinghua University, Beijing, China*

Session Moderator: ***Patrick P. Mercier,*** *University of California San Diego, La Jolla, CA*

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8:30 AM

18.1 An Optically-Addressed Nanowire-Based Retinal Prosthesis with 73% RF-to-Stimulation Power Efficiency and 20nC-to-3μC Wireless Charge Telemetering

A. Akinin[1], J. M. Ford[1], J. Wu[1], C. Kim[2], H. D. Thacker[3], P. P. Mercier[1], G. Cauwenberghs[1]
[1]University of California, San Diego, La Jolla, CA
[2]KAIST, Daejeon, Korea
[3]Nanovision Biosciences, San Diego, CA

DS1

8:38 AM

18.2 CMOS-Driven Pneumatic-Free Scalable Microfluidics and Fluid Processing with Label-Free Cellular and Bio-Molecular Sensing Capability for an End-to-End Point-of-Care System

C. Zhu, J. Maldonado, H. Tang, S. Venkatesh, K. Sengupta
Princeton University, Princeton, NJ

DS1

8:46 AM

18.3 An Integrated Thermal Actuation/Sensing Array with Stacked Oscillators for Efficient and Localized Heating of Magnetic Nanoparticles with Sub-Millimeter Spatial Resolution

Y. Fan, L. Zhang, Q. Zhang, G. Bao, T. Chi
Rice University, Houston, TX

8:54 AM

18.4 A Wireless Multimodality System-on-a-Chip with Time-Based Resolution Scaling Technique for Chronic Wound Monitoring

S-Y. Lu[1], S-S. Shan[1], S-C. Kuo[1], C-Z. Shao[1], Y-H. Yeh[1], I-T. Lin[1], S-P. Lin[2], Y-T. Liao[1]
[1]National Chiao Tung University, Hsinchu, Taiwan
[2]National Chung Hsing University, Taichung, Taiwan

Optical Systems for Emerging Applications

Session Chair: ***Munehiko Nagatani,*** *NTT, Atsugi, Japan*
Session Co-Chair: ***Nick van Helleputte,*** *imec, Heverlee, Belgium*
Session Moderator: ***Naveen Verma,*** *Princeton University, Princeton, NJ*

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DS1

9:15 AM

19.1 Optical Phased-Array FMCW LiDAR with On-Chip Calibration

S. Chung, M. Nakai, S. Idres, Y. Ni, H. Hashemi
University of Southern California, Los Angeles, CA

9:23 AM

19.2 A Mechanically Flexible Implantable Neural Interface for Computational Imaging and Optogenetic Stimulation over 5.4×5.4mm² FoV

S. Moazeni[*1,2], *E. H. Pollmann*[*1], *V. Boominathan*[3], *F. A. Cardoso*[1], *J. T. Robinson*[3], *A. Veeraraghavan*[3], *K. L. Shepard*[1]
[1]Columbia University, New York, NY
[2]University of Washington, Seattle, WA
[3]Rice University, Houston, TX
*Equally-Credited Authors (ECAs)

9:31 AM

19.3 A MEMS-Based Dynamic Light Focusing System for Single-Cell Precision in Optogenetics

C. Yalcin[1], *N. T. Ersumo*[1], *G. Bocchetti*[1], *M. M. Ghanbari*[1], *N. Antipa*[1], *S. Faraji Alamouti*[1], *L. Waller*[1,2], *D. Lopez*[3], *R. Muller*[1,2]
[1]University of California, Berkeley, CA
[2]Chan Zuckerberg Biohub, San Francisco, CA
[3]National Institute of Standards and Technology, Gaithersburg, MD

High-Performance VCOs

Session Chair: ***Andrea Bevilacqua,*** *University of Padova, Padova, Italy*
Session Co-Chair: ***Salvatore Levantino,*** *Politecnico di Milano, Milan, Italy*
Session Moderator: ***Hua Wang,*** *Georgia Tech, Atlanda, GA*

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8:30 AM

20.1 A 5.0-to-6.36GHz Wideband-Harmonic-Shaping VCO Achieving 196.9dBc/Hz Peak FoM and 90-to-180kHz 1/f³ PN Corner Without Harmonic Tuning

H. Guo[1], Y. Chen[1], P-I. Mak[1], R. P. Martins[1,2]
[1]University of Macau, Macau, China
[2]Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

8:38 AM

20.2 A 3.09-to-4.04GHz Distributed-Boosting and Harmonic-Impedance-Expanding Multi-Core Oscillator with -138.9dBc/Hz at 1MHz Offset and 195.1dBc/Hz FoM

Y. Shu[1], H. J. Qian[1], X. Gao[2], X. Luo[1]
[1]University of Electronic Science and Technology of China, Chengdu, China
[2]Zhejiang University, Hangzhou, China

8:46 AM

20.3 A 60GHz 186.5dBc/Hz FoM Quad-Core Fundamental VCO Using Circular Triple-Coupled Transformer with No Mode Ambiguity in 65nm CMOS

H. Jia, W. Deng, P. Guan, Z. Wang, B. Chi
Tsinghua University, Beijing, China

UWB Systems and Wake-Up Receivers

Session Chair: ***Hiroyuki Ito,*** *Tokyo Institute of Technology, Yokohama, Japan*
Session Co-Chair: ***Renaldi Winoto,*** *Mojo Vision, Saratoga, CA*
Session Moderator: ***Yao-Hong Liu,*** *imec, Eindhoven, The Netherlands*

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9:15 AM

21.1 A 1.125Gb/s 28mW 2m-Radio-Range IR-UWB CMOS Transceiver

G. Lee[1], S. Lee[1], J-H. Kim[2], T. W. Kim[1]
[1]Yonsei University, Seoul, Korea
[2]Ewha Womans University, Seoul, Korea

DS2

9:23 AM

21.2 A 3-to-10GHz 180pJ/b IEEE802.15.4z/4a IR-UWB Coherent Polar Transmitter in 28nm CMOS with Asynchronous Amplitude Pulse-Shaping and Injection-Locked Phase Modulation

E. Allebes, G. Singh, Y. He, E. Tiurin, P. Mateman, M. Ding, J. Dijkhuis, G-J. van Schaik, E. Bechthum, J. van den Heuvel, M. El Soussi, A. Breeschoten, H. Korpela, Y-H. Liu, C. Bachmann
imec-Netherlands, Eindhoven, The Netherlands

9:31 AM

21.3 A Fully Integrated 2.7µW -70.2dBm-Sensitivity Wake-Up Receiver with Charge-Domain Analog Front-End, -16.5dB-SIR, FEC and Cryptographic Checksum

K-K. Huang[1], J. K. Brown[2], N. Collins[3], R. K. Sawyer[4], F. B. Yahya[4], A. Wang[1], N. E. Roberts[4], B. H. Calhoun[4], D. D. Wentzloff[2]
[1]Everactive, Santa Clara, CA
[2]Everactive, Ann Arbor, MI
[3]now with Renesas, Palm Bay, FL
[4]Everactive, Charlottesville, VA

DS2

9:35 AM

21.4 A 0.75-to-1GHz Passive Wideband Noise-Cancelling 171µW Wake-Up RX and 440µW Primary RX FE with -86dBm/10kb/s Sensitivity, 35dB SIR and 3.8dB RX NF

H. Bialek[1], S. Ahasan[2], A. Binaie*[2], K. R. Sadagopan[1], M. L. Johnston[1], H. Krishnaswamy[2], A. Natarajan[1]*
[1]Oregon State University, Corvallis, OR
[2]Columbia University, New York, NY
*Equally-Credited Authors (ECAs)

DS2

9:43 AM

21.5 An Integrated 2.4GHz -91.5dBm-Sensitivity Within-Packet Duty-Cycled Wake-Up Receiver Achieving 2µW at 100ms Latency

H. L. Bishop, A. Dissanayake*, S. M. Bowers, B. H. Calhoun*
University of Virginia, Charlottesville, VA
*Equally-Credited Authors (ECAs)

Terahertz for Communication and Sensing

Session Chair: ***Jane Gu,*** *University of California, Davis, Davis, CA*
Session Co-Chair: ***Byung-Wook Min,*** *Yonsei University, Seoul, Korea*
Session Moderator: ***Maryam Tabesh,*** *Google, Mountain View, CA*

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DS2

8:30 AM

22.1 THz Prism: One-Shot Simultaneous Multi-Node Angular Localization Using Spectrum-to-Space Mapping with 360-to-400GHz Broadband Transceiver and Dual-Port Integrated Leaky-Wave Antennas

H. Saeidi, S. Venkatesh*, X. Lu, K. Sengupta*
Princeton University, Princeton, NJ
*Equally-Credited Authors (ECAs)

8:38 AM

22.2 A 300GHz-Band Phased-Array Transceiver Using Bi-Directional Outphasing and Hartley Architecture in 65nm CMOS

I. Abdo[1], C. da Gomez[1], C. Wang[1], K. Hatano[1], Q. Li[1], C. Liu[1], K. Yanagisawa[1], A. A. Fadila[1], J. Pang[1], H. Hamada[2], H. Nosaka[2], A. Shirane[1], K. Okada[1]
[1]Tokyo Institute of Technology, Tokyo, Japan
[2]NTT, Kanagawa, Japan

DS2

8:46 AM

22.3 A 0.42THz Coherent TX-RX System Achieving 10dBm EIRP and 27dB NF in 40nm CMOS for Phase-Contrast Imaging

D. Simic, K. Guo, P. Reynaert
KU Leuven - MICAS, Leuven, Belgium

8:54 AM

22.4 A 250GHz Autodyne FMCW Radar in 55nm BiCMOS with Micrometer Range Resolution

S. H. Naghavi[1], S. Seyedabbaszadehesfahlani[1], F. Khoeini[1], A. Cathelin[2], E. Afshari[1]
[1]University of Michigan, Ann Arbor, MI
[2]STMicroelectronics, Crolles, France

THz Circuits and Front-Ends

Session Chair: ***Swaminathan Sankaran,*** *Texas Instruments, Dallas, TX*
Session Co-Chair: ***Patrick Reynaert,*** *KU Leuven - MICAS, Leuven, Belgium*
Session Moderator: ***Shuhei Amakawa,*** *Hiroshima University, Higashihiroshima, Japan*

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DS1 **9:15 AM**

23.1 270-to-300GHz Double-Balanced Parametric Upconverter Using Asymmetric MOS Varactors and a Power-Splitting-Transformer Hybrid in 65nm CMOS

Z. Chen[1], W. Choi[2], K. O[1]
[1]University of Texas, Dallas, TX
[2]Oklahoma State University, Stillwater, OK

9:23 AM

23.2 A 436-to-467GHz Lens-Integrated Reconfigurable Radiating Source with Continuous 2D Steering and Multi-Beam Operations in 65nm CMOS

H. Jalili, O. Momeni
University of California, Davis, CA

DS1 **9:31 AM**

23.3 A 605GHz 0.84mW Harmonic Injection-Locked Receiver Achieving 2.3pW/√Hz NEP in 28nm CMOS

A. De Vroede, P. Reynaert
KU Leuven - MICAS, Leuven, Belgium

9:39 AM

23.4 An 82fs$_{rms}$-Jitter and 22.5mW-Power, 102GHz W-Band PLL Using a Power-Gating Injection-Locked Frequency-Multiplier-Based Phase Detector in 65nm CMOS

S. Yoo[*1], S. Park*[*1], S. Choi*[*1], Y. Cho[1], H. Yoon[2], C. Hwang[1], J. Choi[1]*
[1]KAIST, Daejeon, Korea
[2]Qualcomm, San Diego, CA
*Equally-Credited Authors (ECAs)

Advanced Embedded Memories

Session Chair: ***Eric Karl,*** *Intel, Hillsboro, OR*

Session Co-Chair: ***Shinichiro Shiratake,*** *Kioxia, Yokohama, Japan*

Session Moderator: ***Jonathan Chang,*** *TSMC, Hsinchu, Taiwan*

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7:00 AM

24.1 A 6.2 GHz Single Ended Current Sense Amplifier (CSA) Based Compileable 8T SRAM in 7nm FinFET Technology

A. Fritsch[1], R. Joshi[2], S. Chakraborty[2], H. Wetter[1], U. Srinivasan[1], M. Hyde[3], O. Torreiter[1], M. Kugel[1], D. Radko[3], H. Kim[3], D. Friedman[2]
[1]IBM, Boeblingen, Germany
[2]IBM Research, Yorktown Heights, NY
[3]IBM, Poughkeepsie

7:08 AM

24.2 A 14nm-FinFET 1Mb Embedded 1T1R RRAM with a 0.022μm² Cell Size Using Self-Adaptive Delayed Termination and Multi-Cell Reference

J. Yang[1,2], X. Xue[3], X. Xu[1], Q. Wang[1], H. Jiang[2], J. Yu[1], D. Dong[1], F. Zhang[1], H. Lv[1], M. Liu[1]
[1]Institute of Microelectronics of the Chinese Academy of Sciences, Beijing, China
[2]Zhejiang Lab, Hangzhou, China
[3]Fudan University, Shanghai, China

7:16 AM

24.3 A 3nm Gate-All-Around SRAM: Featuring an Adaptive Dual-BL and an Adaptive Cell-Power Assist Circuit

T. Song, W. Rim, H. Kim, K. H. Cho, T. Kim, T. Lee, G. Bae, D-W. Kim, S. Kwon, S. Baek, J. Jung, J. Kye, H. Jung, H. Kim, S-M. Jung, J. Park
Samsung Electronics, Hwaseong, Korea

7:24 AM

24.4 A 5nm 5.7GHz@1.0V and 1.3GHz@0.5V 4kb Standard-Cell-Based Two-Port Register File with a 16T Bitcell with No Half-Selection Issue

H. Fujiwara, Y-H. Nien, C-Y. Lin, H-Y. Pan, H-W. Hsu, S-R. Wu, Y-Y. Liu, Y-H. Chen, H-J. Liao, J. Chang
TSMC, Hsinchu, Taiwan

DRAM

Session Chair: ***Dong Uk Lee,*** *SK hynix, Icheon, Korea*
Session Co-Chair: ***Bor-Doou Rong,*** *Etron, Hsinchu, Taiwan*
Session Moderator: ***Kyu-Hyoun (KH) Kim,*** *IBM T. J. Watson, Yorktown Heights, NY*

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7:45 AM

25.1 A 24Gb/s/pin 8Gb GDDR6 with a Half-Rate Daisy-Chain-Based Clocking Architecture and IO Circuitry for Low-Noise Operation

K. Kim, J-H. Chae, J. Yang, J. Kang, G. Lee, S. Byeon, Y. Kim, B. Kim, D-H. Kim, Y. Cho, K. Choi, H. Park , J. Ji, S. Jeong, Y. Joo, J. Cha, M. Park , H. Kim, S. Park, K. Kong, S. Kim, S. Lee , J. Chun, H. Kim, S. Cha
SK hynix Semiconductor, Icheon, Korea

7:53 AM

25.2 A 16Gb Sub-1V 7.14Gb/s/pin LPDDR5 SDRAM Applying a Mosaic Architecture with a Short-Feedback 1-Tap DFE, an FSS Bus with Low-Level Swing and an Adaptively Controlled Body Biasing in a 3rd-Generation 10nm DRAM

Y-H. Kim, H-J. Kim, J. Choi, M-S. Ahn, D. Lee, S-H. Cho, D-Y. Park, Y-J. Park, M-S. Jang, Y-J. Kim, J. Choi, S-W. Yoon, J-W. Jung, J-K. Park, J-W. Lee, D-H. Kwon, H-S. Cha, S-H. Cho, S-H. Kim, J. You, K-H. Kim, D-H. Kim, B-C. Kim, Y-K. Kim, J-H. Kim, S-K. Choi, C-Y. Kim, B-W. Na, H-I. Choi, R. Oh, J-D. Ihm, S-J. Bae, N. S. Kim, J-B. Lee
Samsung Electronics, Hwaseong, Korea

8:01 AM

25.3 An 8Gb GDDR6X DRAM Achieving 22Gb/s/pin with Single-Ended PAM-4 Signaling

T. M. Hollis[1], R. Schneider[2], M. Brox[2], T. Hein[2], W. Spirkl[2], M. Bach[2], M. Balakrishnan[2], S. Dietrich[2], F. Funfrock[2], M. Ivanov[2], N. Jovanovic[2], M. Kuzmenka[2], D. Lauber[2], J. Ocon-Garrido[2], D. Ovard[1], K. Pfefferl[2], S. Piatkowski[2], G. Piscopo[2], M. Plan[2], J. Polney[2], J. Pottgiesser[2], S. Rau[2], F. Vitale[2], M. Walter[2], M. Alvarez-Gonzalez[2], M. Broschwitz[2], C. Chetreanu[2], A. Sorrentino[2], J. Weller[2], P. Mayer[2], M. Richter[2], C. S. Garcia[2], A. Schneider[2], S. N. Wong[3]
[1]Micron Technology, Boise, ID
[2]Micron Semiconductor, Munich, Germany
[3]Micron Semiconductor, Singapore, Singapore

DS1 **8:09 AM**

25.4 A 20nm 6GB Function-In-Memory DRAM, Based on HBM2 with a 1.2TFLOPS Programmable Computing Unit Using Bank-Level Parallelism, for Machine Learning Applications

Y-C. Kwon[1], S. H. Lee[1], J. Lee[1], S-H. Kwon[1], J. M. Ryu[1], J-P. Son[1], S. O[1], H-S. Yu[1], H. Lee[1], S. Y. Kim[1], Y. Cho[1], J. G. Kim[1], J. Choi[1], H-S. Shin[1], J. Kim[1], B. Phuah[1], H. Kim[1], M. J. Song[1], A. Choi[1], D. Kim[1], S. Kim[1], E-B. Kim[1], D. Wang[2], S. Kang[1], Y. Ro[3], S. Seo[3], J. Song[3], J. Youn[1], K. Sohn[1], N. S. Kim[1]
[1]Samsung Electronics, Hwaseong, Korea
[2]Samsung Electronics, San Jose
[3]Samsung Electronics, Suwon, Korea

RF Power-Amplifier and Front-End Techniques

Session Chair: ***Hongtao Xu,*** *Fudan University, Shanghai, China*
Session Co-Chair: ***Toshiya Mitomo,*** *Toshiba, Kanagawa, Japan*
Session Moderator: ***James Buckwalter,*** *University of California, Santa Barbara, CA*

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DS1

7:00 AM

26.1 A 26-to-60GHz Continuous Coupler-Doherty Linear Power Amplifier for Over-An-Octave Back-Off Efficiency Enhancement
T-Y. Huang, N. S. Mannem, S. Li, D. Jung, M-Y. Huang, H. Wang
Georgia Institute of Technology, Atlanta, GA

7:08 AM

26.2 A Doherty-Like Load-Modulated Balanced Power Amplifier Achieving 15.5dBm Average P_{out} and 20% Average PAE at a Data Rate of 18Gb/s in 28nm CMOS
V. Qunaj, P. Reynaert
KU Leuven - MICAS, Leuven, Belgium

7:16 AM

26.3 A mm-Wave Power Amplifier for 5G Communication Using a Dual-Drive Topology Exhibiting a Maximum PAE of 50% and Maximum DE of 60% at 30GHz
E. F. Garay, D. J. Munzer, H. Wang
Georgia Institute of Technology, Atlanta, GA

7:24 AM

26.4 A Reflection-Coefficient Sensor for 28GHz Beamforming Transmitters in 22nm FD-SOI CMOS
Y. Zhang, G. Mangraviti, J. Nguyen, Z. Zong, P. Wambacq
imec, Heverlee, Belgium

7:32 AM

26.5 A Watt-Level Quadrature Switched/Floated-Capacitor Power Amplifier with Back-Off Efficiency Enhancement in Complex Domain Using Reconfigurable Self-Coupling Canceling Transformer
B. Yang, H. J. Qian, X. Luo
University of Electronic Science and Technology of China, Chengdu, China

7:40 AM

26.6 A 5-to-6GHz Current-Mode Subharmonic Switching Digital Power Amplifier for Enhancing Power Back-Off Efficiency
A. Zhang, C. Yang, M. Ayesh, M-W. Chen
University of Southern California, Los Angeles, CA

7:48 AM

26.7 An Impedance-Transforming N-Path Filter Offering Passive Voltage Gain
M. Khorshidian, H. Krishnaswamy
Columbia University, New York, NY

Discrete-Time ADCs

Session Chair: ***John Keane,*** *Keysight Technologies, Santa Clara, CA*
Session Co-Chair: ***Chih-Cheng Hsieh,*** National Tsing Hua University, Hsinchu, Taiwan
Session Moderator: ***Bob Verbruggen,*** *Xilinx, Dublin, Ireland*

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7:00 AM

27.1 A 250kHz-BW 93dB-SNDR 4th-Order Noise-Shaping SAR Using Capacitor Stacking and Dynamic Buffering

J. Liu[1], D. Li[2], Y. Zhong[1], X. Tang[3], N. Sun[1,3]
[1]Tsinghua University, Beijing, China
[2]Xidian University, Xi'an, China
[3]University of Texas, Austin, TX

7:08 AM

27.2 14.1-ENOB 184.9dB-FoM Capacitor-Array-Assisted Cascaded Charge-Injection SAR ADC

K. Choo, H. An, D. Sylvester, D. Blaauw
University of Michigan, Ann Arbor, MI

7:16 AM

27.3 A 13.8-ENOB 0.4pF-C_{IN} 3rd-Order Noise-Shaping SAR in a Single-Amplifier EF-CIFF Structure with Fully Dynamic Hardware-Reusing kT/C Noise Cancelation

T-H. Wang, R. Wu, V. Gupta, S. Li
Georgia Institute of Technology, Atlanta, GA

7:24 AM

27.4 A 0.4-to-40MS/s 75.7dB-SNDR Fully Dynamic Event-Driven Pipelined ADC with 3-Stage Cascoded Floating Inverter Amplifier

X. Tang[1], X. Yang[1], J. Liu[2], W. Shi[1], D. Z. Pan[1], N. Sun[1,2]
[1]University of Texas, Austin, TX
[2]Tsinghua University, Beijing, China

7:32 AM

27.5 An 80MHz-BW 640MS/s Time-Interleaved Passive Noise-Shaping SAR ADC in 22nm FDSOI Process

C-Y. Lin, Y-Z. Lin*, C-H. Tsai, C-H. Lu*
MediaTek, Hsinchu, Taiwan
*Equally-Credited Authors (ECAs)

7:40 AM

27.6 A 25MHz-BW 75dB-SNDR Inherent Gain Error Tolerance Noise-Shaping SAR-Assisted Pipeline ADC with Background Offset Calibration

H. Zhang[1], Y. Zhu[1], C-H. Chan[1], R. Martins[1,2]
[1]University of Macau, Macau, China
[2]Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

7:48 AM

27.7 A 79dB-SNDR 167dB-FoM Bandpass ΔΣ ADC Combining N-Path Filter with Noise-Shaping SAR

L. Shen[1,2], Z. Gao[3], X. Yang[2], W. Shi[2], N. Sun[2,3]
[1]Peking University, Beijing, China
[2]University of Texas, Austin, TX
[3]Tsinghua University, Beijing, China

Biomedical Systems

Session Chair: ***Joonsung Bae,*** *Kangwon National University, Chuncheon, Korea*
Session Co-Chair: ***Jennifer Lloyd,*** *Analog Devices, Santa Clara, CA*
Session Moderator: ***Chris Van Hoof,*** *IMEC, Leuven, Belgium*

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7:00 AM

28.1 A Distortion-Free VCO-Based Sensor-to-Digital Front-End Achieving 178.9dB FoM and 128dB SFDR with a Calibration-Free Differential Pulse-Code Modulation Technique
J. Huang, P. P. Mercier, University of California, San Diego, CA

7:08 AM

28.2 A 400-to-1000nm 24µW Monolithic PPG Sensor with 0.3A/W Spectral Responsivity for Miniature Wearables
S-J. Jung, J. Ryu, W. Kim, S. Lee, J. Kim, H. Park, T. Jang, H. Jeong, J. Kim, J. Park, R. Kim, J. Park, H. Jo, W. J. Kim, J. Yang, B. Sohn, Y. Han, I. Lim, S. Yoo, C. Park, D-G. Jang, B-H. Ko, J. Lim, J. Kim, K. Lee, J. Lee, Y. Park, L. Yan
Samsung Electronics, Hwaseong, Korea

DS2

7:16 AM

28.3 A 28µW 134dB DR 2nd-Order Noise-Shaping Slope Light-to-Digital Converter for Chest PPG Monitoring
Q. Lin[1,2], S. Song[1], R. Van Wegberg[3], M. Konijnenburg[3], D. Biswas[1], C. Van Hoof[1,2], F. Tavernier[2], N. Van Helleputte[1]
[1]imec, Leuven, Belgium; [2]KU Leuven, Leuven, Belgium; [3]imec - Holst Centre, Eindhoven, The Netherlands

7:24 AM

28.4 A 400mV$_{pp}$ 92.3dB-SNDR 1kHz-BW 2nd-Order VCO-Based ExG-to-Digital Front-End Using a Multiphase Gated-Inverted Ring-Oscillator Quantizer
C. Pochet, J. Huang, P. P. Mercier, D. A. Hall, University of California, San Diego, CA

DS2

7:32 AM

28.5 A 0.6V/0.9V 26.6-to-119.3µW ΔΣ-Based Bio-Impedance Readout IC with 101.9dB SNR and <0.1Hz 1/f Corner
T. Zhang[1], H. Son*[1], Y. Gao[1], J. Lan[1], C-H. Heng[2]*
[1]Institute of Microelectronics, A*STAR, Singapore; [2]National University of Singapore, Singapore, Singapore
*Equally-Credited Authors (ECAs)

DS2

7:40 AM

28.6 A 22.6µW Biopotential Amplifier with Adaptive Common-Mode Interference Cancelation Achieving Total-CMRR of 104dB and CMI Tolerance of 15V$_{pp}$ in 0.18µm CMOS
N. Koo[1], H. Kim[2], S. Cho[1]
[1]KAIST, Daejeon, Korea; [2]Korea Aerospace Research Institute, Daejeon, Korea

7:48 AM

28.7 A 0.00378mm² Scalable Neural Recording Front-End for Fully Immersible Neural Probes Based on a Two-Step Incremental Delta-Sigma Converter with Extended Counting and Hardware Reuse
D. Wendler[1], D. De Dorigo[1], M. Amayreh[2], A. Bleitner[1], M. Marx[1], Y. Manoli[1,2]
[1]University of Freiburg - IMTEK, Freiburg im Breisgau, Germany; [2]Hahn-Schickard, Villingen-Schwenningen, Germany

7:56 AM

28.8 Multi-Modal Peripheral Nerve Active Probe and Microstimulator with On-Chip Dual-Coil Power/Data Transmission and 64 2nd-Order Opamp-Less ΔΣ ADCs
M. ElAnsary, J. Xu, J. Sales Filho, G. Dutta, L. Long, A. Shoukry, C. Tejeiro, C. Tang, E. Kilinc, J. Joshi, P. Sabetian, S. Unger, J. Zariffa, P. Yoo, R. Genov, University of Toronto, Toronto, Canada

Digital Circuits for Computing, Clocking and Power Management

Session Chair: ***Ping-Hsuan Hsieh,*** *National Tsing Hua University, Hsinchu, Taiwan*
Session Co-Chair: ***Mingoo Seok,*** *Columbia University, New York, NY*
Session Moderator: ***Keith Bowman,*** *Qualcomm, Raleigh, NC*

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7:00 AM

29.1 A 40nm 64Kb 56.67TOPS/W Read-Disturb-Tolerant Compute-in-Memory/Digital RRAM Macro with Active-Feedback-Based Read and In-Situ Write Verification
J-H. Yoon[1], M. Chang[1], W-S. Khwa[2], Y-D. Chih[3], M-F. Chang[2], A. Raychowdhury[1]
[1]Georgia Institute of Technology, Atlanta, GA
[2]TSMC Corporate Research, Hsinchu, Taiwan
[3]TSMC Design Technology, Hsinchu, Taiwan

7:08 AM

29.2 A 21×21 Dynamic-Precision Bit-Serial Computing Graph Accelerator for Solving Partial Differential Equations Using Finite Difference Method
J. Mu[1], B. Kim[1,2], [1]Nanyang Technological University, Singapore, Singapore; [2]now with University of California, Santa Barbara, CA

7:16 AM

29.3 80ns Fast-Lock 0.4-to-6.5GHz Clock Generator with Self-Referenced Asynchronous Adaptive Droop Mitigation
P. Mosalikanti, Q. S. Wang, K-Y. J. Shen, M. Neidengard, S. F. Syed Farooq, V. Grossnickle, N. Kurd, Intel, Portland, OR

DS2 **7:24 AM**

29.4 A Fractional-N Digital MDLL with Background Two-Point DTC Calibration Achieving -60dBc Fractional Spur
Q. Zhang[1], S. Su[1], C-R. Ho[2], M. S-W. Chen[1]
[1]University of Southern California, Los Angeles, CA
[2]Inphi, Santa Clara, CA

DS2 **7:32 AM**

29.5 A 0.008mm² 1.5mW 0.625-to-200MHz Fractional Output Divider with 120fs$_{rms}$ Jitter Based on Replica-DTC-Free Background Calibration
C-Y. Lin, Y-T. Hung, T-J. Wang, T-H. Lin, National Taiwan University, Taipei, Taiwan

7:40 AM

29.6 A Distributed Digital LDO with Time-Multiplexing Calibration Loop Achieving 40A/mm² Current Density and 1mA-to-6.4A Ultra-Wide Load Range in 5nm FinFET CMOS
D-H. Jung, T-H. Kong, J-H. Yang, S. Kim, K. Kim, J. Park, M. Choi, J. Shin, Samsung Electronics, Hwaseong, Korea

7:48 AM

29.7 A Single-Inductor 4-Output SoC with Dynamic Droop Allocation and Adaptive Clocking for Enhanced Performance and Energy Efficiency in 65nm CMOS
C-H. Huang, X. Sun, Y. Chen, R. Pamula, A. Mandal, V. Sathe, University of Washington, Seattle, WA

DS2 **7:56 AM**

29.8 115nA@3V ULPMark-CP Score 1205 SCVR-Less Dynamic Voltage-Stacking Scheme for IoT MCU
X. Li[1], Y. Xu[1,2], L. Ren[1], W. Ge[1,2], J. Cai[1], X. Liu[1,2], J. Yang[1,2]
[1]Nanjing Low Power IC Technology Institute, Nanjing, China
[2]Southeast University, Nanjing, China

Non-Volatile Memory

Session Chair: ***Yasuhiko Taito,*** *Renesas Electronics, Kodaira, Japan*

Session Co-Chair: ***Violante Moschiano,*** *Micron Semiconductor, Avezzano, Italy*

Session Moderator: ***Shinichiro Shiratake,*** *Kioxia, Yokohama, Japan*

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8:30 AM

30.1 A 176-Stacked 512Gb 3b/Cell 3D-NAND Flash with 10.8Gb/mm² Density with a Peripheral Circuit Under Cell Array Architecture

J-W. Park, D. Kim, S. Ok, J. Park, T. Kwon, H. Lee, S. Lim, S-Y. Jung, H. Choi, T. Kang, G. Park, C-W. Yang, J-G. Choi, G. Ko, J. Shin, I. Yang, J. Nam, H. Sohn, S-I. Hong, Y. Jeong, S-W. Choi, C. Choi, H-S. Shin, J. Lim, D. Youn, S. Nam, J. Lee, M. Ahn, H. Lee, S. Lee, J. Park, K. Gwon, W. Jeong, J. Choi, J. Kim, K-W. Jin

SK hynix Semiconductor, Icheon, Korea

8:38 AM

30.2 A 1Tb 4b/Cell 144-Tier Floating-Gate 3D-NAND Flash Memory with 40MB/s Program Throughput and 13.8Gb/mm² Bit Density

A. Khakifirooz[1], S. Balasubrahmanyam[2], R. Fastow[1], K. H. Gaewsky[2], C. W. Ha[1], R. Haque[2], O. W. Jungroth[2], S. Law[1], A. S. Madraswala[2], B. Ngo[2], N. Prabhu V[2], S. Rajwade[1], K. Ramamurthi[2], R. S. Shenoy[1], J. Snyder[2], C. Sun[1], D. Thimmegowda[1], B. M. Pathak[2], P. Kalavade[1]

[1]Intel, Santa Clara, CA
[2]Intel, Folsom, CA

8:46 AM

30.3 A 512Gb 3b/Cell 7th-Generation 3D-NAND Flash Memory with 184MB/s Write Throughput and 2.0Gb/s Interface

J. Cho, D. Kang, J. Park, S-W. Nam, J-H. Song, B-K. Jung, J. LYU, H. Lee, W-T. Kim, H. JEON, S. KIM, I-M. Kim, J-I. Son, K. KANG, S-W. Shim, J. Park, E. Lee, K-M. Kang, S-W. Park, J. Lee, S. H. Moon, P. KWAK, B. Jeong, C. A. Lee, K. KIM, J. Ko, T-H. Kwon, J. Lee, Y. Lee, C. Kim, M-W. Lee, J-Y. Yun, H. Lee, Y. Choi, S. Hong, J. Park, Y. Shin, H. Kim, H. Kim, C. Yoon, D. S. Byeon, S. Lee, J-Y. LEE, J. Song

Samsung Electronics, Seoul, Korea

8:54 AM

30.4 A 1Tb 3b/Cell 3D-Flash Memory in a 170+ Word-Line-Layer Technology

T. Higuchi[1], T. Kodama[1], K. Kato[1], R. Fukuda[1], N. Tokiwa[1], M. Abe[1], T. Takagiwa[1], Y. Shimizu[1], J. Musha[1], K. Sakurai[1], J. Sato[1], T. Utsumi[1], K. Yoneya[1], Y. Suematsu[1], T. Hashimoto[1], T. Hioka[1], K. Yanagidaira[1], M. Kojima[1], J. Matsuno[1], K. Shiraishi[1], K. Yamamoto[1], S. Hayashi[1], T. Hashiguchi[1], K. Inuzuka[1], A. Sugahara[1], M. Honma[1], K. Tsunoda[1], K. Yamamoto[1], T. Sugimoto[1], T. Fujimura[1], M. Kaneko[1], H. Date[1], O. Kobayashi[1], T. Minamoto[1], R. Tachibana[1], I. Yamaguchi[1], J. Lee[2], V. Ramachandra[2], S. Rajendra[2], T. Tang[2], S. Darne[2], J. Lee[2], J. Li[2], T. Miwa[2], R. Yamashita[2], H. Sugawara[2], N. Ookuma[2], M. Kano[2], H. Mizukoshi[2], Y. Kuniyoshi[2], M. Watanabe[2], K. Akiyama[2], H. Mori[2], A. Arimizu[2], Y. Katano[2], M. Ehama[2], H. Maejima[1], K. Hosono[1], M. Yoshihara[1]

[1]KIOXIA, Yokohama, Japan
[2]Western Digital, Milpitas, CA

Analog Techniques

Session Chair: ***Marco Berkhout,*** *Goodix, Nijmegen, The Netherlands*
Session Co-Chair: ***Drew A. Hall,*** *University of California, San Diego, CA*
Session Moderator: ***Jiawei Xu,*** *Fudan University, Shanghai, China*

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9:15 AM

31.1 An 82mW ΔΣ-Based Filter-Less Class-D Headphone Amplifier with -93dB THD+N, 113dB SNR and 93% Efficiency

A. Matamura[1], N. Nishimura[1], P. Birdsong[2], A. Bandyopadhyay[2], A. Spirer[2], M. Markova[2], S. Liu[2]
[1]Analog Devices, Tokyo, Japan
[2]Analog Devices, Wilmington, MA

9:23 AM

31.2 A 0.9V 28MHz Dual-RC Frequency Reference with 5pJ/Cycle and ±200ppm Inaccuracy from -40°C to 85°C

W. Choi[1], J. A. Angevare[2], I. Park[1], K. A. A. Makinwa[2], Y. Chae[1]
[1]Yonsei University, Seoul, Korea
[2]Delft University of Technology, Delft, The Netherlands

9:31 AM

31.3 A 0.14mm² 16MHz CMOS RC Frequency Reference with a 1-Point Trimmed Inaccuracy of ±400ppm from –45°C to 85°C

H. Jiang, S. Pan, Ç. Gürleyük, K. A. A. Makinwa
Delft University of Technology, Delft, The Netherlands

9:39 AM

31.4 A Chopper-Stabilized Amplifier with -107dB IMD and 28dB Suppression of Chopper-Induced IMD

T. Rooijers[1], S. Karmakar[1], Y. Kusuda[2], J. H. Huijsing[1], K. A. A. Makinwa[1]
[1]Delft University of Technology, Delft, The Netherlands
[2]Analog Devices, San Jose, CA

Frequency Synthesizers

Session Chair: ***Wei Deng,*** *Tsinghua University, Beijing, China*
Session Co-Chair: ***Jaehyouk Choi,*** *KAIST, Daejeon, Korea*
Session Moderator: ***Wanghua Wu,*** *Samsung, San Jose, CA*

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Live Session: Recap and Q&A will be scheduled according to the following program.
Both On-demand content and recorded live Q&A content will be available until March 31, 2021.

8:30 AM

32.1 A 365fs$_{rms}$-Jitter and –63dBc-Fractional Spur 5.3GHz-Ring-DCO-Based Fractional-N DPLL Using a DTC Second/Third-Order Nonlinearity Cancelation and a Probability-Density-Shaping ΔΣM

H. Park[1], C. Hwang*[1], T. Seong*[1,2], Y. Lee[3], J. Choi[1]*
[1]KAIST, Daejeon, Korea; [2]Ulsan National Institute of Science and Technology, Ulsan, Korea
[3]Samsung Electronics, Hwaseong, Korea; *Equally-Credited Authors (ECAs)

8:38 AM

32.2 A 14nm Analog Sampling Fractional-N PLL with a Digital-to-Time Converter Range-Reduction Technique Achieving 80fs Integrated Jitter and 93fs at Near-Integer Channels

W. Wu[1], C-W. Yao[1], C. Guo[1], P-Y. Chiang[1], P-K. Lau[1], L. Chen[1], S. W. Son[1], T. B. Cho[2]
[1]Samsung Semiconductor, San Jose, CA; [2]Samsung Electronics, Hwaseong, Korea

8:46 AM

32.3 A 12.9-to-15.1GHz Digital PLL Based on a Bang-Bang Phase Detector with Adaptively Optimized Noise Shaping Achieving 107.6fs Integrated Jitter

M. Mercandelli[1], A. Santiccioli*[1], S. M. Dartizio*[1], A. Shehata[1], F. Tesolin[1], S. Karman[1], L. Bertulessi[1], F. Buccoleri[1], L. Avallone[2], A. Parisi[1], A. L. Lacaita[1], M. P. Kennedy[2], C. Samori[1], S. Levantino[1]*
[1]Politecnico di Milano, Milan, Italy; [2]University College Dublin, Dublin, Ireland; *Equally-Credited Authors (ECAs)

8:54 AM

32.4 A 104fs$_{rms}$-Jitter and –61dBc-Fractional Spur 15GHz Fractional-N Subsampling PLL Using a Voltage-Domain Quantization-Error Cancelation Technique

J. Kim[1], Y. Jo*[1], Y. Lim*[2], T. Seong[2], H. Park[1], S. Yoo[1], Y. Lee[3], S. Choi[1], J. Choi[1]*
[1]KAIST, Daejeon, Korea; [2]Ulsan National Institute of Science and Technology, Ulsan, Korea
[3]Samsung Electronics, Hwaseong, Korea; *Equally-Credited Authors (ECAs)

9:02 AM

32.5 A 24GHz Self-Calibrated ADPLL-Based FMCW Synthesizer with 0.01% rms Frequency Error Under 3.2GHz Chirp Bandwidth and 320MHz/μs Slope

Z. Shen[1], H. Jiang[1], F. Yang[1], Y. Wang[2], Z. Zhang[1], J. Liu[1], H. Liao[1]
[1]Peking University, Beijing, China; [2]University of British Columbia, Vancouver, BC, Canada

9:10 AM

32.6 A K-Band 12.1-to-16.6GHz Subsampling ADPLL with 47.3fs$_{rms}$ Jitter Based on a Stochastic Flash TDC and Coupled Dual-Core DCO in 16nm FinFET CMOS

E. Thaller[1], R. Levinger[2], E. Shumaker[2], A. Farber[2], S. Bershansky[2], N. Geron[2], A. Ravi[3], R. Banin[2], J. Kadry[2], G. Horovitz[2], C. Krassnitzer[1], C. Duller[1], P. Torta[1], M. Elzinga[4], K. Azadet[5]
[1]Intel, Villach, Austria; [2]Intel, Israel, Israel; [3]Intel, Hillsboro, OR; [4]Intel, Folsom, CA; [5]Intel, Santa Clara, CA

9:14 AM

32.7 A 32kHz-Reference 2.4GHz Fractional-N Oversampling PLL with 200kHz Loop Bandwidth

J. Qiu, Z. Sun, B. Liu, W. Wang, D. Xu, H. Herdian, H. Huang, Y. Zhang, Y. Wang, A. Shirane, K. Okada
Tokyo Institute of Technology, Tokyo, Japan

9:22 AM

32.8 A 98.4fs-Jitter 12.9-to-15.1GHz PLL-Based LO Phase-Shifting System with Digital Background Phase-Offset Correction for Integrated Phased Arrays

A. Santiccioli[1], M. Mercandelli*[1], S. M. Dartizio*[1], F. Tesolin[1], S. Karman[1], A. Shehata[1], L. Bertulessi[1], F. Buccoleri[1], L. Avallone[2], A. Parisi[1], D. Cherniak[3], A. L. Lacaita[1], M. P. Kennedy[2], C. Samori[1], S. Levantino[1]*
[1]Politecnico di Milano, Milano, Italy; [2]University College Dublin, Dublin, Ireland; [3]Infineon Technologies, Villach, Austria
*Equally-Credited Authors (ECAs)

High-Voltage, GaN and Wireless Power

Session Chair: ***Min Chen,*** *Analog Devices, Santa Clara, CA*

Session Co-Chair: ***Bernhard Wicht,*** *University of Hannover, Hannover, Germany*

Session Moderator: ***Kousuke Miyaji,*** *Shinshu University, Nagano, Japan*

On Demand Content will be available on Friday, February 5, 2021, 5:00PM PST
Live Session: Recap and Q&A will be scheduled according to the following program.
Both On-demand content and recorded live Q&A content will be available until March 31, 2021.

8:30 AM

33.1 A Fully Integrated GaN-on-Silicon Gate Driver and GaN Switch with Temperature-compensated Fast Turn-on Technique for Improving Reliability

H-Y. Chen[1], Y-Y. Kao[1], Z-Q. Zhang[1], C-H. Liao[1], H-Y. Yang[1], M-S. Hsu[1], K-H. Chen[1], Y-H. Lin[2], S-R. Lin[2], T-Y. Tsai[2]
[1]National Chiao Tung University, Hsinchu, Taiwan; [2]Realtek Semiconductor, Hsinchu, Taiwan

DS2

8:38 AM

33.2 A 600V GaN Active Gate Driver with Dynamic Feedback Delay Compensation Technique Achieving 22.5% Turn-On Energy Saving

J. Zhu[1], D. Yan[1], S. Yu[1], W. Sun[1], G. Shi[1], S. Liu[1], S. Zhang[2]
[1]Southeast University, Nanjing, China; [2]Central Semiconductor Manufacturing Corporation, Wuxi, China

8:42 AM

33.3 An Automotive-Use 2MHz 100V_{OUT} Flicker-Free Frequency-Modulated GaN-Based Buck-Boost LED Driver Achieving Bootstrap Charge Balancing and 16.8dBμV Radiated EMI Noise Reduction

X. Ke[1], W. C. Liu[1], M. K. Song[1], J. Xue[1], C. Zheng[2], K. Liu[2], Y. Leng[2], M. Chen[1]
[1]Analog Devices, Santa Clara, CA; [2]Analog Devices, Hangzhou, China

8:50 AM

33.4 An 8A 998A/inch³ 90.2% Peak Efficiency 48V-to-1V DC-DC Converter Adopting On-Chip Switch and GaN Hybrid Power Conversion

X. Yang, H. Cao, C. Xue, L. He, Z. Tan, M. Zhao, Y. Ding, W. Li, W. Qu, Zhejiang University, Hangzhou, China

DS2

8:58 AM

33.5 A 1.25W 46.5%-Peak-Efficiency Transformer-in-Package Isolated DC-DC Converter Using Glass-Based Fan-Out Wafer-Level Packaging Achieving 50mW/mm² Power Density

D. Pan[1], G. Li[1], F. Miao[1], B. Deng[1], J. Wei[2], D. Yu[2], M. Liu[3], L. Cheng[1]
[1]University of Science and Technology of China, Hefei, China; [2]Xiamen University, Xiamen, China
[3]Institute of Microelectronics of the Chinese Academy of Sciences, Beijing, China

9:02 AM

33.6 A Wireless Power Transfer System with Up-to-20% Light-Load Efficiency Enhancement and Instant Dynamic Response by Fully Integrated Wireless Hysteretic Control for Bioimplants

J. Tang, L. Zhao, C. Huang, Iowa State University, Ames, IA

9:10 AM

33.7 A Frequency-Splitting-Based Wireless Power and Data Transfer IC for Neural Prostheses with Simultaneous 115mW Power and 2.5Mb/s Forward Data Delivery

Y. Park[1], S-T. Koh[1], J. Lee[2], H. Kim[1], J. Choi[1], S. Ha[3], C. Kim[1], M. Je[1]
[1]KAIST, Daejeon, Korea; [2]Samsung Electronics, Hwaseong, Korea
[3]New York University Abu Dhabi, Abu Dhabi, United Arab Emirates

DS2

9:18 AM

33.8 A Decentralized Daisy-Chain-Controlled Switched-Capacitor Driver for Microrobotic Actuators with 10× Power-Reduction Factor and Over 300V Drive Voltage

Y. Li, B. L. Dobbins, J. T. Stauth, Dartmouth College, Hanover, NH

9:26 AM

33.9 A Hybrid Switching Supply Modulator Achieving 130MHz Envelope-Tracking Bandwidth and 10W Output Power for 2G/3G/LTE/NR RF Power Amplifiers

D. Kim, J-S. Bang, J. Baek, S. Park, Y-H. Jung, J. Han, I-H. Kim, S-Y. Jung, T. Nomiyama, J-S. Paek, J. Lee, T. B. Cho
Samsung Electronics, Hwasung, Korea

Emerging Imaging Solutions

Session Chair: ***Kazuko Nishimura,*** *Panasonic, Moriguchi, Japan*
Session Co-Chair: ***Johan Vanderhaegen,*** *Google, Mountain View, CA*
Session Moderator: ***Matteo Perenzoni,*** *Fondazione Bruno Kessler (FBK), Trento, Italy*

On Demand Content will be available on Friday, February 5, 2021, 5:00PM PST
Live Session: Recap and Q&A will be scheduled according to the following program.
Both On-demand content and recorded live Q&A content will be available until March 31, 2021.

DS2

8:30 AM

34.1 An 8960-Element Ultrasound-on-Chip for Point-of-Care Ultrasound

N. Sanchez[*1], *K. Chen*[*1], *C. Chen*[1], *D. McMahill*[1], *S. Hwang*[1], *J. Lutsky*[1], *J. Yang*[1], *L. Bao*[1], *L. K. Chiu*[1], *G. Peyton*[1], *H. Soleimani*[1], *B. Ryan*[1], *J. Petrus*[1], *Y-J. Kook*[1], *T. S. Ralston*[2], *K. G. Fife*[2], *J. M. Rothberg*[2]
[1]Butterfly Network, Guilford, CT
[2]4Catalyzer, Guilford, CT
*Equally-Credited Authors (ECAs)

8:38 AM

34.2 A 21pJ/frame/pixel Imager and 34pJ/frame/pixel Image Processor for a Low-Vision Augmented-Reality Smart Contact Lens

R. Singh, S. Bailey, P. Chang, A. Olyaei, M. Hekmat, R. Winoto
Mojo Vision, Saratoga, CA

8:46 AM

34.3 A 32×32 Pixel 0.46-to-0.75THz Light-Field Camera SoC in 0.13µm CMOS

R. Jain, P. Hillger, J. Grzyb, E. Ashna, V. Jagtap, R. Zatta, U. R. Pfeiffer
University of Wuppertal, Wuppertal, Germany

8:54 AM

34.4 An Energy-Replenishing Ultrasound Pulser with 0.25CV²f Dynamic Power Consumption

J. Choi[1], *Y. Park*[1], *J. B. Oh*[2], *J-Y. Kim*[3], *J. Y. Hwang*[4], *S. Ha*[5], *C. Kim*[1], *M. Je*[1]
[1]KAIST, Daejeon, Korea
[2]Endolfin, Anyang, Korea
[3]Daegu Catholic University Medical Center, Daegu, Korea
[4]Daegu Gyeongbuk Institute of Science and Technology, Daegu, Korea
[5]New York University Abu Dhabi, Abu Dhabi, United Arab Emirates

Adaptive Digital Techniques for Variation Tolerant Systems

Session Chair: ***Arijit Raychowdhury,*** *Georgia Institute of Technology, Atlanta, GA*
Session Co-Chair: ***Mijung Noh,*** *Samsung Electronics, Hwaseong, Korea*
Session Moderator: ***Keith Bowman,*** *Qualcomm, Raleigh, NC*

On Demand Content will be available on Friday, February 5, 2021, 5:00PM PST
Live Session: Recap and Q&A will be scheduled according to the following program.
Both On-demand content and recorded live Q&A content will be available until March 31, 2021.

8:30 AM

35.1 An Octa-Core 2.8/2GHz Dual-Gear Sensor-Assisted High-Speed and Power-Efficient CPU in 7nm FinFET 5G Smartphone SoC

B-J. Huang, E-W. Fang, S-Y. Hsueh, R. Huang, A. Lin, C-H. Chiang, Y-H. Lin, W-W. Hsieh, B. Chen, Y-C. Zhuang, C-Y. Wu, J-M. Chen, Y. Chen, C-T. Wan, E. Wang, A. Chiou, P. Kao, Y. Tsai, H. H. Chen, S-A. Hwang
MediaTek, Hsinchu, Taiwan

DS2

8:38 AM

35.2 A 0.021mm² PVT-Aware Digital-Flow-Compatible Adaptive Back-Biasing Regulator with Scalable Drivers Achieving 450% Frequency Boosting and 30% Power Reduction in 22nm FDSOI Technology

Y. Moursy[1], T. Raupp Da Rosa[1], L. Jure[1], A. Quelen[2], S. Genevey[1], L. Pierrefeu[1], E. Grand[1], J. Winkler[3], J. Park[4], G. Pillonnet[2], V. Huard[1], A. Bonzo[1], P. Flatresse[1]
[1]Dolphin Design, Meylan, France
[2]CEA-Léti, Grenoble, France
[3]Globalfoundries, Dresden, Germany
[4]Globalfoundries, Santa Clara, CA

8:46 AM

35.3 Thread-Level Power Management for a Current- and Temperature-Limiting System in a 7nm Hexagon™ Processor

V. K. Kalyanam[1], E. Mahurin[1], K. Bowman[2], S. Venkumahanti[1]
[1]Qualcomm, Austin, TX
[2]Qualcomm, Raleigh, NC

Hardware Security

Session Chair: ***Hirofumi Shinohara,*** *Waseda University, Fukuoka, Japan*
Session Co-Chair: ***Massimo Alioto,*** *National University of Singapore, Singapore, Singapore*
Session Moderator: ***Ingrid Verbauwhede,*** *KU Leuven, Leuven, Belgium*

On Demand Content will be available on Friday, February 5, 2021, 5:00PM PST
Live Session: Recap and Q&A will be scheduled according to the following program.
Both On-demand content and recorded live Q&A content will be available until March 31, 2021.

DS2

9:15 AM

36.1 Unified In-Memory Dynamic TRNG and Multi-Bit Static PUF Entropy Generation for Ubiquitous Hardware Security

S. Taneja, V. Konandur Rajanna, M. Alioto
National University of Singapore, Singapore, Singapore

DS2

9:23 AM

36.2 An EM/Power SCA-Resilient AES-256 with Synthesizable Signature Attenuation Using Digital-Friendly Current Source and RO-Bleed-Based Integrated Local Feedback and Global Switched-Mode Control

A. Ghosh[1], D. Das[1], J. Danial[1], V. De[2], S. Ghosh[2], S. Sen[1]
[1]Purdue University, West Lafayette, IN
[2]Intel, Hillsboro, OR

9:31 AM

36.3 A Modeling Attack Resilient Strong PUF with Feedback-SPN Structure Having <0.73% Bit Error Rate Through In-Cell Hot-Carrier Injection Burn-In

K. Liu, Z. Fu, G. Li, H. Pu, Z. Guan, X. Wang, X. Chen, H. Shinohara
Waseda University, Kitakyushu, Japan

9:39 AM

36.4 A Physically Unclonable Function Combining a Process Mismatch Amplifier in an Oscillator Collapse Topology

J. Park, J-Y. Sim
Pohang University of Science and Technology, Pohang, Korea

9:43 AM

36.5 An Automatic Self-Checking and Healing Physically Unclonable Function (PUF) with $<3\times10^{-8}$ Bit Error Rate

Y. He, D. Li*, Z. Yu, K. Yang*
Rice University, Houston, TX
*Equally-Credited Authors (ECAs)

Live panels and Q&A will be scheduled according to the following program.
Special Events will be recorded and recordings will be available after the live sessions until March 31, 2021.

Live Panel and Q&A
7:00 – 8:00 am

Special Event:
What Technologies Will Shape the Future of Computing?

Organizers: **Hugh Mair**, MediaTek, Austin, TX
Shinichiro Shiratake, Kioxia, Yokohama, Japan
Eric Karl, Intel, Hillsboro, OR
Thomas Burd, AMD, Santa Clara, CA
Jonathan Chang, TSMC, Hsinchu, Taiwan

Moderator: **Hugh Mair**, MediaTek, Austin, TX

General-purpose computing has derived performance gains from clock frequency and instructions-per-clock for over four decades; achieving an impressive ~10^5 performance increase over the same timeframe. With the future of the traditional computing roadmap in doubt, this event will discuss what other technologies could help shape the future of computing.

How much further can we push traditional CPU micro-architectures? Will 3D integration help extend the traditional roadmap for another decade? Will dedicated accelerators become mainstream alternatives for everyday computing tasks? Can memory materials or architectures provide a performance breakthrough for traditional architectures and what if error-free memory is no longer a constraint?

Panelists: **Debbie Marr**, Intel, Hillsboro, OR
Samuel Naffziger, AMD, Fort Collins, CO
Henk Corporaal, Eindhoven University, Netherlands
Ken Takeuchi, University of Tokyo, Japan
Naresh Shanbhag, University of Illinois, Urbana-Champaign, IL

Live Panel and Q&A
7:00 – 8:00 am

Special Event:
Going Remote: Challenges and Opportunities to Remote Learning, Work, and Collaboration

Organizers: **Alicia Klinefelter,** *NVIDIA, Durham, NC*
Huichu Liu, *Facebook, Menlo Park, CA*
Luca Benini, *ETH Zürich, Zürich, Switzerland*
Yvain Thonnart, *CEA-List, Grenoble, France*
Keith Bowman, *Qualcomm, Raleigh, NC*

Moderator: **Alicia Klinefelter,** *NVIDIA, Durham, NC*

For years there has been a call to increase remote work, conferencing, and education. Although many companies have geographically distributed teams and students have moved to online instruction, remote working and learning has yet to become the norm despite the available technology and resources. Remote work and education provide positive environmental benefits as well as improved work-life integration and flexibility. Today, key challenges include effective communication, laboratories, isolation, and privacy. Being at the forefront of innovation, our community often leads technology adoption. In this special event, we explore how to shape the inevitable shift to more distributed and remote styles of working and learning.

Panelists: **Kathy Wilcox**, *AMD, Boxborough, MA*
David Bol, *UCLouvain, Louvain-la-Neuve, Belgium*
Alvin Loke, *NXP Semiconductors, San Diego, CA*
Ofer Shacham, *Facebook, Menlo Park, CA*

On Demand Content will be available on Friday, February 5, 2021, 5:00PM PST
Live Session: Recap and Q&A will be scheduled according to the following program.
Both On-demand content and recorded live Q&A content will be available until March 31, 2021.

This year, the Demonstration Session extending in selected regular papers, both Academic and Industrial, will take place on Friday, February 19th from 7:00 - 8:00 am. These demonstrations will feature real-life applications made possible by new ICs presented at ISSCC 2021, as noted by the symbol **DS1**

2.2 High-Performance and Small Form-Factor mm-Wave CMOS Radars for Automotive and Industrial Sensing in 76-to-81GHz and 57-to-64GHz Bands

2.3 SOLI: A Tiny Device for a New HMI Interface

4.5 BioAIP: A Reconfigurable Biomedical AI Processor with Adaptive Learning for Versatile Intelligent Health Monitoring

4.6 A 144Kb Annealing System Composed of 9×16Kb Annealing Processor Chips with Scalable Chip-to-Chip Connections for Large-Scale Combinatorial Optimization Problems

6.6 Full-Duplex Receiver with Wideband Multi-Domain FIR Cancellation Based on Stacked-Capacitor, N-Path Switched-Capacitor Delay Lines Achieving >54dB SIC Across 80MHz BW and >15dBm TX Power-Handling

7.1 A 4-tap 3.5μm 1.2Mpixel Indirect Time-of-Flight CMOS Image Sensor with Peak Current Mitigation and Multi-User Interference Cancellation

7.3 A 189×600Back-Illuminated Stacked SPAD Direct Time-of-Flight Depth Sensor for AutomotiveLiDAR Systems

7.7 A 0.2-to-3.6TOPS/W Programmable Convolutional Imager SoC with In-Sensor Current-Domain Ternary-Weighted MAC Operations for Feature Extraction and Region-of-Interest Detection

7.8 A 1-inch 17Mpixel 1000fps Block-Controlled Coded-Exposure Back-Illuminated Stacked CMOS Image Sensor for Computational Imaging and Adaptive Dynamic Range Control

8.1 A 224Gb/s DAC-Based PAM-4 Transmitter with 8-Tap FFE in 10nm CMOS

8.3 An 8b DAC-Based SST TX Using Metal Gate Resistors with 1.4pJ/b Efficiency at 112Gb/s PAM-4 and 8-Tap FFE in 7nm CMOS

8.5 A Scalable Adaptive ADC/DSP-Based 1.25-to-56Gbps/112Gbps High-Speed Transceiver Architecture Using Decision-Directed MMSE CDR in 16nm and 7nm

9.7 A 184μW Real-Time Hand-Gesture Recognition System with Hybrid Tiny Classifiers for Smart Wearable Devices

9.9 A Background-Noise and Process-Variation-Tolerant 109nW Acoustic Feature Extractor Based on Spike-Domain Divisive-Energy Normalization for an Always-On Keyword Spotting Device

10.1 A 116μW 104.4dB-DR 100.6dB-SNDR CT $\Delta\Sigma$ Audio ADC Using Tri-Level Current-Steering DAC with Gate-Leakage Compensated Off-Transistor-Based Bias Noise Filter

10.6 A 12b 16GS/s RF-Sampling Capacitive DAC for Multi-Band Soft-Radio Base-Station Applications with On-Chip Transmission-Line Matching Network in 16nm FinFET

17.1 A Two-Stage Cascaded Hybrid Switched-Capacitor DC-DC Converter with 96.9% Peak Efficiency Tolerating 0.6V/μs Input Slew Rate During Startup

17.2 A Masterless Fault-Tolerant Hybrid Dickson Converter with 95.3% Peak Efficiency 20V-to-60V Input and 3.3V Output for 48V Multi-Phase Automotive Applications

17.3 A 1.25GHz Fully Integrated DC-DC Converter Using Electromagnetically Coupled Class-D LC Oscillators

18.2 CMOS-Driven Pneumatic-Free Scalable Microfluidics and Fluid Processing with Label-Free Cellular and Bio-Molecular Sensing Capability for an End-to-End Point-of-Care System

18.3 An Integrated Thermal Actuation/Sensing Array with Stacked Oscillators for Efficient and Localized Heating of Magnetic Nanoparticles with Sub-Millimeter Spatial Resolution

19.1 Optical Phased-Array FMCW LiDAR with On-Chip Calibration

23.1 270-to-300GHz Double-Balanced Parametric Upconverter Using Asymmetric MOS Varactors and a Power-Splitting-Transformer Hybrid in 65nm CMOS

23.3 A 605GHz 0.84mW Harmonic Injection-Locked Receiver Achieving 2.3pW/√Hz NEP in 28nm CMOS

25.4 A 20nm 6GB Function-In-Memory DRAM, Based on HBM2 with a 1.2TFLOPS Programmable Computing Unit Using Bank-Level Parallelism, for Machine Learning Applications

26.1 A 26-to-60GHz Continuous Coupler-Doherty Linear Power Amplifier for Over-An-Octave Back-Off Efficiency Enhancement

On Demand Content will be available on Friday, February 5, 2021, 5:00PM PST
Live Session: Recap and Q&A will be scheduled according to the following program.
Both On-demand content and recorded live Q&A content will be available until March 31, 2021.

This year, the Demonstration Session extending in selected regular papers, both Academic and Industrial, will take place on Friday, February 19th from 8:15 - 9:15 am. These demonstrations will feature real-life applications made possible by new ICs presented at ISSCC 2021, as noted by the symbol **DS2**

5.1 A 1.5µW 0.135pJ•%RH^2 CMOS Humidity Sensor Using Adaptive Range-Shift Zoom CDC and Power-Aware Floating Inverter Amplifier Array

9.3 A 40nm 4.81TFLOPS/W 8b Floating-Point Training Processor for Non-Sparse Neural Networks Using Shared Exponent Bias and 24-Way Fused Multiply-Add Tree

9.6 A 1/2.3inch 12.3Mpixel with On-Chip 4.97TOPS/W CNN Processor Back-Illuminated Stacked CMOS Image Sensor

11.3 A 480Gb/s/mm 1.7pJ/b Short-Reach Wireline Transceiver Using Single-Ended NRZ for Die-to-Die Applications

11.4 A High-Accuracy Multi-Phase Injection-Locked 8-Phase 7GHz Clock Generator in 65nm with 7b Phase Interpolators for High-Speed Data Links

12.2 Improving the Range of WiFi Backscatter Via a Passive Retro-Reflective Single-Side-Band-Modulating MIMO Array and Non-Absorbing Termination

13.3 A 6-to-8GHz 0.17mW/Qubit Cryo-CMOS Receiver for Multiple Spin Qubit Readout in 40nm CMOS Technology

21.2 A 3-to-10GHz 180pJ/b IEEE802.15.4z/4a IR-UWB Coherent Polar Transmitter in 28nm CMOS with Asynchronous Amplitude Pulse-Shaping and Injection-Locked Phase Modulation

21.4 A 0.75-to-1GHz Passive Wideband Noise-Cancelling 171µW Wake-Up RX and 440µW Primary RX FE with -86dBm/10kb/s Sensitivity, 35dB SIR and 3.8dB RX NF

21.5 An Integrated 2.4GHz -91.5dBm-Sensitivity Within-Packet Duty-Cycled Wake-Up Receiver Achieving 2µW at 100ms Latency

22.1 THz Prism: One-Shot Simultaneous Multi-Node Angular Localization Using Spectrum-to-Space Mapping with 360-to-400GHz Broadband Transceiver and Dual-Port Integrated Leaky-Wave Antennas

22.3 A 0.42THz Coherent TX-RX System Achieving 10dBm EIRP and 27dB NF in 40nm CMOS for Phase-Contrast Imaging

28.3 A 28µW 134dB DR 2nd-Order Noise-Shaping Slope Light-to-Digital Converter for Chest PPG Monitoring

28.5 A 0.6V/0.9V 26.6-to-119.3µW $\Delta\Sigma$-Based Bio-Impedance Readout IC with 101.9dB SNR and <0.1Hz 1/f Corner

28.6 A 22.6µW Biopotential Amplifier with Adaptive Common-Mode Interference Cancelation Achieving Total-CMRR of 104dB and CMI Tolerance of 15V_{pp} in 0.18µm CMOS

29.4 A Fractional-N Digital MDLL with Background Two-Point DTC Calibration Achieving -60dBc Fractional Spur

29.5 A 0.008mm^2 1.5mW 0.625-to-200MHz Fractional Output Divider with 120fs_{rms} Jitter Based on Replica-DTC-Free Background Calibration

29.8 115nA@3V ULPMark-CP Score 1205 SCVR-Less Dynamic Voltage-Stacking Scheme for IoT MCU

33.2 A 600V GaN Active Gate Driver with Dynamic Feedback Delay Compensation Technique Achieving 22.5% Turn-On Energy Saving

33.5 A 1.25W 46.5%-Peak-Efficiency Transformer-in-Package Isolated DC-DC Converter Using Glass-Based Fan-Out Wafer-Level Packaging Achieving 50mW/mm^2 Power Density

33.8 A Decentralized Daisy-Chain-Controlled Switched-Capacitor Driver for Microrobotic Actuators with 10× Power-Reduction Factor and Over 300V Drive Voltage

34.1 An 8960-Element Ultrasound-on-Chip for Point-of-Care Ultrasound

35.2 A 0.021mm^2 PVT-Aware Digital-Flow-Compatible Adaptive Back-Biasing Regulator with Scalable Drivers Achieving 450% Frequency Boosting and 30% Power Reduction in 22nm FDSOI Technology

36.1 Unified In-Memory Dynamic TRNG and Multi-Bit Static PUF Entropy Generation for Ubiquitous Hardware Security

36.2 An EM/Power SCA-Resilient AES-256 with Synthesizable Signature Attenuation Using Digital-Friendly Current Source and RO-Bleed-Based Integrated Local Feedback and Global Switched-Mode Control

Live panels and Q&A will be scheduled according to the following program.
Special Events will be recorded and recordings will be available after the live sessions until March 31, 2021.

Live Panel and Q&A - 8:15 – 9:15 am

Special Event:
Favorite Circuit Design and Testing Mistakes of Starting Engineers

Organizers:
Ramesh Harjani, *University of Minnesota, Minneapolis, MN*
Mike Chen, *University of Southern California, Los Angeles, LA*
Marco Berkhout, *Goodix Technology, Nijmegen, The Netherlands*
Johan Vanderhaegan, *Google, Mountain View, CA*

Moderator:
Ramesh Harjani, *University of Minnesota, Minneapolis, MN*

This special event will focus on typical mistakes that all starting graduate students seem to make when they first start designing circuits. Many of these errors are simple and easily avoided if only they are pre-warned. These errors show up at different phases of design, simulation, layout and testing. Renowned speakers will share their experience and provide examples of their own mistakes!

Panelists:
Thomas H. Lee, *Stanford University, Palo Alto, CA*
Robert Bogdan Staszewski, *University College Dublin, Dublin, Ireland*
Kathleen Philips, *IMEC, Eindhoven, The Netherlands*
Howard C. Luong, *HKUST, Kowloon, Hong Kong, China*
Vadim Ivanov, *Texas Instruments, Tucson, AZ*

Live Presentations and Q&A - 8:15 – 9:25 am

Special Event:
ICs in PandemICs

Organizers:
Negar Reiskarimian, *MIT, Cambridge, MA*
Zeynep Toprak-Deniz, *IBM, Yorktown Heights, NY*

Co-Organizers:
Kathy Wilcox, *AMD, Boxborough, MA*
Alice Wang, *Everactive, Santa Clara, CA*
Jane Gu, *University of California, Davis, CA*
Ulkuhan Guler, *Worcester Polytechnic Institute, Worcester, MA*
Yaoyao Jia, *NC State University, Raleigh, NC*
Alicia Klinefelter, *Nvidia, Durham, NC*
Rikky Muller, *University of California, Berkeley, Berkeley, CA*
Farhana Sheikh, *Intel, Hillsboro, OR*
Yildiz Sinangil, *Apple, Bay Area, SF*
Trudy Stetzler, *Halliburton, Houston, TX*
Vivienne Sze, *MIT, Cambridge, MA*
Rabia Yazicigil, *Boston University, Boston, MA*
Deeksha Lal, *Anokiwave, Billerica, MA*
Dina Reda El-Damak, *University of Science and Technology, Zewail City, Egypt*

Moderator:
Ulkuhan Guler, *Worcester Polytechnic Institute, Worcester, MA*

Live panels and Q&A will be scheduled according to the following program.
Special Events will be recorded and recordings will be available after the live sessions until March 31, 2021.

Live Presentations and Q&A
8:15 – 9:25 am
Special Event:
ICs in PandemICs

The COVID-19 pandemic has imposed a powerful test across the globe. As the current pandemic unfolds, revolutionary social and economic changes have accelerated that would otherwise have taken decades to materialize, especially the digital transformation enabling virtual presence. The IC industry continues to forge ahead, providing the building blocks for innovations that improve the economic and social prosperity of the world. From smarter robots to automation, from connected medical devices to AI-driven data analytics, cost-effective, secure, portable and high-accuracy IC technology is already in place. This evening event brings together experts from industry and academia in cloud-connected biosensors, advance algorithms and artificial intelligence (AI) to discuss our preparedness to combat the spread of infectious diseases now and in the future. The talks will feature recent work on accelerated drug discovery, enhanced contact tracing, continuous remote patient monitoring and data analysis with related security and privacy concerns.

Distinguished Speakers

8:15 - 8:35 AM

Accelerating Innovation with Confidence: A Look at Cloud Security (All the Way Down to the Transistors!)
Hillery Hunter
CTO of IBM Cloud, IBM

8:35 - 8:55 AM

Building a Time Machine for Drug Discovery and Healthcare Research
Prerna Dogra
Senior Product Manager – AI for Healthcare, Nvidia

Invited Talks

8:55 - 9:10 AM

AI-Enhanced Neural Prostheses
Mahsa Shoaran
Assistant Professor of Electrical Engineering, Center for Neuroprosthetics, EPFL

9:10 - 9:25 AM

Pandemics - An opportunity for biomedical IC?
Milin Zhang
Assistant Professor, Department of Electronic Engineering, Tsinghua University

Live panels and Q&A will be scheduled according to the following program.
Special Events will be recorded and recordings will be available after the live sessions until March 31, 2021.

Live Panel and Q&A - 7:00 am
Special Event:
Making a Career Choice

This interactive event will include several distinguished panelists representing a broad variety of career choices in the areas of start-ups, industry, research, and academia available to graduates in electrical and computer engineering. Following short introductory remarks by each panelist, this forum will open for audience interaction in which the audience is invited to express a broad range of questions to the panelists.

Moderators:
Denis Daly, *Apple, Cambridge, MA*
Zeynep Lulec, *Analog Devices, Canada*
Rabia Tugce Yazicigil, *Boston University, Boston, MA*

Panelists:
Alison Burdett, *Sensium Healthcare, UK*
Rituparna Mandal, *MediaTek, India*
Matheus Moreira, *Chronos Tech, CA*
Dante Muratore, *Stanford, CA*
Aisha Walcott-Bryant, *IBM, Kenya*
Seng-Pang (Ben) U, *Synopsys Macau & University of Macau*

Live panels and Q&A will be scheduled according to the following program.
Special Events will be recorded and recordings will be available after the live sessions until March 31, 2021.

Live Presentations and Q&A - 8:15 am
Special Event:
Student Research Preview (SRP)

Student Research Preview (SRP) will highlight selected student research projects in progress. The SRP consists of approximately 14 ninety-second presentations followed by a Poster Session, by graduate students from around the world, which have been selected on the basis of a short submission concerning their on-going research.

Selection is based on the technical quality and innovation of the work. This year, the SRP will be presented in two theme sections: Analog/RF Circuits & Systems; Digital & Machine Learning.

The Student Research Preview will include an inspirational lecture by Dr. Jennifer Lloyd. The SRP is open to all ISSCC registrants.

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Advisor:	Kevin Zhang, TSMC
Advisor:	Jan Van der Spiegel, University of Pennsylvania
Media/Publications:	Laura Fujino, University of Toronto
A/V:	Trudy Stetzler, Halliburton, Houston, TX

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Samira Zaliasl	Ferric, NY
Milin Zhang	Tsinghua University, China
Yan Zhu	University of Macau, China

F1: Striking the Balance Between Energy Efficiency & Flexibility: General-Purpose vs Special-Purpose ML Processors

Organizers: **Luca Benini,** *ETHZ, Zurich, Switzerland*
SukHwan Lim, *Samsung, Hwaseong, Gyeonggi, Korea*
Yong Pan Liu, *Tsinghua University, Beijing, China*
Tanay Karnik, *Intel, Hillsboro, OR*
Hsie-chia Chang, *National Chiao Tung University, HsinChu, Taiwan*

ML is being deployed in an increasing range of applications and platforms. In the early days of the "Cambrian explosion" of ML processors, simple metrics have been adopted for comparison and benchmarking, such as TOPS/W and TOPS/mm^2 for performance on specific networks. In reality, a number of factors impact actual application performance, ranging from hardware utilization (e.g. the stated peak TOPS are often not achieved due to idle MAC units), to number-format/precision requirements, model transformation, pre/post-processing computations, etc. With a focus on full-stack system performance, this forum discusses hardware and software challenges in designing and deploying ML acceleration platforms from the edge to the cloud.

On Demand Content will be available on Friday, February 12, 2021, 5:00PM PST
Live Session: Recap and Q&A will be scheduled according to the following program.
Both On-demand content and recorded live Q&A content will be available until March 31, 2021.

Agenda

Time	Topic
7:00 AM	**Introduction** **Luca Benini,** *ETHZ, Zurich, Switzerland*
7:15 AM	**Emulating Large Machine Learning Accelerators with Small Research Chips** **Brian Zimmer,** *Nvidia, Mountain View, CA*
7:30 AM	**Extending RISC-V Platforms for ML at the Extreme Edge of the IoT** **Davide Rossi,** *University of Bologna, Bologna, Italy*
7:45 AM	**Unified Ascend: From Tasks to Processor Design** **Hu Yuxing and Xia Jing,** *HiSilicon-Technologies, Shen Zhen, China*
8:00 AM	**Co-Designing Hardware and Models for Efficient Neural Network Inference** **Paul N. Whatmough,** *Arm ML Research, Waltham, MA*
8:15 AM	**Balancing Hardware Flexibility and Efficiency for Deep Learning** **Michaela Blott,** *Xilinx Research, Dublin, Ireland*
8:30 AM	**Hybrid Digital and Analog Computing for Efficiency and Generality Optimization** **Wang Shaodi,** *WITIN Tech, Beijing, China*
8:45 AM	**Bridging the Gap: Software Cost of Hardware Specialization** **Jacques Pienaar,** *Google, Mountain View, CA*
9:00 AM	**Efficient Machine Learning: Algorithms-Circuits-Devices Co-design** **Hai Helen Li,** *Duke University, Durham, NC*

F2: Pushing the Frontiers in Accuracy for Data Converters and Analog Circuits

Organizer: **Youngcheol Chae,** *Yonsei University, Seoul, Korea*

Co-Organizer: **Yun-Shiang Shu,** *MediaTek, Hsinchu, Taiwan*

Committee: **Jens Anders,** *University of Stuttgart, Stuttgart, Germany*
Viola Schaffer, *Texas Instruments, Tucson, AZ*
Takashi Oshima, *Hitachi, Tokyo, Japan*
Marco Corsi, *Texas Instruments, Dallas, TX*

New applications continue to arise in which the limits of conventional approaches are no longer sufficient and so must be expanded. Over the last decade, the accuracy of analog circuits and data converters has been improved by several orders of magnitude. However, there is still room for improvement with new and creative circuit techniques. This forum covers the advances in analog circuits and data converters with a focus on the ultimately achievable accuracy.

On Demand Content will be available on Friday, February 12, 2021, 5:00PM PST
Live Session: Recap and Q&A will be scheduled according to the following program.
Both On-demand content and recorded live Q&A content will be available until March 31, 2021.

Agenda

Time	Topic
7:00 AM	**Introduction** **Youngcheol Chae,** *Yonsei University, Seoul, Korea*
7:15 AM	**Fundamental Challenges in Analog Circuit Design** **Bernhard Boser,** *University of California, Berkeley, Berkeley, CA*
7:30 AM	**Designing High-Accuracy Bandgap Voltage References** **Vadim Ivanov,** *Texas Instruments, Tucson, AZ*
7:45 AM	**Precision MEMS-Based Frequency References** **Kamran Souri,** *SiTime, Delft, The Netherlands*
8:00 AM	**Circuit techniques for mechanical stress compensation** **Mario Motz,** *Infineon Technologies AG, Villach, Austria*
8:15 AM	**Precision Amplifiers: the Past and the Future** **Qinwen Fan,** *TU Delft, Delft, The Netherlands*
8:30 AM	**Digital to Analog Converters with High Linearity and Dynamic Range** **Ayman Shabra,** *MediaTek, Woburn, MA*
8:45 AM	**Architectural and Design Challenges in High-Resolution Continuous-Time Delta-Sigma Data Converters** **Shanthi Pavan,** *IIT Madras, Chennai, India*
9:00 AM	**Highly-Linear Nyquist-Rate Data Converters** **Jesper Steensgaard,** *Analog Devices, Camas, WA*

F3: Silicon Technologies in the Fight Against Pandemics – from Point of Care to Computational Epidemiology

Organizer: **Nick Van Helleputte,** *imec, Leuven, Belgium*

Co-Organizers: **Arijit Raychowdhury,** *Georgia Institute of Technology, Atlanta, GA*
Ping-Hsuan Hsieh, *National Tsing Hua University, Hsinchu, Taiwan*
Jun Deguchi, *Kioxia, Kawasaki, Japan*
Matteo Perenzoni, *Fondazione Bruno Kessler, Trento, Italy*
Esther Rodriguez-Villegas, *Imperial College London, London, United Kingdom*

Committee: **Long Yan,** *Samsung Electronics, Hwaseong, Korea*
Andreia Cathelin, *STMicroelectronics, Crolles, France*
Keith Bowman, *Qualcomm, Raleigh, NC*
Chris Van Hoof, *imec, Leuven, Belgium*

COVID-19 resulted in massive human casualties and an economic collapse across the globe. To prepare for the future, this Forum introduces the key challenges with detection and prevention of pandemics and highlights some potential opportunities for employing silicon technologies to quickly diagnose, treat, and prevent diseases. IC technologies that enable point-of-care diagnostics, continuous health monitoring, and lab-on-chip RNA detection continue to revolutionize healthcare. Further, high-performance computing (HPC) accelerates drug discovery, vaccine development, as well as real-time tracking of the spread of diseases and their socio-economic impacts. This Forum will address a wide spectrum of topics at the intersection of circuit/system design and bio-engineering.

On Demand Content will be available on Friday, February 12, 2021, 5:00PM PST
Live Session: Recap and Q&A will be scheduled according to the following program.
Both On-demand content and recorded live Q&A content will be available until March 31, 2021.

Agenda

Time	Topic
7:00 AM	**Introduction** **Nick Van Helleputte,** *imec, Leuven, Belgium*
7:15 AM	**Silicon for Pandemics: The Role of Point-of-Care Diagnostics in COVID-19 and the Future** **Jennifer Lloyd,** *Analog Devices, Santa Clara, CA*
7:30 AM	**Single-Molecular Bioelectronics** **Kenneth Shepard,** *Columbia University, New York, NY*
7:45 AM	**Analyze the Patient, Engineer the Therapy** **Liesbet Lagae,** *imec, Leuven, Belgium*
8:00 AM	**CMOS Ion-Sensing Arrays Enabling Rapid Diagnostics and Surveillance for Infectious Diseases: Addressing COVID-19** **Pantelis Georgiou,** *Imperial College London, United Kingdom*
8:15 AM	**Analog Front-End Design Techniques for Robust Health Monitoring and Biosensing** **Minkyu Je,** *KAIST, Daejeon, Korea*
8:30 AM	**Cardiovascular Disease Detection, Analysis, and Evaluation System-On-Chip and Platform** **Shuenn-Yuh Lee,** *National Cheng Kung University, Tainan, Taiwan*
8:45 AM	**AI/ML-Aided Diagnosis of Biomarkers** **Bruno Michel,** *IBM Research, Zurich, Switzerland*
9:00 AM	**Towards Scalable Real-Time Computational Epidemiology to Support COVID-19 Response** **Madhav Marathe,** *University of Virginia, Charlottesville, Viginia, VA*

F4: Electronics for a Quantum World

Organizers: **Edoardo Charbon,** *EPFL, Neuchâtel, Switzerland*
Alicia Klinefelter, *NVIDIA, Durham, NC*

Committee: **Massimo Alioto,** *National University of Singapore, Singapore*
Yao-Hong Liu, *IMEC, Eindhoven, Netherlands*
Munehiko Nagatani, *NTT, Atsugi, Japan*
Arijit Raychowdhury, *Georgia Institute of Technology, Atlanta, GA*
Andreia Cathelin, *STMicroelectronics, Crolles, France*
Boris Murmann, *Stanford University, Stanford, CA*

We have seen an emergence of quantum-computing activity in recent years from an uptick of startups to investments at established companies. Yet, there is more to quantum systems than simply computing. In fact, quantum systems by themselves do not work, and classical electronics are needed to interface with quantum devices.

In this forum, we look at electronics, in particular CMOS electronics, for use in combination with quantum devices from the designer's perspective. We explore these systems from specifications to testing, often at cryogenic temperatures, and discuss recent successes and future trends.

On Demand Content will be available on Friday, February 12, 2021, 5:00PM PST
Live Session: Recap and Q&A will be scheduled according to the following program.
Both On-demand content and recorded live Q&A content will be available until March 31, 2021.

Agenda

Time	Topic
7:00 AM	**Introduction** **Edoardo Charbon,** *EPFL, Neuchâtel, Switzerland*
7:15 AM	**Introduction to Quantum Computing** **Lan Wei,** *University of Waterloo, Waterloo, Canada*
7:30 AM	**Quantum Gates and Circuits on a Quantum Computer** **Matthias Steffen,** *IBM, Yorktown Heights, NY*
7:45 AM	**Distributed Cryogenic CMOS Platform for Autonomous Quantum Control** **David Reilly,** *Microsoft and the University of Sydney, Camperdown, Australia*
8:00 AM	**Si-Spin-Qubit Quantum-Matrix Architecture Requirements, Consequence on Cryocontrol** **Maud Vinet,** *CEA-LETI, University Grenoble Alpes, Grenoble, France*
8:15 AM	**Cryogenic CMOS Integrated Circuits for Control of Superconducting Quantum Computers: Status and Challenges** **Joseph Bardin,** *University of Massachusetts, Amherst, MA*
8:30 AM	**A Cryogenic CMOS Multiqubit Controller** **Bishnu Patra,** *Delft University of Technology, Delft, Netherlands*
8:45 AM	**The Superconducting Nanowire as a New Electronic Device** **Karl K. Berggren,** *MIT, Cambridge, MA*
9:00 AM	**Room-Temperature Quantum Sensing on CMOS for Magnetometry and Time-Keeping** **Ruonan Han,** *MIT, Cambridge, MA*
9:15 AM	**CMOS-Based Quantum Random-Number Generators** **Gianluca Boso,** *ID Quantique SA, Carouge, Switzerland*

F5: Enabling New System Architectures with 2.5D, 3D, and Chiplets

Organizers: **Christopher Gonzalez**, *IBM, Yorktown Heights, NY*
Huichu Liu, *Facebook, Menlo Park, CA*

Committee: **Mijung Noh,** *Samsung Electronics, Hwaeong-si, Gyeonggi-do, Korea*
Eric Karl, *Intel, Portland, OR*
Thomas Toifl, *Cisco Systems, Wallisellen, Switzerland*
Shawn Hsu, *National Tsing Hua University, Hsinchu, Taiwan*

The end of transistor scaling drives innovative 2.5D, 3D and chiplet technologies to further extend Moore's law. Recent advancements in multi-die integration effectively reduce the costs at advanced nodes while providing more flexibility, modularity and heterogeneous integration, which require designers to rethink the system architectures to exploit these advantages. This forum focuses on the most recent advancements of the 2.5D, 3D and chiplet technologies as well as the key components for integration to enable new system architectures. This forum aims to bring together technologists, designers and architects from industry and academia to discuss the practical challenges and solutions in 2.5D/3D technologies, and to provide insights on how to leverage the technology benefits with different system requirements.

On Demand Content will be available on Friday, February 12, 2021, 5:00PM PST
Live Session: Recap and Q&A will be scheduled according to the following program.
Both On-demand content and recorded live Q&A content will be available until March 31, 2021.

Agenda

Time	Topic
7:00 AM	**Introduction** **Huichu Liu**, *Facebook, Menlo Park, CA*
7:15 AM	**Foundry Solutions for 2.5D/3D integration** **Douglas Yu**, *TSMC, HsinChu, Taiwan*
7:30 AM	**New Directions in 2.5D/3D Heterogeneous Integration of FPGAs** **Farhana Sheikh,** *Intel, Portland, OR*
7:45 AM	**3D-Stacked Memory Architecture with 2.5D Heterogenous Integration** **Kyomin Sohn,** *Samsung, Hwasung-City, Korea*
8:00 AM	**2.5D and 3D Polylithic Integrated Circuit Technologies** **Muhannad S. Bakir,** *Georgia Tech, Atlanta, GA*
8:15 AM	**MCM/Chiplet Solutions** **Samuel Naffziger,** *AMD, Fort Collins, CO*
8:30 AM	**High-Speed Interconnect Challenges within Systems Leveraging Advanced Packaging Techniques** **Walker Turner,** *NVIDIA, Raleigh-Durham, NC*
8:45 AM	**Evolving Image Sensor Architecture through Stacking Devices** **Yusuke Oike,** *Sony, Kanagawa, Japan*
9:00 AM	**3D System Integration: Technology Landscape and Long-Term Roadmap** **Eric Beyne,** IMEC, *IMEC, Leuven, Belgium*

F6: Optical and Electrical Transceivers for 400GbE and Beyond

Organizer: **Tony Chan Carusone,** *University of Toronto, Toronto, Canada*

Co-Organizer: **Sudip Shekhar,** *University of British Columbia, Vancouver, Canada*

Committee: **Yohan Frans,** *Xilinx, San Jose, CA*
Wei-Zen Chen, *National Chiao Tung University, Hsin-Chu, Taiwan*
Thomas Toifl, *Cisco Systems, Wallisellen, Switzerland*
Munehiko Nagatani, *NTT Corporation, Kanagawa, Japan*
Franz Dielacher, *Infineon Technologies, Vilach, Austria*
William Redman-White, *HiLight Semiconductor, Southampton, United Kingdom*

The proliferation of 400Gb/s Ethernet (400GbE) in our computing and networking infrastructure is stimulating rapid transformations in our wireline links. A wide array of new technologies are under research to support next-generation 800GbE in the areas of optics, packaging, modulation, coding, and transceiver architectures and circuits. Over the past two decades, progress on wireline interface bandwidth scaling has followed a relatively clear path. But, for many, the coming years seem less certain. In this forum, eight experts illuminate the future, sharing their diverse expertise across the broad range of topics that promise to have impact on optical and electrical transceiver R&D in the 2020's.

On Demand Content will be available on Friday, February 12, 2021, 5:00PM PST
Live Session: Recap and Q&A will be scheduled according to the following program.
Both On-demand content and recorded live Q&A content will be available until March 31, 2021.

Agenda

Time	Topic
7:00 AM	**Introduction** **Tony Chan Carusone,** *University of Toronto, Toronto, Canada*
7:15 AM	**Optical Transceivers for 400GbE and Beyond** **Mark Nowell,** Cisco, Ottawa, Canada
7:30 AM	**100_Gb/s PAM4 Silicon-Photonic Optical Transceivers** **Ganesh Balamurugan,** *Intel Labs, Hillsboro, Oregon*
7:45 AM	**Silicon Photonics for Spatial Division Multiplexing and Advanced Optical Transceivers** **Hon Ki Tsang,** *The Chinese University of Hong Kong, Hong Kong*
8:00 AM	**VCSEL-Based Optical Transmitters Above 100Gb/s** **Urs Hecht,** *Technishce Universitat, Berlin, Germany*
8:15AM	**DSP and FEC Architectures for Beyond 400Gb/s Data Center Interconnects** **Ilya Lyubomirsky,** *InPhi, Sunnyvale, CA*
8:30 AM	**Signalling, Modulation, Coding and Signal-Processing Architectures to Support 400GbE and Beyond** **Troy Beukema,** *IBM Research, New York, NY*
8:45 AM	**112Gb/s-and-Beyond Long-Reach and Short-Reach Electrical Interfaces** **Nhat Nguyen,** *Rambus, San Jose, CA*
9:00 AM	**Design of Communication Circuits for Side-by-Side and Stacked Chiplets** **Kenny Cheng-Hsiang Hsieh,** *TSMC, Hsinchu, Taiwan*

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Online: This is the only way to register and will give you immediate email confirmation of your events. Go to the ISSCC website at www.isscc.org and select the link to the Registration website. The 2021 ISSCC will be a Virtual meeting so there will be no on-site registration.

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You can register at this time. There is an added incentive to register early, prior to January 10. Early registrations will receive the ability to view the 2020 ISSCC Tutorials. Registration will run until March 1, 2021. Those registering at the IEEE Member rate must provide their IEEE Membership number.

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Technical Book Display

Is still TBD.

Several technical publishers will have collections of professional books and textbooks for sale during the Conference.

Demonstration Sessions

Hardware demonstrations will support selected papers on Friday morning, February 19.

Publications:

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