ISSCC 50th Anniversary Supplement 1954-2003

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50TH ANNIVERSARY

Welcome

On behalf of the ISSCC 50th-Anniversary Committee, I would like to welcome you to the ISSCC 50th-Anniversary Supplement. The purpose of this Supplement is to document the history of ISSCC from its early beginnings to the present day. To accomplish this, articles have been solicited to document the history of the formation of the Conference, including its expansion to international status with the addition of European and Far-East Program Committees. The history of the first decade, as documented in an article created on the occasion of the 40th Anniversary by Arthur Stern, is reprinted here. It is accompanied by a new article, by David Pricer, on the history of the intervening 40 years.

Historical overviews of traditional technical topics: Analog, Communications, Signal Processing, Digital, Memory, Imagers, and Sensors & MEMS - are also included to highlight key ISSCC papers. The full papers corresponding to the references in these articles, can be reviewed on the SSCS DVD, and on the new ISSCC DVD available soon.

To recognize individual contributions during the 50 years of the Conference, an Author Honor Roll has been created, identifying those authors with 10 or more publications presented over this historic 50-year period. A number of these authors will be recognized at the Conference for their accomplishment. In particular, James Meindel has authored/coauthored 47 papers presented at ISSCC. Note that the supporting data was compiled manually by searching the index on the SSCS DVD, the 2001 and 2002 ISSCC CDROMs, and the ISSCC 2003 Advance-Program author list. Accordingly, we apologize in advance to anyone who has been omitted accidentally from the list. Please contact me if you feel that you should be recognized.

Reproductions of some early photos of ISSCC events have also been included, along with supporting background articles: one by Christer Svenssen on the history of feature-size prediction over the past 40 years; another by K.C. Smith, on a brief history of the Press at ISSCC.

In addition to this Supplement, a museum space at ISSCC 2003 documents the contents of this Supplement and highlights many chips from papers referenced herein. Furthermore, a video presenting excerpts of living-history interviews with five of the early pioneers in the creation of ISSCC, is available for viewing in the museum theatre, as well as on the hotel's TV system. Those interviewed are: Arthur Stern, then at GE; Richard Baker, at MIT Lincoln Labs; Murlin Corrington, at RCA; John Linvill, at Bell Labs; and Jerry Suran, also at GE. I would like to express our appreciation for their contributions, both now and then.

I would also like to offer my personal thanks to the 50th-Anniversary Committee members: K.C. Smith, W. David Pricer, Laura Fujino, Timothy Tredwell, and Anantha Chandrakasan, all of whom were instrumental in the solicitation and editing of the articles in this supplement, and the production of the video. I also wish to recognize Nancy Pricer for her help with the video interviews; Ali Sheikholeslami, Joyce Wong (his graduate student), and Ellen Bonney for their work on the museum materials; Bruce Bateman, the authors and reviewers of the articles in this Supplement.

I hope that you find the history of ISSCC, as presented in this Supplement and the museum, both informative and entertaining.

Sincerely,

John Trnka

John Trnka
ISSCC-50th-Anniversary-Committee Chair

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The International Solid-State Circuits Community and Its Annual Conference – Genesis and First Decade

Reprinted from the ISSCC 40th-Anniversary Supplement

Arthur P. Stern: President, IEEE, 1975; Chairman, Professional Group on Circuit Theory, 1968-69; ISSCC Chair, 1960; ISSCC Secretary, 1956; ISSSCC Program Chair, 1959; ISSCC International Committee Chair, 1961; ISSCC Committee Member, 1956-58; ISSCC Sponsors Advisory Committee Member, 1959-68.

A major conference requires a great deal of work, money, and dedication; to endure for forty years in the midst of sustained technological change is no minor feat. Technical history, like all history, isn't charitable and practices no kindness. It discards mercilessly into the trash bin of oblivion most activities, which are not responsive to changing needs ... Only the strong and adaptable survive.

ISSCC's durability and the allegiance of its constituency, the international solid-state circuits community, indicate that ISSCC is a vital tool in the community's self-realization and self-preservation.

Contemplating the longevity of ISSCC, several questions arise: How did ISSCC come about? How did it become an institution? What attributes made ISSCC survive? How did it serve its supporting community and how does it fit with the community's other needs? What were the objectives of its founders?

This retrospective sketches the environment and the events which led to the creation of ISSCC, as well as the changes in its first formative decade. Thus, two purposes will be served: First, some answers to the above questions will be obtained. Second, it is timely to outline the genesis and early evolution of ISSCC before the fading of memories and the disappearance of individuals shroud those events in the impenetrable haze and dark recesses of the distant past.

Early Transistor Days

The invention of the transistor, announced in late 1947, was described by Bardeen and Brattain in 1948 [1]. The news stunned the electronics world and clarification heightened expectations [2]. Nevertheless, no circuit application papers were published for a long time.

This is not really surprising:

* Initially, even inside the Bell Telephone Laboratories (BTL), the hub of transistor work in those days, few useful devices were available.
* Though BTL was cooperative in sharing basic information, other organizations faced delays and "teething problems".
* Shockley's sensational news on the junction transistor resulted in further delay by causing those involved with point-contact transistors to redirect their efforts [3].
* Absent a steady flow of information, the situation was uncertain. Many independent device efforts were pursued but hesitation and indecision prevailed among circuit engineers.

The first circuit-oriented papers appeared in 1950. They were few in number and limited in scope [4,5,6]. Finally, July 1951, three years after Bardeen and Brattain, saw a broad paper dealing with circuits by Wallace and Pietenpol [7]. It instantly became a classic.

The situation improved in 1952:

* First, it became known that the Proceedings of the IRE (the Institute of Radio Engineers, one of the two predecessor institutes of IEEE, the Institute of Electrical and Electronics Engineers), in those days the most respected journal in electronics, was planning a Special Issue on transistors and their applications for November, 1952.
* Second, by mid-1952, quite a few organizations had succeeded in making more or less useful transistors of both the point-contact and the junction types.

Events then unfolded rapidly.

IRE "Technical Subcommittee 4.1: Transistor Circuitry"

Even prior to significant publications about transistor circuits, engineers engaged in this work became aware of each other and established informal links. A "transistor circuits community" was created spontaneously: people devoted to their evolving specialty were only a phone call away from each other and wanted to share experiences.

In the 1950s IRE was the natural "home" for an emerging technical community in electronics. (The American Institute of Electrical Engineers (AIEE), which merged with IRE in 1964 to form IEEE, was rooted primarily in power engineering). IRE had two mechanisms to accommodate a new community:

1. "Professional Groups" (these became "Societies" in the 1970s) had just appeared as IRE units, and were not easy to form: administrative requirements were unwieldy. Also, it wasn't really clear that such a formal approach was needed. The leaders of the Professional Group on Circuit Theory (PGCT) were eager to welcome transistor circuit engineers and their papers, even though the orientation of most PGCT members was toward "poles and zeros".
2. IRE had an active committee structure generating technical standards. A committee could form a new subcommittee by simple majority vote.

The latter approach was chosen. Perceiving a need of the nascent transistor circuits community, William R. Bennett, Chairman of "Technical Committee 4: Circuits", and John G. Linvill, a Committee member and a leader of transistor circuit work in BTL, decided to establish a new subcommittee. This came into being by vote of Committee 4 on November 14, 1952 as "Subcommittee 4.1: Transistor Circuitry" [8]. Linvill became Chairman and proceeded to recruit Subcommittee members from among those doing advanced transistor circuit work in major organizations. (There was no "one man, one vote" in those days: Subcommittee members came from companies located in and around New York.) The genesis of "Subcommittee 4.1", or as it became known simply "4.1", (in the late 50s it was renumbered to "4.10") had a major impact on the evolution of the solid-state circuits community. "4.1" became, as somebody jocularly put it, "the only IRE standards committee which didn't have the slightest intent to write standards". (The device people acted earlier and had already established, under "Committee 7: Electron Devices," a "Subcommittee 7.7: Solid-State Devices" with subordinate Task Groups.)

Soon after its creation, Subcommittee 4.1 defined its mission:

1. Conducting "regular meetings" every two or three months to encourage the advancement of the state of the art by exchanging information on recent progress and new trends.
2. Holding annual "expanded meetings" with about 50 leading technical people attending. Papers were presented orally on new developments. To encourage information flow unhampered by organizational restrictions, no minutes or records were kept. "Expanded meetings" were held in various locations (University of Connecticut, Cornell University, and State College of Pennsylvania come to mind). They were unusual: unlimited freedom of thought-sharing prevailed. The meetings acted as real stimuli of progress where leading technical people communicated unimpeded by company boundaries.
3. A third type of meeting was also visualized: an open meeting of the "speaker versus audience" type, attended by anybody interested. The Chairman was to explore ways to create such a meeting.
4. The importance of maintaining balance between material and device technologies, on the one hand, and circuit and system disciplines, on the other, was understood. Boundaries could not be well defined. The guiding principle was that overlaps are preferable to gaps.

Numerous individuals wished to become "4.1" members. To protect its privacy and effectiveness, the Subcommittee decided to admit only one member from each organization. Members could invite an alternate or a guest to committee meetings. Thus membership became highly prized and sought after. These rules were relaxed in later years. (Many non-members attended "expanded meetings" and formed the Subcommittee's informal "circle of friends".)

The November 1952 Special Issue of the Proceedings of the IRE

The Special Issue was a major event, which galvanized the evolving transistor circuits community into action:

* The Special Issue revealed to the public, as well as to "isolated" potential members of the transistor circuits community, that a sizeable group of people had been doing a great deal of diverse work in transistors and transistor circuits. More than that, key people, their affiliations, and locations became generally known.
* It became clear that transistors, not yet in ample supply, were made in quantities sufficient to support circuit R&D work. A small, rather ephemeral industry was launched; its members made and sold sample device quantities bought avidly by people interested in experimenting with applications.
* The Special Issue in effect "anointed" transistor circuit development as pioneering work and spread a "mantle of approval" over those engaged in it.
* All device and circuit work took place in the US. Other, industrially advanced countries were not involved for years. The world was still in the aftermath of World War II. Technical activities in the United Kingdom, France, Germany, and Japan were aimed at reconstruction rather than new developments.

In sum: The Special Issue of the Proceedings placed transistors and transistor circuits formally on the map of major efforts. People became interested in conferences dealing with these areas. (As one would expect, two technical communities evolved, devoted to devices and circuits, respectively, working interactively but autonomously.)

The gates were opened and the rush started.

The Philadelphia Section of IRE

In the early fifties, the Philadelphia Section of IRE was among the most active ones. Its geography was "compact", it was more convenient for members to attend section meetings than in other large metropolitan areas. The area was home to major electronics companies (Remington Rand, Philco, Burroughs, RCA Camden, Leeds and Northrup, etc.).

The Section benefitted from interactions with the Moore School of Electrical Engineering of the University of Pennsylvania and with John G. Brainerd, its forward-looking Director.

In August 1953, the Section, which by that time had already sponsored conferences of national scope in color television, circuit theory, etc., decided to host a national conference on transistor circuits [9].

The First Conference Gets Underway

The Philadelphia Section's plans matched those of Subcommittee 4.1. Subsequent events took place rapidly and are described by Herbert J. Carlin, Vice Chairman of PGCT [l0]. (Figure 1 on page 16) The first "Conference on Transistor Circuits" was under way!

Work assignments were made expeditiously:

* Subcommittee 4.1 took charge of the technical program. Its Chairman, John G. Linvill, chaired the Program Committee. All "4.1" members were invited to Program Committee membership and all but one accepted. The Program Committee was augmented by people from the Subcommittee's "circle of friends", from the Philadelphia IRE Section, and from AIEE.
* The Philadelphia Section of IRE took care of administrative tasks, including finances, publicity, and hotel arrangements.
* The Moore School of Electrical Engineering organized and provided Conference facilities and associated arrangements.

The First Decade: 1954-1963

The first Conferences had several characteristics in common:

* They were sponsored by IRE PGCT and the Philadelphia Section, AIEE Electronics Committee and Philadelphia Section, and the University of Pennsylvania's Moore School.
* The Sponsors ascertained that the Conference was managed responsibly from the technical and the financial viewpoints.
* The Sponsors provided continuity by stimulating orderly management succession. This was done informally: next year's Chairman, Secretary, and Program Chairman were appointed by consensus of the Sponsors, the current year's leadership, and occasional advisors. The selection criteria involved the candidates' affiliation and personal qualifications. Chairman and Secretary were selected as a "pair" from the same company. (In the early years the Chairman's role was ceremonial, the Secretary managed the Conference,) The Program Chairman was a member of "4.1" or belonged to its "circle of friends".

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* Conference functions were performed as follows: Subcommittee 4.1 and its "circle" were members of the Program Committee and influenced program content and emphasis. (With the passage of time, the influence of "4.1" waned; the Conference became progressively more independent.) The Philadelphia IRE and AIEE Sections and Moore School managed local arrangements and most administrative matters.

*The Conferences were held in Philadelphia on Thursday and Friday in mid-February at the University of Pennsylvania (Irvine Auditorium and University Museum).

* For many years successive Conference leaders emphasized:
  - broadening the technology base to include an increasing variety of solid-state activities;
  - maintaining dynamic balance between material/device versus circuit/system emphasis;
  - preserving the Conference's pioneering, avant-garde nature, to discourage papers on straight forward design, and to reject papers of public relations or advertising nature;
  - enforcing high standards of technical excellence to motivate growth, as well as acceptance of the Conference as "home" by its fast public relations or advertising nature; growing technical community.

Adhering to these principles, the Conference's reputation and attendance grew rapidly, at times explosively, and contributed materially to building the solid-state circuits technical community whose enduring loyalty became the foundation of the long chain of Conferences.

A Brief Historical Summary of the First Decade

1954 - The First Conference (Chairman: Irving G. Wolff, RCA; Secretary: John S. Donal, RCA; Program Chairman: John G. Linvill, BTL), named "Conference on Transistor Circuits", was held on February 18 and 19, and included 4 regular sessions. (A summary of this 1st Conference can be found in the 1993 40th Anniversary Supplement as Figure 2 on page 17) The attendance of over 600 was a pleasant surprise and led to the decision to try to make the Conference an annual event. Registration fee was $3 (early), $4 (late). Conference headquarters was the Penn Sherwood Hotel.

The program covered transistor properties and representation, and rather basic small- and large-signal circuits.

1955 - The Second Conference (Chairman: Donald G. Fink, Philco; Secretary: William H. Forster, Philco; Program Chairman: Howard E. Tompkins, Borroughs) followed the format of the first. Attendance was over 700. The program covered transistor oscillators, linear and digital computer circuits, and large-signal operation. An historic "first" was "Informal Discussion Sessions" on Thursday evening. People with similar interests got together for "roundtable discussions" on topics chosen by mutual consent. By encouraging free exchange of information, and by acquainting leading technical people with each other, these sessions became major attractions of the Conference and among its most productive ingredients.

1956 - The Third Conference (Chairman: George L. Haller, General Electric; Secretary: Arthur P. Stern, General Electric; Program Chairman: Harry J. Woll, RCA) had a sharply-increased attendance of close to 1200 and a number of foreign guests.

The program was still centered on transistors. The 4 regular sessions were augmented by 2 tutorial ones.

Another innovation was foreshadowed in the address of the Chairman who called for diversifying the Conference's technical scope to include solid-state circuits of various types beyond transistors.

1957 - The Fourth Conference (Chairman: Arthur L. Samuel, IBM; secretary: Joseph C. Logue, IBM; Program Chairman: George H. Royer, Westinghouse), reflecting the suggestion made in 1956, had a new name: 'Transistor and Solid-state Circuits Conference". Headquarters were shifted to the Bellevue-Stratford Hotel. The emphasis remained on transistor circuits but a session was devoted to applications of magnetic, ferroelectric, and unijunction devices. Another first" was a Conference Record containing the figures and diagrams of the papers presented. (A sample page of this record can be found in the 1993 40th Anniversary Supplement on page 48.)

1958 - The Fifth Conference (Chairman: James H. Mulligan, New York University; Secretary: Sidney S. Shamis, New York University; Program Chairman: Richard H. Baker, MIT) saw important changes:
Deviating from prior years, when the Conference Chairman had an honorary role, and management was by the Conference Secretary (a technical manager in the same company), Jim Mulligan was really managing several innovations:

* Lewis Winner, experienced in technical publications and publicity, was engaged to issue a "Digest of Technical Papers" containing summaries of all papers presented. Lew organized the Digest, as well as other publicity activities for 31 years, bringing credit to the Conference and to himself. Robert F. Cotellessa (New York University) initially acted as Digest Editor.
* The loose group of Conference sponsors were organized into a Sponsors Advisory Committee chaired by Murlan S. Corrington (RCA), endowed with authority to plan future Conferences and to appoint key officers.
* Headquarters was shifted to the then-new and spacious Philadelphia Sheraton Hotel.

The program included core memories, magnetostrictive devices, dielectric modulators, etc. The number of regular sessions was increased to 5, and that of evening discussion sessions to 4.

1959 - The Sixth Conference (Chairman: Jack A. Morton, BTL; Secretary: Tudor R. Finch, BTL ; Program Chairman: Arthur P Stern, General Electric) was named "Solid-State Circuits Conference", officially removing the emphasis from transistors.

Innovations were mostly in the program area: a keynote speaker was added (M. J. Kelly, BTL); sessions dealt with microwave electronics, memory techniques, applications of silicon controlled rectifiers, superconductive elements, Hall effect devices, and ceramic filters. The number of regular sessions was increased to 8, and evening discussion sessions also to 8.

1960 - The Seventh Conference (Chairman: Arthur P. Stern, General Electric; Secretary: Sorab K. Ghandhi, General Electric; Program Chairman: Tudor R. Finch, BTL) was given its definitive name: "International Solid-state Circuits Conference" (briefly: "ISSCC"). It was the first and biggest international Conference, attended by an all time high of about 3300 participants, many from outside the U.S. Its spectacular success made it a pattern-setter for subsequent Conferences.

Conference duration was expanded to 3 days, starting Wednesday rather than Thursday, with 8 regular sessions. The evening discussion sessions were formalized and their number was increased to 12. Keynote speakers were: C. Guy Suits (General Electric) and M. J. O. Strutt (Swiss Federal Institute of Technology) the first keynote speaker from outside the US.

The program emphasized tunnel diodes, parametric circuit techniques, thin film structures, complex magnetic devices, and presented the first microelectronics session.

1961 -The Eighth Conference (Chairman: Tudor R. Finch, BTL; Secretary: Franklin H. Blecher, BTL; Program Chairman: Jerome J. Suran, General Electric);

1962 -The Ninth Conference (Chairman: Jerome J. Suran, General Electric; Secretary: Edward G. Nielsen, General Electric; Program Chairman: Richard B. Adler, MIT);

1963 - The Tenth Conference (Chairman: Franklin H. Blecher, BTL; Secretary: Francis J. Witt, BTL; Program Chairman: Sorab K. Ghandhi, Philco); all retained the duration, format, and organization of 1960 ... the Conference had reached a steady state.

Gradual changes were:

* International content was increased and, in 1961, an International Arrangements Committee was created.
* The number of regular sessions was increased to 10 and the evening discussion sessions were further refined.
* Program emphasis was on increased power, frequency, and integration; papers on circuits using a large variety of new devices were presented; system applications were given more space; integrated electronics commanded growing attention.
* Keynote speakers on timely and at times provocative subjects became a regular part of the program: in 1961, J. G. Linvill; in 1962, Pierre Aigrain; in 1963, J. H. Mulligan.

The Conferences were attended by about 2000 people. Conference administration became complex but efficient:

* The Sponsors Advisory Committee (SAC) functioned smoothly and reelected Chairman Murlan S. Corrington year after year.
* Robert Mayer (Minneapolis Honeywell, later Sun Oil) became practically permanent Treasurer and Henry G. Sparks (Moore School) Local Arrangements Chairman.
* The Digest of Technical Papers was published by Lew Winner who did a consistently outstanding, dedicated job.

ISSCC attained a state of dynamic equilibrium, characterized by progressive program plans, adaptive assimilation of change, and administrative consolidation.

Impact of ISSCC on the ISSC Community

By the end of its first decade, ISSCC was accepted as the major annual event in its field where authors wished to present papers. Frequent attendance became quasi-obligatory for leading members of the worldwide solid-state circuits community. Attempts to create comparable events overseas were made from time to time and resulted in good meetings (e.g., 1959 Munich, 1960 London, 1961 Paris) but had no competitive impact on ISSCC.

ISSCC satisfied the needs of the community:

* It provided an annual forum where contributors from all around the world could present new approaches and developments on short notice of 4 to 5 months from submission to presentation.
* The contributions did not remain oral. The Conference Digest became a respected publication providing, in summary form, an easily accessible permanent record.
* It offered opportunities for oral information exchange via numerous evening discussion sessions. These frequently lasted many hours, some beyond midnight, and led to rapport between participants from distant locations.

The growth and stabilization of ISSCC had a negative impact on its creator: "Subcommittee 4.1: Transistor Circuitry" which in 1957 was renamed "Subcommittee 4.10: Solid-state Circuits".

The influence and effectiveness of "4.1" peaked in 1955-1957. With the advent of many products utilizing solid-state circuits, its discussions increasingly involved engineers working on competitive products for competing companies. This fact introduced reticence and formal boundaries in the process of information exchange. Regular "4.1" meetings which previously had consisted of uninhibited technical discussions ran into competitive constraints. The candor of the meetings had to be curtailed. This was even more so for the "expanded meetings," where new thoughts and approaches had been freely exposed and discussed during the early years. That which could be discussed in a competitive environment found a home in ISSCC's evening discussion sessions, which thus replaced much of "4.10's" earlier function ... ("Sic transit gloria mundi": the creation devoured its creator. Not unusual in history, almost standard for revolutions. And solid-state certainly was a revolution!) The surviving activities of the Subcommittee became part of PGCT after the IRE-AIEE merger. The Digest of Technical Papers gave the community a fine publication but it was not a technical periodical published several times a year and lacked other trappings of a technical journal. Many ISSCC authors wished to have their papers printed in full length. Initially, this was done by periodicals, which accepted solid-state circuits articles, and were occasionally willing to publish Special Issues dedicated to solid-state circuits. For example, IRE Transactions on Circuit Theory had Special issues on Solid-state Circuits in 1956 and in 1957 [11,12]. The Proceedings of the IEEE published a Special Issue on Integrated Electronics in 1964 [13]. The Transactions of other IRE Professional Groups (Computers, Electron Devices, Microwave Theory and Techniques) also published articles on solid-state circuits, so that ample opportunities for publication became available. The community continued to clamor for its own periodical. Already in the late 50s there were discussions about a new journal but action may have been delayed by the success of the Digest. Further delay resulted from the fact that no less than four Professional Groups (Circuit Theory, Computers, Electron Devices, and Microwave Theory and Techniques) claimed a proprietary interest in solid-state circuits and in a potential regular solid-state circuits publication. Finally, after years of discussion and negotiation, the IEEE Solid-State Circuits Council, representing all four interested Professional Groups, was established, chaired by John G. Linvill. The Council sponsored the creation of the Journal of Solid-State Circuits in 1966. James D. Meindl (then US. Army Electronics Command, later Stanford University), ISSCC Program Chairman that year, became its first Editor. The first two issues of the Solid-State Circuits Journal were entirely dedicated to papers of the 1966 ISSCC [14]. The first issue's Guest Editor was Sorab K. Ghandhi, who had been ISSCC Program Chairman in 1963. Thus the solid-

state circuits community's instruments of communication and self-expression were complete with:

* the ISSCC for rapid reaction as an annual forum, the evening discussion sessions providing opportunity for personal interfacing, debating, and rapport; and
* the Solid-State Circuits Journal as its regular periodical which rapidly established its own reputation for excellence.

For many years they have acted together as an infrastructure, which has served the solid-state circuits community well.

Concluding Perspective

Four decades — from the viewpoint of history: a very short span, a passing shade, a flying speck of dust. From the viewpoint of the human condition: a long stretch, two generations of technical leadership, who knows how many generations of device and circuit innovation, more than the age of many leading companies. DEC is younger, Intel much younger, Apple very much younger. Industrial and technical giants have disappeared since the creation of ISSCC or have undergone a metamorphosis so radical that they can't be recognized: RCA, Remington Rand, Burroughs come to mind.

A point upon which most observers agree is that the remarkable durability of ISSCC is due to its sustained relevance through successive technical upheavals of which it was principal witness and articulate recorder. That fact should generate respect for the adaptability and effectiveness of its design and for the foresight of its designers.

Epilogue

To write a retrospective on ISSCC's origin and first years was a delightful and fascinating assignment.

Objectively, the topic is worthwhile because of ISSCC's role in the solid-state revolution, which made such a profound impact on the lives of most humans.

Subjectively, the task gave me a chance to revisit the field, which, decades ago, meant so much to my associates and me. It was gratifying to talk and renew friendships with people for whom I had affection and respect while participating with them in the challenge of the 50s: the creation of the solid-state circuits art and, along with it, of ISSCC. Sharing in that endeavor was an exciting experience, when we were young, ambitious, brash, creative, always in the passing lane ... leaving the sedate world of vacuum-tube electronics far behind, and leading the pack.

As an amateur historian, I knew something about the perennial debate between two schools of historiography: those who demand documentary evidence (their medieval antecedents proclaimed: "quod non est in actis, non est in mundo", i.e., "if it isn't documented, it never happened") and those who savor memories and memoirs of witnesses and survivors. The vagaries of recall by observers of historic events are well known. Nevertheless, I was astounded by the discrepancies between recollections of people who were members of a rather small group intimately involved with each other in activities that, at that time, were of primary importance to all of them.

To approximate the truth, I had to seek the written record constantly, no matter how elusive or vaguely allusive it was, in order to verify facts against memories. However, many things are not recorded or the record cannot be found ... and recollections have a truth and reality of their own, they contribute to the "elan vital". Whether they are strictly accurate is less significant than the fact that they are representative of a creative era and they evoke the spirit of adventure.

In this retrospective, I interpreted events in a manner with which some may disagree and emphasized events and personalities, which others may not have chosen. For any personal slights, certainly not intended, sincere apologies are tendered.

Acknowledgements

In preparing this work I benefited from the assistance of the pioneers of the still vital and rapidly changing field of solid-state circuits. John Linvill, Jerry Suran, Jim Mulligan, Jack Raper, Jim Angell, Dick Baker, Frank Blecher, Murlan Corrington, Bob Cotellessa, Jim Early, Don Fink, Soli Ghandhi, Gerry Herzog, Arthur Lo, Joe Logue, Roy Mattson, Bob Mayer, John Mayo, Jim Meindl, Don Pedersen, Dave Pricer, Bob Pritchard, Sid Shamis, Ralph Showers, Henry Sparks, Eric Sumner, Howard Tompkins, Harry Woll, John Wuorinen, thanks for your memories, for your help and for what you have done for the solid-state community! And those who are no longer with us: Jack Morton, Tudor Finch, John Brainerd, Lew Winner, Dick Adler, Bob Henle, Bill Forster, we remember them and their accomplishments with affection and respect. The support of Richard Steele, Associate Director of the Engineering Societies Library in New York, and the documents he brought to light enabled me to complete this work.

Finally, I am indebted to my friend and associate of many decades, James Litton, Jr., for his review and for his insightful suggestions.

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ISSCC — The Later Years

W. David Pricer, Consultant

The Internationalization of the Conference

Back in 1954, the organizers of what would become the International Solid-State Circuits Conference did not know they were founding an international conference, or even an annual event. The only international presence at the first Conference consisted of one attendee each from Canada and Japan. That perspective changed rapidly over the first few years: The first overseas papers appeared in 1958. In 1960, after experimenting with almost-yearly title changes, the organizers settled on the present "International" title of the Conference.

Converting regional birth into international breadth was more difficult. As late as 1961, four northeast-region American companies (BTL, GE, IBM and RCA) contributed over 50% of all conference papers.

The first overseas Program Committee members appeared in 1960. These were, of necessity, "corresponding" members. Much of the industrialized world was still recovering from the aftermath of World War II. Overseas travel was considered expensive, and a major hurdle to conference participation. Military-sponsored research was still a major source of solid-state funding. The Office of Naval Research provided travel for overseas speakers through the Military Air-Transport Service. The other armed services soon joined this support, and the practice continued into the 1970s.

By 1965, the number of overseas program committee members had increased to 8, and by 1968 the acceptance of overseas papers was considered to be on a par with those from North America. Throughout the 1960s overseas members contributed primarily by soliciting submitted papers, and with written commentary mailed to the US Program Committee.

In 1970, the overseas membership was greatly expanded and began meeting separately in both Europe and Japan under the leadership of Jan van Vessem and Takuo Sugano, respectively. Selected members were dispatched to the final program committee meeting in Philadelphia with the results of these deliberations. The Executive Committee was expanded to include the overseas Chairs.

Today, there are thirty-two members of the European Program Committee and thirty-four members of the Far-East Program Committee, not counting liaison members. Overseas members participate in all aspects of the conference organization and technical-program selection. Approximately one half of all ISSCC papers presented, originate from outside North America. Some papers have authors on multiple continents. The "I" in "ISSCC" is real!

Evolution of the Technical Program and the Program Committee

As reported in Arthur Stern's article, the original Program Committee was formed by recruits drawn from the Circuit-Theory Group 4.10 Committee. The Program Committee soon adopted the practice of rotating membership, such that each year, 30 percent would "retire" and be replaced by "new" members. In the formative years, the Program Committee would also reorganize itself yearly into new subcommittees, the better to grapple with an ever-changing menu of new paper topics. In an era unconstrained by the demands of integration, a broad spectrum of technologies found their way into the "solid-state tent'. A few of these technologies, like tunnel diodes, had very short life times.

In 1968, the Program Sub-Committees evolved, to become Digital, Analog (Linear), Microwave, and Other. The rather non-descript "Other" referred to a brave band of committee members prepared to review many examples of one-of-a-kind papers. By the mid-sixties the enormous economic power of circuit integration had marginalized many competing solid-state technologies, particularly magnetics, as well, as semiconductor devices requiring unique diffusion profiles. Solid-state came to mean solid-state integrated semiconductor circuits. This four-subcommittee organization of the Program Committee would remain stable for the next fifteen years.

1984 was the last year of the Microwave Subcommittee. Microwave technology had largely remained in discrete circuits or low-level integration. The microwave program had become a conference within a conference exhibiting little overlap with wider attendee interest. Microwave was thereafter dropped from the program. Diversification in integrated circuit application rapidly filled the void.

By 1987, Digital had split into separate Digital and Memory subcommittees, and a Signal-Processing subcommittee had joined the Program Committee roster. "Other" was subsequently given the more genteel title of "General" voiding some rather bad insider jokes.

In 1992, the proliferation of subcommittee disciplines resumed, with the launching of the Emerging Technologies Subcommittee. This was the first subcommittee specifically chartered to seek out solid-state applications, which had not already found a home in ISSCC. Both the subcommittee title and its charter were eventually expanded to Technology Directions. Papers reviewed by this subcommittee have become one of the most-highly-ranked features of the Conference.

Through the 1990s, an explosion in communications papers brought further additions to the list of separate subcommittee disciplines. A steady growth in submitted papers throughout the late 1990s and early 21st century have kept each new subcommittee's paper review schedule fully loaded. The 2003 Subcommittees consist of: Analog, Digital, Imagers Displays and MEMs, Memory, Signal Processing, Technology Directions, Wireless & RF Communications, and Wireline Communications They reviewed 450 submitted papers to bring you the 2003 program.

The Move from Philadelphia

ISSCC was founded in Philadelphia by the University of Pennsylvania and the local chapters of the IRE and the AIEE (forerunners of the IEEE). In the formative years, ISSCC garnered broad support from established electronics firms in the American northeast. Many of these firms were within easy driving distance of the Conference's home at the campus of the University of Pennsylvania.

However, by the mid-1960s, the center of semiconductor development in the United States was shifting west, and the international nature of the Conference was coming into much sharper focus. Western attendees gradually became more vocal about moving the Conference to San Francisco. Unsurprisingly, the founders preferred their Philadelphia home. They had a surprisingly-effective, if somewhat perverse-sounding argument. 'When an engineer says he wants to attend a conference in Philadelphia in February, management knows he is sincere.' Strong Conference attendance, even in weak economic years, seemed to validate this view.

A campaign by western attendees, orchestrated by David Hodges, convinced the sponsors to try San Francisco in 1978.

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The first year, California attendance was large and the response was gratifying. The Conference then continued to alternate coasts, with New York soon substituting for Philadelphia.

After a decade of consistently stronger attendance in California, the Conference, in 1990 made San Francisco its permanent home.

The Role of the Executive Committee

ISSCC is the single largest financial entity within the oversight of the IEEE Solid-State Circuits Society. Although it is strictly a non-profit organization, financial sobriety requires that it be run like a business.

From the very beginning, the operations of the Executive Committee were made entirely separate from those of the Program Committee. The organizational philosophy was to keep the Program Committee firmly focused on the quality of the program without the distractive concerns for conference operations or financial balance. This separation, which was somewhat innovative for the time, has now become common industry practice. In the beginning, this 'business' committee was called the "National Committee", a name reflecting the regional origins of the Conference. The name was changed to "Executive" once the Conference firmly gained its international stature.

The Executive Committee's structure has changed considerably over the years. From the early years through 1980, the post of Conference (and Executive Committee) Chair was usually filled by last year's Program Chair. In roughly these same years, continuity-of-business-acumen was provided by the Treasurer Bob Mayer, Digest Editor Lew Winner, Local Arrangements Chair Henry Sparks, and the Chair of the Sponsors Committee Murlin Corrington. All four of these people had been continuously active in the leadership of the Conference from the formative years. Other posts like Secretary and International Arrangements rotated more often. In the 1980s all four of these pioneers would retire or die.

Starting in 1980, the term of Executive Chair was extended to multiple years, typically 5 to 8. Since 1980, there have been just four Chairs: Jack Raper, David Pricer, John Trnka, and Tim Tredwell. All four would oversee significant changes in the Conference.

The Lew Winner Years

Lew Winner began his career as a technical writer and New York City radio commentator. In 1956, he was recruited to help edit what was then called the "Technical Addendum to the Program Booklet". This would eventually become the "Digest of Technical Papers", but initially looked more like today's "Visual Supplement". He and Editorial Chair, Jack Raper, assisted by Lew's wife, Beatrice, maintained a standard of excellence for decades. Over the next three decades, the fortunes of Lew and the ISSCC would become progressively more intertwined. In retrospect, it is difficult to say which influenced the other the most.

Lew's early association with ISSCC was tenuous. He didn't even put his name on the first 'Digest'. Formal arrangements stipulated that he would be paid, but only if the Conference first showed a surplus. His title was Public Relations, which he kept to the end, and well beyond the point when it was anywhere near descriptive of his duties.

By the mid-1970s Lew was effectively the general manager of the Conference. As many of the pioneers retired in the 1980s, he further assumed some of their duties. He worked Herculean hours for a modest fee. His ability to resist sleep deprivation was storied. For fifty weeks a year, his life WAS the ISSCC. Then for two weeks each year, he took a hotel room in Fort Lauderdale, sat on the beach and compiled the Conference statistics. That was Lew's vacation! As noted in his 1988 obituary, in his later years, he came to enjoy playing the role of the curmudgeon, demanding excellence from anyone associated with the Conference, and delivering scorn, in the event it wasn't immediately forthcoming.

The Expansive Years

In the first thirty-five years of the Conference, the technical program grew from 18 papers to about 90, while maintaining the strictest standards for paper acceptance. The evening hours were filled with panel discussion, the more controversial, the better. The attendee could expect an experience that was Spartan, intense and just 2 _ days long. Over the next fifteen years, ISSCC gradually added new features.

The Visuals Supplement (originally the Slide Supplement) first appeared in 1990. Speakers often use as many as 20 projected 'slide' images, including some that have been added to their paper at the last minute. The "Supplement" vastly simplified note taking for the attendee. It also eliminated a crescendo of camera-shutter clicks, as each new 'slide' image was projected on the screen. The "Supplement" also provided one entirely unexpected benefit: Speakers came to be required to submit their slide images to Editor Laura Fujino before paper presentation. Deficient slides could be detected before general presentation. She and a small band of students and helpers, now provide last-minute enhancements to poorly-organized or marginally-readable images.

The Short Course was introduced in 1993. It is primarily directed toward engineers facing significant new knowledge demands. The subject changes each year, but the instructors are always recognized experts in rapidly-moving fields. Over the years, the 'take-home' materials have been expanded from printed handouts of the notes to a CD ROM with all course 'slide' images, complete bibliographies, and copies of many relevant background papers and materials.

Short papers also appeared in 1993. Previously the Program Committee frequently needed to choose between 'technical benchmark' papers and papers with really neat circuit 'ideas'; the latter too frequently losing out. Short papers gave the committee more flexibility in compiling a balanced program.

The tutorials were introduced in 1995. Their purpose is radically different from the Short Course. The tutorials are positioned before the presentation of the regular papers and are intended to provide 'instant background' for attendees contemplating papers out of their own field, prior to the Conference. Repeated sessions allow attendees to sign up for up to three such tutorials This feature of the Conference has been very popular, with many sessions sold out.

In 1996, ISSCC finally broke with its austere past, and sponsored a social hour. Attendees took the opportunity to "network".

Starting in 1996, and every year thereafter, ISSCC has provided each attendee with a CD ROM. The CD ROM allows electronic searching of all the information in the Digest and Visuals Supplement. That CD was followed in 2000 by an SSCS-sponsored single archival DVD with all ISSCC articles from 1955 onward, and the Journal of Solid-State Circuits from 1966 onward.

ISSCC began experimenting with electronic projection in the late 1970s. The early equipment had a low level of light intensity and was relegated to session-overflow rooms.

In 2001, ISSCC went to all-electronic projection. Because ISSCC uses the highest-available light-intensity systems, attendees can now take notes in near-normal ambient room light.

In the same year, ISSCC added WEB registration, which provides instant confirmation of successful registration. This is particularly helpful in organizing limited-seating functions such as the tutorials and the Short Course.

For many years, the independent Solid-State Circuits and Technology Committee has sponsored a concurrent event, called a workshop, targeted for experts in a particular solid-state field. In 2001, at ISSCC, ISSCC began offering additional workshops of its own. There are now four such events, two each occurring on the first and last days of the Conference.

In 2002, ISSCC started experimenting with special-topic evening sessions on Sunday. These feature carefully-selected topics with a mixture of invited presentations and panel-like discussions. The Conference was now a full five-day event with a rotating spectrum of special features.

On a slightly different front, ISSCC is now three years into a program directed toward eventual complete electronic submission of papers. The Conference is just now beginning to see the benefits in accuracy and scheduling. As in other such endeavors, software compatibility is the principal hurdle.

Reflections

ISSCC has now managed an unbroken fifty-year record of technical excellence. As in most things, success has not come as an accident. The vitality of ISSCC has rested for its entire history on two pillars. The topic of the Conference was (and is) universally important. Equally true, the people selected to make the Conference happen, knew this wasn't 'just another conference': This was the "Olympics". They responded in their efforts accordingly.

Fifty years of past success does not guarantee fifty more years of anything. For success to continue, to happen, solid-state technology must retain its vast importance. As well, the generations of leaders yet to come, will need to retain the necessary vision. Finally, ISSCC will have to grapple with its own success.

Several times in its history, the Conference attendance has "spiked" above 3000, only to subside to more sustainable levels in the following years. Yet, the attendance growth experienced in the past ten years appears to be sustainable. This is possibly the result of the fact that the Conference has responded to apparent attendees interest with a vastly-expanded program, both in added papers and in new features.

Yet, as in all things, there are limitations. ISSCC is rapidly approaching the limits of suitable meeting space in its San Francisco home. At five days duration, the rigorous program is testing the limits of attendee endurance. Yes, there will be challenges!

Acknowledgements

It is impossible in articles spanning so many years to acknowledge all the people who made significant contributions to ISSCC. In addition to those already mentioned in both this and Arthur Stern's articles, the following have served this Conference in roles spanning a decade or more.

Ken Smith is the long term Awards Chair and Press Chair. Ken along with Editor Laura Fujino, are a husband and wife team. I'm never sure where one's duties start and the other's end. John Kennedy has been the Treasurer since 1982, and a major reason we pass audits. Diane Suiters of Courtesy Associates joined the team in 1988. She is Operations Chair, and the principal reason we can run a conference this complicated. Frank Hewlett is presently the Conference Secretary, but his past service includes many other posts including Program Chair. John Wuorinen has served in many roles, and was our Digest Editor from 1988 until 2002. Jan Van der Spiegel is both the connection to our founding sponsor, the University of Pennsylvania, and the liaison between a breathtaking ensemble of Conference committees.

1955 IRE–AIEE–U of P
CONFERENCE ON
TRANSISTOR CIRCUITS
FEBRUARY 17-18, 1955
IRVINE AUDITORIUM
UNIVERSITY OF PENNSYLVANIA
PHILADELPHIA, PA.

Advance Program

WEDNESDAY, FEBRUARY 16
7:00 P.M.—REGISTRATION OPENS
Penn Sherwood Hotel
THURSDAY, FEBRUARY 17
8:00 A.M.—REGISTRATION OPENS
Irvine Auditorium
9:30 A.M.-12:00 Noon—SESSION I—Irvine Auditorium
OSCILLATORS
Chairman: J. J. SUHAY, General Electric Company, Syracuse, N. Y.
Introductory remarks by Mr. D. G. Fink, Director of Research of Philco Corporation and Chairman of the National Committee for the 1955 Conference; and welcome by officials of the University of Pennsylvania.
1.1 "Transistor Superregenerative Detection," W. F. Chow—General Electric Company, Syracuse
1.2 "Field-effect Transistor Applications," C. Huang, M. Marshall, and L. R. White—Sylvania Electric Products, Inc., Ipswich
1.3 "A Stabilized Transistor Oscillator," E. Keonjian—General Electric Company, Syracuse
1.4 "A Symmetrical Transistor Oscillator With Low Second-harmonic Distortion," W. M. Grim, Jr.—Servomechanisms Lab, MIT
12:00 Noon-2:00 P.M.—LUNCH
Houston Hall
2:00 P.M.-5:00 P.M.—SESSION II—Irvine Auditorium
LINEAR SYSTEMS
Chairman: RICHARD B. ADLER, Research Lab of Electronics, MIT
2.1 "Predictions Based on the Maximum Oscillator Frequency," P. Drouilhet—Philco Corporation and MIT
2.2 "The Relationship of Transistor Parameters to Amplifier Performance," J. G. Linvill—Bell Telephone Laboratories
2.3 "Principles of Automatic Gain Control of Transistor Amplifiers," W. F. Chow and A. P. Stern—General Electric Company, Syracuse
2.4 "A Transistor Transmitter-receiver Unit," C. C. Bopp—Crosley Division of AVCO
2.5 "A Transistor Amplifier and Discriminator with Bias Stabilization," T. A. Patchell—Minneapolis-Honeywell, Brown Instrument Division
SEE REVERSE SIDE FOR REGISTRATION INFORMATION
6:00 P.M.—COCKTAIL-BUFFET
Penn Sherwood Hotel
7:00 P.M.—INFORMAL GROUP DISCUSSIONS
Penn Sherwood Hotel
FRIDAY, FEBRUARY 18
8:30 A.M.—REGISTRATION OPENS
Irvine Auditorium
9:00 A.M.-12:00 Noon—SESSION III—Irvine Auditorium
DIGITAL-COMPUTER CIRCUITS
Chairman: RICHARD ENDRES, RCA Victor Division, Camden, N. J.
3.1 "The Regeneration Analysis of Junction-transistor Multivibrators," D. O. Pederson—Bell Telephone Laboratories
3.2 "Junction-transistor Flip-flops with Differential-transformer Coupling," Howard Kennedy and A. B. Jacobsen—Motorola Research Laboratory
3.3 "A Multistable Transistor Circuit," R. A. Henle —International Business Machines Corporation
3.4 "Transistors in Computer Circuits," D. E. Deuitch—RCA Victor Division, Camden, N. J.
3.5 "Transistor Flip-flop Units for Digital Computing Systems," R. H. Baker—MIT
12:00 Noon-2:00 P.M.—LUNCH
Houston Hall
2:00 P.M.-4:30 P.M.—SESSION IV—Irvine Auditorium
"LARGE-SIGNAL" OPERATION
Chairman: ROBERT MAYER, Minneapolis-Honeywell, Brown Instrument Division
4.1 "An N-stage Series Transistor Circuit," K. H. Beck—Minneapolis-Honeywell, Brown Instrument Division
4.2 "Junction-transistor Circuits for Analogue-to-binary Code Conversion," F. H. Blecher—Bell Telephone Laboratories
4.3 "A Temperature-compensated Transistor Power Converter," C. E. Paul—Bell Telephone Laboratories
4.4 "Transistors as Power-conversion Devices," R. R. Smyth—Technical Operations, Inc.
4.5 "Power-transistor Switching Circuits," E. Slobodzinski and C. Huang—Sylvania Electric Products, Inc., Ipswich

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SPONSORSHIP AND SCOPE

on Transistor Circuits is sponsored jointly by the IRE Profession on
ice and Electronics Division of AIEE, and the University of Penn he
fter the first one held at the same location a year ago and will i ers
inear transistor circuit applications. Emphasis will be on material r aly
re and the program is designed to be of greatest value to engineers dy
of transistor circuit behavior.

will be available at the Penn Sherwood Hotel after the Cocktail-Buf its
e who wish to hold informal round-table discussions. Arrangements f of
ade at the Conference.

any of the papers in professional journals is planned in lieu of Conference Trans-

LOCATION

of Pennsylvania is host for the Conference, and has offered the facilities of Irvine
meetings and adjacent Houston Hall for the lunches.
ium is located at the corner of 34th and Spruce Streets, Philadelphia, Pennsylvania.
ia is easily reached by street cars No. 13 and 42 on Chestnut and Walnut Streets and
tation of the Pennsylvania Railroad is less than a mile from the Auditorium.

ACCOMMODATIONS

herwood Hotel at 39th and Chestnut Streets has reserved a block of rooms for those at-
sference. Those who arrive Wednesday evening may register or confirm their reserva-
nference at the Hotel to avoid possible delays at Irvine Auditorium on Thursday morn-
al cocktail-buffet, followed by the round-table discussions, will be held at the Penn Sher-
hursday evening.

ll be served to a limited number on both Thursday and Friday at Houston Hall. For those
eat elsewhere, Philadelphia offers many fine restaurants.

REGISTRATION

ation and hotel reservation forms are being mailed to members of the sponsoring professional
he Eastern part of the United States. Others may obtain them from Mr. W. J. Poppowsky,
Honeywell Regulator Company, 176 W. Louden Street, Philadelphia 20, Pa. Fees for the Con-
as follows:

	Advance	*At Conference*
Registration	$ 5.00	$ 4.00
Thursday Lunch	1.75	2.00
Cocktail-buffet	4.50	5.00
Friday Lunch	1.75	2.00
	$11.00	$13.00

ed fees apply only to those registering by mail before February 12, 1955.
ecause of limited facilities and to assist the Local Arrangements Committee, advance registration
neal purchases are strongly recommended.

Advance Program from the 1955 Conference.

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50 Years of ISSCC Technical and General Chairs

Year	Technical Chair	Affiliation	City	State	General Chair	Affiliation	City	State
1954	J. G. Linvill	Bell Labs			I. Wolf	RCA		
1955	H. E. Tompkins	Burroughs Corp			D. Fink	Philco		
1956	H. Woll	RCA Labs	Princeton	NJ	G. L. Haller	General Electric	Syracuse	NY
1957	G. Royer	IBM	Poughkeepsie	NY	A. L. Samuel	IBM		
1958	R. Baker	MIT Lincoln Labs	Lexington	MA	J. H. Mulligan, Jr	New York University	New York	NY
1959	A. P. Stern	General Electric	Syracuse	NY	J. Morton	Bell Labs	Murray Hill	NJ
1960	T. R. Finch	Bell Labs	Murray Hill	NJ	A. P Stern	General Electric	Syracuse	NY
1961	J. J. Suran	General Electric	Syracuse	NY	T. R. Finch	Bell Labs	Murray Hill	NJ
1962	R. B Adler	MIT	Cambridge	MA	J. J. Suran	General Electric	Syracuse	NY
1963	S. K. Ghandhi	Philco Scientific Lab	Blue Bell	PA	F. H. Blecher	Bell Labs	Murray Hill	NJ
1964	P. B. Myers	Marietta Corp	Baltimore	MD	E. O. Johnson	RCA	Somerville	NJ
1965	G. B. Herzog	RCA Labs	Princeton	NJ	J. B. Angell	Stanford Univ.	Stanford	CA
1966	G. B. Herzog	RCA Labs	Princeton	NJ	J. D. Meindl	US Army Electronics Cmd.	Fort Monmouth	NJ
1967	R. H. Baker	MIT	Cambridge	MA	J. S. Mayo	Bell Labs	Holmdel	NJ
1968	R. L. Petritz	Texas Instruments	Dallas	TX	J. S. Mayo	Bell Labs	Whippany	NJ
1969	R. S. Engelbrecht	Bell Labs	Murray Hill	NS	J. D. Meindl	Stanford Univ.	Stanford	CA
1970	T. E. Bray	General Electric	Syracuse	NY	R. S Engelbrecht	Bell Labs	Holmdel	NJ
1971	R. R. Webster	Texas Instruments	Dallas	TX	J. A. Raper	General Electric	Syracuse	NY
1972	S. Triebwasser	IBM Research	Yorktown Heights	NY	R. R. Webster	Texas Instruments	Dallas	TX
1973	V. I. Johannes	Bell Labs	Holmdel	NJ	S. Triebwasser	IBM Research	Yorktown Heights	NY
1974	H. Sobol	Collins Radio	Dallas	TX	V. I. Johannes	Bell Labs	Holmdel	NJ
1975	W. D. Pricer	IBM	Essex Junction	VT	H. Sobol	Collins Radio	Dallas	TX
1976	J. H. Wuorinen	Bell Labs	Whippany	NJ	W. D. Pricer	IBM	Essex Junction	VT
1977	D. A. Hodges	Univ. of California	Berkeley	CA	J. H. Wuorinen	Bell Labs	Whippany	NJ
1978	J. D. Heightley	Sandia Labs	Albuquerque	NM	D. A. Hodges	Univ. of California	Berkeley	CA
1979	W. S. Kosonocky	RCA Labs	Princeton	NJ	J. D. Heightley	Sandia Labs	Albuquerque	NM
1980	J. D Plummer	Stanford Univ.	Stanford	CA	J. A. Raper	General Electric	Syracuse	NY
1981	B. A. Wooley	Bell Labs	Holmdel	NJ	J. A. Raper	General Electric	Syracuse	NY
1982	P. R. Gray	Univ. of California	Berkeley	CA	J. A. Raper	General Electric	Syracuse	NY
1983	L. M. Terman	IBM Research	Yorktown Heights	NY	J. A. Raper	General Electric	Syracuse	NY
1984	P. W. Verhofstadt	Fairchild uProc. Div.	Mountain View	CA	J. A. Raper	General Electric	Syracuse	NY
1985	H. J. Boll	Bell Labs	Murray Hill	NJ	J. A. Raper	General Electric	Syracuse	NY
1986	A. Grebene	Micro Linear Corp	San Jose	CA	J. A. Raper	General Electric	Syracuse	NY
1987	R. Baertsch	General Electric	Schenectady	NY	J. A. Raper	General Electric	Syracuse	NY
1988	W. Herndon	Fairchild Research Ctr.	Palo Alto	CA	W. D. Pricer	IBM	Essex Junction	VT
1989	H. E. Mussman	AT&T Bell Labs	Naperville	IL	W. D. Pricer	IBM	Essex Junction	VT
1990	C. W. Gwyn	Sandia Labs	Albuquerque	NM	W. D. Pricer	IBM	Essex Junction	VT
1991	J. T. Trnka	IBM	Rochester	MN	W. D. Pricer	IBM	Essex Junction	VT
1992	A. R. Shah	Texas Instruments	Dallas	TX	W. D. Pricer	IBM	Essex Junction	VT
1993	R. C. Jaeger	Auburn Univ.	Auburn	AL	W. D. Pricer	IBM	Essex Junction	VT
1994	D. Monticelli	National Semiconductor	Santa Clara	CA	W. D. Pricer	IBM	Essex Junction	VT
1995	T. Tredwell	Eastman Kodak	Rochester	NY	W. D. Pricer	IBM	Essex Junction	VT
1996	F. W. Hewlett	Sandia Labs	Albuquerque	NM	W. D. Pricer	IBM	Essex Junction	VT
1997	R. K. Hester	Texas Instruments	Dallas	TX	J. T Trnka	IBM	Rochester	MN
1998	J. Cressler	Auburn Univ.	Auburn	AL	J. T Trnka	IBM	Rochester	MN
1999	S. S. Taylor	Triquent Semiconductor	Hillsboro	OR	J. T Trnka	IBM	Rochester	MN
2000	R. Crisp	Rambus, Inc.	Mountain View	CA	J. T Trnka	IBM	Rochester	MN
2001	G. Gulak	Univ. of Toronto	Toronto	Canada	J. T Trnka	IBM	Rochester	MN
2002	W. Sansen	Katholieke Univ.	Leuven	Belgium	T. Tredwell	Eastman Kodak	Rochester	NY
2003	A. Chandrakasan	MIT	Cambridge	MA	T. Tredwell	Eastman Kodak	Rochester	NY

A History of the Far-East Program Committee at ISSCC

Takuo Sugano
Toyo University, Tokyo, Japan

Preliminary participation of non-US members in the ISSCC Program Committee was introduced at a very early stage with one or two participants from outside the USA; Then, in 1964, non-US membership was increased to eight in the ISSCC1965 Program Committee. However, no-one from the Far East was invited to join the Program Committee until 1966. In the 1967 Committee, two Japanese, H. Yanai and T. Sugano, joined the Program Committee, which included eight overseas members in all. This initiated the first participation in the Program Committee from the Far East. Later, T. Miwa and T. Sugano served the Program Committee as overseas members from the Far East in 1968 and 1969; then in 1970, the number of the overseas members from the Far East increased to three, the representatives being J. Nishizawa, M. Uenohara and T. Sugano.

As a culmination of this evolution, the Far-East Program Committee was established in 1970 as one of the Overseas Program Groups in the ISSCC1971 Program Committee, for which R.R. Webster was the General Chair, who presided over the US and Overseas Groups. The Overseas Groups were composed of the European Program Committee, the Far-East Program Committee, and the Israel-Canada-South America Program Committee.

The 1971 Far-East Program Committee consisted of 11, including 7 Japanese members and 4 others from Australia, Korea, Taiwan, and the USSR. T. Miwa kindly assisted me in organizing the Far-East Program Committee based on his experience as an overseas member of the ISSCC1968 and ISSCC1969 Program Committees. His assistance and collaboration was highly appreciated. From the beginnings of the Far-East Program Committee, the Chair was selected in a two-year rotation. The ISSCC2003 Far-East Program Committee, which is currently active, is the 33rd in this long history. A list of the successive Chairs and Secretaries of the Far-East Committee is provided below. Until now, all Chairs and Secretaries have come from Japan, but the membership has become more international than in 1971.

The Far-East Program Committee has grown in both its membership and in its activities related to ISSCC program assembly. For ISSCC2003, the Far-East Program Committee has 34 regular members, including the Chair, the Secretary and the Assistant Secretary, and 6 Liaison members, who are Japanese residing in California. Of the 34 regular members, 24 are from Japan, 7 from Korea, and 3 from Australia, China, and Taiwan, respectively.

The significant contributions of the Far-East Program Committee to the assembly of the ISSCC technical program are clearly seen from the remarkable increase of the number of presentations by Far-East authors, as illustrated on page S14. Until 1967, the contributions from the Far East to ISSCC were very limited, being zero or one each year, with exception in 1961, in which three papers related to applications of Esaki diodes and parametrons were presented by Japanese speakers. In ISSCC1972, that is one year after the establishment of the Far-East Program Committee, the number of presentations from the Far East jumped to 11, including a keynote address entitled "Solid-State Electronics in Public Telecommunication of Japan". Since then, contributions from the Far East have increased steadily: Although the number of papers accepted for presentation varies each year, the number of presentations has exceeded 50 at some of the recent ISSCCs. It must be noted, as well, that contributions from the Far East have become truly international, presently scientific and technological work from various Far-Eastern regions such as Hong Kong, India, Japan, Korea, Singapore, and Taiwan, have been presented. Since 1994, a keynote address has been regularly delivered by a speaker from the Far East at every ISSCC, directly reflecting the activity of the Far-East Program Committee, supported by the growth of the solid-state electronics industry, and the advancement of research on solid-state circuits in the Far East.

I would like to thank John Trnka, IBM, for offering me the opportunity to contribute this paper to the 50th-Anniversary Supplement, and for providing the list of the past Far-East Chairs and Secretaries. Many thanks, also must go to Dr. H. Watanabe and Dr. M. Fukuma, both at NEC, for their assistance in preparing this manuscript, by supplying materials related to the technical program, and papers from past ISSCCs since 1955.

Far East Chairs and Secretaries

Year	Chair	Affiliation	City	Country	Secretary	Affiliation	City	Country
1971	T Sugano	Univ. of Tokyo	Tokyo	Japan				
1972	T Sugano	Univ. of Tokyo	Tokyo	Japan	S Hamada	NTT	Tokyo	Japan
1973	S Hamada	NTT	Tokyo	Japan	H. Mukai	NTT	Tokyo	Japan
1974	S Hamada	NTT	Tokyo	Japan	K. Kataoka	NTT	Tokyo	Japan
1975-1976	Y. Tarui	Electrotechnical Lab	Tokyo	Japan	T. Sekigawa	Electrotechnical Lab	Tokyo	Japan
1977-1978	M. Uenohara	Nippon Elect Co	Kawasaki	Japan	K. Ayaki	Nippon Elect Co	Kawasaki	Japan
1979	M. Watanabe	NTT	Tokyo	Japan	K. Kataoka	NTT	Tokyo	Japan
1980	M. Watanabe	NTT	Tokyo	Japan	K. Kurumada	NTT	Tokyo	Japan
1981-1982	K. Kurokawa	Fujitsu	Kawasaki	Japan	H. Ishikawa	Fujitsu	Tokyo	Japan
1983-1984	M. Nagata	Hitachi CRL	Tokyo	Japan	M. Kubo	Hitachi CRL	Tokyo	Japan
1985-1986	Y. Takeishi	Toshiba	Kawasaki	Japan	Y. Nishi	Toshiba	Kawasaki	Japan
1987-1988	H. Sasaki	NEC	Kawasaki	Japan	A. Morino	NEC	Kawasaki	Japan
1989-1990	T. Sudo	NTT	Atsugi	Japan	S. Horiguchi	NTT	Atsugi	Japan
1991-1992	T. Nakano	Mitsubishi	Itami	Japan	O. Tomisawa	Mitsubishi	Itami	Japan
1993-1994	H. Ishikawa	Fujitsu	Atsugi	Japan	S. Hijiya	Fujitsu	Atsugi	Japan
1995-1996	G. Kano	Matsushita	Osaka	Japan	T. Baba	Matsushita	Osaka	Japan
1997-1998	M. Kubo	Hitachi	Tokyo	Japan	K. Shimohigashi	Hitachi CRL	Tokyo	Japan
1999-2000	Y. Unno	Toshiba	Yokohama-City	Japan	A. Kanuma	Toshiba	Kawasaki	Japan
2001-2002	H. Watanabe	NEC	Kawasaki	Japan	T. Arai	NEC	Kawasaki	Japan
2003	Y. Hagiwara	Sony	Atsugi	Japan	M. Katakura	Sony	Atsugi	Japan

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A History of the European Program Committee at ISSCC

Rudy Van de Plassche
past European Chair

Formal European involvement in ISSCC began in 1965, when Leo Tummers of Philips Research became a member of the US Program Committee, and the focal point for Europe. He continued in this role through 1967. In 1968, the European leadership was transferred to Jan van Vessem, who, along with Otto Folberth from Germany as secretary, formed the first formal European Program Committee. Van Vessem was acknowledged by the US Committee as the first European chair. This chairmanship in the early history of the European Committee was limited to 3 years. With time, the duration of the chair position's term was increased to a maximum of six years. In 2000, the ISSCC European Outstanding Paper Award was created and named for Jan Van Vessem, the first European Chair.

The early European Committees were comprised of between 10 and 15 members drawn from the larger European semiconductor manufacturers such as Philips, Thomson, Siemens, and CSEM. Over time, the committee has grown to its present size of approximately 30 members representing all regions of Europe, and including representation from many smaller companies as well as universities involved in semiconductor-related development. Correspondingly, over time, the number of submitted papers has grown from about 15 in the late 60s, to the current number of approximately 80. Acceptance rates have also increased to the current 50% level, comparable with both the North-American and Far-East acceptance rates. Clearly, the effort of the European Committee over the past 25 years has been a significant driver of the growth in European participation in ISSCC.

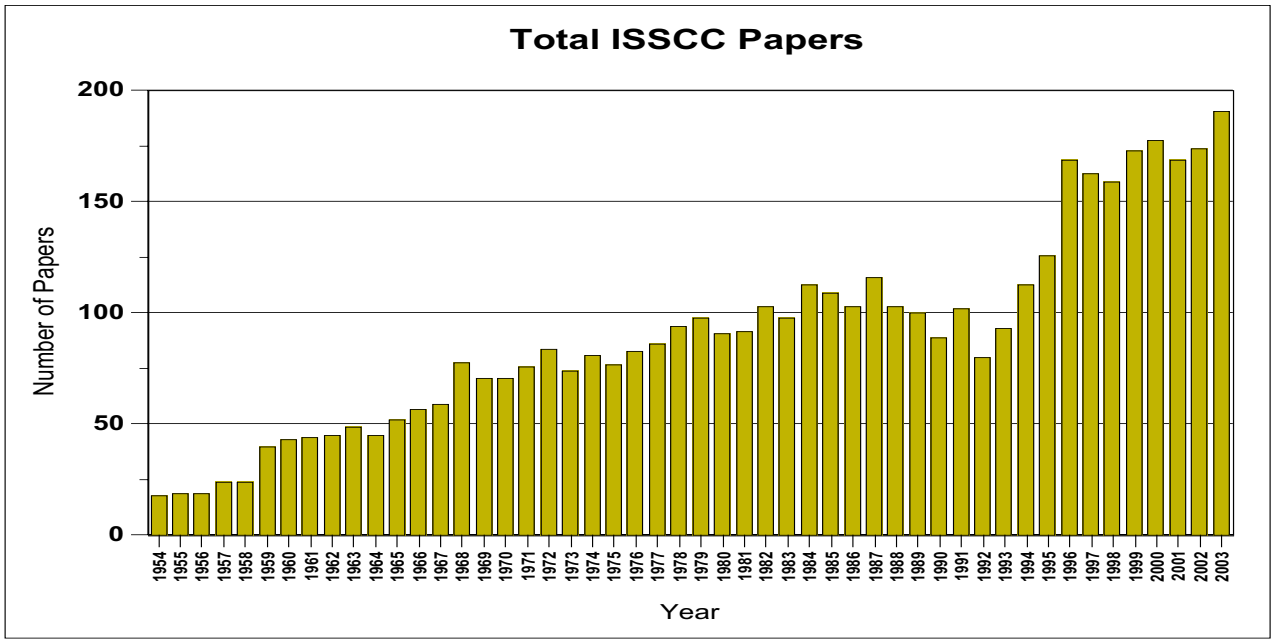
With the opening of Eastern Europe in the early 1990's, the European Committee under the leadership of Kurt Hoffman of Siemens was able to contact colleagues in Moscow, Russia, and arrange an exchange visit. As a result, Dr. Stanislaw Gariaino and Dr Boris K Pleshko visited Munich in the fall of 1990, and toured Germany and The Netherlands. Their passports were lost in Amsterdam, but thanks to Jan Lohstroh of the European Committee, they completed their tour and returned to Moscow. The exchange was very successful, and led to a Special Session on Technology in the USSR at ISSCC1991. The highlight of special session was a paper describing a Mini-Fab for low-volume production. This special session was a significant amount of work for the European Committee, as communications were at best difficult and sometimes impossible. Language difficulty and ISSCC paper-quality expectations drove a major paper-editing process. Following ISSCC1991, the spring European Program committee meeting was held in Zelenograd, close to Moscow, to complete the exchange. Unfortunately, it was not possible to sustain the formal linkage with Eastern Europe due to poor communications, travel expense, and quality of available papers.

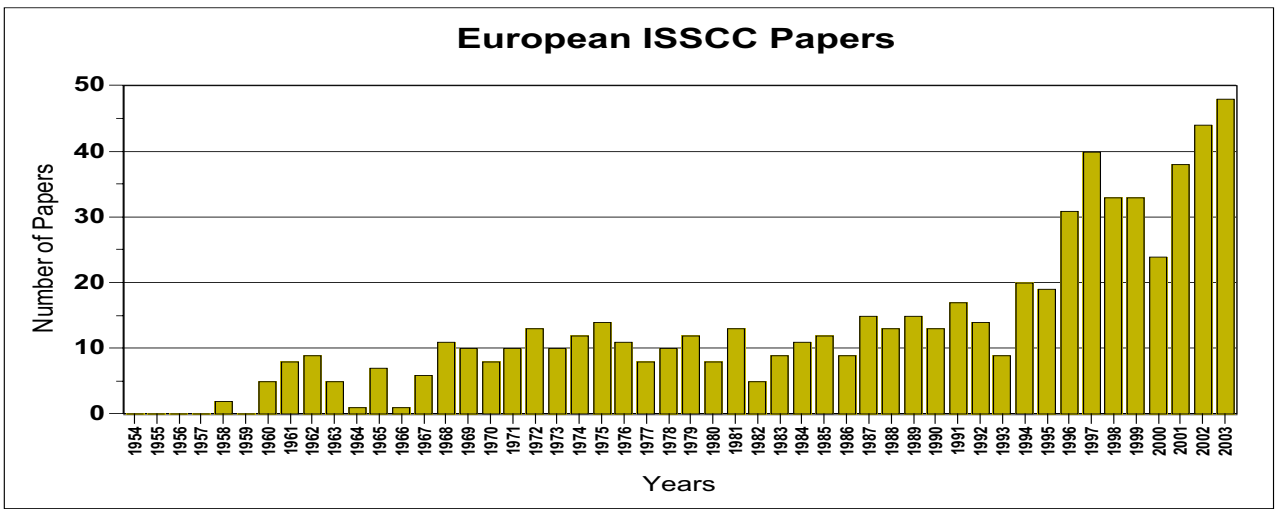
The following table provides a listing of the European Chairs and their affiliations during their tenure:

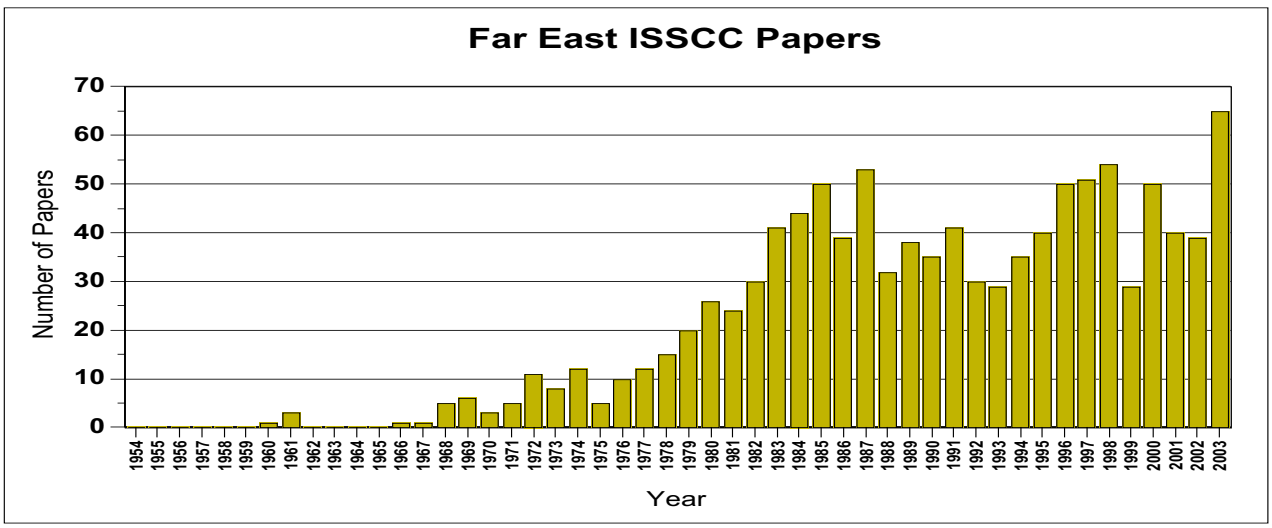
European Chairs and Secretaries

Year	Chair	Affiliation	City	Country	Secretary	Affiliation	City	Country
1971-1972	J. C. van Vessem	Philips	Nijmegen	The Netherlands	O. Folberth	IBM	Boeblingen	Germany
1973-1974	J. C. van Vessem	Philips	Nijmegen	The Netherlands	H. Ruechardt	Siemens	Munich	Germany
1975	O. Folberth	IBM	Boeblingen	Germany	H. Ruechardt	Siemens	Munich	Germany
1976	O. Folberth	IBM	Boeblingen	Germany	O. W. Memelink	Tech. Hogeschool Twente	Enschede	The Netherlands
1977-1978	N. C de Troye	Philips Research	Eindhoven	The Netherlands	S. S. Roy	Inter. Computers	Manchester	England
1979	N. C de Troye	Philips Research	Eindhoven	The Netherlands	W. Engl	Tech. Hochschule Aachen	Aachen	Germany
1980-1983	H. H. Berger	IBM	Boeblingen	Germany	P. Jespers	Katholieke Univ.	Louvain	Belgium
1984-1985	J. Borel	Thomson EFCIS	Grenoble	France	P. Schouter	Thomson-CSF	St. Egreve	France
1986-1988	J. Lohstroh	Philips Research	Eindhoven	The Netherlands	J. Danneels	Bell Telephone	Antwerp	Belgium
1989-1994	K. Hoffman	Univ. der Bundeswehr	Neubiberg	Germany	R. van de Plassche Research	Philips	Eindhoven	The Netherlands
1995-1996	R. van de Plassche	Philips Research	Eindhoven	The Netherlands	M. Degrauwe	CSEM	Neuchatel	Switzerland
1997-2000	R. van de Plassche	Philips Research	Eindhoven	The Netherlands	W. Sansen	Katholieke Univ.	Leuven	Belgium
2001-2002	R. van de Plassche	Philips Research	Eindhoven	The Netherlands	J. Sevenhans	Alcatel	Antwerpen	Belgium
2003	J. Sevenhans	Alcatel	Antwerpen	Belgium	A. Theuwissen	Philips Semicond.	Eindhoven	The Netherlands

History of Papers at ISSCC







Data Compiled by: John Trnka – Total ISSCC Papers, Albert Theuwissen – European ISSCC Papers, Takuo Sugano – Far East ISSCC Papers

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A Half-Century of Press Relations at ISSCC

Kenneth C. Smith
University of Toronto, Toronto, Canada

Preamble

Although the documentation of press-related activity at ISSCC over these 50 years is neither formal nor complete, there is a pervading sense, and some documentation, that the Press have played an important role. Far from the least- significant of the peripheral evidence of this fact is the very early attachment of Lewis Winner (radio-commentator/print-journalist) to the Conference. In fact, his initial (speculative) assignment was to issue a Digest of summaries of all papers, and to organize public relations, generally. Then, with the success of the Digest, and the Conference as a whole, Lew's role expanded to more than a full-time job by 1978. As sole proprietor of this one-man-band, he orchestrated, conducted, and implemented Conference activities until his death in 1988. The Press was one of his more important instruments.

Since the time of his death, upon which his many roles were divided amongst a host of individuals, press relations was put in the hands of two others in succession, first of Jack Raper, from 1988 to 1993, and now, beginning in 1994, of Kenneth C. Smith, with the invaluable assistance of Laura Fujino for a long time, but most intensely since 1997.

While the obvious explicit role of ISSCC's Press-Relations activity has been to interest and inform members of the Press, who in turn would inform the technical and general public, there is some implicit sense that it was also intended as a means to less-direct other ends. Certainly these days, and for the last ten years, the strategy has been to target less-technical management through the influence of the financial Press. For it is such upper management who exert financial control over the essential life-line to ISSCC's success - the participation of volunteers, of authors, and of attendees - all of which depends on a positive corporate (financial) attitude. Thus, our goal has been to convince management that, even in hard times, ISSCC is where the action is, will be foretold, and will be demonstrated; In short, if informed early action leads to success, then ISSCC is where to invest!

The Very Early Years

Prior to 1958, there is little explicit evidence of Press-related activity associated with what was then known as the Transistor Conference. Its origins in a workshop whose intent was to facilitate technical-information exchange unfettered by corporate/legal restrictions, doubtless led to an ambivalence about publicity. However, the early growth rate of the meeting, from an attendance of 600+ in 1954 to 3300 in 1960, for example, provides evidence of an effective means of information distribution. But, at first, this was likely less formal, within the few corporations involved, and amongst their technical friends, all of whom were eager to obtain any available information, as interest in semiconductor circuits surged. As well, it was in 1957, when a recognition of the value of "openness" was demonstrated by the creation of the "Conference Record of Figures and Diagrams", that more-public promotion began, (see page S21).

Highlights of Press/Publicity Activity over the Latter Years

(With timescale set by reference to the associated Conference year):

1958 Lewis Winner is retained on speculation as publicist and Digest publisher
1958 A Press Room is set up in Houston Hall at the University of Pennsylvania, with two phones (at a cost of $11)
1958 A Press luncheon at the Conference is initiated
1959 Lewis Winner accepts a permanent role at ISSCC (along with his corresponding roles at other Conferences)
1960 Mass mailing of 32,000 copies of pre-Conference publicity
1961 First Pre-Conference Press Luncheon held at Sardi's
1962 Conference announcements in English and German mailed to 123 journals
1964 At the New York Pre-Conference Press Luncheon at Sardi's, 5 publications agree to preview the entire (advance) program
1965 Lew Winner identifies 63 columns of post-Conference reporting by in the Press
1966 Voice of America requests, and is given, a list of overseas speakers
1967 "Electronic Design", and "Microwave" are allowed to view (but not copy) galley proofs of the Digest, to assist them in planning post-Conference publications
1967 The at-Conference Press Luncheon has grown to become a recognition luncheon for overseas speakers and award winners
1967 Use of cameras and tape recorders at the Evening Sessions becomes a big issue, resulting in a clamp-down
1971 Pre-publication becomes an acute problem with 3 or 4 papers apparently leaked to the Press prior to the Conference
1972 First-time appearance of Swedish press at the Conference (from "Electronick", Stockholm)
1973 "Electronic News" provides a 4-page report
1976 "Electronics" plans a 5-page post-Conference article
1978 Beatrice Winner, Lew's wife, traditionally in charge of Digest accuracy, passes on in 1977
1980 Lew Winner shows a 90-page scrapbook of Press clippings at the closing Executive-Committee meeting
1984 "Electronic Design" coverage runs to 23 pages
1985 Lew Winner participates in a telephone interview from London with the London Times
1988 Lew Winner passes on before the New York Pre-Conference Press-Review meeting; Jack Raper takes over the Press-Relations task
1990 In response to requests by the Press, the Pre-Conference Press Meeting is moved from the first Thursday of January to early in the first week of December
1989 A second Pre-Conference Press Meeting is inaugurated in San Francisco
1993 The last Pre-Conference Press Meeting is held at Sardi's
1993 Jack Raper retires as Press-Relations Chair, KC Smith takes over
1994 A formal bound book, the "Press Kit", is inaugurated. It has 120 pages, with the Advance Program as a back-cover insert.
1995 A Far-East Press Conference is inaugurated in Tokyo in early November
1995 The west-coast (San Francisco) Pre-Conference Press Meeting is moved to San Jose for one year due to a conference-timing conflict for regular Press attendees. In 1996, the west-coast Pre-Conference Press meeting is replaced for this and subsequent years, by a series of pre-arranged visits to Press in the San Francisco and the Bay area.
1997 The "Press Gallery", a display of ISSCC-related publications from around the world, is inaugurated. Located in the hallway leading to the Ballrooms at the San Francisco Marriott Hotel, it is intended to show attendees the breadth of world interest in ISSCC. Its concentration is both on publications following the previous Conference, as well as those appearing before and during the current one. Some material from even earlier Conferences is also presented.
2002 A CD including the Press Kit and Advance Program is inaugurated
2003 A Korean Press Conference is begun in Seoul in early November

Final Reflections of 50 Years

The Press have been, and continue to be, an important part of the Conference's success. Their influence has certainly contributed positively to the universal feeling of ISSCC's importance to the solid-state industry, and the cognate creativity it supports. Without the influence of the Press, a great many important individuals, both technical and financial, would be far less informed!

50 Years of Analog Development at ISSCC

David Robertson
Analog Devices

Disclaimer: The task of compressing 50 years of "Analog History of ISSCC" into a few pages is an impossible one; In fact, this writer would not even claim to present a definitive "Best of ISSCC" list. Instead, what is provided here is a selection of highlights and historical trends from ISSCC, the Conference that has become one of the showcases of analog IC innovation. Avid historians are referred to Paul Brokaw's article in the 40th-Anniversary Commemorative Supplement [26] for a more comprehensive treatment (all of the papers Paul cites are included in the list here). Of course, one of the most entertaining ways of following the history of innovation at the Conference is to read the papers themselves. With these apologies offered up front, let us take a quick tour through 5 decades of analog papers at ISSCC.

The Early Years (no pun intended): transistors, not tubes.
Over the first several years both the name and the content of the Conference evolved. Electronic circuits of the day were dominated by vacuum tubes, and the papers in the early Conferences often focused on the different characteristics of the solid-state devices – chiefly junction transistors, junction diodes, and tunnel diodes. In many cases, the authors of these papers have lent their names to fundamental elements of today's analog transistors and models: J.M. Early, J.J. Ebers, and J.L Moll (all from Bell Labs) are just a few examples. Generally speaking, the "analog" circuit functions of amplification and oscillation were the subject exploration and demonstration.

The 1960s: Linear Monolithic Circuits — op amps, references, and regulators.
Through the second decade of the Conference, analog papers reflected the technology's increasing level of analog integration, and the emergence of circuits that sought to exploit the different properties of solid-state devices, including large but non-linear gain. The great working example is the operational amplifier, and papers through the 1960s reflected the advancement of its art, while introducing many circuits and principles that continue to dominate today [4, 5]. The phase-locked loop, introduced by Grebene in [23], is another important case. Signal-processing circuits built explicitly on the exponential characteristics of the bipolar transistor also emerged [22], while other fundamentals were exploited to produce temperature-stable voltages based on intrinsic principles of the transistors [1,2]. Again, for their work at the time, names of authors such as Widlar, Wilson, and Gilbert were branded into the analog IC lexicon in association with unique circuits.

The 1970s: A/D and D/A converters, the emergence of analog LSI.
Integration pushed the technology in many ways — the growth of digital signal processing, enabled by digital integration, created the demand for Analog-to-Digital and Digital-to-Analog converters to connect emerging new processors to real-world signals. The converters themselves tended to drive the state of the art in linear integration, and pushed the envelope at the transistor, circuit, and architecture levels [9,10,11,12,13,14]. The digital world was inherently discrete-time, but discrete time and switching techniques were extensively explored as well in the analog world in the 1970s. Old dogs — like op amps and filters —learned new tricks, in the form of chopper-stabilized amplifiers [7] and switched-capacitor implementations of analog filters [24].

The 1980s: Rapid growth of Analog CMOS, oversampling, and calibration — the push for dynamic range.
The trend toward higher levels integration continued through the 1980s, and "high-performance IC's" began to move from the expensive instrument and aerospace world into the consumer mainstream (where digital audio was one prevalent example). Analog papers at ISSCC were pushing to increasing levels of dynamic range to economically support these applications. In this process, the analog process technologies shifted from pure bipolar to BiCMOS and even CMOS, bringing significant digital content onto the analog chips, leading to "mixed signal" ICs. Digital functionality was applied to the classic analog problem of matching, leading to presentation of self-calibrated architectures and oversampled sigma-delta converters [15, 16, 17, 18,19, 20]. CMOS implementations of analog functions opened the door to integration of analog blocks, particularly converters, onto large predominantly-digital chips. Circuit innovation also continued at a rapid pace, in many cases involving new circuit configurations to deal with the constraints of CMOS transistors and more-"digital" processes.

The 1990s: Faster speeds, shrinking lithographies, shrinking voltages —analog moves to VLSI.
As data-communications applications became one of the technology drivers, the 1990s saw an increasing emphasis on high speeds and greater bandwidths. Process technologies advanced into the sub-micron and deep-sub-micron range, providing speed and integration benefits, but also providing new challenges for analog, in the form of lower supply voltages. Analog innovations were often coming in the form of new architectures, and circuit purists would observe that block diagrams outnumbered circuit schematics in many of the analog papers. With demand for both analog and digital signal processing expanding wildly, however, there was plenty of new development in both dimensions to follow.

Conclusion
These few paragraphs cannot possibly do justice to the river of innovation that ISSCC has chronicled over 50 years, and it is too soon to select "classics" from the 1990s. Inspecting the papers referenced by this year's Conference submissions, in addition to the list provided below, provides just a starting point.

Annotated Bibliography: (References grouped by circuit type, in chronological order)

References and Regulators
[1] D.F. Hilbiber (Fairchild Semiconductor), "A New Semiconductor Voltage Standard," *ISSCC Digest of Technical Papers*, pp. 32-33, February 1964. [Although this circuit was crude and not suitable for integration, it pointed out the analytical roots of important biasing and voltage-reference principles.]
[2] R.J. Widlar (National Semiconductor), "New Developments in IC Voltage Regulators," *ISSCC Digest of Technical Papers*, pp. 158-159, February 1970. [This paper demonstrated the bandgap reference principle in a complete monolithic and ready-for-use form.]

Amplifiers
[3] H.C. Lin, M.J. Geisler, K.K. Yu (Westinghouse), "A Unipolar-Bipolar Transistor Configuration for Integrated Audio Amplifiers," *ISSCC Digest of Technical Papers*, pp. 100-101, February 1963. [This circuit marks the appearance at the Conference of monolithic circuits combining FETs along with Bipolars.]
[4] G.R. Wilson (Tektronix), "A Monolithic Junction FET-NPN Operational Amplifier," *ISSCC Digest of Technical Papers*, pp. 20-21, February 1968.

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[This paper shows the process-compatible FET in a more ambitious circuit.]
[5] R.J. Widlar (National Semiconductor), "New Approaches for the Design of Monolithic Operational Amplifiers," *ISSCC Digest of Technical Papers*, pp. 10-11, February 1969. [Although some of the content of this invited paper had prior exposure, it serves as an example of the fundamental contributions of its author.]
[6] R.B. Poujois, D, Baylac, J.M. Ittel Barbier (LETI), "Low-Level MOS Transistor Amplifier using Storage Techniques," *ISSCC Digest of Technical Papers*, pp. 152-153, February 1973. [In this paper, switches and MOS capacitors in an MOS process were used to implement a chopper-stabilized amplifier.]
[7] R.W. Russell, D.D. Culmer (National Semiconductor), "Ion-Implanted JFET-Bipolar Monolithic Analog Circuits," *ISSCC Digest of Technical Papers*, pp. 140-141, February 1974. [Here, the processing catches up to the circuit with a circuit that sparked a proliferation of "Bi-FET' circuits.]

A/D and D/A Converters

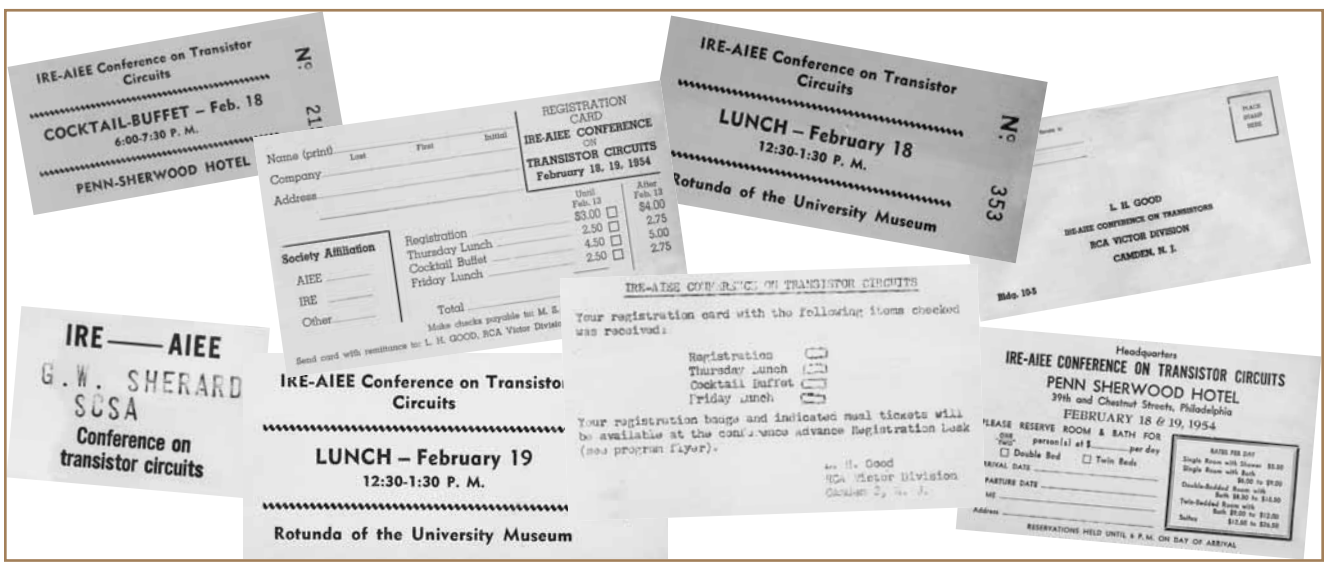
[8] M.B. Rudin, R. O'Day, R. Jenkins (Fairchild Semiconductor), "System/Circuit Device Considerations in the Design and Development of a D/A and A/D Integrated Circuits Family," *ISSCC Digest of Technical Papers*, pp. 16-17, February 1967. [This paper is a good example of the subsystem levels of integration at its time, and also shows the state of DAC technology then.]
[9] J.J. Pastoriza, H. Krabbe, A.A. Molinari (Analog Devices), "A High-Performance Monolithic D/A Converter Circuit," *ISSCC Digest of Technical Papers*, pp. 122-123, February 1970. [The combination of binary currents from equalized-current-density devices, combined with replica biasing introduced in this paper, became the canonical form for bipolar DACs.]
[10] R.E. Suarez, P.R. Gray, D.A. Hodges (UC Berkeley), "An All-MOS Charge-Redistribution D/A Conversion Technique," *ISSCC Digest of Technical Papers*, pp. 194-195, February 1974. [A switched-capacitor scheme using charge as the analog signal was introduced in this paper.]
[11] A. G. E. Dingwall, B. D. Rosenthal (RCA), "Low-Power Monolithic COS/MOS dual-slope 11-bit A/D Converter," *ISSCC Digest of Technical Papers*, pp. 146-147, February 1976. [This paper presents early monolithic CMOS ADC.]
[12] R. J. van de Plassche (Philips), "Dynamic Element Matching for High-Accuracy Monolithic D/A Converters," *ISSCC Digest of Technical Papers*, pp. 148-149, February 1976. [This paper introduced dynamic element matching in a data converter.]
[13] R. H. McCharles, V. A. Saletore, W. C. Black Jr., D. A. Hodges (UC Berkeley), "An Algorithmic Analog-to-Digital Converter," *ISSCC Digest of Technical Papers*, pp. 96-97, February 1977. [This paper presents an early switched-capacitor ADC.]
[14] J.G. Peterson (TRW), "A Monolithic, Fully Parallel, 8b A/D Converter," *ISSCC Digest of Technical Papers*, pp. 128-129, February 1979. [This paper presents an early "high-speed" monolithic ADC.]
[15] H. Lee, D. A. Hodges, P. R. Gray (UC Berkeley), "A Self Calibrating 12b 12µs CMOS ADC," *ISSCC Digest of Technical Papers*, pp. 64-65, February 1984. [This paper presents an early demonstration of self-calibration.]
[16] M.W. Hauser, P.J. Hurst, R.W. Brodersen (UC Berkeley), "MOS ADC-Filter Combination That Does Not Require Precision Analog Components," *ISSCC Digest of Technical Papers*, pp. 80-81, February 1985. [The oversampling 1b converter architecture that proved so useful is first described at ISSCC.]
[17] A. G. F. Dingwall, V. Zazzu (RCA), "An 8MHz 8b CMOS Subranging ADC," *ISSCC Digest of Technical Papers*, pp. 72-73, February 1985. [One of the first high-speed CMOS ADCs that was not a flash architecture. It may not be a stretch to say it heralded the age of high-speed, high-resolution (>6 bits) CMOS ADCs.]
[18] T. Hayashi, Y. Inabe, K. Uchimura, T. Kimura (NTT), "A Multistage Delta-Sigma Modulator without Double Integration Loop," *ISSCC Digest of Technical Papers*, pp. 182-183, February 1986. [First cascaded ("MASH") sigma-delta modulator.]
[19] S. H. Lewis, P. R. Gray (UC Berkeley), "A Pipelined 5MHz 9b ADC," *ISSCC Digest of Technical Papers*, pp. 210-211, February 1987. [A benchmark early pipelined ADC paper.]
[20] B. DelSignore, D. Kerth, N. Sooch, E. Swanson (Crystal Semiconductor), "A Monolithic 20b Delta-Sigma A/D Converter ," *ISSCC Digest of Technical Papers*, pp. 170-171, February 1990. [This paper pushes the frontier of precision using a non-precision process technology.]
[21] R. Adams, K.Q. Nguyen, K. Sweetland (Analog Devices), "A 113-dB SNR Oversampling DAC with Segmented Noise-Shaped Scrambling," *ISSCC Digest of Technical Papers*, pp. 62-63, February 1998. [Representative of an emerging use of oversampling techniques for shifting element-mismatch errors into "harmless" parts of the frequency spectrum.]

Analog Signal Processing: Filters, PLLs, Mixers, etc.

[22] B. Gilbert (Tektronix), "A DC-500MHz Amplifier/Multiplier Principle," *ISSCC Digest of Technical Papers*, pp. 114-115, February 1968. [Two powerful techniques outlined in this paper led to new types of circuits and applications, and pointed the way to a unifying principle that clarified many other issues.]
[23] A.B. Grebene, H.R. Camenzind (Signetics), "Phase Locking As A New Approach For Tuned Integrated Circuits," *ISSCC Digest of Technical Papers*, pp. 100-101, February 1969. [This paper described a circuit that opened up many applications and inspired new IC designs.]
[24] I.A. Young, D.A. Hodges, P.R. Gray (UC Berkeley), "Analog NMOS Sampled-Data Recursive Filter," *ISSCC Digest of Technical Papers*, pp. 156-157, February 1977. [An analog filter realization separates normalized frequency characteristic from frequency-determining elements.]
[25] T. C. Choi, R. T. Kaneshiro, R. Brodersen, P. R. Gray, W. Jett, and M. Wilcox (UC Berkeley), "High frequency CMOS Switched Capacitor Filters for Communication Applications," *ISSCC Digest of Technical Papers*, pp. 246-247, February 1983. [This paper introduced the folded-cascode OTA.]

40-Year Retrospective

[26] A. Paul Brokaw, "Analog at ISSCC: Selections From the First 40 Years," *Commemorative Supplement to the Digest of Technical Papers*, pp. 27-47, February 1993. [A more detailed examination of the analog history of the first 40 years of the Conference]



Memorabilia from the first Conference.

50 Years of Communication Circuits at ISSCC

Thomas H. Lee, Stanford University
Paul C. Davis, Consultant

Fifty years ago, the young semiconductor industry was preoccupied with understanding basic physics, inventing new devices, and developing practical manufacturing techniques. Application progress was rapid, due in part to the spreading of information at ISSCC. Communication applications showed up early in the form of a paper from the 1955 Conference by C. C. Bopp, "Transistor Transmitter-Receiver Unit" [1], describing a 24Mc/s (megahertz didn't exist yet) transceiver with surface-barrier and point-contact transistors. Alloy transistors coexisted and competed with such devices for a time in the 1950s, but all three technologies lost out to the planar process, and are simply historical curiosities now.

Transistors have also competed with diodes for use in active communications circuits. Parametric amplification (discovered accidentally in the mid-1940s) transfers power to a signal from an oscillator, rather than from a DC source. The noise figures are potentially excellent because a pure (although nonlinear) diode-junction reactance mediates the power transfer. At the time, only the unwieldy maser evinced lower noise. The 1959 paper by R. S. Engelbrecht, "Nonlinear-Reactance (Parametric) Traveling-Wave Amplifiers for UHF" [2], shows how to build "paramps". This technique uses W. S. Percival's distributed amplifier concept from the 1930s to achieve bandwidths above 500MHz without a transistor in sight!

Another amplifying diode was also the product of chance "and the prepared mind". While troubleshooting problems with Sony's new 2T7 transistor, Leo Esaki discovered the negative resistance associated with tunneling in heavily-doped junctions. He first published his findings in early 1958, and the huge number of tunnel-diode papers at the 1960 ISSCC speaks to the excitement generated by his discovery. An overview by G. C. Dacey precedes a report of 3GHz oscillations in tunnel-diode circuits by M. E. Hines and W. W. Anderson [4]. Because it was hard to obtain unilateral operation, and because conventional devices kept improving, interest in the diodes had faded by the time Esaki won his Nobel Prize in 1973.

Interest in tunnel diodes was so intense in 1960 that ISSCC attendees may have failed to notice a paper by H. Norman, J. Last and I. Haas of Fairchild, "Solid-State Micrologic Elements" [5], which described the first digital ICs built in the new silicon planar process. Three years later, the company would use that process to build the first IC characterized specifically for RF operation, the five-transistor, 100MHz μA703.

Diode-based high-frequency circuits continued to develop throughout the next couple of decades. Another negative-resistance device, anticipated theoretically in 1958, had its ISSCC debut in 1965 in "The Read Diode - An Avalanching Transit-Time, Negative-Resistance Oscillator", by C. A. Lee, R. L. Batdorf, W. Wiegmann, and G. Kaminsky [6], with reports of oscillations in the 100-200MHz frequency range using a simple circuit. Avalanche-mode diodes progressed to supplying 10 dB of gain at millimeter wave frequencies by 1974 (H. Hayashi, F. Iwai, T. Fujita, M. Akaike, H. Kato, "80GHz IMPATT Amplifier" [7]).

Supplementing avalanche-mode and tunnel diodes are those using the transferred-electron mechanism. The Gunn diode in the 4GHz oscillator described in 1967 (T. Ikoma and H. Yanai, "Effect of External Circuits on Gunn Oscillation" [8]), produces less noise than avalanche-based devices such as the Read diode and its many cousins. Countless radar detectors used by "speed-conscious" automobile drivers employ Gunn oscillators.

The telephone industry that gave birth to transistors had to wait a decade or so for its off-spring to mature to usefulness in that domain. The very first transatlantic telephone cable (TAT-1, which carried 36 voice channels), put into service in 1956, had been forced to use pentode vacuum tubes in their repeaters. It was not until 1963 that transistorized repeaters finally found their way into submarine telephony. Telstar, the first active communications satellite, took transatlantic communications out of the water and into space. Launched on July 10th, 1962, it employed semiconductor electronics throughout, including solar cells for power. Although suffering a premature death from high-energy particles (generated by an unfortunately-timed H-bomb test), Telstar captured the public imagination, and even inspired a song (Telstar, by the Tornadoes) that became an international hit.

The end of the 1960s saw the first integrated phase-locked loop, in bipolar technology (A. Grebene and H. Camenzind, "Phase Locking as a New Approach for Tuned Integrated Circuits" [9]). This achievement transformed the PLL from a piece of 1930s esoterica into so ubiquitous a building block that it is now difficult to identify a modern communications systems without one.

Although the PLL perfectly realizes the promise of high integration, other communications-circuit achievements up to the mid-1970s primarily involved new device types at low integration levels, or ICs that still required a large complement of external passive components.

Examples include the appearance of the MESFET at the 1972 ISSCC (W. Baechtold, "X and Ku Band Amplifiers with GaAs Schottky-Barrier FETs" [10]), a device which continues to dominate cell-phone power amplifiers to this day. A dual-gate MOSFET 50-to-76 MHz tunable RF amplifier followed a year later (K. E. Manchester, J. D. Macdougall, O. Tkal, T. W. Chu, "Monolithic Varactor Tuned RF Amplifier IC with Ion Implantation" [11]). Bipolar RF technology continued to march onward, too, as seen in the 7W output-power level reported in the 1975 paper by A. Presser, E. F. Belohoubek, and H. Belorek, "Recent Advances in Bipolar Power Amplifiers for the 3-5GHz Frequency Range" [12].

Starting in the mid- to late-1970s, increasing levels of integration finally began to have a significant influence on the communications art. This shift drove, and was driven by, a gradually-accelerating transition to digital communications, which had begun in earnest with inaugural T-1 service in 1962, and accelerated by the first packet-switched system, ARPANET, toward the end of the decade.

Prime evidence of this shifting landscape appears in a 1976 ISSCC paper (J. Tsividis, P. Gray, D. Hodges, J. Chacko, "An All-MOS Companded PCM Voice Encoder" [13]). Numerous integrated codecs were to follow in subsequent years. An integrated DTMF IC at the 1977 ISSCC (M. Callahan, C. Johnson, "Integrated Dual Tone Multi-Frequency Telephone Dialer" [14]) underscored the continuing importance of telephony. The 1970s was also the decade of the CB radio craze (usually ignored in scholarly research), as A. Dingwall's 1977 ISSCC paper reminds us ("Monolithic C2L/CMOS Frequency Synthesizer for CB" [15]). The popularity of CB radio serves as powerful testimony to the enduring nature of voice communications as a wireless "killer app", which was to find more structured expression in cellular-telephone systems, beginning with trial service in 1978 of an analog FM system in Chicago. Switched-capacitor filters also appeared at the 1977 ISSCC (I. Young, D.

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Hodges, P. Gray, "Analog NMOS Sampled-Data Recursive Filter" [16]), permitting the accurate realization of sophisticated transfer functions with MOS IC technology for the first time. Requiring only an accurate clock, SC filters are an ideal fit with inexpensive MOS technology, and share ubiquity with PLLs.

Perhaps not as glamorous, but just as essential and ubiquitous, are the interface circuits that must tolerate the hostile environment of outside telephone lines (Aull, et. al., 1981). These units evolved into the front-end of modern PC modems.

Moore's law continued to work its magic throughout the 1980s. Bipolar and NMOS IC technology met increasing competition from CMOS. A 24th-order echo canceler (E. Swanson, R. Starke, G. Gross, K. Olsen, C. Waldron, "A Fully Adaptive Transversal Canceler and Equalizer Chip" [18]) demonstrated both the power of the new technologies, and the continued importance of telephony.

Traditional microwave circuits became increasingly dissonant with the high transistor count of ICs that were then commonplace, and 1984 marked the first absence of a microwave-circuits session at ISSCC, as progress in that domain came to be reported in a separate conference.

But, fiber-optic systems grew in prominence around this time. The development in the early 1970s of fiber with under 20dB/km loss (now below 0.3dB/km) sounded the death knell for millimeter-waveguide systems. Initial deployment of land-based fiber systems was contemporaneous with the appearance of early cellular systems. A 1984 ISSCC paper (D. Ross, R. Paski, D. Ehrenberg, W. Eckton, S. Moyer, "A Regenerator Chip Set for High Speed Digital Transmission" [19]) describes a complete 300 Mb/s repeater system for the first transatlantic fiber cable, TAT-8, deployed in 1988 with a capacity of 40,000 voice channels.

Serial data links, both optical and wireline, continued to develop throughout the 1980s and 1990s, with rapid increases in data rates. In recognition of the importance of this area, a "Gigahertz Communications ICs" session first appeared at ISSCC in 1992 [20]. These activities initially overshadowed wireless communications systems somewhat. The unexpected and rapid increase in cellphone popularity finally began to draw attention back to wireless systems as the 1980s ended. "A GPS Receiver with Synthesized Local Oscillator" (R. Herman, C. Mason, H. Warren, R. Meier [21]) appeared at the 1989 ISSCC, followed in 1991 by "A Single-Chip VHF and UHF Receiver for Radio Paging" (G. Luff, R. Youell, J. Wilson, T. Richards, R. Pilaski [22]).

The cell phone's popularity was abetted by the lower costs accompanying higher integration of the analog RF and baseband functions, and in particular by the use of digital signal processors. By the mid-1990s, worldwide wireless activity focused on chips for second-generation digital-cell phone systems, as typified by the paper, "Highly-Integrated Transmitter RFIC with Monolithic Narrowband Tuning for Digital Cellular Handsets" (K. Negus, B. Koupal, J. Wholey, K. Carter, D. Millicker, C. Snapp, N. Marion [23]) from 1994's ISSCC, which also marked the first wireless-communications session. By 1995, several ISSCC papers were describing highly-integrated chips or chipsets for GSM cell phones (e.g., "A 2.7V to 4.5V Single-Chip GSM Transceiver RF Integrated Circuit" (T. Stetzler, I. Post, J. Havens, M. Koyama [24]).

Telecommunications grew explosively in the latter half of the 1990s. These developments are perhaps too recent for placement in proper historical context, but it seems safe to say that future retrospective articles will note efforts to use "digital" CMOS to perform RF as well as baseband functions, the growth of wireless LANs, optical networks with ever-higher bit rates (thanks to WDM and other technologies), and the evolution of cellular systems into more data-centric networks. It will be fun to revisit this article in ten or twenty years, and compare it with the real history of the intervening times.

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50 Years of Signal Processing at ISSCC

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Aeluros

The Field

The technical field of Signal Processing encompasses all forms of sampled-data manipulation where the data (or signal) has a physical origin, or destination. In the context of ISSCC, signal processing refers to solid-state circuits designed to process samples that may be in digital or analog format. Physical origins or destinations include mechanical (audio) and electromagnetic waves (either in conductors or in free space), such as for telephony, radio, imaging, or optical transmission.

The restriction to sampled data is an important one, and distinguishes signal processing from purely continous-time processing, as is performed by traditional analog circuits. While discrete time (or space) is of the essence, what characterizes signal processing at ISSCC is also the continuous real-time nature of the processing, as opposed to the matched process of data collection followed by off-line processing.

The Early Years

Definitions aside, signal processing has a long and distinguished history at the Conference. However, the pace of development has definitely quickened in the last 25 years. An early example of sampled-data (analog) processing was presented by Franks in 1960 [1], in a paper describing a sampled-data bandpass filtering process based on junction-diode switching.

Development of signal-processing circuits began to accelerate in the 1970s. Significant milestones in analog and digital sampled-data-processing are exemplified by the papers on CCD circuits [2], and the first integrated digital filter [3]. The sampled-analog CCD technique was used in what was perhaps the first dedicated implementation of the Discrete Fourier Transform [4]. The most significant advantage of CCD and switched-capacitor [5] circuits was that no analog-to-digital conversion was needed for the signals. However, the increased effort required to obtain a robust design of ever-more-complex analog sampled-data circuits resulted in a market opportunity for digital solutions.

Simultaneous progress in the area of A/D and D/A data-conversion circuits permitted the use of highly-integrated digital signal-processing functions in an economical manner. In particular, the early 1980s saw the first examples of programmable DSP circuits [6,7,8]. The VLSI era also introduced the first examples of complex hard-wired or dedicated DSP functions [9] on a chip. With increasingly-complex numerical algorithms, ease of programming was provided by DSPs that used floating-point rather than fixed-point instruction sets [10].

The More-Recent Era

Since the mid 1980s, both analog and digital signal processing were strongly affected by a change from NMOS and bipolar/BiMOS to CMOS technology. This allowed a succession of new application areas, such as speech synthesis and coding/decoding [11,12,13], speech recognition [14], and image processing [15,16,17]. At the same time, although more slowly, "digital" CMOS was being adopted for the fabrication of analog signal-processing functions.

By exploiting the progress of CMOS developed for microprocessors, digital signal processing benefited from higher design densities and lower operating voltages and lower power consumption. In the 1990s, there was rapid development of DSP circuits for video encoding/compression, as an alternative to general-purpose image processing. The earliest example of a dedicated MPEG encoder with motion estimation was presented in 1993 [18]. Such video directed circuits were at the forefront of DSP complexity, with designs increasing in size from one million to several tens of millions of transistors by the end of the decade.

The clock-speed leaders of the 1990s were circuits for the read channels of magnetic-storage devices. The trend was toward integrated mixed-signal designs that included both analog and digital signal processing. Early examples of CMOS read-channel implementations were presented in 1993 [19,20]. Analog signal processing continued to develop in co-existance with digital logic in low-voltage digital CMOS processes. All the while, there was a ongoing contest between analog and digital proponents to produce the highest speed and lowest power solution.

The second half of the decade was marked by increased interest in mobile and broadband communications, both wireline and wireless. Programmable DSPs were extensively specialized for digital cellular phones [21,22], and the development of cable modems and DSL modems created several new types of dedicated communications DSPs[23]. Gigabit Ethernet and broadband wireless likewise required dedicated DSP hardware [24]. The popularity of mobile devices also ushered in a new age of energy awareness, where power efficiency became a primary system goal to be attained through a combination of technological, design, and algorithmic changes [23,25,26]. This field had already existed for 20 years hidden in the niche occupied by micropower wrist-watch circuits, but was now being developed for a much broader range of applications.

Conclusions

Overall, the history of solid-state signal processing has been marked by the parallel development of increasingly-complex programmable and dedicated DSP circuits. The trend continues to this day, with the programmable processors increasing in performance, and assuming processing functions that required dedicated hardware only a few years earlier. Dedicated DSPs, in turn, are being developed for a succession of new application areas, ones that proved out of reach of the programmable processors, whether for speed or power-consumption reasons.

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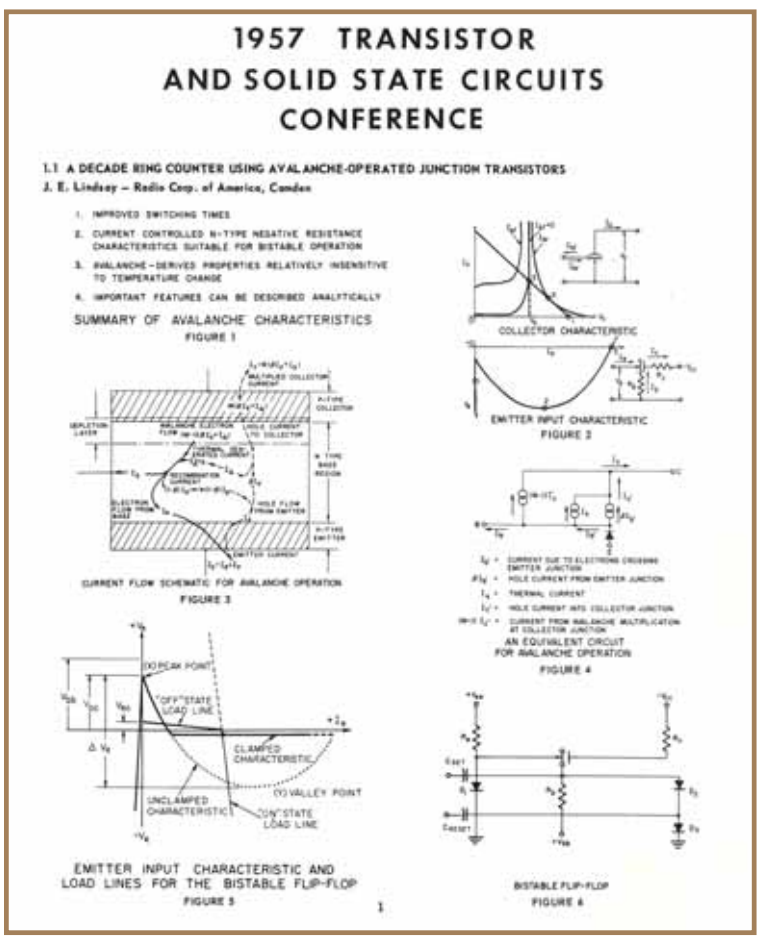

1957 TRANSISTOR
AND SOLID STATE CIRCUITS
CONFERENCE

1.1 A DECADE RING COUNTER USING AVALANCHE-OPERATED JUNCTION TRANSISTORS
J. E. Lindsay – Radio Corp. of America, Camden

1. IMPROVED SWITCHING TIMES
2. CURRENT CONTROLLED N-TYPE NEGATIVE RESISTANCE CHARACTERISTICS SUITABLE FOR BISTABLE OPERATION
3. AVALANCHE-DERIVED PROPERTIES RELATIVELY INSENSITIVE TO TEMPERATURE CHANGE
4. IMPORTANT FEATURES CAN BE DESCRIBED ANALYTICALLY

SUMMARY OF AVALANCHE CHARACTERISTICS
FIGURE 1

COLLECTOR CHARACTERISTIC
EMITTER INPUT CHARACTERISTIC
FIGURE 2

CURRENT FLOW SCHEMATIC FOR AVALANCHE OPERATION
FIGURE 3

AN EQUIVALENT CIRCUIT FOR AVALANCHE OPERATION
FIGURE 4

EMITTER INPUT CHARACTERISTIC AND LOAD LINES FOR THE BISTABLE FLIP-FLOP
FIGURE 5

BISTABLE FLIP-FLOP
FIGURE 6

1

This 1957 "Technical Addendum to the Program Booklet" was the forerunner of the "ISSCC Digest of Technical Papers".

50 Years of Digital Logic and Microprocessors at ISSCC

Ian Young
Intel

The first Conference leading to what we now know as ISSCC was held in 1954, with a session devoted to "Transistor Switching Circuits". Generally speaking, in the early years of the Conference, authors developed understanding of the operation of the transistor, and presented logic circuits based on either bipolar or FET devices. Bipolar-transistor logic-circuit families began to evolve with the introduction of direct-coupled transistor logic by Harris [1]. The original logic had low noise margin, and it exhibited a tendency to current-robbing which degraded its speed. So resistors were inserted in series with the base and collector, trading off some speed for adequate noise margin. In 1957, the fast-switching, but high-power-consuming, ECL logic family was first presented by Yourke [2]. At that time, it broke the nanosecond barrier with its current switching technique that did not allow the bipolar transistor to saturate. Initially used in mainframe computers and digital transmission circuits, it is still applied today to achieve the highest-speed logic.

The first description at ISSCC of a real integrated circuit was of a logic system by Wallmark et al [3] using direct-coupled J-FET transistors that formed a switch-based logic. The following year, Norman et al [4] identified that the real benefit of transistor integration was that it enabled basic logic elements to achieve high speed. They created the first successful integrated circuits using direct-coupled bipolar transistor logic. Eventually, in 1962, the widely-adopted all-transistor bipolar TTL was presented in the paper by Beeson and Ruegg [5]. TTL introduced the "totem-pole" push-pull output, operated from a single power supply, and enabled higher scales of integration. Tarui et al added the Schottky diode clamp to TTL to attain higher speed [7]. By this time, designers needed a more accurate bipolar-transistor model for effective high-speed-circuit design. The need was met with the Gummel-Poon high-level-injection bipolar model [8]. Presented in 1970, it is still the primary bipolar model used in circuit simulation today.

In 1963, CMOS logic technology was announced at the Conference by Wanlass and Sah [6]. It provided the advantages of low power and robust operation, and held out the promise of high levels of integration. However, CMOS presented manufacturing challenges, and it took almost two decades for CMOS technology to arrive in high production and become the mainstream logic technology it is today. In the meantime, circuit designers used the higher-power single-channel PMOS logic in mainstream applications like registers and calculators.

In the early 1970s, integration had arrived at the level where multiple functional blocks could be integrated on a single chip. The invention of the single-chip general-purpose CPU occurred in 1974, when NMOS gate-stability problems were solved. As described by Shima et al [8], manufacturing shifted to NMOS logic for an 8-bit microprocessor [9] called the 8080, and the PC industry was launched. The lower power-delay product of NMOS static logic in this microprocessor enabled the integration of more logic functions, and thus increased the CPU performance over an all-PMOS implementation. Logic using single-channel NMOS technology continued to evolve from static logic to clocked dynamic logic for lower power and increased logic density. In 1981, the first 32b microprocessor [10] was implemented with CMOS technology. It introduced glitch-free domino dynamic logic which provided higher layout density and much-higher speed. Domino logic is still being implemented in microprocessor designs today.

With logic integration and transistor speed continuing their rapid increase, microcomputer designers focused on clock frequency for increased performance. The resulting RISC computer architecture [11], [12], created by research groups at Berkeley and Stanford, increased clock frequency significantly by using a small streamlined instruction set, executing in a synchronous pipeline with reduced control-logic complexity. By the time RISC microprocessors were in commercial applications, they had added on-chip Cache [15].

By, 1987, even though much of the attention of VLSI designers was focused on the higher level of functional-block integration, transistor-logic and circuit-design innovation continued. The circuit-design and micro-architecture push to higher frequency, along with process-technology line-width reduction, meant that the propagation delay of the on-chip interconnect started to become a major factor in determining performance in VLSI circuits. Bakoglu and Meindl [13] showed the benefit of interconnect repeaters in reducing the effect of interconnect RC delay. The cascoding of differential pairs of NMOS devices was proposed by Heller and Griffin [14] to achieve higher speed and improved layout density with its all-NMOS switching and differential output signaling. With increasing transistor integration, the microprocessor chip-to-chip I/O setup and hold timing was degraded by the large on-chip clock-buffer delay. This was becoming a functional limitation. So, Johnson and Hudson [16] integrated an analog delay-locked loop to compensate for the on-chip clock-buffer delay.

The first microprocessor to exceed 100MHz was a CISC processor presented in 1991 [17], with an on-chip floating-point unit and cache memory. In addition to the transistor- and circuit-design improvements, it used a triple-metal process to gain performance from high circuit-packing density. This processor integrated a Phase-Locked Loop [18] on-chip to mitigate clock-buffer delay, and to improve I/O timing. This PLL also enabled the synthesis of processor frequencies that could increase above the system clock rate, so that processor performance could scale with process technology and circuit-design improvements. To improve the I/O bandwidth of ASIC busses, Gunning et al. [19] proposed low-swing I/O driver and receiver circuits for multi-drop I/O terminated transmission lines. This technique later became widely used for microprocessor front-side busses.

The pace of microprocessor-frequency escalation through the 1990s did not slow down, but rather, it accelerated. A 200MHz 64b RISC microprocessor, capable of issuing two instructions per clock cycle, was presented by Dobberpuhl et al in 1992 [20]. This processor demonstrated the benefit of using high-frequency-circuit techniques optimized with the computer micro-architecture and logic implementation of functional blocks. To realize such a high clock frequency, the clock-distribution and latch-design methodology was critical.

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In 1995, microprocessor micro-architecture went to the next level of complexity: Out-of-order speculative-execution with register renaming was implemented in a CISC microprocessor [21]. It also used super-pipelining to achieve higher performance by increasing the clock rate. Three parallel instruction decoders converted CISC instructions into micro-operations, and executed them out-of-order. The processor accessed a large second-level off-chip cache through a full-speed 64-bit point-to-point buss. Also in 1995, a RISC processor by Chanas et al [22] extended its 32b architecture to 64b, adding additional instructions and a dedicated multi-media functional unit to accelerate video- and image-signal-processing operations.

Deeper pipelines continued to be pursued by microprocessor designers, since higher-frequency operation resulted directly in higher performance. Now, a gate delay was becoming a significant portion of the clock period, so designers pursued techniques to minimize the cycle time wasted propagating in and out of latches and flip-flops. Partovi et al introduced new forms of pulsed latches and flip-flops [23] that offered improvements to microprocessor clock frequency and power.

The rapid increase in microprocessor clock frequency, along with the increasing number of latches and flip-flops, made it difficult for processors to go into low-power light-weight hand-held computers. The 0.5W 160MHz 32b RISC microprocessor designed by Montanaro et al [24] was the first processor where the instruction set, micro-architecture, and circuit techniques were optimized together for maximum performance at such a low level of power consumption.

In 2000, 8 years after achieving 100MHz, high-performance microprocessors crossed the 1GHz clock-frequency barrier. The1GHz CISC processor [25] used high-speed bulk CMOS transistors and aluminum interconnects.

With higher levels of ULSI integration continuing, Gigahertz microprocessors integrated very large amounts of L2 cache, as well as multi-processors on-chip [27]. For high performance at low power, Nishi et al [26] implemented a 1GIPS 1W processor having a tightly-coupled 4-way multiprocessor with multi-threaded execution and low-voltage circuits.

We are now in an era where performance and power need to be optimally designed at all levels of microprocessor and digital ULSI design and implementation. As it has been throughout the history of the integrated circuit, performance and power consumption will continue to drive integration and circuit-design innovation.

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50 Years of Memories at ISSCC

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The Pioneering Days

ISSCC is the premier showcase for memory developments. Innovations in memory technology, design, and architecture, have been presented in this Conference, almost from the beginning. The first two memory papers presented circuits for "magnetic drum recording" [1] and the "switching characteristics of magnetic core" [2]. From 1957 to 1964, most of the memory papers concerned magnetic core, cryotron, tunnel-diode, and superconducting memory devices. The first paper that discussed IGFET applications for digital storage was presented by G.R. Kuster in 1965 [3]. This paper is one of the pioneering efforts in demonstrating the use of MOS transistors as part of a memory element.

L. M. Terman, in his article in the ISSCC 40th-Anniversary Commemorative Supplement, summarized the memory development of the first four decades of ISSCC [4]. In summary, it can be said that although many technologies, circuits, cell structures, and device architectures, have been presented in this Conference, from its early days, only a few technologies and architectures become commercial successes. Thus memories, based on bipolar, CCD, Josephson-Junction, magnetic-bubble, VMOS, BiCMOS, Silicon-on-Sapphire, and GaAs, are now only of historic importance.

The first full memory session at ISSCC entitled "Semiconductor Memories" was chaired by L. Spandorfer in 1969. Memories bearing some resemblance to present-day versions appeared first in 1970. Subsequently, memory technology has become the driving force for technology development and device scaling. In the last 35 years, line widths have reduced from 15 µm to 0.1 µm, while the memory density has increased from 1 Kbits to 4 Gbits. The three predominant memory technologies presented in this Conference are DRAM, SRAM, and NVM. In all these years, each has seen innovations in cell structure, device architecture, and "faster and smaller" transistors needed to achieve a higher level of integration.

Dynamic RAM

A 1K NMOS DRAM using a 3T memory cell was presented in 1970 by Regitz and Karp [5]. It implemented on-chip decoding, buffers, and column-sense amplifiers. Two years later Stein, Sihling and Doering presented the now-classic 1T1C memory cell [6]. Their paper also introduced dummy cells and a cross-coupled latch sense-amplifier. Besides density, usability became the focus, and the modern RAS/CAS interface with page-mode and RAS-only refresh was introduced by Schroeder and Proebsting in 1977 [7]. In search of ways to improve yield, redundancy techniques were investigated, and the first paper discussing redundancy (on a commercial 64Kb DRAM) and its impact on production yields was presented in 1979 [8]. In the same year, the 5V-only power supply DRAM design was presented [9].

In 1980, K. Itoh and his colleagues proposed the folded -bit-line architecture which became the architecture-of-choice for most of the DRAMs to follow [10]. To realize densities of 1Mb and above, the trench-cell [11] and stack-cell [12] structures were implemented in 1984. The twisted-bit-line structure, used in today's DRAMS, was introduced in 1988 [13]. A proposal for the first low-voltage DRAM with a single 1.5V power supply was made in 1989 [14].

In 1999, to enhance the DRAM throughput, three competing I/O interface architectures (DDR, RDRAM and SLDRAM) were proposed. The battle between RDRAM and DDR is still going on. In the new millennium, a "real" (without using multi-level cell) 4Gb DRAM was disclosed [15].

Static RAM

Static RAMs are used primarily as cache memories with CPUs, and are performance-driven. However, the larger cell size required has kept the SRAM density levels two to three generations behind developments in DRAM and Flash memory. The first associative memory using NMOS transistors with resistor loads was presented in 1966 by R. Igarashi and his colleagues [16]. A year later, in 1967, a bipolar 16b SRAM, capable of a 100ns cycle time, was disclosed [17], Also in 1967, a CMOS SRAM using Silicon-on-Sapphire technology, an early precursor to SOI, was presented by J.F. Allison and his colleagues [18]. To achieve higher densities, J.M. Caywood and his colleagues used a self-refreshing DRAM cell in an SRAM architecture in 1979[19]. This is one of the early efforts which led, ultimately, to modern day pseudo-static RAMs.

In 1988 sub-micron BiCMOS technology was introduced in SRAMs to enhance speed [20]. The high cost and scalability issues associated with BiCMOS technology limited its use, and CMOS became the technology of choice. In 1989, a 4Mb CMOS chip using dynamic-bit-line loads was demonstrated [21]. In 1990, a Thin Film Transistor (TFT) load cell was proposed for a 4Mb CMOS SRAM [22]. However, the low-yield problems of the TFT cell did not make it a commercially viable product, and with time it phased out. Since 1992, the introduction of stand-alone SRAMs has stopped, and the emphasis has shifted to embedded applications particularly for high-bandwidth systems. There is new interest developing again in SOI SRAM devices, but the jury is still out as to the viability of SOI as an SRAM technology.

Nonvolatile Memories

The technological challenges of providing a memory with permanent data retention, and a fast and easy data-altering capability, forced the development of many more nonvolatile memory-cell structures than for any other memory technology. The evolution of nonvolatile memories progressed from core memories in the 1950s and 19660s to mask programmable ROMs and bipolar PROMs in the 1970s. Many technologies were investigated as a way to achieve a usable combination of electrical data alterability and data retention. The rush to use UV-EPROM began in 1971, following the ground-breaking paper by D. Froman-Bentchkowsky [23]. The first stacked-gate single-transistor EPROM with hot-electron injection and UV erase was reported by P. Salsbury and his colleagues, in 1977 [24]. The first-commercially viable floating-gate EEPROM device using FN tunneling for program and erase was presented in 1980 by W. Johnson and his colleagues [25].

Techniques to achieve program and erase with a single 5V supply on a 16 Kb EEPROM using an internal charge pump and EPROM redundancy were reported in 1982 [26]. The first Flash memory with poly-to-poly erase was introduced in 1985 by F. Masuoka and his colleagues [27]. The first EPROM reporting bipolar PROM speeds at 16K density was presented in 1985 by S. Pathak and her colleagues [28].

Advancements in new cell structures and arrays continued to be presented at the Conference throughout the 1980s, with NOR, NAND, AND, DINOR, and other variations. The concept of stor-

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ing two bits per cell on a NOR Flash memory was reported in 1995, where a 32Mb density was achieved using 16 million cells [29]. This started the race for multi-bit memory designs. The debate over the relative viability of multibit cells versus single-bit cells with the scaled voltages and line widths is still on. There is also new interest developing in nitride and MNOS types of structures for multibit charge storage .

Emerging Memory Technologies

In the quest for a "Unified Memory", many innovative ideas and technologies have been presented at ISSCC from time to time. Some of these ideas became viable product lines, while others remain as technical curiosities. Multiport SRAMs, CAMs, Video RAMs, FIFOs, and NVRAM are examples of some which initiated their own product families. Now, with the emergence of SoC, the demand for embedded memory has increased dramatically. Today, SRAMs are mostly embedded, and there is a large effort to integrate DRAMs and Flash memories economically on a system chip.

Ferroelectric Memory was first discussed in this Conference in 1988 [30]. In the last 14 years, we have seen many papers discussing various ferroelectric architectures and densities. Other innovative memory technologies presented in this Conference include, "multi-bit DRAM" in 1985, "HEMT SRAM" in 1991, "NAND-cell DRAM" in 1993, "SOI DRAM", and "neuron-MOS memory" in 1994, as well as "Single-Electron memory" in 1996 and 1998. Recently, "MRAMs" in 2000 [31], and "OUM" (Ovonic Unified Memory) in 2002, have generated a lot of interest in the memory-design community. Only time will tell which of these memory technologies will become mainstream. Our quest for the ideal memory is still on.

Conclusion

In the preceeding 50 years, there have been more than 700 memory papers presented at ISSCC. Thus, it is difficult, if not impossible to cover the corresponding myriad of developments in a short review, such as this. I offer apologies to the authors whose work I could not accommodate due to both my ignorance and limitations of space.

It has been my privilege to be associated with the exciting field of memory throughout its development. As a result, during the research underlying this paper, I have recalled the excitement of many presentations, evening-panel discussions, and wild speculations made by my compatriots. Accordingly, I salute all the authors whose work over the years made ISSCC such an exciting, enjoyable and educational event. Finally, I would like to thank the Memory-Sub-Committee members of 2003, and past-memory Sub Committee Chair B. Bateman who helped me compile this article.

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50 Years of Solid-State Image Sensors at ISSCC

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The title of this essay might suggest that solid-state image sensors occupy the complete 50 years of ISSCC history, but that is not the case. In fact, the two technologies which are in use today, namely CCDs and CMOS imagers, were both reported for the first time at ISSCC in the very early 1970s. Charge-coupled devices (CCDs) were invented in the late 1960s, but found their success in the consumer market only in the mid 1980s. This was due mainly to the fact that the technology and techniques needed for commercialization became more or less mature around that time. Later, about a decade ago, CMOS image sensors began to challenge CCDs. Following their introduction, CMOS imagers followed a migration path similar to that shown by CCDs: Several years after the first announcements, CMOS imagers became commercially available. Again, this time, a similar sequence was followed: first announcements; a decade of more- or-less silence; and then, finally, the commercial release. Over the past 3 decades, solid-state imaging has evolved from the laboratory into every camera now built, from consumer to professional, from toys to astronomical instruments. ISSCC has had a major role in this wide-spread use of CCDs and CMOS image sensors. The Conference reported regularly on the major breakthroughs in the field.

In what follows, ISSCC milestones in the field of solid-state imaging are listed:

1) In 1970, Sangster described Bucket-Brigade Devices or BBDs. BBDs can be seen as the predecessors of CCDs. BBDs are charge-transfer devices in which the charge packets are transported by means of MOS transistors, while CCDs realize this transport by means of MOS capacitors [1],
2) In 1971 Weckler and Dyck showed a self-scanned photodiode array, in which pixels and scanning electronics are integrated in a single chip [2],
3) As far as low-noise operation of image sensors is concerned, the use of a Floating Diffusion Amplifier (FDA) in combination with Correlated-Double Sampling (CDS) is seen as an absolute must! These techniques were published, respectively, in 1971 by Kosonocky and Carnes [3] and in 1973 by White et al [4]. Today, FDAs and CDS circuitry are still in use in all CCDs and in many CMOS sensors,
4) The first CCD sensor which could be used in an NTSC-compatible single-sensor color camera was announced in 1980 by Ishirara et al. They described an interline-transfer CCD with a color-filter array [5]. In the same year, the very first (n-)MOS color imaging device was published by Aoki et al [6].
5) Probably the last boost really needed for CCDs to become a consumer product was provided by the vertical anti-blooming structure. Today, all consumer CCDs make use of this technique, which was reported by Ishihara et al in 1982 [7],
6) A major attempt to combine a CCD imager with CMOS driving circuitry on a single chip was described in 1988 by Theuwissen et al [8].
7) The Amplified MOS Imager (AMI), was the first version of what became known later as APS CMOS image sensors. A paper describing this technology was presented in 1990 by Andoh et al [9].
8) The ultimate goal of CMOS image sensors is a complete camera on a single chip: In 1998, two groups showed the feasibility of this idea: Loinaz et al [10] and Smith et al [11] announced a single-chip video camera.
9) How CCD know-how can be implemented in CMOS imagers to improve their performance was described in 2000 by Yonemoto et al [12]. The authors introduce pinned-photodiode into CMOS technology,
10) Two key advantages of CMOS image sensors are their low power comsumption and their wide functionality. Two papers based on these advantages were published in 2000 by Cho et al [13] and in 2001 by Kleinfelder et al [14]. The first paper describes a micropower image sensor which is capable of operating at 1.2 V. The second reports on a Digital Pixel Sensor (DPS) in which every pixel of the CMOS image sensor gets its own in-pixel analag-to-digital converter.

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50 Years of Sensors (and MEMS) at ISSCC

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Solid-state sensing has been a strong technical area at ISSCC for most of the past 50 years. While early solid-state sensing relied simply on the piezoresistive properties of silicon, it is now based on a variety of physical and chemical phenomena embedded in sophisticated microelectromechanical systems (MEMS). Along with such sensing elements, these microsystems often contain associated submicrometer digital and analog circuitry.

The history of the evolution from basic sensing concepts to complex microsystems can be traced through some of the key breakthrough and survey papers presented at ISSCC over the years.

1) Early work in the 1960s pointed out the potential of both physical and chemical sensors combined with electronics: In 1963, Stern [1] described the use of silicon strain-gage elements and thermistors in industrial instrumentation. Also in 1963, Lettvin [2], reported on the basic principles of a K+ chemical sensor. In 1964, Rindner et al [3] presented new devices and circuits involving the extremely high sensitivity of a pn junction to an applied stress.
2) In 1966, Newell [4] presented new circuit aspects of the resonant-gate transistor, an early concept that has driven much of the research and development of modern-day resonant micromachined microbeam and comb-drive microsensor and microactuator devices.
3) Silicon Hall-effect magnetic-field transducers were reported in 1968 by Fry [5]. This work presented sensing concepts based on the deflection of carriers in the inversion channel of an MOS device under an applied magnetic field. In particular, the concept of a split-drain Hall-effect device was presented.
4) In 1971, Wise and Angell [6] reported pioneering work on microprobes in biomedicine. A multielectrode probe, which contained integrated buffer amplifiers capable of recording the electrical activity of single neurons, represented an important breakthrough in neurophysiology. This early use of silicon IC technology in making neural probes was an important early micromachining development leading to modern MEMS approaches.
5) Early microprowered telemetry transmitters for biomedical applications were also described in 1971 by Ko et al [7]. This paper was one of the first to describe the use of modular blocks that could potentially be integrated into monolithic chips, an important concept on the way to today's multi-functional microsystems.
6) In 1974, significant progress in the application of solid-state sensors in biomedicine was reported in several key areas: Meindl [8] presented a paper on IC technology for transducers and preprocessing electronics in four medical areas: chronically implantable systems (e.g. pacemakers), percutaneous and intraoperative instruments, transcutaneous sensor arrays, and sensory aids for the handicapped. Plummer et al [9] described the use of piezoelectric transducers for ultrasonic imaging of the body's internal organs. Saraswat and Meindl [10] reported on the development of a high-voltage MOS transistor for driving piezoelectric tactile displays.
7) Early diaphragm pressure sensors were described by Borky and Wise [11] in 1979. These mechanical sensors were based on the piezoresistive effect in silicon, a basic approach found in a wide range of commercial automotive and biomedical sensors.
8) The integration of microsensors with on-chip signal processing is one of the enabling features of many modern-day MEMS. In 1986, Najafi and Wise [12] demonstrated micromachined implantable multielectrode arrays with on-chip signal processing. Multi-functional circuits capable of amplification, multiplexing, and output buffering, were demonstrated in a bulk-micromachined process.
9) In 1995, Payne et al [13] described the opportunities provided by surface micromachining combined with on-chip bipolar/MOS electronics in integrated accelerometers. This approach continues to be commercially successful with now over 100 million integrated surface-micromachined accelerometers produced including integrated gyroscopes [14].
10) The last five years of the ISSCC have seen several emerging concepts in biochemical sensing, a new field believed by many to have enormous potential. Caillat et al [15] in 1998 presented the concept of active CMOS biochips implementing electrically-addressed DNA probes. Lauwers et al [16] in 2001 reported on a multi-parameter biochemical microsensors for continuous monitoring of concentrations of blood gases, ions, and biomolecules. This paper is somewhat symbolic of today's state-of-the-art in integrated MEMS: seven different chemical substances are detected in a multi-sensory approach; on-chip interface electronics are used to process multiple electrical signals; on-chip temperature control is implemented; EPROM circuits provide information storage; and control electronics and telemetry manage the flow of sensed information.

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Forty Years of Feature-Size Predictions (1962-2002)

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Preamble

The modern integrated circuit was invented more than 40 years ago. Very soon speculation began about its limitations — the maximum density of logic elements, the minimum energy consumption per logic operation, and so on. I thought it would be interesting to look back on these predictions from, today's perspective. Accordingly, a review of the predictions of the smallest-possible feature size over the last forty years is given below.

The Early Years

Let us begin by considering the context in which the first prediction were made. The modern integrated circuit was invented just prior to 1960, through the contribution of the first monolithic IC by Kilby [1], and the first IC utilizing planar interconnects by Noyce [2]. Before that time, miniaturization of electronics was exploited through small modules incorporating discrete devices and thin-film circuits (creating evaporated "circuit boards", with integrated passive elements). Although the concept of the FET transistor was patented in 1927 by Lilienfield, it was not until 1960 that the first silicon MOS transistor was successfully fabricated [3]. Moore had not yet formulated his famous law [4], and the concept of device scaling was not to be introduced until 1974 [5]. The main interest in device dimensions was related to miniaturization, or packaging density, as controlled by the three-dimensional size of a device, and its power dissipation.

First Predictions

In 1962, Wallmark and Marcus performed a thorough analysis of the minimum size and maximum packing density of semiconductor devices. The basic concept underlying their analysis was straightforward; they considered the possible spread of the resistance value of a minimum-sized semiconductor cube. Three causes of resistance variation were considered: variation due to doping fluctuations, variation due to edge uncertainty, and variation due to the effects of cosmic radiation. Figure 1 shows the minimum feature size versus the material resistivity as determined by various factors such as impurity fluctuation, edge uncertainty, etc [6]. In their work, they assumed that it should be possible to fabricate a "medium-size computer" of 10^5 elements with reasonable yield. This complexity measure was used to set a threshold, in which the fraction of cubes exceeds a resistance tolerance of 10% should be less than 10^{-5}. For doping fluctuations, this constraint led to a minimum number of doping atoms of $2 \cdot 10^4$ per cube, a value which can be converted to a minimum cube size depending on material and doping. For edge uncertainty, Wallmark and Marcus concluded that optical methods would have a resolution too poor to be a viable technique. Instead, they considered e-beam lithography, and assumed an edge uncertainty of 10nm (taken as edge variance in a Gaussian-edge position model). With this edge uncertainty, they arrived at a minimum cube size of 2μm. As for the effect of cosmic radiation, their analysis gave limits similar to those for doping fluctuation. In conclusion, they predicted a minimum feature size of 2μm (in contrast to the actual dimensions 25μm prevalent at that time).

There were of course even earlier predictions based on physical limits not related to integrated circuits. For example, in 1959, physicist R. Feynman proposed that the whole world literature could be stored within a cube with 20-mil sides using memory element with 100 atoms each [7]. Later, in 1960, Swanson published a more formal paper in which he estimated the smallest size of a memory device based on considerations of the retention time of an element utilizing collective phenomena such as occur in ferromagnetic or ferroelectric materials. He found that such an element needed at least 100 basic units (spins, or polarized molecules) [8]. With a lattice constant of about 4Å, this resulted in the smallest possible dimension of about $(2nm)^3$, similar to Feynman's prediction almost a year earlier.

Later Developments

In 1972, Hoeneisen and Mead presented a careful analysis of minimum device sizes, considering not only the device structure itself but also its context, the circuit. For the MOS case (n-MOS logic with so-called non-saturated enhancement-load) they concluded that gate-oxide breakdown is the most-critical factor limiting the gate length to 0.24μm (at a 2V main-supply voltage and a 4V gate voltage on the load n-MOS)) [9]. They also found that the minimum-sized transistor, not considering the circuit, must have a gate length larger than 0.15μm. In these considerations, doping fluctuation played an important role using arguments similar to those presented by Wallmark and Marcus in 1962.

During the second half of the 1980s, so-called short-channel effects were analyzed, such as drain-induced barrier lowering (DIBL). DIBL leads to a reduction in threshold voltage for short-channel devices and also called (V_t "roll-off"), which in turn leads to increased leakage currents. In 1989, Pimbley and Meindl concluded that MOST channel length can be reduced to 60nm, when using a very thin gate oxide thickness, very shallow drain junction depth, and high-channel doping levels. [10]. In 1991, Antoniadis and Chung, concluded that the minimum usable channel length was about 80nm, using the same arguments [11]. They also concluded that DIBL was primarily an electrostatic problem; for its elimination, the gate must shield the source from the drain field. Later, it was suggested that by using a double gate structure, DGMOS, this shielding becomes considerably more effective. In 1992, Frank et al, using Monte-Carlo simulations demonstrated that a 30nm-long DGMOS device is feasible, although they did not really discuss the limits of device size [12]. In 1997, Pikus and Likharev made a simple and elegant analysis of a double-gate MOS device [13]. They concluded that in a small-enough device, doping is not necessary since transport is essentially ballistic, and short-channel effects are controlled purely by the geometry (through electrostatics as Antoniadis pointed out). What happens with a short channel is that the voltage gain becomes too small due to a decreased output impedance (compared to the transconductance). With a minimum voltage-gain constraint of 10, they arrived at a minimum channel length of 10nm. (Note that this is for logic; for a DRAM, in which transistor voltage gain is not needed, they concluded that a minimum gate length of 4nm is usable).

In 2001, Frank et al gave a comprehensive review of the limits of device scaling in an invited paper published in the Proceedings of the IEEE [14]. They noted several physical phenomena that limit the channel length of the MOS transistor. As noted earlier, the most critical phenomenon is DIBL. Minimum DIBL occurs in double-gate device structures using minimum oxide thickness, and minimum channel thickness. However, oxide thickness is limited in turn to about 2nm, by direct-tunneling leakage current. But, correspondingly, for such thin oxides the effect of oxide thickness on DIBL is relatively limited. Another limit is direct drain-source-tunneling leakage current. Their final conclusion is that transistors with channel length as low as 8 to 10nm can be fabricated experimentally. However, for large integrated circuits, he predicts that a minimum gate length of 13nm is required in order to allow for reasonable tolerances.

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Retrospective

The various predictions of the minimum feature size versus the year of publication have been plotted in Figure 2, together with the actual feature size at the time. Over the last 40 years, we have seen that the predictions have varied widely, from 2µm to 10nm. How is it possible to come to such different conclusions?

Wallmark's first attempt in 1962 did not consider a specific device, but rather assumed semiconductors with quite small tolerances assembled in large integrated circuits. The primary limitation of his analysis is the assumption that the lithography-definition error has a Gaussian amplitude distribution. Most of the edge uncertainty is not stochastic, but related to deterministic phenomena such as diffraction, optical aberration, etc. Therefore, the edge definition given by "spot size" should not be enhanced by taking the Gaussian tail into account. This fact is quite obvious, as today, as we now produce 180nm chips, not with e-beams but with light of 248nm wavelength [15]. Still, one would certainly expect some "noise" mechanism to be involved in lithography, one that affects the smallest geometry in a stochastic manner. However, no such mechanism seems to be identified today [16]. As a possible second source of failure, doping fluctuations have been managed over the years by increased doping levels, and eventually by concluding that a double-gate MOST is not dependent on doping level at all. However Wallmark's third concern, cosmic radiation, is still considered to constitute a limit, but recent careful analysis indicates that it is less critical than Wallmark assumed, due to reduced collection of charge in highly-doped substrates, combined with reduced collection area [17]. On the other hand, Hoeneisen and Mead considered real devices with a fixed device design and with quite high voltages. While they found that breakdown was a limiting factor, today with low-enough voltages (below the silicon bandgap), we no longer have band-to-band breakdown. Rather, since mid 1980s, drain-induced barrier lowering (DIBL) has dominated feature-size discussions. This DIBL limitation is still considered valid.

Thus, the predictions started with a very general view (semiconductors, as a whole) and "ended" with a very specialized device (the DGMOST) as a general solution. Are there other alternatives such as single electron transistors (SET), organic materials, etc for which other limitations disappear? It is important to note that at 8nm, we are very close to a direct source-drain tunneling limit, which, in fact, is very fundamental. From Figure 2, we note that the predictions of smallest feature size have always been about one order of magnitude lower than the value prevalent at the time. Maybe this is natural, but it is also somewhat disappointing, being likely evidence of a lack of fantasy in our predictors. However, there is one clear exception to this "rule", the prediction of 2nm by Swanson from 1960. Furthermore, we see no saturation of either actual or predicted feature size. A possible conclusion is that even the latest prediction is too pessimistic. Maybe we will finally end up (or "bottom out") at 2nm, Swanson's prediction from 1960!

Acknowledgements

I would like to dedicate this paper to Professor J. Torkel Wallmark, who made possibly the first prediction of integrated-circuit limits in 1962, and who was my teacher, supervisor and collaborator in the period1965-1978.

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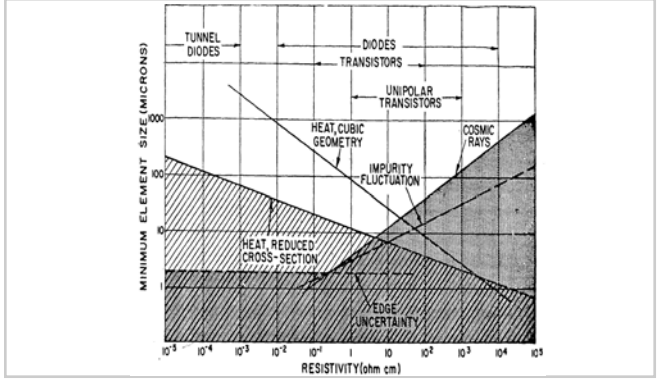

Figure 1: Minimum feature size versus material resistivity due to various limitations, Wallmark and Marcus 1962 [6].

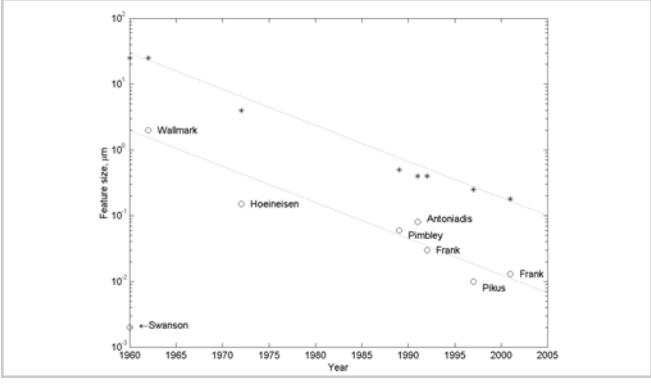

Figure 2: Predicted (O) and actual (*)(for the year of the prediction) feature sizes versus year of publication.

The IRE reports the successful operation of the first “Transistor Conference”.

The 1958 Keynote was delivered by William Shockley (center right) shown here flanked by ISSCC organizers Brainerd, Winner and Mulligan.

An overflow audience attended this evening panel session when 1960 became ‘the year of the tunnel diode’. Leo Easki was keynoter.

This 1960 photograph shows the National Committee, the forerunner of today’s Executive Committee. From left to right are Bill Howard, Lewis Winner, Bob Cotellesssa, Tudor Finch, Art Stern, Sorab Ghandhi, Solomon Charp, Murlan Corrington, Bob Mayer, and Henry Sparks. The group is notable both for professional accomplishment and for dedication to IEEE affairs. Cotellessa, the treasurer, was Vice President of the IEEE from 1973-1976. Finch was Program Chairman this year and remained active in related professional committees until his death. Stern, here in the role of Conference Chairman, served in a number of IEEE offices before becoming IEEE President in 1975. Corrington, Chairman of the Sponsor’s Committee, remained in that and related roles until 1977. Mayer, who was Local Arrangements Chair in 1960, became the Conferences Treasurer and remained in that role until his retirement in 1982. Sparks succeeded Mayer as Local Arrangements Chair and continued to serve the Conference throughout the Philadelphia years.

The 1963 Program Committee meeting at the NYC Headquarters of the IEEE during paper selection

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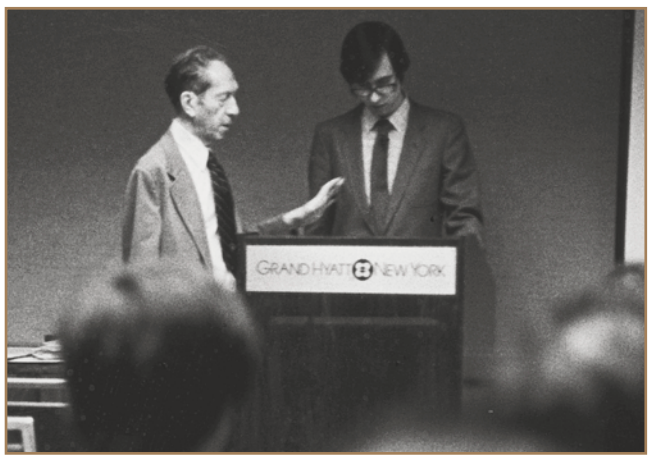
1963 Press Conference, one of many yearly such events held at New York City's Sardi's Restaurant.

1979 was the last year ISSCC was held in Philadelphia. The audience is shown at the Sheraton Grand Ballroom.

Jim Meindl, Gerry Herzog and Dick Baker were in a jocular mood in this 1966 photograph. The program must have been success!



The speakers' rehearsal sessions were originally intended for overseas speaker but eventually extended to all paper presenters. In this 1981 photograph, ISSCC's Lew Winner instructs a Japanese speaker how to speak in New York City English!

In 1985 ISSCC celebrated the 30th anniversary of the Digest. Executive Chair Jack Raper prepares to cut the cake with a ceremonial sword. Lew Winner presides. Program Chair Harry Boll Looks on cautiously.

ISSCC 50-Year Anniversary Author Honor Roll

ISSCC offers thanks and recognition to the authors below each of whom has 10 or more ISSCC regular publications over the 50 years of the Conference.
A special recognition goes to James Meindl who has 47 ISSCC regular publications.

Name	Year of 1st Paper	Most Recent Paper	Affiliation	City	State/ Country
Meindl, James	1966	2003	Georgia Institute of Technology	Atlanta	GA
Gray, Paul	1970	2001	UC Berkeley	Berkeley	CA
Hodges, David	1963	1993	UC Berkeley	Berkeley	CA
Brodersen, Robert W	1975	2000	UC Berkeley	Berkeley	CA
Wooley, Bruce	1970	2003	Stanford University	Stanford	CA
Horowitz, Mark	1982	2003	Stanford University	Stanford	CA
Abidi, Asad	1984	2003	UCLA	Los Angeles	CA
Steyaert, Michel	1988	2002	Katholieke Univ.	Leuven	Belgium
Razavi, Behzad	1992	2003	UCLA	Los Angeles	CA
Yamashina, Masakazu	1987	2000	NEC	Kanagawa	Japan
Sakurai, Takayasu	1984	2003	Univ. of Tokyo	Tokyo	Japan
Samueli, Henry	1991	2001	Broadcom	Irvine	CA
Ishibashi, Koichiro	1987	2003	Hitachi CRL	Tokyo	Japan
Sansen, Willy	1976	2003	Katholieke Univ.	Leuven	Belgium
Huang, Qiuting	1995	2003	Swiss Federal Institute	Zurich	Switzerland
Song, Bang-Sup	1983	2003	Univ. of Illinois	Urbana	IL
Yoshihara, Tsutomu	1983	1995	Mitsubishi Electric Corp	Kyoto	Japan
Hurst, Paul J	1983	2002	UC Davis	Davis	CA
Masuhara, Toshiaki	1971	1988	Hitachi CRL	Tokyo	Japan
Meyer, Robert G	1971	1997	UC Berkeley	Berkeley	CA
Minato, Osamu	1976	1990	Hitachi	Tokyo	Japan
Huijsing, Johan	1975	2002	Delft University	Delft	The Netherlands
Masuoka, Fujio	1984	2000	Tohoku Univ	Sendai	Japan
Mizuno, Masayuki	1995	2003	NEC	Kanagawa	Japan
Solomon, James E	1966	1986	SDA Systems	Santa Clara	CA
van de Plassche, Rudy	1971	1999	Broadcom	Bunnik	The Netherlands
Arimoto, Kazutami	1986	2003	Mitsubishi	Itami	Japan
Baertsch, Richard D	1971	1994	General Electric	Schenectady	NY
Lewis, Stephen	1987	2002	UC Davis	Davis	CA
Matsuzawa, Akira	1984	2003	Matsushita	Osaka	Japan
Nakamura, Kazuyuki	1990	2002	NEC	Kanagawa	Japan
Sakai, Yoshio	1978	1988	Hitachi Ltd.	Tokyo	Japan
Allstot, David	1978	1999	Univ. of Washington	Seattle	WA
Brokaw, Paul	1974	1997	Analog Devices	Wilmington	MA
Castello, Rinaldo	1984	2002	Univ. of Pavia	Pavia	Italy
De Man, Hugo	1973	2003	IMEC	Leuven	Belgium
Iizuka, Tetsuya	1980	1990	Toshiba Corporation	Kawasaki	Japan
Itoh, Kiyoo	1976	2001	Hitachi	Tokyo	Japan
Langmann, Ulrich	1985	2002	Ruhr Univ.	Bochum	Germany
Lee, Hae-Seung	1989	2002	MIT	Cambridge	MA
Ogiue, Katsumi	1979	1989	Hitachi Ltd.	Tokyo	Japan
Takada, Masahide	1986	1996	NEC Corporation	Sagamihara	Japan

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