2018

PRESS KIT

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As of November 6, 2017, there is not enough information to guarantee its correctness.

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ISSCC 2018
VISION STATEMENT

The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and use to maintain technical currency, and to network with leading experts.

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Preamble

FAQ on ISSCC

What is ISSCC?

ISSCC (International Solid-State Circuits Conference) is the **flagship** conference of the IEEE Solid-State Circuits Society. According to the SIA, the Semiconductor industry generated US$338.9 billion in sales in 2016 and ISSCC continues to be the premier technical forum for presenting advances in solid-state circuits and systems.

Who Attends ISSCC?

Attendance at ISSCC 2018 is expected to be around **3000**. Corporate attendees from the semiconductor and system industries typically represent around **60%**.

Where is ISSCC?

The **65th ISSCC** will be held at the San Francisco Marriott Marquis on February 11th through February 15th 2018.

Are there Keynote Speakers?

After a day devoted to educational events, ISSCC 2018 begins formally on Monday, February 12, 2018 with four exciting plenary talks:

- Vince Roche, President, Chief Executive Officer, Analog Devices, USA
- Barbara De Salvo, Chief Scientist and Scientific Director, CEA-Leti, France
- Yukihiro Kato, Senior Executive Director, Denso, Japan
- David Patterson, Professor of the Graduate School at UC Berkeley

What is the Technical Coverage at ISSCC?

ISSCC covers a full spectrum of design approaches in advanced technical areas broadly categorized as: (1) Communication Systems, (2) Analog Systems, (3) Digital Systems, and (4) Innovations including micro-machines and MEMS, imagers, sensors, biomedical devices, as well as forward-looking developments that may take three or more years for commercialization.

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How are ISSCC Papers Selected?

Currently around 600 submissions are received each year across the broad spectrum of specified topics. Review is by a team of over 150 scientific and industry experts from the Far-East, Europe, and North America. These experts are organized into 11 Sub-Committees that cover the 4 broad areas described earlier:

- **Communication Systems** includes Wireless, RF, and Wireline Subcommittees
- **Analog Systems** includes Analog, Power Management, and Data Converter Subcommittees
- **Digital Systems** includes Memory, Digital Circuits, and Digital Architectures and Systems Subcommittees
- **Innovative Topics** includes Imagers/MEMS/Medical Devices/Displays and Technology Directions Subcommittees

What Companies are Presenting this year?

Companies presenting papers at ISSCC 2018 include AMD, Analog Devices, Broadcom, IBM, Intel, Infineon, MediaTek, NXP Semiconductors, Nvidia, Panasonic, Qualcomm, Samsung, ST Microelectronics, Texas Instruments, TSMC, Toshiba and Xilinx, just to name a few. A more complete list can be found in the Index.

Are there educational sessions?

ISSCC features a variety of educational events which include:

- Ten Tutorials (targeted toward participants looking to broaden their horizon)
- Six Forums (targeted toward experts in an information sharing context)
- One Short Course (targeted toward in-depth appreciation of a current hot topic)

Are There Other Events?

A more complete list of all activities at ISSCC 2018:

- Four Plenary Presentations
- Five Invited Talk on System Issues
- Technical Sessions (30 distinct sessions)
- Six Evening Sessions and Panels
- Educational Sessions Featuring:
  - Ten Tutorials
  - Six Forums
  - One Short Course
- Student Research Preview (for the introduction of graduate-student research-in-progress)
- Demonstration Sessions from Academia and Industry
- Networking Social Events
- Author Interview Sessions
- Workshop on Circuits for Social Good
- Industry Showcase
- A Number of University Alumni Events
- Book Display

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How Do I Use this Press Kit?

The Press Kit provides a PREAMBLE section that features this FAQ and other general information. The kit also includes SESSION OVERVIEWS AND HIGHLIGHTS of all 30 technical sessions into which the 202 papers are grouped, together with brief descriptions and context for each. As well, there is an abstract for each of the Plenary talks. For your convenience, the Kit includes two structural charts in the INDEX section: (a) a list of the 4 Technical Topics and their associated Subcommittees (11) and Sessions (30); (b) a list of contributing companies and institutions with their associated papers. Thus, to located information of interest you can access Chart 4.1 to identify sessions of interest, after which you might logically access its Session's Overview or Highlight section. Alternatively, if your interest is in particular organization then Chart 4.1 will direct you immediately to papers of interest each of which is detailed in its corresponding Session Overview and possibly in the Highlights section. For anyone's interest it is useful to use Chart 4.1 to access the appropriate Trend information which provides a broad historical view of the context of your interest and often includes reference to current ISSCC 2018 papers.

Anything New This Year?

This year, for the first time, ISSCC will hold a Workshop on Circuits for Social Good, which will highlight various ways that circuits can help address some of the most important challenges facing society today, ranging from health care to energy conservation. The workshop includes speakers from industry, academia, and startups as well as interactive round-table discussions on topics such as machine learning, medical devices, next-generation communications, and security.

ISSCC will hold an Industry Showcase event the evening of Monday, February 12th, where companies will provide short "pitches" on their technology/product innovation, followed by an interactive session with attendees at individual company booths/tables.

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Overview: ISSCC 2018 – Silicon Engineering a Social World

Continued advances in solid-state circuits and systems have brought evermore powerful communication and computational capabilities into mobile form factors. Such ubiquitous smart devices lie at the heart of a revolution shaping how we connect, collaborate, build relationships, and share information. These social technologies allow people to maintain connections and support networks that otherwise would not be possible; they provide the ability to access information instantaneously and from any location, thereby helping to shape the world's events and culture, empowering citizens of all nations, providing social networks allowing worldwide communities to develop and bond with common interests.

Plenary Session (Session 1)

The Plenary Session on the morning of Monday, February 12, 2018, will feature four renowned speakers:

- Vince Roche, President, Chief Executive Officer, Analog Devices, USA, will discuss “Semiconductor Innovation: Is the Party Over or Just Getting Started?”, and explore what is the next paradigm for semiconductor innovation and what is our path forward as scientists, technologists, and industry overall.
- Barbara De Salvo, Deputy Director for Science and Long Term Research, CEA-Leti, France, will give her insights into “Brain-Inspired Technologies: Towards Chips that Think”, and will illustrate a research strategy encompassing algorithms, circuits, and components, all in support of brain-inspired technologies to meet the needs of 21st century applications.
- Yukihiro Kato, Senior Executive Director, Denso, Japan, will describe “Future Mobility Society Enabled by Semiconductor Technology”, and discuss how the automotive industry is in the midst of a once-in-a-century transformation caused by electrification, automated driving, and connected vehicles.
- David Patterson, Professor of the Graduate School at UC Berkeley, will discuss “50 Years of Computer Architecture: From Mainframe CPUs to Neural-Network TPUs”, reviewing a half-century of computer architecture, from the IBM System 360 to modern domain-specific computer architectures such as Google’s Tensor Processing Unit.

Highlights of these Plenary talks are provided in the following section.

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ISSCC 2018

PLENARY SESSION – INVITED PAPERS

Plenary Session — Invited Papers

Chair: ***Anantha Chandrakasan,*** Massachusetts Institute of Technology, Cambridge, MA

ISSCC Conference Chair

Associate Chair: ***Alison Burdett*****,** Sensium Healthcare, Oxford, UK

ISSCC International Technical-Program Chair

1.1 Semiconductor Innovation: Is the Party Over or Just Getting Started?

Vince Roche*, President, Chief Executive Officer, Analog Devices, MA*

The future pace of semiconductor innovation is by no means certain. A little more than a decade ago, Dennard scaling ground to a halt. Symposia and media outlets have been speculating on what comes after Moore's Law for years now. Beyond these technology challenges, business challenges, as well, are putting pressure on traditional semiconductor innovation: semiconductor prices continue their steady decline while small-geometry wafer fab facilities now cost close to $10B to build.

In this environment, is there any room for continued innovation or is the future of the semiconductor industry defined by incrementalism, commoditization, and financial engineering? If our future is the latter, how will we meet the demands of a world where businesses, governments, and societies are digitizing at a blazing pace? The spread of pervasive ubiquitous sensing, rapid advances in artificial intelligence, heterogeneous integration, and the continued impact of digitization on virtually every industry on earth will require more, not less, semiconductor innovation.

The physicist and philosopher Thomas Kuhn might describe our situation as the crisis that catalyzes a new paradigm. So what is the next paradigm for semiconductor innovation? What is our path forward as scientists, technologists, and an industry?

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1.2 Brain-Inspired Technologies: Towards Chips that Think

***Barbara De Salvo**, Deputy Director for Science and Long Term Research, CEA-Leti, Grenoble, France*

Since the late 50s, brain-inspired computing has been regarded as an interesting alternative to conventional computational paradigms. Today, the omnipresence of "big data" and worldwide social interactions requires technologies capable of analyzing complex objects (such as sounds, images, or videos), in real time, and interact with humans in a cognitive way. The demand for computational efficiency and "intelligent" features has gone well beyond what can be achieved with traditional solutions. The advent of the Internet-of-Things has also introduced a new paradigm that supports a decentralized and hierarchical communication architecture, where a great deal of analytics processing should be done at the edge and at the end-devices instead of in the cloud. Specialized low-power architectures, inspired by the human brain, have thus recently become one of the most active research areas in the computing landscape, offering tremendous opportunities for novel applications. To map the embedded systems requirements, new challenges in brain-inspired technologies should be addressed, in particular automatic sensor fusion, system fault tolerance and data-privacy, while achieving high recognition accuracy, low power consumption, and reducing cost.

In this talk, we will illustrate a research strategy – one encompassing algorithms, circuits, and components — to develop brain-inspired technologies and meet the needs of 21st-century applications. To explore the architecture of neural networks, an open software platform has been created and several neural network circuits conceived and fabricated. The use of innovative components, such as emerging resistive memories, advanced CMOS, and 3D technologies has been explored to allow for the implementation of cognitive tasks in neural networks. Those novel components bring memory closer to the processing unit and offer extraordinary potential to implement "intelligent" features, approaching the way knowledge is created and processed in the human brain. Several concrete examples will be given to illustrate how brain-inspired technologies are developed using a holistic research approach, where process development and integration, circuit design, system architecture, and learning algorithms are simultaneously optimized, opening the door to new disruptive applications.

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1.3 Future Mobile Society Enabled by Semiconductor Technology

***Yukihiro Kato**, Executive Director, Denso, Aichi, Japan*

The automotive industry is in the midst of a once-in-a-century greatest transformation. The transformation of the automobile is a consequence of three technology trends: (1) electrification, (2) driving automation, and (3) vehicle interconnection. All three of these require dramatic advancement within semiconductor technologies. In this talk, our vision of the future mobile society is presented, focusing especially on automotive semiconductor electronics. To promote the electrification of the car, power semiconductors are a key technology. The energy conversion efficiency of the motor has been increased by IGBTs, and next-generation SiC MOSFETs will further increase efficiency. However, to put automated driving to practical use, both advanced sensors and intelligent SoCs are required. Improved performance of sensors, such as cameras, LIDARs, and millimeter-wave radars, with increased range and resolution, are required to precisely monitor the total environment of the car. Path planning for automated driving involves recognizing the vehicle's proximity to nearby objects and the free space available. In this process, deep learning is an exceedingly useful method and highly sophisticated SoCs with GPUs are essential for its implementation. Finally, from the viewpoint of a connected vehicle, cars will shift from lumps of metal into something like a giant smartphone! Of course, in the connected vehicle, you can make a phone call, receive and/or transmit emails, do shopping, make payments, and so on. As well, updated maps are constantly available. But, also, each vehicle must be constantly aware of the status and intent of nearby vehicles. Clearly, to implement the intricacies of such an interconnected vehicle network, we need a myriad of semiconductors including communication ICs.

1.4 50 Years of Computer Architecture: From Mainframe CPUs to Neural-Network TPUs

***David Patterson**, Google, Mountain View, CA, University of California, Berkeley, CA*

This talk reviews a half-century of computer architecture: We start with the IBM System 360, which in 1964 introduced the concept of "binary compatibility". Next, came the idea of the "dominant microprocessor architecture", for which the early candidate was the Intel 432 which was shortly replaced by the emergency introduction of the Intel 8 0x86 in 1978. However, for the next 20 years, the Reduced Instruction Set Computers (RISC) became dominant. Then, the Very Long Instruction Word (VLIW) HP/Intel Itanium architecture was heralded as their replacement in 2001, but instead the role was usurped by AMD's introduction of the 64 bit 80 x86. Thus, while the 80 x86 dominated the PC-Era, RISCs have led thereafter, currently with 20B shipped annually (versus 0.4B 80 x86s). Since the ending of Moore's Law and Dennard scaling has stalled performance of general-purpose microprocessors, domain-specific computer architectures are the only option left. An early example of this trend introduced by Google in 2015 is the Tensor Processing Unit (TPU) for cloud-based deep neural networking.

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ISSCC 2018

EVENING EVENTS

Evening Events

ISSCC 2018 will continue the popular tradition of evening panels and evening sessions, where experts, often of opposing views, discuss topics which range from the lighthearted to the controversial (but always informative and entertaining!). This year's panels are "Figures-of-Merit on Trial"; "Lessons Learned – Great Circuits That Didn't Work (Oops, If Only I Had Known!)"; and "Can Artificial Intelligence Replace My Job? – The Dawn of a New IC Industry with AI".

In addition, ISSCC 2018 will include additional evening events including a Workshop on Circuits for Social Good and an Industry Showcase.

Evening Panel: Figures-of-Merit on Trial

Monday, February 12

This panel will probe the weaknesses and strengths of popular analog FoMs in an entertaining and educational way: To this end, the room will become a tribunal with the moderator as judge. For each FoM on trial, two panelists will officiate, one becoming the defending advocate of the FoM, and the other the prosecutor, while the audience will become the jury, that will decide which of the two contestants will win.

Evening Panel: Lessons Learned – Great Circuits That Didn't Work (Oops, If Only I Had Known!)

Tuesday, February 13

Working on your first (or last) IC can be exciting, stressful, rewarding, and embarrassing. Whatever the lesson learned, be assured that it was experienced by pioneers before you. Failures (mistakes or just bad ideas!) can be valuable learning experiences, but are rarely revealed. Tonight, we provide an opportunity for recognized experts to share their past mistakes and failures, and disclose lessons learned. After the panelists have confessed, the audience can also contribute "learning experiences" (in less than a minute). Inevitably, this collection of revelations will be motivating: inspiring to the young and inexperienced; and virtuous for gurus in sharing a universal truth – first-time perfection is rare!

Evening Panel: Can Artificial Intelligence Replace My Job? – The Dawn of a New IC Industry with AI

Tuesday, February 13

The emergence of artificial intelligence (AI) capable of human tasks and more and better, is approaching fast. Shortly, most businesses, including the IC industry, will choose AI over humans, if AI can deliver the same results with lower risks and costs. Consequently, many questions arise for us: what will be the respective roles of AI and humans in developing ICs? How will AI shape the IC industry? What is the right career choice for young people in the field? This panel will showcase diverse experts who will share their vision on this daunting new development in our business.

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Workshop on Circuits for Social Good

Sunday, February 11

The Workshop on Circuits for Social Good highlights various ways that circuits can help address some of the most important challenges facing society today, ranging from health care to energy conservation.

The program aims to give a broad perspective of how one can have impact. It begins with several keynotes and invited talks from industry, academia and startups followed by interactive round-table discussions on topics including machine learning, medical devices, next generation communications, security and IoT, as well as discussions on career paths in research, product development, and entrepreneurship.

Industry Showcase

Monday, February 12

This year, for the first time, ISSCC will hold an Industry Showcase event on the evening of Monday, February 12th, which will highlight how advances in silicon circuits, SoCs and systems are fueling the most innovative industrial applications and products of the future. The event will feature short presentations as well as interactive demonstrations from each of the Industry Showcase participants, and represent an exciting introduction to the next generation of applications and products enabled by advances in solid-state integrated circuits.

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ISSCC 2018

SESSION OVERVIEWS AND HIGHLIGHTS

Conditions of Publication

PREAMBLE

The Session Overviews and Highlights to follow serve to capture the context, highlights, and potential impact, of the papers to be presented in each Session at ISSCC 2018 in February in San Francisco

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- That you will maintain at least one reference to ISSCC 2018 in the body of your text, ideally retaining the date and location. For detail, see the FOOTNOTE below.
- That you will provide a courtesy PDF of your excerpted press piece and particulars of its placement to press_relations@isscc.net

FOOTNOTE

- From ISSCC's point of view, the phraseology included in the box below captures what we at ISSCC would like your readership to know about this, the 65th appearance of ISSCC, on February 11th to February the 15th, 2018, in San Francisco.

> This and other related topics will be discussed at length at ISSCC 2018, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 11 - February 15, 2018,
>
> at the San Francisco Marriott Marquis Hotel.

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Session 2 Overview: Processors

Digital Architectures and Systems Subcommittee

Session Chair: *Thomas Burd, AMD, Sunnyvale, CA*

Session Co-Chair: *Muhammad Khellah, Intel, Hillsboro, OR*

Subcommittee Chair: *Byeong-Gyu Nam, Chungnam National University, Korea, DAS*

Continued growth in cloud-to-edge applications driving innovations in digital processors. The first two papers of this session cover next-generation server-class processors. This is followed by an energy-efficient 14nm graphics processor. An SoC configurable with 1-4 chips on an MCM to service multiple markets is described next. The last three papers demonstrate the first implementation of the datagram transport layer security (DTLS) protocol in hardware, an MSP430-compatible microcontroller with dual-mode enabling minimum-power and minimum-energy, and a net-zero-energy (NZE) smart mote SiP for IoT applications.

- In Paper 2.1, Intel describes SkyLake-SP Xeon, a 28-core server-class CPU in a 14nm tri-gate process featuring a MESH on-die interconnect fabric, on-die IVRs, and 6 DDR4 channels capable of 2667GT/s per channel.

- In Paper 2.2, IBM presents a 14nm FinFET z14, with 50% more L2 cache, 2× larger L3 caches, 25% more cores, enhanced branch prediction, and cryptography, running 200MHz faster than the previous generation under the same power envelope.

- In Paper 2.3, Intel describes a 14nm graphics processor featuring fine-grain DVFS with execution-unit turbo and retentive sleep, enabling up to 30% energy reduction at iso-performance.

- In Paper 2.4, AMD describes “Zeppelin”, a chiplet-architected SoC manufactured using14nm FinFET technology, with eight x86 “Zen” cores per chip. Configurable with one-to-four die in a multi-chip module (MCM), individual chiplets are connected in a range of products with AMD’s coherent Infinity Fabric.

- In Paper 2.5, MIT presents the first implementation of the datagram transport layer security (DTLS) protocol in a 65nm 4mm^2 test chip, resulting in a 10× reduction in code size and a 438× improvement in energy-efficiency over a software solution.

- In Paper 2.6, the National University of Singapore presents an MSP430 microcontroller enabling minimum-power (595pW) and minimum-energy mode (14-33pJ/cycle) in a 9.5mm^2 180nm chip with cold start up from a 0.54mm^2 solar cell at 55lux.

- In Paper 2.7, Intel demonstrates a complete cm-scale self-powered and secure IoT edge mote in 14nm, with 0.2mW (idle), 25mw (peak) power consumption integrated with an x86 core, CNN and crypto engines, sub-mW wake-up radio, and a 512KB memory, operable from 200KHz-950MHz.

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Session 2 Highlights: Processors

[2.1] SkyLake-SP: A 14nm 28-Core Xeon Processor

Paper 2.1 Authors: Simon Tam, Harry Muljono, Min Huang, Sitaraman Iyer, Kalapi Royneogi, Nagmohan Satti, Rizwan Qureshi, Wei Chen, Tom Wang, Hubert Hsieh, Sujal Vora, Eddie Wang

Paper 2.1 Affiliation: Intel Corporation, Santa Clara, CA

[2.2] IBM z14TM: A 14nm Microprocessor for the Next-Generation Mainframe

Paper 2.2 Authors: Christopher Berry[1], James Warnock[2], John Isakson[3], John Badar[4], Brian Bell[1], Frank Malgioglio[1], Guenter Mayer[5], Dina Hamid[1], Jesse Surprise[1], David Wolpert[1], Ofer Geva6, Bill Huott[1], Leon Sigal[2], Sean Carey[1], Richard Rizzolo[1], Ricardo Nigaglioni[3], Mark Cichanowski[3], Dureseti Chidambarrao[7], Christian Jacobi[1], Anthony Saporito[1], Arthur O'neill[1], Robert Sonnelitter[1], Christian Zoellin[1]

Paper 2.2 Affiliation: [1]IBM Systems, Poughkeepsie, NY, [2]IBM Systems, Yorktown Heights, [3]IBM Systems, Austin, [4]IBM Systems, Rochester, MN, [5]IBM Systems, Boeblingen, Germany, [6]IBM Systems, Tel Aviv, Israel, [7]IBM Systems, Hopewell Junction, NY.

[2.4] "Zeppelin": An SoC for Multichip Architectures

Paper 2.4 Authors: Noah Beck[1], Sean White[1], Milam Paraschou[2], Samuel Naffziger[2]

Paper 2.4 Affiliation: [1]AMD Boxborough, MA, [2]AMD, Fort Collins, CO

Subcommittee Chair: Byeong-Gyu Nam, Chungnam National University, Daejeon, Korea, DAS

CONTEXT AND STATE OF THE ART

- Increasing core counts and advanced 14nm process technology in server microprocessors continue to provide higher performance and efficiency in hyper scale data centers.
- Advances in cryptography acceleration enable secure computing.
- Multichip module (MCM) package technology enables flexibility to address the different power and performance requirements of the mainstream and high-performance desktop, and server markets.

TECHNICAL HIGHLIGHTS

- **Intel announces 28-core 14nm Xeon processor with on-die MESH interconnect and 6 DDR4 channels**
- Intel describes the SkyLake-SP Xeon processor, a server-class CPU with 28 cores in 11 metal layers in 14nm tri-gate process technology. The processor has a two dimensional MESH on-die interconnect fabric serving the cores. Multiple on-die power planes are serviced by on-die fully integrated voltage regulars. Additional on-die capabilities include 6 DDR4 channels offering 2667GT/s per channel, 10.4GT/s processor-to-processor UPI links and PCI links.

- **IBM introduces the z14TM processor in 14nm with 25% more cores and advanced cryptography acceleration**
- IBM presents the next generation z14TM processor designed in 14nm. This processor has 50% more L2 cache, 2× the amount of L3 cache, 25% more cores, runs 200MHz faster than previous designs, while maintaining the same power envelope. It also has significant microarchitectural updates for branch prediction, cache management and cryptography.

- **AMD's "Zeppelin" SoC provides a flexible building block for multichip modules with configurations suitable for mainstream and high-end desktops, and servers.**
- AMD describes "Zeppelin", an SoC architected as a chiplet, configurable with one to four chips in an MCM to serve multiple markets, including servers, mainstream desktops, and high-end desktops. Utilizing 14nm FinFET process technology, the SoC

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has over 4.8B transistors on a 213mm^2 die. Each die contains eight x86 cores, 16MB of L3 cache, memory and I/O controllers, and integrated Southbridge capabilities. These functions are connected on the SoC and between chips with the new AMD coherent Infinity Fabric.

APPLICATIONS AND ECONOMIC IMPACT

- Next-generation server class microprocessors showcase 14nm technology, providing leadership performance and security.
- Multichip module (MCM) package technology enables building-block processors to be uniquely packaged to address the different power/performance requirements of mainstream and high performance desktop, and server markets.
- Three separate methods of processor integration and scalability provide flexible solutions across the system space. The multichip module method of integration allows for a single die design to span various market segments with improved yield and cost. Likewise, two-dimensional meshes allow for increased performance of many-core systems on a single die. Finally, system-level integration continues to provide significant advancements in security and processing power.

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Session 3 Overview: Analog Techniques

Analog Subcommittee

Session Chair: *Youngcheol Chae, Yonsei University, Seoul, Korea*

Session Co-Chair: *Mahdi Kashmiri, Robert Bosch, CA*

Subcommittee Chair: *Kofi Makinwa, Delft University of Technology, Delft, The Netherlands*

Analog techniques continue to defy simple categories. This session illustrates the diversity and vigor of modern analog circuitry. Entries span the range of amplifiers, Class-D audio, references, programmable filters and oscillators. New frontiers of precision, power, and performance are established. The first paper describes a low-noise voltage buffer with 0.6pA input current and 0.6μV offset. The second and third papers describe sub-0.5V operation of a crystal oscillator and an RC oscillator with Allan deviation floor down to 250ppb. The next three papers expand the performance of Class-D audio amplifiers in terms of power, THD+N, and quiescent current. The last paper describes a programmable FIR filter operating at 3.25GS/s.

- In Paper 3.1, Delft University of Technology presents an auto-zeroed stabilized voltage buffer with 0.6pA input current and 0.6μV offset. A digitally assisted offset-reduction scheme reduces its excess low-frequency (LF) noise while achieving a voltage noise of 29nV/√Hz.
- In Paper 3.2, the University of Macau presents a sub-0.5V 16/24MHz crystal oscillator for energy-harvesting BLE radios with only 14.2nJ startup energy and 31.8μW steady-state power.
- In Paper 3.3, Delft University of Technology presents an RC-based frequency reference that achieves an inaccuracy of ±250ppm from -45°C to 85°C and an Allan Deviation floor of 250ppb.
- In Paper 3.4, Qualcomm presents a 2×20W Class-D amplifier with a peak THD+N of 0.0013% and a 0.006% THD+N at its full power level. The feedback path only needs to process the error signal between the reference and output and thus the performance at full power level is enhanced by coefficient adjustment, lowering the loop order, and freezing the modulation index.
- In Paper 3.5, MediaTek presents a 3.15W Class-D amplifier achieving 0.0004% (-108dB) THD+N and 112dB SNR (A-weighted). Such high linearity is achieved with negative output-common-mode injection and G_m noise-cancellation techniques.
- In Paper 3.6, National Cheng Kong University presents a Class-D audio amplifier that proposes a PWM-residual-aliasing reduction technique, providing about 33% quiescent current reduction.
- In Paper 3.7, Virginia Tech presents a 3.25GS/sec 4th-order programmable FIR filter for wideband analog signal processing in 32nm SOI CMOS technology. Split CDACs are used to generate the programmable coefficient multipliers providing high linearity up to the Nyquist rate.

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Session 3 Highlights: Analog Techniques

[3.4] A 2×20W 0.0013% THD+N Class-D Audio Amplifier with Consistent Performance up to Maximum Power Level

[3.5] A 0.0004% (-108dB) THD+N, 112dB-SNR, 3.15W Fully Differential Class-D Audio Amplifier with G_m Noise Cancellation and Negative Output-Common-Mode Injection Techniques

Paper 3.4 Authors: *Julian Aschieri, Eric Cope, Tony Lai, Franklin Zhao, Walter Grandfield, Pete Rathfelder, Michael Clifford, Qiyuan Liu, Siddartha Kavilipati, Aaron Vandergriff, Gerald Miaille*

Paper 3.4 Affiliation: *Qualcomm, Tempe, AZ*

Paper 3.5 Authors: *Wen-Chieh Wang, Yu-Hsin Lin*

Paper 3.5 Affiliation: *MediaTek, Hsinchu, Taiwan*

Subcommittee Chair: *Youngcheol Chae, Yonesi University, Seoul, Korea, Analog Subcommittee*

CONTEXT AND STATE OF THE ART

- By processing only the error signal, error-feedback Class-D amplifiers enhance audio quality by maintaining their performance at full power levels (20W). Furthermore, improved noise and linearity, up to 0.0004% THD+N, is obtained through the use of noise cancellation and linearity-enhancement techniques.

TECHNICAL HIGHLIGHTS

20W Class-D amplifier achieving 0.006% THD+N.

- In Paper 3.4, Qualcomm presents a 2×20W Class-D amplifier with a peak THD+N of 0.0013% and a 0.006% THD+N at its full power level. The feedback loop only needs to process the error signal between the reference and output. Performance at full power levels is enhanced by coefficient adjustment, lowering the loop order, and freezing the modulation index.

Class-D amplifier achieving 0.0004% (-108dB) THD+N.

- In Paper 3.5, MediaTek presents a 3.15W Class-D amplifier achieving 0.0004% (-108dB) THD+N and 112dB SNR (A-weighted). Such high linearity is achieved with the help of negative output-common-mode injection and G_m noise-cancellation techniques.

APPLICATIONS AND ECONOMIC IMPACT

- Class-D amplifiers approach the performance of linear amplifiers, but at higher efficiency levels, enabling more power-efficient systems with less dissipation and feature size.

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Session 4 Overview: mm-Wave Radios for 5G and Beyond

Wireless Subcommittee

Session Chair: *Chun-Huat Heng, National University of Singapore, Singapore*

Session Co-Chair: *David McLaurin, Analog Devices, NC*

Subcommittee Chair: *Stefano Pellerano, Intel, Hillsboro, OR, Wireless*

Millimeter-wave beamforming and full-duplex techniques are increasingly important for 5G and next-generation radio systems. This session includes two papers describing architectures and techniques for 5G basestations, two massive MIMO papers with tileable phased-array chips scalable to hundreds of elements, an eight-element receiver supporting autonomous analog beam steering, a reconfigurable receiver for concurrent dual-band or multi-stream operation, and a full-duplex transceiver sharing a single self-interference-cancelling antenna.

- In Paper 4.1, Analog Devices presents an invited paper on various architectures and technologies for 5G mm-wave radios. Popular architectures are discussed together with related process technologies, and opportunities for innovation in mm-wave circuit integration for future systems will be explored.
- In Paper 4.2, Broadcom presents a 144-element phased-array transceiver using a tiled approach in 28nm CMOS for 802.11ad. It has 51dBm EIRP and supports scan angle of ±60° in azimuth and ±10° in elevation.
- In Paper 4.3, the Georgia Institute of Technology describes a 23-to-30GHz 8-element receiver supporting autonomous spatial signal tracking or blocker rejection. It achieves 1-to-2μs response time for beamforming on the desired signal.
- In Paper 4.4, Qualcomm proposes a 28nm, 28GHz CMOS phased-array transceiver supporting 12 elements each on 2 MIMO layers targeting 5G basestations. It attains TX P_{out} of 8dBm per element, 12% PAE including an integrated switch, and RX NF<5dB.
- In Paper 4.5, Carnegie Mellon University presents a reconfigurable multimode 28/37GHz 4-element hybrid beamforming receiver supporting either concurrent dual-band or multistream single-band operation. The receiver incorporates an LMS-like beam-steering adaptation technique, and achieves 35dB image rejection.
- In Paper 4.6, Bell Laboratories describes a scalable mm-wave transceiver with eight receive elements and sixteen transmit elements per tile in 0.18μm SiGe. It achieves >8dBm P_{sat} per element, <0.25W per TX or RX element, and is potentially scalable to >100 elements.
  In Paper 4.7, the Georgia Institute of Technology proposes a 64GHz full-duplex transceiver sharing a single on-chip multiport self-interference-cancelling antenna. The multiport antenna attains >35dB TX-to-RX isolation across 60 to 75GHz, and total front-end SIC > 60dB across 63 to 65GHz.

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Session 4 Highlights: mm-Wave Radios for 5G and Beyond

[4.2] A 60GHz 144-Element Phased-Array Transceiver with 51dBm max EIRP and ±60° Beam Steering for Backhaul Application

[4.7] A 64GHz Full-Duplex Transceiver Front-End with an On-Chip Multiport Self-Interference-Cancelling Antenna and an All-Passive Canceller Supporting 4Gb/s Modulation in One Antenna Footprint

Paper 4.2 Authors: *Tirdad Sowlati, Saikat Sarkar, Bevin Perumana, Wei Liat Chan, Bagher Afshar, Michael Boers, Donghyup Shin, Timothy Mercer, Wei-hong Chen, Anna Papio Toda, Alfred Grau Besoli, Seunghwan Yoon, Sissy Kyriazidou, Phil Yang, Vipin Aggarwal, Nooshin Vakilian, Dmitriy Rozenblit, Masoud Kahrizi, Joy Zhang, Alan Wang, Padmanava Sen, David Murphy, Ali Sajjadi, Alireza Mehrabani, Brima Ibrahim, Bo Pan, Kevin Juan, Shelley Xu, Claire Guan, Guy Geshvindman, Khim Low, Namik Kocaman, Hans Eberhart, Koji Kimura, Igor Elgorriaga, Vincent Roussel, Hongyu Xie, Leo Shi, Venkat Kodavati*

Paper 4.2 Affiliation: *Broadcom, Irvine, CA*

Paper 4.7 Authors: *Taiyun Chi, Jong Seok Park, Sensen Li, Hua Wang*

Paper 4.7 Affiliation: *Georgia Institute of Technology, Atlanta, GA*

Subcommittee Chair: *Stefano Pellerano, Intel, Hillsboro, OR, Wireless*

CONTEXT AND STATE OF THE ART

- Millimeter-wave antenna arrays allow fine beamsteering with large radiated power and compact size. Scalability of arrays to hundreds of elements is required to extend the range of >60GHz transceivers for wireless backhaul applications.
- Full-duplex (FD) techniques can improve spectral efficiency and have the potential to double the data-rate for wireless systems. While state-of-the-art FD has been demonstrated with off-chip antennas, FD with on-chip antennas enables higher integration for short-range mm-wave radios.

TECHNICAL HIGHLIGHTS

Scalable mm-wave transceiver enables phased arrays with 144 antennas for wireless backhaul applications

- In Paper 4.2, Broadcom presents a 144-element phased-array transceiver using a tiled approach in 28nm CMOS for 802.11ad. It has 51dBm radiated power and supports scan angle of 60° in azimuth and 10° in elevation.

Millimeter-wave full-duplex transceiver achieving self-interference cancellation with an integrated multi-port antenna

- In Paper 4.7, the Georgia Institute of Technology proposes a 64GHz full-duplex transceiver with a multiport self-interference-cancelling (SIC) antenna integrated on-chip. The multiport antenna attains >35dB TX-to-RX isolation across 60 to 75 GHz, and total front-end SIC > 60dB across 63 to 65 GHz.

APPLICATIONS AND ECONOMIC IMPACT

- Millimeter-wave massive MIMO systems could provide the high throughput required for 5G wireless backhaul and last-mile Gb/s internet connectivity. Highly integrated phased antenna arrays with >100 elements can enable low-cost solutions for these applications.

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- Full-duplex transceivers have the potential to double the data-rate of mm-wave wireless links and improve the sensitivity of radars. A highly efficient integrated antenna with self-interference cancellation could reduce cost and power consumption in these systems.

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Session 5 Overview: Image Sensors

IMMD Subcommittee

Session Chair: *Hayato Wakabayashi, Sony Electronics, San Jose, CA*

Session Co-Chair: *Makoto Ikeda, University of Tokyo, Tokyo, Japan*

Subcommittee Chair: *Makoto Ikeda, University of Tokyo, Tokyo, Japan*

The session presents advances in image sensors covering BSI, global shuttering, organic photoconductive film, pixel scaling, dynamic vision, high frame rate imaging, 3D time-of-flight, and SPADs. The first paper, by Sony, presents a BSI global shutter with in-pixel ADC. Then, Panasonic presents a global shutter using organic film with in-pixel noise cancellation. Samsung presents a 0.9μm pixel with complete deep-trench isolation. Sony presents a low-power event-driven imager with motion detection. TSMC presents a 13.5Mpixel BSI image sensor with a readout subsampling architecture that allows 514fps at 720p. NHK presents a high-speed image sensor achieving 8K video up to 480fps. Toshiba presents a LiDAR SoC enabling range measurements up to 200m. Microsoft presents a BSI time-of-flight image sensor with 3.5μm global-shutter pixels with modulation frequencies up to 320MHz. Delft University presents a direct time-of-flight image sensor with modular SPAD-based pixel arrays fabricated in 3D-stacked 45/65nm CMOS. Finally, FBK presents a SPAD array coupled with TDCs to measure spatial correlations of entangled photons at a rate of 800kHz.

- In Paper 5.1, Sony presents a 1.46MP BSI global shutter CMOS image sensor using a pixel-parallel single-slope ADC. Using a Cu-Cu bonding pixel unit, positive feedback, and the digital bucket relay of a repeater through multistage flip-flop connection, all pixels are converted simultaneously with a 14b single-slope ADC having a size of $6.9\times6.9μm^2$, in a subthreshold region with operating current of 7.74nA.
- In Paper 5.2, Panasonic presents an 8K4K resolution organic photoconductive film CMOS image sensor operating in both rolling shutter and global shutter mode at 60fps using in-pixel capacitive-coupled noise cancelation. The noise canceller is also used to expand the full-well capacity up to 450ke- with a density of $50ke^-/μm^2$, which is 10dB higher than that of a silicon global-shutter CMOS image sensor.
- In Paper 5.3, Samsung presents a 1/2.8-inch 24Mpixel CMOS image sensor with 0.9μm unit pixels separated by full-depth DTI. Full-well capacity is increased up to 6,000e-, which is even larger than a conventional 1.0μm pixel; dark noise characteristics are also improved. Better optical performance is also achieved by using an optimized back-side design and a higher aspect ratio of full-depth DTI.
- In Paper 5.4, Sony presents a 1/4-inch 3.9Mpixel low-power event-driven back-illuminated stacked CMOS image sensor deployed with a readout circuit that detects motion for each pixel under lighting conditions from 1lux to 64,000lux. Utilizing pixel summation in a shared floating diffusion (FD) for each pixel block, moving object detection is realized at 10fps, while consuming only 1.1mW, a 99% reduction in power from the full resolution 60fps power of 95mW.
- In Paper 5.5, TSMC presents a new architecture to achieve 4× and 9× higher frame rates for 4-to-1 and 9-to-1 subsampled videos implemented in a 1.1um pitch, 13.5MP 3D-stacked CMOS image sensor using 1 bank of column ADCs. A digitally controlled column-switching matrix combined with a hard-wired vertical signal routing is designed to utilize all the ADCs in subsampling operation.
- In Paper 5.6, NHK presents a 2.1μm 33Mpixel CMOS image sensor for 8K video using a column-parallel 3-stage pipeline ADC composed of Folding-Integration (FI), dual-cyclic and SAR. In the 120fps 14b mode, the 6-times sampling in the FI and digital CDS reduce random noise and VFPN to 3.2e- and 0.24e-, respectively. In the 480fps mode, the dual-cyclic and SAR achieve 480fps operation.
- In Paper 5.7, Toshiba presents a TDC/ADC hybrid LiDAR SoC with a smart accumulation technique (SAT) to achieve 200m range imaging with 240×90 pixel resolution for reliable self-driving systems. The SAT using ADC information enhances the effective pixel resolution with an accumulation activated by recognizing only the target reflection, while the hybrid architecture enables a wide measurement range from 0 to 200m.
- In Paper 5.8, Microsoft presents a 1024×1024 Time-of-Flight image sensor with $3.5\times3.5μm^2$ global shutter pixels with analog binning in a TSMC 65nm 1P8M BSI CMOS image sensor process with modulation frequencies of up to 320MHz. The pixels have modulation contrast of 87%@200MHz, 78%@320MHz and QE=44%@860nm, while the readout chain implements adaptive gain with either 9b 3.4GS/s or 10b 1.7GS/s ADC.
- In Paper 5.9, Delft presents a direct time-of-flight image sensor with modular 2×8×8 SPAD-based pixel arrays, 14b range, 500μW, 60ps always-on TDCs shared through 6-level decision trees, in-pixel 21b memories, and in-locus data processing,

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fabricated in a 3D-stacked 45/65nm CMOS technology. A maximum distance of 430m and worst-case accuracy of 0.4% was recorded, while 256×256 3D images were obtained through laser scanning.

- In Paper 5.10, FBK presents a 32×32-pixel image sensor fabricated in standard 150nm CMOS, for the measurement of spatial correlations of entangled photons. Each 44.64μm pixel includes a SPAD coupled to a 205ps 8b TDC to correlate simultaneous photons. On-chip mechanisms allow the sensor to observe events at 800kHz and readout at 250kfps skipping irrelevant data.

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Session 5 Highlights: Image Sensors

[5.8] A 1Mpixel 65nm BSI 320MHz Demodulated TOF Image Sensor with 3.5µm Global Shutter Pixels and Analog Binning

Paper Authors: *Cyrus S Bamji, Swati Mehta, Barry Thompson, Tamer Elkhatib, Stefan Wurster, Onur Akkaya, Andrew Payne, John Godbaz, Mike Fenton, Vijay Rajasekaran, Larry Prather, Satya Nagaraja, Vishali Mogallapu, Dane Snow, Rich McCauley, Mustansir Mukadam, Iskender Agi, Shaun McCarthy, Zhanping Xu, Travis Perry, William Qian, Vei-Han Chan, Prabhu Adepu, Gazi Ali, Muneeb Ahmed, Aditya Mukherjee Sheethal Nayak, Dave Gampell, Sunil Acharya, Lou Kordus, Pat O'Connor*

Paper Affiliation: *Microsoft, Mountain View, CA*

Subcommittee Chair: *Makoto Ikeda, University of Tokyo, Tokyo, Japan, IMMD*

[5.1] A Back-Illuminated Global-Shutter CMOS Image Sensor with Pixel-Parallel 14b Subthreshold ADC

Paper Authors: *Masaki Sakakibara[1], Koji Ogawa[1], Shin Sakai[1], Yasuhisa Tochigi[1], Katsumi Honda[1], Hidekazu Kikuchi[1], Takuya Wada[1], Yasunobu Kamikubo[1], Tsukasa Miura[1], Masahiko Nakamizo[1], Naoki Jyo[2], Ryo Hayashibara[2], Yohei Furukawa[3], Shinya Miyata[3], Satoshi Yamamoto[1], Yoshiyuki Ota[1], Hirotsugu Takahashi[1], Tadayuki Taura[1], Yusuke Oike[1], Keiji Tatani[1], Takashi Nagano[1], Takayuki Ezaki[4], Teruo Hirayama[4]*

Paper Affiliation: *[1]Sony Semiconductor Solutions, Atsugi, Japan, [2]Sony Semiconductor Manufacturing, Kumamoto, Japan, [3]Sony LSI Design, Fukuoka, Japan, [4]Sony, Atsugi, Japan*

Subcommittee Chair: *Makoto Ikeda, University of Tokyo, Tokyo, Japan, IMMD*

CONTEXT AND STATE OF THE ART

- Global shutter enables simultaneous capture of an entire image, rather than the conventional rolling shutter approach. Global shutter is now realized using BSI and 3D-stacking for high-speed video, as well as for time-of-flight sensors. Global shutter is also implemented with organic photoconductive film, which concurrently offers extended dynamic range.
- The trend towards 3D-stacking for integration of the sensor layer and ASIC layer continues to increase functionality with smart motion detection and with increased subsampling modes for high frame rate imaging.
- High speed and high resolution continue to improve as demonstrated by 8K video at 480fps.
- SPADs used for direct time-of-flight and other modalities are now being implemented using BSI and 3D stacking.
- Range finding up to 200m using LiDAR with a smart accumulation advances the state of the art in depth sensing with increased effective pixel resolution.
- Pixel size continues to scale to 0.9µm with complete deep-trench isolation technology.

TECHNICAL HIGHLIGHTS

- **Microsoft presents a 1024×1024 Time-of-Flight image sensor with 3.5×3.5µm^2 global-shutter pixels with analog binning in a TSMC 65nm 1P8M BSI CMOS image sensor process with modulation frequencies of up to 320MHz.**
- The pixels have modulation contrast of 87%@200MHz, 78%@320MHz and QE=44%@860nm, while the readout chain implements adaptive gain with either 9b 3.4GS/s or 10b 1.7GS/s ADC.
- **Sony presents a 1.46MP BSI global-shutter CMOS image sensor using a pixel-parallel single-slope ADC.**
- Using a Cu-Cu bonding pixel unit, positive feedback, and the digital bucket relay of a repeater through multistage flip-flop connection, all pixels are converted simultaneously with a 14b single-slope ADC having a size of 6.9×6.9µm^2, in a subthreshold region with operating current of 7.74nA.

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APPLICATIONS AND ECONOMIC IMPACT

- The Microsoft BSI image sensor has the smallest pixel and highest resolution used in time-of-flight imaging. The applications anticipated are for gaming, virtual reality, augmented reality and the Internet of Things.
- The Sony high performance BSI global shutter implemented using in-pixel ADC is the first of its kind enabled by 3D-stacking technology. Scientific imaging and industrial automation applications are anticipated.

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Session 6 Overview: Ultra High Speed Wireline

Wireline Subcommittee

Session Chair: *Mounir Meghelli, IBM T.J. Watson Research, Yorktown Heights, NY*

Session Co-Chair: Hyeon-Min Bae, KAIST, Daejeon, Korea

Subcommittee Chair: *Frank O'Mahony, Intel, Hillsboro OR, Wireline*

High-speed serial I/Os continue to be pushed to higher bandwidth and density for every new generation of systems, which enable the scaling of data centers, fueled by a world that is becoming increasingly connected and digital. This session starts with the presentation of two low-power transmitters demonstrating a data rate of 112Gb/s using PAM-4 modulation, both implemented in advanced CMOS FinFet technologies. It continues with a presentation of a multi-standard 4-lane 1.25-to-28.05Gb/s transceiver designed in 14nm CMOS FinFET technology and supporting up to 40dB of channel loss at a power efficiency of 6pJ/b. Three papers describing PAM-4 transceivers are presented next, two implemented in 16nm CMOS FinFET technology targeting long reach links at 56Gb/s and 64Gb/s respectively, and one implemented in 28nm CMOS FDSOI targeting 64Gb/s short reach links. Finally, the session concludes with a paper describing a 4.16pJ/b 32Gb/s PAM-4 transceiver implemented in 65nm CMOS technology.

- In Paper 6.1, Intel presents a reconfigurable 56GS/s 3-tap FFE TX that operates up to 112Gb/s with PAM-4 or at 56Gb/s with NRZ. The transmitter employs a quarter-rate architecture, a 1UI pulse-generator-based 4-to-1 serializer combined with a CML driver, a multi-segment π-coil for pad bandwidth extension, and per-lane duty-cycle correction and quadrature-error correction circuits. Implemented in a 10nm FinFET CMOS technology, the TX achieves 2.07pJ/b efficiency at 112Gb/s with 0.0302mm^2 area.
- In Paper 6.2, IBM Research describes a 112Gb/s PAM-4 transmitter that is based on a quarter-rate 56GS/s 8b SST DAC along with a digital 8-tap FIR filter for channel equalization. Implemented in a 14nm bulk CMOS FinFET technology the circuit occupies an area of 0.095 mm^2 and consumes 286mW from a 0.95V supply.
- In Paper 6.3, Rambus presents a multi-standard, long-reach, low-power 4-lane 1.25-to-28.05Gb/s transceiver implemented in 14nm CMOS FinFET technology. By using a per-lane PLL-based CDR, the receiver supports independent data rate across the four lanes. Independent rate between the transmitter and the receiver of a single lane is also supported. The measured reach of this design is 40dB at 28.05Gb/s at a power efficiency of 6pJ/b. The area of each lane is 0.38mm^2.
- In Paper 6.4, Xilinx describes a 19-to-56Gb/s PAM-4 transceiver in 16nm FinFET. The transceiver features a fully adaptive receiver consisting of a multi-stage CTLE, a configurable 3-to-7b ADC, a 14-tap FFE/1-tap DFE DSP, and a baud-rate CDR. It also includes a 4-tap FIR voltage mode transmitter. For 56Gb/s transmission over a 32dB channel, the design achieves <1e-12 BER without explicitly added crosstalk and <1e-6 with 2mV$_{rms}$ of added crosstalk, while consuming 9.7pJ/b. With the ADC operating in 3b mode, the transceiver achieves 6.4pJ/b over a 7.4dB channel.
- In Paper 6.5, the University of Toronto presents a 64Gb/s PAM-4 transceiver including a 1.39pJ/b 1Vppd transmitter with 3-tap FFE and a 32GS/s 4.41pJ/b ADC-based receiver front-end with half-rate sampling CTLE and 6b ADC with 1b folding. The transmitter has programmable nonlinearity compensation and achieves an RLM of 99%, while generating 162fs$_{rms}$ jitter. The ADC quantizer is reconfigurable to allow power scaling over channels with 9-to-30dB loss. A greedy search algorithm is used to seek BER-optimal non-uniformly spaced quantizer thresholds.
- In Paper 6.6, STMicroelectronics describes a low-power PAM-4 transceiver in 28nm CMOS FDSOI, targeting CEI-56G-VSR applications. The voltage-mode transmitter yields larger eye openings compared to the current-mode alternative. The receiver includes CDR, eye monitor, adaptation logic and a flexible CTLE meeting the tight PAM-4 equalization demands through optimal adaptation at low, mid, and high frequency. A BER of 1e-12 is measured at 64Gb/s over a 16dB-loss channel with a power efficiency of 4.9pJ/b.
- In Paper 6.7, Peking University introduces a 32Gb/s 133mW PAM-4 transceiver implemented in 65nm CMOS. A one-tap DFE featuring a phase-adaptive clock is proposed to alleviate the tight timing constraints of the direct feedback implementation. The threshold voltages at the receiver slicers are adaptively optimized for different channels. Transmission over a 23dB loss channel achieves better than 1e-12 BER at a power efficiency of 4.16pJ/b.

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Session 6 Highlights: Ultra High Speed Wireline

[6.1] A 112Gb/s PAM-4 Transceiver with 3-Tap FFE in 10nm CMOS

[6.2] A 112Gb/s 2.6pJ/b 8-Tap FFE PAM-4 SST TX in 14nm CMOS

[6.4] A Fully Adaptive 19-to-56Gb/s PAM-4 Wireline Transceiver with a Configurable ADC in 16nm FinFET

Paper 6.1 Authors: *Jihwan Kim, Ajay Balankutty, Rajeev Dokania, Amr Elshzly, Hyung Seok Kim, Sandipan Kundu, Skyler Weaver, Kai Yu, Frank O'Mahony*

Paper 6.1 Affiliation: *Intel, Hillsboro, OR*

Paper 6.2 Authors: *Christian Menolfi[1], Matthias Braendli[1], Pier Andrea Francese[1], Thomas Morf[1], Alessandro Cevrero[1], Marcel Kossel[1], Lukas Kull1, Danny Luu[1,2], Ilter Ozkaya[1,3], Thomas Toifl[1]*

Paper 6.2 Affiliation: *[1]IBM Zurich Research Laboratory, Rueschlikon, Switzerland, [2]ETH Zurich, Switzerland, [3]EPFL, Lausanne, Switzerland*

Paper 6.4 Authors: *Parag Upadhaya[1], Chi Fung Poon[1], Siok Wei Lim[2], Junho Cho[1], Arianne Roldan[2], Wenfeng Zhang[1], Jin Namkoong[1], Toan Pham[1], Bruce Xu[1], Winson Lin[1], Hongtao Zhang[1], Nakul Narang[2], Kee Hian Tan[2], Geoff Zhang[1], Yohan Frans[1], Ken Chang[1]*

Paper 6.4 Affiliation: *[1]Xilinx, San Jose, CA, [2]Xilinx, Singapore, Singapore*

Subcommittee Chair: *Frank O'Mahony, Intel, Hillsboro, OR, Wireline*

CONTEXT AND STATE OF THE ART

- The data-rate of serial interfaces for chip-to-chip or chip-to-optics interconnects is projected to achieve 112Gb/s in order to meet increasing bandwidth demand in data centers and telecommunication infrastructures. Power and area efficiencies will continue to improve in order to meet the demand for higher bandwidth and achieve better energy efficiencies of data centers in particular.
- Next generation transceivers for 100Gb/s+ serial links will continue to explore the use of high-order modulation schemes, taking advantage of more advanced CMOS technology nodes for the implementation of efficient digital signal processing and high sampling rate analog-to-digital and digital-to-analog converters.

TECHNICAL HIGHLIGHTS

- **A low-power 112Gb/s transmitter implemented in 10nm FinFET.**
  In Paper 6.1, Intel presents a reconfigurable 56GS/s 3-tap FFE TX that operates up to 112Gb/s in PAM-4 mode or at 56Gb/s in NRZ mode. The transmitter, which employs a quarter-rate architecture, achieves 2.07pJ/bit power efficiency at the highest speed and fits in a 0.0302mm^2 area.

- **A DAC-based 112Gb/s low power PAM-4 Transmitter.**
  In Paper 6.2, IBM describes a 112Gb/s PAM-4 transmitter based on a quarter-rate 56GS/s 8b source-series terminated DAC along with a digital 8-tap FIR filter for channel equalization. Implemented in a 14nm bulk CMOS FinFET technology, the circuit occupies an area of 0.095 mm^2 and achieves a power efficiency of 2.6pJ/b at the highest speed.

- **Power efficient ADC-based 19-to-56Gb/s flexible transceiver in 16nm FinFET.**
  Xilinx describes a 19-to-56Gb/s PAM-4 transceiver. Its fully adaptive receiver consists in particular of a configurable 3-to-7b ADC, a digital 14-tap FFE/1-tap DFE, and a baud-rate-based clock and data recovery. The transmitter includes a 4-tap FFE and

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a voltage mode driver. Operating at 56Gb/s over a 32dB channel, the transceiver achieves a bit error rate below 1e-6 with 2mV_{rms} of added crosstalk while consuming 9.7pJ/b.

APPLICATIONS AND ECONOMIC IMPACT

- Continued performance scaling for datacenters and high-performance computing requires dense, power- and cost-efficient high-bandwidth data communication. The first two papers of the session are strong early demonstrations of serial data rate scaling to 112Gb/s.
- The third paper is showing that 56Gb/s PAM-4 transceivers for energy-efficient data transmission over lossy electrical links are achieving a higher maturity level and becoming readily available for the deployment of next generation systems.
- Advanced CMOS technology nodes will facilitate the increased use of high order digital modulation and sophisticated digital signal processing techniques, which are key to scaling the speed of serial data links. All 3 papers employ pulse amplitude modulation in FinFET technologies, and papers 6.2 and 6.4 are augmented by significant digital signal processing.

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Session 7 Overview: Neuromorphic, Clocking and Security Circuits

Digital circuits Subcommittee

Session Chair: *Youngmin Shin, Samsung Electronics Co., Hwaseung, Korea*

Session Co-Chair: *Phillip Restle, IBM, Yorktown Height, NY*

Subcommittee Chair: *Edith Beigne, CEA-LETI, Grenoble, France, Digital Circuits*

The eight papers in this session highlight developments in neuromorphic accelerator, clocking circuit and security building blocks. A highlighted paper demonstrates a neuromorphic accelerator with stochastic synapses and embedded online reinforcement learning in autonomous micro-robots. The clocking papers presented demonstrate an all-digital multiplying DLL, a synthesizable fractional-N PLL and a synthesizable period-jitter sensor. Improvements to random-number generators and physically unclonable functions provide lower error rates and lossless stabilization by a novel remapping scheme

- In Paper 7.1, the University of Macau presents an MDLL with an all-digital frequency tracking loop in 28nm CMOS occupying 0.0056mm^2. The frequency tracking loop consumes 0.3mW and the MDLL achieves 292fs integrated jitter with -249dB FoM.
- In Paper 7.2, Samsung Electronics describes a fully synthesizable period-jitter sensor that does not require a reference clock or calibration. Three jitter sensors with different sizes are fabricated in 10nm CMOS and they consume 1.5mW, 6mW, 24mW, respectively, and occupy 0.0012mm^2, 0.005mm^2 and 0.02mm^2, respectively.
- In Paper 7.3, Pohang University demonstrates a fractional-N ADPLL for DVFS with a frequency-tracking speculating dual-interpolation TDC. The PLL, implemented in 0.0043mm^2 with 28nm CMOS, achieves a wide frequency/voltage range without calibration. The PLL FoM is -225dBc/Hz at 2GHz 1.0V and -203dBc/Hz at 20MHz 0.3V.
- In Paper 7.4, Georgia Institute of Technology presents a 3.4mm^2 55nm CMOS test chip demonstrating online reinforcement learning in autonomous micro-robots. Ultra-low-power operation is achieved through time-domain mixed-signal circuit design and stochastic synaptic connections. Measured performance is 3.12TOPS/W and peak energy-efficiency is 1.25pJ/MAC.
- In Paper 7.5, National Chiao Tung University presents a buck converter in 55nm with a true random-number-based pseudo hysteresis controller enhancing security against power-side-channel attacks (PSCA) and power-injection attacks (PIA) simultaneously. Measured peak electromagnetic interference noise of 54.32dBμV meets the EN 55032 Class B requirement.
- In Paper 7.6, Carnegie Mellon University presents a secure camouflaged logic family to protect IP in ICs during manufacturing and defend against reverse engineering. A camouflaged 4b carry-select adder was implemented in 65nm bulk CMOS running at 3.6GHz at 1V V_{DD} and room temperature. Circuits can be performance-boosted or securely erased in the field.
- In Paper 7.7, eMemory presents a physically unclonable function (PUF) scheme using an oxide rupture mechanism with proved uniformly random and reliable output under varying operating conditions. Bit error rate is consistently low regardless of voltage, temperature, aging and fab corner in 55nm CMOS with a unit size of 0.66μm^2.
- In Paper 7.8, Sungkyunkwan University presents a leakage-based physically unclonable function (PUF) with 445F^2 area per bit in 180nm CMOS. Lossless stabilization is achieved by a remapping scheme, where PUF cells in unstable challenge-response pairs (CRPs) are remapped to construct stable CRPs, avoiding costly CRP loss in a conventional trimming approach. Lowest achieved BER is 0.004%.

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Session 7 Highlights:
Neuromorphic, Clocking, and, Security Circuits

[7.1] A 0.0056mm² All-Digital MDLL Using Edge Re-Extraction, Dual-Ring VCOs and a 0.3mW Block-Sharing Frequency Tracking Loop Achieving 292fs_{rms} Jitter and -249dB FOM

[7.4] A 55nm Time-Domain Mixed-Signal Neuromorphic Accelerator with Embedded Reinforcement Learning for Autonomous Micro-Robots

[7.8] A 445F² Leakage-Based Physically Unclonable Function with Lossless Stabilization Through Remapping for IoT Security

Paper 7.1 Authors: *Pui-In Mak[1], S.Yang[1], J.Yin[1], R.P.Martins[1,2],*

Paper 7.1 Affiliation: *[1]University of Macau, Macau, China, [2]Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal*

Paper 7.4 Authors: *A.Raychowdhury[1], A.Amravati[1], S.B.Nasir[1], S.Thangadurai[1], I.Yoon[1],*

Paper 7.4 Affiliation: *[1]Georgia Institute of Technology, Atlanta, GA*

Paper 7.8 Authors: *J.Lee[1], D.Lee[1], Yongmin.Lee[1], Yoonmyung.Lee[1],*

Paper 7.8 Affiliation: *[1]Sungkyunkwan University, Suwon, Korea*

Subcommittee Chair: *Edith Beigne, CEA-LETI, Grenoble, France, Digital Circuits*

CONTEXT AND STATE OF THE ART

- Low-power neuromorphic circuits can enable functions such as reinforcement learning for IoT devices.
- Providing important security functions, such as encryption/decryption, random-number generation, and others using hardware-based solutions offers excellent energy efficiency.
- Cryptography is one common security application performed on-chip – these building blocks are well known to be susceptible to reverse engineering, probing, and side-channel attacks, particularly the monitoring of current/power profiles to disclose secret keys.
- Post-manufacturing programmable circuits can camouflage logic and simultaneously obscure design IP from the manufacturer, as well as combat reverse engineering.
- Standard approaches to combat power-side-channel attacks involve high overhead techniques, such as differential circuit design or other non-conventional design styles. Seamless low-overhead strategies to obscure power profiles are therefore desirable.
- Synthesizing increasingly sophisticated digital PLLs (DPLLs) using standard design tools is advantageous in reducing design times and improves technology portability.
- It is valuable to sense clock jitter on-chip without the need for a reference clock using only synthesizable logic.

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TECHNICAL HIGHLIGHTS

University of Macau presents Macau presents a MDLL with an all-digital frequency tracking loop in 28nm CMOS

- In Paper 7.1, the University of Macau presents an MDLL with an all-digital frequency tracking loop in 28nm CMOS occupying 0.0056mm^2. The frequency tracking loop consumes 0.3mW and the MDLL achieves 292fs integrated jitter with -249dB FoM.

Georgia Institute of Technology shows neuromorphic chip with reinforcement learning in autonomous micro-robots

- In Paper 7.4, Georgia Institute of Technology presents design and measurement results for a 3.4mm^2 55nm CMOS test chip demonstrating online reinforcement learning in autonomous micro-robots. Ultra-low-power operation is achieved through time-domain mixed-signal circuit design and stochastic synaptic connections. Measured performance is 3.12TOPS/W, and peak energy efficiency is 1.25pJ/MAC.

Sungkyunkwan University presents a leakage-based PUF with remapping scheme and achieving very low BER

- In Paper 7.8, Sungkyunkwan University presents a leakage-based physically unclonable function (PUF) with 445F^2 area per bit in 180nm CMOS. Lossless stabilization is achieved by a remapping scheme, where PUF cells in unstable challenge-response pairs (CRPs) are remapped to construct stable CRPs, avoiding costly CRP loss in a conventional trimming approach. Lowest achieved BER is 0.004%.

APPLICATIONS AND ECONOMIC IMPACT

- With the increasing pervasiveness of IoT devices, data and IP security has become an important issue. Hardware encryption for secure data transfer and IP supply-chain protection is essential to prevent economic loss from individual identity theft, as well as attacks on infrastructure.
- Inexpensive secure data transfers reduce the cost of consumer transactions.
- Synthesizable digital PLLs and jitter sensors can use standard digital design tools to dramatically reduce design costs and improve technology portability.

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Session 8 Overview: Wireless Power and Harvesting

Power Management Subcommittee

Session Chair: *Yuan Gao, IME A*STAR, Singapore*

Session Co-Chair: *Zhiliang Hong, Fudan University, China*

Subcommittee Chair: *Axel Thomsen, Cirrus Logic, Austin TX, Power Management Subcommittee*

Innovations in energy harvesting continue to enhance power-conversion efficiency, reduce circuit self-startup voltage, and system static-power consumption. Various new energy sources including a triboelectric nanogenerator and MEMS AlN-on-Si piezoelectric harvesters have been reported. New design methodologies for wireless-power and piezoelectric-vibration-energy harvesting are improving the state of the art.

- In Paper 8.1, Oregon State University and Texas Instruments present a 2.4GHz antenna co-integrated wireless energy harvester powered by a WiFi radio. Implemented in 65nm CMOS, the circuit only consumes 960pW and achieves sensitivity of -34dBm in normal mode and -31dBm in cold-start mode.
- In Paper 8.2, National Chiao Tung University presents a 6.78MHz GaN-based Class-E wireless-power system. A dual-loop control for automatic matching-point searching and linearization-compensation-capacitance tuning is proposed. Peak efficiency up to 90% is achieved under 70W output power.
- In Paper 8.3, University of Macau presents a 6.78MHz cross-coupled reconfigurable wireless-power transceiver for device-to-device (D2D) charging. With the proposed near-optimum switch-timing control schemes, the peak D2D total efficiency is 78.1% and the maximum charging power is 2.7W.
- In Paper 8.4, Fudan University presents a 13.56MHz wireless power- and data-transfer receiver for implantable biomedical devices. To avoid the efficiency reduction due to the large AM modulation depth and to maintain RX low-power consumption, the receiver with shifted limiters is co-designed with an active rectifier using dynamic impedance matching and adaptive conversion-ratio tuning. Power conversion efficiency of 75.4% at 0.1% AM MD is achieved.
- In Paper 8.5, University of California, San Diego, presents a multi-input single-inductor multi-output energy harvester employing event-driven MPPT control to achieve 89% peak efficiency and a 60,000× dynamic range in a 28nm FDSOI process.
- In Paper 8.6, Korea University presents a triboelectric energy-harvesting system based on a high-voltage dual-input buck converter with a maximum power-point analysis. Implemented in a 0.18µm CMOS BCD process, the input voltage ranges up to 70V, and the maximum power conversion efficiency is 51.1%.
- In Paper 8.7, University of Freiburg presents an interface circuit for piezoelectric energy harvesting with fully autonomous conjugate-impedance matching. Implemented in a 0.35µm CMOS, the bandwidth is increased by 156% over the natural frequency of the circuit, and the power output at the resonant frequency is increased by 26%.
- In Paper 8.8, CEA-LETI-MINATEC presents an SECE piezoelectric energy-harvesting interface circuit in 40nm CMOS. The circuit is optimized to work under shock stimulus and features a 30nA quiescent current in sleep mode and an event-driven sequencing in harvesting mode. The peak end-to-end efficiency is 94%, and the circuit can harvest vibrations in the 80nW-to-14mW power range with up to 10V input voltage.
- In Paper 8.9, University of Cambridge presents an inductorless split-electrode-synchronized-switch harvesting-on-capacitors (SE-SSHC) rectifier, fully integrated in 0.18µm CMOS, for piezoelectric energy harvesting. Co-integrated with a custom MEMS device comprising of a split-electrode topology, up to 821% of power-harvesting improvement is demonstrated with a peak power of 186µW.
- In Paper 8.10, KAIST presents a 13.56MHz time-interleaved resonant-voltage-mode wireless-power receiver in 0.18µm CMOS. The resonant-capacitor-interleaving scheme isolates the LC tank from the output and maintains optimal power transfer regardless of the operation phase. The circuit achieves the maximum receiver efficiency of 67.8%.

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Session 8 Highlights: Wireless Power and Harvesting

[8.1] A 960pW Antenna Co-Integrated Wireless Energy Harvester for WiFi Backchannel Wireless Powering

Paper Authors: *K. Sadagopan[1], J. Kang[1], Y. Ramadass[2], A. Natarajan[1]*

Paper Affiliation: *[1]Oregon State University, Corvallis, OR, [2]Texas Instruments, Santa Clara, CA*

Subcommittee Chair: *Axel Thomsen, Cirrus Logic, Austin TX, Power Management Subcommittee*

CONTEXT AND STATE OF THE ART

- Leveraging the ubiquitous WiFi infrastructure to wirelessly power sensors can enable perpetually powered sensors with long lifetimes for several monitoring and asset-tracking Internet-of-Everything applications.

TECHNICAL HIGHLIGHTS

Energy-harvesting devices drawing power from ambient low-level WiFi signals

- Record sensitivity for wireless energy harvester in the 2.4GHz band. The devices demonstrates 1.5× better sensitivity than prior devices while enabling optimal power extraction from a WiFi beacon.
- The circuit only consumes 960pW and operates from an input power level of -34dBm in normal mode and -31dBm in cold-start mode.

APPLICATIONS AND ECONOMIC IMPACT

- Harvesting from WiFi is one of the most promising energy-harvesting solutions. Increased efficiency due to the antenna-rectifier co-design and sub-nano-power design are the key to enabling energy-autonomous tiny IoE nodes.

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Session 9 Overview: Wireless Transceivers & Techniques

Wireless Subcommittee

Session Chair: *Alan Wong, EnSilica, United Kingdom*

Session Co-Chair: *Xin He, NXP, Netherlands*

Subcommittee Chair: *Stefano Pellerano, Intel, Hillsboro, OR, Wireless*

Wireless technologies continue to penetrate and support a wide range of application areas. This session includes state-of-the-art wireless transceivers for car radar, synthetic-aperture imaging radar, RF-to-bits cellular base stations, and 60GHz dual polarization MIMO. Furthermore, wireless techniques to enhance performance are presented, including a full duplex self-interference-cancellation FDD transceiver, an automatic tracking 3flo suppression notch filter technique for LTE HPUE and a high-efficiency outphasing PA using a triaxial balun combiner.

- In Paper 9.1, Texas Instruments describes an RF-to-bits 3TX/4RX automotive radar transceiver operating at 76 to 81GHz implemented in 45nm CMOS. The 10dBm TX has binary and linear phase modulation for MIMO and beamforming; a 15MHz BW I/Q RX has <18dB NF and a PLL chirp generator delivering <-91dBc/Hz phase noise with 4GHz ramps at up to 100MHz/µs.
- In Paper 9.2, Nanyang Technological University describes a 4×4 phased-array transceiver implemented in 65nm for airborne/spaceborne Synthetic Aperture Radar Imaging reporting <30cm resolution. The TX has 14.7dBm output power, <2dB ripple, 1GHz chirp bandwidth and 1-to-10MHz/µs tunable chirp rate while the RX attains –37dBm IP_{1dB} and 5.7-to-6.5dB NF.
- In Paper 9.3, Analog Devices describes a wideband 65nm CMOS direct-conversion 2RX/2TX/1FBRX RF-to-bits basestation transceiver with operating bandwidths of 200/450/450MHz for 2G/3G/4G/5G macro basestations. For FDD systems the TRX achieves >90dB in-band SFDR for GSM blocker scenarios and <-85dBc non-IM3 in-band TX emissions.
- In Paper 9.4, Intel describes a 60GHz receiver baseband that supports dual polarization MIMO. The work presents a mixed-signal 384-coefficient FFE and 2400-coefficient DFE-based area-efficient receiver baseband, integrated with CDR. The prototype supports up to 40Gb/s LOS 16QAM and 14GB/s NLOS QPSK and is implemented in 28nm CMOS.
- In Paper 9.5, Intel describes a 60GHz dual-polarization MIMO transceiver. It utilizes orthogonal polarization modes to enable simultaneous independent data streams. Using two TX/RX with a single PCB antenna, the work demonstrates over-the-air 2×13.9Gb/s 16QAM.
- In Paper 9.6 the Tokyo Institute of Technology presents a wideband transceiver achieving 120Gb/s data-rate 16QAM. It simultaneously up/downconverts two 15GHz signal channels located at 70GHz and 105GHz. The 70GHz and 105GHz LO signals are generated by a doubler and a tripler from an external 35GHz source.
- In Paper 9.7, the University of Washington describes a full duplex transceiver with integrated balance duplexer. Together with two feedforward self-interference-cancellation signal paths, it achieves cancellation of 70dBc (40MHz BW) and 65dBc (80MHz BW), with an RX NF degradation of 1.6dB at 12.5dBm PA output power at around 1.8GHz.
- In Paper 9.8, Samsung Electronics presents a 1.4~to~2.7GHz transmitter with automatic tracking 3flo notch filter at mixer output to lower CIM3. At 5.1dBm output for LTE PC2 HPUE it achieves -54.4dBc CIM3 while consuming 136.8mW DC power.
- In Paper 9.9, the University of California, San Diego describes a 28GHz outphasing PA using a triaxial balun as the low loss Chireix combiner. The SiGe PA reaches a saturated output power P_{sat} of 23dBm from a 4V supply with a peak PAE of 41% at 21dBm and a PAE of 34.7% at 6dB backoff.

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Session 9 Highlights: Wireless Transceivers & Techniques

[9.1] A Multimode 76-to-81GHz Automotive Radar Transceiver with Autonomous Monitoring

Paper Authors: *B. Ginsburg[1], K. Subburaj[2], S. Samala[1], K. Ramasubramanian[2], J. Singh[2], S. Bhatara[2], S. Murali[2], D. Breen[1], M. Moallem[1], K. Dandu[1], S. Jalan[3], N. Nayak[1], R. Sachdev[2], I. Prathapan[2], K. Bhatia[1], T. Davis[1], E. Seok[1], H. Parthasarathy[2], R. Chatterjee[2], V. Srinivasan[1], V. Giannini[4], A. Kumar[2], R. Kulak[1], S. Ram[2], P. Gupta[2], Z. Parkar[2], S. Bharadwaj[2], Y. Rakesh[2], K. A. Rajagopal[2], A. Shrimali[2], V. Rentala[1]*

Paper Affiliation: *[1] Texas Instruments, Dallas, TX*

[2] Texas Instruments, Bangalore, India

[3] Intel, Bangalore, India

[4] Uhnder, Austin, TX

Subcommittee Chair: *Stefano Pellerano, Intel, Hillsboro, OR, Wireless*

CONTEXT AND STATE OF THE ART

- Enabling autonomous driving in future automobiles will require car radar systems with long range and strong detection capability while achieving low cost and robustness
- Automotive radar is currently focused on BiCMOS implementations in the 76-to-81GHz radar band

TECHNICAL HIGHLIGHTS

A fully-integrated 76-to-81GHz CMOS ADAS radar transceiver with high resolution and flexible multi-range functionality.

- In Paper 9.1, Texas Instruments describes an RF-to-bits 3TX/4RX automotive radar transceiver operating at 76 to 81GHz implemented in 45nm CMOS. The 10dBm TX has binary and linear phase modulation for MIMO and beamforming; a 15MHz BW I/Q RX has <18dB NF and a PLL chirp generator delivering <-91dBc/Hz phase noise with 4GHz ramps at up to 100MHz/µs.

APPLICATIONS AND ECONOMIC IMPACT

- The radar system is targeted for front and corner radars in automobiles. Such systems are expected to play an important role in realizing autonomous driving applications.
- Increasing the use of collision-avoidance radar through integrated, low-cost CMOS radar will lead to increased safety and save lives.

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Session 10 Overview: *Sensor Systems*

IMMD SUBCOMMITTEE

Session Chair: *Michael Kraft, University of Leuven, Belgium*
Session Co-Chair: *Masayuki Miyamoto, Wacom, Japan*

Subcommittee Chair: *Makoto Ikeda, University of Tokyo, Japan, IMMD*

The session describes advances in sensor systems covering topics of sensors for inertial navigation, capacitive touch and stylus systems, ultrasound and bolometers. The first paper presents a frequency-modulated gyroscope using rate chopping to reject drift. The second paper describes a personal inertial navigation system for GPS denied environments. The third paper presents a capacitive touch system with palm rejection functionality. The fourth paper presents a highly noise-immune stylus analog front-end that supports pen pressure for both passive electrically coupled resonance (ECR) and active styluses. The fifth paper demonstrates a pitch-matched front-end ASIC that realizes subarray beamforming and digitization for ultrasound imaging. The sixth paper demonstrates a 64-channel frontend ASIC for intracardiac echocardiography (ICE) catheters. The seventh paper presents a 2×2 transformer-based magnetic sensor array, which can detect magnetic nanoparticles with better than 0.3ppm accuracy. Finally, the eighth paper presents a low-cost 80×60-pixel thermal infrared imager featuring 100mK temperature resolution.

- In Paper 10.1, UC Berkeley presents a frequency-modulated gyroscope that measures rate signal directly as frequency variations and employs a rate chopping technique to reject drift. The sensor can also be operated in a long and short-term mode of operation.
- In Paper 10.2, the University of Utah, UC Berkeley, Ozyegin University and Case Western Reserve University describe a personal navigation system for operations under a GPS denied environment. The system demonstrates a position accuracy of 5.5m over 3km walking distance without GPS.
- In Paper 10.3, Hanyang University, Leading UI, Chun-Ang University and MiraeTNS present a multiple-way interactive capacitive-touch system (MI-CTS) with the palm rejection functionality. The system is based on a multiple-frequency driving method and successfully demonstrated with an 85” 198×112 and two 32" 104×64 touch-screen panels.
- In Paper 10.4, Samsung Electronics presents a highly noise-immune stylus analog front-end (AFE) that supports pen pressure for both passive electrically coupled resonance (ECR) and active styluses. The measured SNR with a 1mm ECR stylus is 56dB under a charger and display noise environment.
- In Paper 10.5, Delft University presents a pitch-matched front-end ASIC that realizes subarray beamforming and digitization at 10× lower power and 3.3× smaller area per element than prior work. This is achieved by employing subarray beamforming ADCs that merge the delay-and-sum and digitization functions in the charge domain.
- In Paper 10.6, the Georgia Institute of Technology and the University of Leeds demonstrate a 64-channel frontend ASIC for intracardiac echocardiography (ICE) catheters. The 2.6×11 mm^2 ASIC is implemented in 60V 0.18μm HV-BCD technology, effectively reducing the number of wires in the catheter from more than 64 to only 22.
- In Paper 10.7, the California Institute of Technology presents a 2×2 transformer-based magnetic sensor array, implemented in a CMOS process, which can detect magnetic nanoparticles with better than 0.3ppm accuracy and as little as 3mW power consumption. The capability of the sensor is demonstrated by performing an in-vitro DNA detection experiment.
- In Paper 10.8, KAIST presents a low-cost 80×60-pixel thermal infrared imager featuring 100mK temperature resolution with integrated biasing DAC. The extremely low-noise DAC architecture avoids the use of slow low-pass filter, achieving a sensor startup time as low as 100ms.

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Session 10 Highlights: Sensor Systems

[10.2] Personal Inertial Navigation System Employing MEMS Wearable Ground Reaction Sensor Array and Interface ASIC Achieving a Position Accuracy of 5.5m Over 3km Walking Distance Without GPS

Paper Authors: *Qingbo Guo[1], William Deng[2], Ozkan Bebek[3], Cenk Cavusoglu[4], Carlos Mastrangelo[1], Darrin Young[1]*

Paper Affiliation: *[1]University of Utah, Salt Lake City, UT, [2]University of California at Berkeley, Berkeley, CA, [3]Ozyegin University, Istanbul, Turkey, [4]Case Western Reserve University, Cleveland, OH*

Subcommittee Chair: *Makoto Ikeda, University of Tokyo, Tokyo, Japan, IMMD*

CONTEXT AND STATE OF THE ART

- GPS sensors in smart phones have enabled a broad set of applications, ranging from ride sharing, to maps, to AR.
- Such sensors are inoperable in GPS-denied environments.
- Inertial navigation is a long-standing technology used transportation systems.
- There is a need for location-based services in such environments, as enabled by personal small-footprint inertial navigation.

TECHNICAL HIGHLIGHTS

- **Personal inertial navigation system deployed within the heal of a boot for GPS-denied environments**
- A personal inertial navigation system for operations under GPS-denied environment is presented. The system employs a MEMS-based 13×26 high-density flexible capacitive ground reaction sensor array achieving a sensitivity of 3.7fF/kPa, a low-power interface ASIC consisting of a programmable offset-cancellation capacitance-to-voltage converter followed by a 12b ADC, and a 9-axis inertial measurement unit (IMU). A prototype system is designed and implemented inside a heel region of a boot. With an effective system calibration technique and sensors data fusion and processing algorithm to suppress IMU offset and time drift, the system achieves high position accuracy of 5.5m over 3100m walking distance exhibiting various ground surfaces without GPS.

APPLICATIONS AND ECONOMIC IMPACT

- A personal navigation system without GPS will enable a variety of new applications, ranging from wearable electronics to smart sensors to personalized proximity-based services.

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Session 10 Highlights: Sensor Systems

[10.5] A 0.91mW/Element Pitch-Matched Front-End ASIC with Integrated Subarray Beamforming ADC for Miniature 3D Ultrasound Probes

Paper Authors: *Chao Chen[1], Zhao Chen[1], Deep Bera[2], Emile Noothout[1], Zu-Yao Chang[1], Mingliang Tan[1], Hendrik J. Vos[1,2], Johan G. Bosch[2], Martin D. Verweij[1,2], Nico de Jong[1,2], Michiel A.P. Pertijs[1]*

Paper Affiliation: *[1]Delft University of Technology, Delft, The Netherlands, [2]Erasmus MC, Rotterdam, The Netherlands*

Subcommittee Chair: *Makoto Ikeda, The University of Tokyo, Tokyo, Japan, IMMD*

CONTEXT AND STATE OF THE ART

- It is desirable in certain scenarios to combine the multiple medical imaging modalities of MRI and ultrasound.
- This combination has been impeded by the challenges of RF heating of wiring to ultrasound transducers, as well as the number of wires necessary for adequate field-of-view sonography.
- 3D ultrasound compounds these problems by requiring even more wiring.
- Reducing the number of wires required for ultrasound addresses the above issue, as well as increases flexibility and reduces cost.

TECHNICAL HIGHLIGHTS

- **Pitch-matched ASIC within the intracardiac echocardiography catheter performs subarray beamforming and digitization at 10× lower power**
- A pitch-matched front-end ASIC realizes subarray beamforming and digitization at 10× lower power and 3.3× smaller area per element than prior work, with a pitch-matched layout. The beamforming ADC directly digitizes the output of switched-capacitor delay lines in the charge domain, eliminating the need for power-hungry buffer stages. By combining the digitized outputs of every 4 subarrays with a high-speed datalink, the ASIC demonstrates the feasibility of digital channel-count reduction in miniature ultrasound probes.

APPLICATIONS AND ECONOMIC IMPACT

- Heath care costs are reduced by more accurate diagnosis via enhanced imaging.
- Low-power techniques in ultrasound extend the application space untethering them from cart-based systems.
- 3D ultrasonic imaging can be achieved with lower power budgets, enabling broader deployment of such technologies.

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Session 11 Overview: SRAM

Memory Subcommittee

Session Chair: *Jonathan Chang,TSMC, Hsinchu, Taiwan*

Session Co-Chair: *Chun Shiah, Etron, Hsinchu, Taiwan*

Subcommittee Chair: *Leland Chang, IBM, Yorktown Heights, NY*

SRAM continues to be the critical technology enabler for a wide range of applications from low-power to high-performance computing. This session showcases the leading-edge SRAM developments from the semiconductor industry. Intel presents the smallest SRAM bitcell for 10nm technology, with design assist techniques to enable low V_{MIN} operation. Samsung presents the smallest bitcell for 7nm technology and shows a double-write driver techniques to further improve V_{MIN}. TSMC demonstrates a 7nm 5GHz L1 cache for high-performance computing.

- In paper 11.1 Intel presents a 23.6Mb/mm^2 SRAM in 10nm FinFET with the smallest 10nm SRAM bitcell. It adopts column-based transient voltage collapse and a stepped wordline to lower the minimum operation voltage (V_{MIN}).

- In paper 11.2 Samsung Electronics presents a 7nm FinFET SRAM using EUV lithography. It adopts a 0.026μm^2 bitcell and V_{MIN} is improved with a proposed selective double bitline scheme in combination with a negative bitline scheme.

- In paper 11.3 TSMC presents a 7nm L1 cache memory compiler, which operates at a 5GHz clock frequency. It implements a self-timing scheme with small-signal sensing and a folded architecture to increase the performance.

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Session 11 Highlights: SRAM

[11.1] A 23.6Mb/mm² SRAM in 10nm FinFET Technology with Pulsed PMOS TVC and Stepped-WL for Low-Voltage Applications

[11.3] A 5GHz 7nm L1 Cache Memory Compiler for High-Speed Computing and Mobile Applications

Paper 11.1 Authors: Zheng Guo, Daeyeon Kim, Satyanand Nalam, Jami Wiedemer, Xiaofei Wang, Eric Karl

Paper 11.1 Affiliation: Intel, Hillsboro, OR

Paper 11.3 Authors: Michael Clinton[1], Rajinder Singh[1], Marty Tsai[1], Shayan Zhang[1], Bryan Sheffield[1], Jonathan Chang[2]

Paper 11.3 Affiliation: [1]TSMC, Austin, TX, [2]TSMC, Hsinchu, Taiwan

Subcommittee Chair: *Leland Chang, IBM, Yorktown Heights, NY, Memory*

CONTEXT AND STATE OF THE ART

- SRAM continues to scale over process technologies since first implemented in 10/7nm node.
- Intel scaled 10nm technology to 23.6Mb/mm² with improved assist circuits.
- TSMC demonstrated a 5GHz, 7nm L1 cache memory compiler.

TECHNICAL HIGHLIGHTS

- **Paper 11.1 – A *23.6Mb/mm² SRAM in 10nm FinFET Technology***
  In Paper 11.1, a 23.6Mb/mm² high-density SRAM array and a 20.4Mb/mm² low-voltage SRAM array utilizing 0.0312μm² and 0.0367μm² bitcells in 10nm FinFET technology are presented. Pulsed PMOS transient voltage collapse write-assist circuit is used to minimize the write energy overhead of TVC. A stepped-WL technique is used to complement TVC to enable a 150mV write V_{MIN} improvement for HDC with minimum impact to read stability.

- **Press Headline for Paper 11.3 –A 5GHz, 7nm L1 Cache Memory Compiler for High Speed Computing and Mobile Applications**
  In Paper 11.3, an L1 cache memory compiler designed using a 7nm high-k metal gate FinFET technology and the HC 6T SRAM bitcell achieves greater than 5GHz operation in high-performance computing (HPC) applications. The memory implements a self-timing scheme with small-signal sensing, a "folded" architecture and a "turbo" mode to improve performance during overdrive conditions.

APPLICATIONS AND ECONOMIC IMPACT

- Demonstrate that SRAM scaling for 7/10nm technology with record low SRAM bitcell area.
- Demonstrate SRAM for a wide range of applications from mobile to high-performance computing.

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Session 12 Overview: DRAM

Memory Subcommittee

Session Chair: *Seung-Jun Bae, Samsung Electronics, Hwaseong, Korea*

Session Co-Chair: *Wolfgang Spirkl, Micron Semiconductor, Munchen, German*

Subcommittee Chair: *Leland Chang, IBM, Yorktown Heights, NY*

Demand for high-performance and high-capacity DRAMs is increasing more dramatically, than in the past, due to the emergence of new areas such as machine learning, VR and AR. In line with this trend, new innovations with capacities of 16Gb and data-rate speeds of 18Gb/s/pin are introduced this year. These changes are common to high-performance computing, gaming graphics, mobile, and server fields, including artificial intelligence. Two graphics DRAM papers of next generation GDDR6 standard shows a maximum data rate of 16~18Gb/s/pin with single-ended signaling, and 16Gb high-density DRAMs in a 10nm process node are introduced in LPDDR4X and DDR4. HBM2 is extended to an 8H stack for 64Gb density while keeping a BW of 341GB/s.

- In paper 12.1, Samsung presents a graphics-DRAM GDDR6 at a data-rate of 18Gb/s/pin with 16Gb density. The chip implements a per-bit trainable single-ended DFE, a ZQ-coded transmitter, and PLL-less clocking to overcome I/O speed limitations due to the DRAM process. Furthermore, this work optimizes clock and power domain crossing and adopts a split-die architecture to improve signal integrity.

- In paper 12.2, Samsung presents a 16Gb 5Gb/s/pin LPDDR4X with in-DRAM ECC with a self-refresh power of 0.1mW/Gb in a 10nm DRAM process. Circuit techniques for achieving high speed and low power are presented and key features include a NBTI-tolerant solution, a PMOS SWD GIDL reduction, adaptive gear-down, a hybrid I/O buffer and a metastable-free DQS aligner.

- In paper 12.3, SK Hynix presents a 64Gb 341GB/s HBM2 DRAM with 8H stack. To increase data rate of the multi-TSV stack, a spiral point-to-point TSV structure and improved bank group control are proposed. TSV self-repair techniques and serial temperature code read-out schemes are introduced for reliable 3D operation.

- In paper 12.4, SK Hynix presents a 16Gb/s/pin GDDR6 with an 8Gb density. Bandwidth extension techniques are introduced: WCK divider with an analog duty correction circuit, 4-to-1 multiplexer with on-chip feedback EQ filter, and loop-unrolled one-tap DFE with a two-stage pre-amplifier.

- In paper 12.5, SK Hynix presents a 16Gb 3.2Gb/s/pin DDR4 DRAM in an 18nm process. To overcome internal power drops in the large die, power pads are placed in the middle of the array and a staggered power up scheme for the memory stack is used to reduce in-rush current. ECC for reliable operation of redundancy fuse latches and module self-repair schemes are introduced.

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Session 12 Highlights: DRAM

[12.1] A 16Gb 18Gb/s/pin GDDR6 DRAM with Per-Bit Trainable Single-Ended DFE and PLL-Less Clocking

Paper 12.1 Authors: *Young-Ju Kim, Hye-Jung Kwon, Su-Yeon Doo, Yoon-Joo Eom, Young-Sik Kim, Min-Su Ahn, Yong-Hun Kim, Sang-Hoon Jung, Sung-Geun Do, Chang-Yong Lee, Jae-Sung Kim, Dong-Seok Kang, Kyung-Bae Park, Jung-Bum Shin, Jong-Ho Lee, Seung-Hoon Oh, Sang-Yong Lee, Ji-Hak Yu, Ji-Suk Kwon, Ki-Hun Yu, Chul-Hee Jeon, Sang-Sun Kim, Min-Woo Won, Gun-hee Cho, Hyun-Soo Park, Hyung-Kyu Kim, Jeong-Woo Lee, Seung-Hyun Cho, Keon-woo Park, Jae-Koo Park, Yong-Jae Lee, YongJun Kim, Young-Hun Seo, Beob-Rae Cho, Chang-Ho Shin, Chan-Yong Lee, YoungSeok Lee, Yoon-Gue Song, Sam-Young Bang, YounSik Park, Seouk-Kyu Choi, Byeong-Cheol Kim, Gong-Heum Han, Seung-Jun Bae, Hyuk-Jun Kwon, Jung-Hwan Choi, Young-Soo Sohn, Kwang-Il Park, Seong-Jin Jang*

Paper 12.1 Affiliation: *Samsung Electronics, Hwaseong, Korea*

Subcommittee Chair: *Leland Chang, IBM, Yorktown Heights, NY, Memory*

CONTEXT AND STATE OF THE ART

- GDDR6 is a new high-speed graphic DRAM JEDEC standard on the basis of discrete components.
- It extends the long-living GDDR5/5X family.

TECHNICAL HIGHLIGHTS

- **A 16Gb GDDR6 dual-die packaged DRAM with 18Gb/s/pin IO speed, the highest reported so far**
- In paper 12.1, Samsung presents a graphics-DRAM GDDR6 with a data-rate of 18Gb/s/pin and a 16Gb density. The chip implements a per-bit trainable single-ended DFE, a ZQ-coded transmitter, and PLL-less clocking to overcome I/O speed limitations due to the DRAM process. Furthermore, this work optimizes clock and power-domain crossing and adopts a split-die architecture to improve signal integrity.

APPLICATIONS AND ECONOMIC IMPACT

- GDDR6 is intended for use in a large variety of high-bandwidth applications such as next generation gaming, virtual reality, high-performance computing, autonomous driving and artificial intelligence.
- GDDR6 provides an economic way to extend existing system solutions to higher I/O bandwidths without leaving the well-established ecosystem of PCBs with discrete components.

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[12.2] A 16Gb LPDDR4X SDRAM with NBTI-Tolerant Circuit Solution, SWD PMOS GIDL Reduction Technique, Adaptive Gear-Down Scheme and Metastable-free DQS Aligner in a 10nm Class DRAM Process

Paper 12.2 Authors: *Ki Chul Chun, Yong-Gyu Chu, Jin-Seok Heo, Tae-Sung Kim, Soohwan Kim, Hui-Kap Yang, Mi-Jo Kim, Chang-Kyo Lee, Juhwan Kim, Hyunchul Yoon, Chang-Ho Shin, Sanguhn Cha, Hyung-Jin Kim, Young-Sik Kim, Kyungryun Kim, Young-Ju Kim, Wonjun Choi, Dae-Sik Yim, Inkyu Moon, Young-Ju Kim, Junha Lee, Young Choi, Yongmin Kwon, Sung-Won Choi, Jung-Wook Kim, Yoon-Suk Park, Woongdae Kang, Jinil Chung, Seunghyun Kim, Yesin Ryu, Seong-Jin Cho, Hoon Shin, Hangyun Jung, Sanghyuk Kwon, Kyuchang Kang, Jongmyung Lee, Yujung Song, Young-Jae Kim, Eun-Ah Kim, Kyung-Soo Ha, Kyoung-Ho Kim, Seok-Hun Hyun, Seungbum Ko, Jung-Hwan Choi, Young-Soo Sohn, Kwang-Il Park, Seong-Jin Jang*

Paper 12.2 Affiliation: *Samsung Electronics, Hwaseong, Korea*

Subcommittee Chair: *Leland Chang, IBM, Yorktown Heights, NY, Memory*

CONTEXT AND STATE OF THE ART

- LPDDR4X is a very low supply voltage extension of LPDDR4

TECHNICAL HIGHLIGHTS

- **A 16Gb LPDDR4X SDRAM with in-DRAM ECC, 5Gb/s/pin I/O speed and 0.1mW/Gb in self-refresh**
- In paper 12.2, Samsung presents a 16Gb 5Gb/s/pin LPDDR4X with in-DRAM ECC with a self-refresh power of 0.1mW/Gb in a 10nm DRAM process. Circuit techniques for achieving high speed and low power are presented and key features include a NBTI-tolerant solution, a PMOS SWD GIDL reduction, adaptive gear-down, a hybrid I/O buffer and a metastable-free DQS aligner.

APPLICATIONS AND ECONOMIC IMPACT

- LPDDR4X is targeted for the huge and growing market of low-power and mobile applications such as smart phones, cameras and smart sensors.

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Session 13 Overview: Machine Learning and Signal Processing

Digital Architectures and Systems Subcommittee

Session Chair: *Dejan Marković, University of California, Los Angeles*

Session Co-Chair: *Masato Motomura, Hokkaido University, Sapporo, Japan*

Subcommittee Chair: *Byeong-Gyu Nam, Chungnam National University, Daejeon, Korea, DAS*

Architectures supporting machine learning for embedded perception and cognition are continuing their rapid evolution, inspired by modern data analytics and enabled by the low energy cost of CMOS processing. This makes it feasible to migrate data analytics toward edge and wearable devices. To further support increased requirements for multiuser connectivity and sparse data, multi-user MIMO and compressive reconstruction are also required.

This session covers trends in machine learning and signal processing for improved accuracy of speech, image, video processing for next-generation mobile/edge and data center devices. The session features programmable accelerators for Convolutional Neural Networks (CNNs), Recurrent Neural Networks (RNNs), and Multi-Layer Perceptron (MLP) algorithms, with digital and mixed-signal processing kernels. The session concludes with a link-adaptive massive MIMO detector and robust compressive-sensing reconstruction processors.

- In Paper 13.1, Google describes a vision for machine-learning (ML) processing. The talk will present the concept of a single ML compute fabric from the device to the data center, and discuss some of the technical challenges that must be overcome to broadly enable a powerful yet cost-effective ML compute fabric.
- In Paper 13.2, Hokkaido University presents a 14.3×8.5mm^2 multi-purpose log-quantized deep neural network (DNN) inference engine stacked on a 96MB 3D SRAM using inductive coupling technology in 40nm. The system features 3-cycle 28.8GB/s memory communication and 7.49TOPS peak performance in binary precision at 1.1V, 300MHz, for cutting-edge DNN workloads.
- In Paper 13.3, KAIST describes a DNN accelerator with variable bit precision from 1b to 16b. Using a flexible DNN core architecture, look-up-table-based bit-serial processing, and off-chip memory management, the 16mm^2 65nm chip achieves 50.6TOPS/W energy efficiency for 1b data at 10MHz, 0.66V.
- In Paper 13.4, KAIST presents a 3D hand-gesture recognition processor for real-time user interaction in smart mobile devices. With a CNN stereo engine, triple ping-pong buffers, and processor-in-memory techniques, the 16mm^2 65nm processor achieves real-time 3D hand-gesture recognition with 9.02mW and 4.3mm error at 0.85V, 50MHz.
- In Paper 13.5, Stanford University and KU Leuven introduce a mixed-signal binary CNN processor based on near-memory data processing. The 2.4×2.4mm^2 28nm 0.6V processor features 328KB of on-chip SRAM for a 9-layer CNN, data parallelism and parameter re-use, achieving a 3.8μJ/classification at 86.05% accuracy on the CIFAR-10 dataset.
- In Paper 13.6, the University of Michigan describes 128×16 massive MIMO detector with link adaptation to meet practical channel conditions with scalable energy. Implemented as a condensed systolic array, the 2mm^2 28nm FDSOI chip achieves 1.8Gb/s at 70pJ/b, 569MHz and 4.3dB processing gain with channel data obtained from real-life measurements.
- In Paper 13.7, National Taiwan University presents a compressive-sensing reconstruction engine with parallel atom searching approach to reduce signal distortion due to measurement noise. The 2.93×2.93mm^2 40nm processor achieves up to 1996KS/s with 93mW power consumption at 0.9V, 67.5MHz.

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Session 13 Highlights: Machine Learning and Signal Processing

[13.2] QUEST: A 7.49TOPS Multi-Purpose Log-Quantized DNN Inference Engine Stacked on 96MB 3D SRAM Using Inductive-Coupling Technology in 40nm CMOS

13.2 Paper Authors: *K. Ueyoshi[1], K. Ando[1], K, Hirose[1], S. Takamaeda-Yamazaki[1], M. Nakamura[2], T. Adachi[2], J. Kadomoto[3], T. Miyata[3], M. Hamada[3], T. Kurorda[3], and M. Motomura[1]*

13.2 Paper Affiliation: *[1]Hokkaido University, Sapporo, Japan, [2]Ultramemory Inc, Hachioji, Japan, [3]Keio University, Yokohama, Japan*

[13.3] A 50.6TOPS/W Energy-Efficient Unified Deep Neural Network Accelerator with 1-to-16b Fully Variable Bit Precision

13.3 Paper Authors: *J. Lee, C. Kim, S. Kang, D. Shin, S. Kim, and H.-J. Yoo*

13.3 Paper Affiliation: *KAIST, Daejeon, Korea*

[13.5] An Always-On 3.8μJ/86% CIFAR-10 Mixed-Signal Binary CNN Processor with All Memory on Chip in 28nm CMOS

13.5 Paper Authors: *D. Bankman[1], L. Yang[1], B. Moons[2], M. Verhelst[2], B. Murmann[1]*

13.5 Paper Affiliation: *[1]Stanford University, Stanford, CA, [2]KU Leuven, Leuven, Belgium*

Subcommittee Chair: *Byeong-Gyu Nam, Chungnam National University, Daejeon, Korea, Digital Architectures and Systems*

CONTEXT AND STATE OF THE ART

- There is growing demand for accelerating deep neural network (DNN) inference both in mobile/edge and data center devices.
- There is a need for reduced numerical precision and enhanced energy efficiency using digital and mixed-signal approaches.

TECHNICAL HIGHLIGHTS

- **First 3D-stacked (with 8 SRAM dies) DNN accelerator featuring 1-4b logarithmically quantized NN arithmetic**
  - Hokkaido University proposes stacking its novel MIMD-parallel multi-purpose DNN accelerator with SRAM dies for achieving balanced capacity, latency and bandwidth, which also features a logarithmic quantized DNN architecture.
- **CNN-RNN unified DNN accelerator with 1-16b programmable LUT-based arithmetic**
  - KAIST presents a DNN accelerator that supports CNN and RNN with a single programmable architecture, that outperforms previous hybrid-type CNN-RNN architectures in energy efficiency
- **A mixed-signal in-memory binary CNN processor**
  - Stanford University and KU Leuven propose a CNN mixed-signal inference processor that is an order-of-magnitude more energy-efficient than previous works, combining an all on-chip memory, data-parallel architecture, and switched-capacitor circuits

APPLICATIONS AND ECONOMIC IMPACT

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- Deep neural network (DNN) algorithms are outperforming conventional techniques in a variety of “smart” application domains, including video, image, and speech processing, owing to higher prediction/inference accuracies.
- DNN computational requirements are distinctively different from conventional workloads, and hence new processing architectures, with superior performance and energy efficiency, are being developed in both industry and academia.

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Session 14 Overview: High-Resolution ADCs

Data Converter Subcommittee

Session Chair: *Matt Straayer, Maxim Integrated, Chelmsford, MA*

Session Co-Chair: *Seung-Tak Ryu, KAIST, Daejeon, Korea*

Subcommittee Chair: *Un-Ku Moon, Oregon State University, Corvallis, OR*

This session's high-resolution analog-to-digital converters (ADCs) with 12-19b ENOB introduce a number of advanced circuit design techniques to achieve very high performance with low power consumption. While many of the proposed designs use an efficient SAR architecture where possible for moderate resolution, higher performance is consistently enabled by delta-sigma and pipeline architectures. Precision is further enabled by techniques such as hardware re-use, calibration, dynamic element matching, chopping, and correlated double-sampling.

- In Paper 14.1, Oregon State University and MediaTek present an efficient dynamic error correction technique for an NRZ feedback DAC in a continuous-time delta-sigma ADC. The 28nm ADC achieves 80dB SNDR in a 50MHz bandwidth while consuming 64.3mW.
- In Paper 14.2, The University of California Los Angeles describes a capacitively coupled continuous-time delta-sigma ADC for a neural recording front-end in 40nm CMOS. Chopping and linearity enhancement techniques are key to demonstrating 15.2b-ENOB with only 4.5uW in 5kHz bandwidth.
- In Paper 14.3, The University of Texas at Austin proposes an error feedback structure with a passive FIR and re-used comparator to realize complex noise transfer function zeros in a noise-shaping SAR ADC. Clocked at 10MHz, the 40nm ADC realizes 79dB SNDR in 625kHz bandwidth and consumes 84uW.
- In Paper 14.4, The University of Ulm introduces an integrator slicing technique in an incremental delta-sigma ADC that allows for improved noise and power tradeoffs in the front-end integrator stages. The 200kS/s prototype in 0.18μm CMOS achieves 91.5dB dynamic range and 1.1mW.
- In Paper 14.5, The Delft University of Technology presents a dynamic zoom ADC with a high-speed asynchronous SAR front-end that works in tandem with a delta-sigma back-end. Fabricated in 0.16μm CMOS, the ADC reaches 118dB SNDR in a 1kHz bandwidth while consuming 280uW.
- In Paper 14.6, The National Tsing Hua University proposes a single-path time-domain voltage-controlled delay line for use in a coarse SAR comparator and a fine incremental delta-sigma integrator to realize a 13b ADC. Power consumption is only 638nW at 270kS/s with 11.9b ENOB.
- In Paper 14.7, Analog Devices introduces a signal independent background calibration technique to achieve 0.3ppm INL in a 20b 1MS/s pipelined SAR ADC in 0.18μm CMOS. The double conversion calibration settles to 0.25ppm within 100k samples, resulting in 101.5dB SNDR with a 5V reference.

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Session 14 Highlights: High Resolution ADCs

[14.2] A 15.2-ENOB Continuous-Time ΔΣ ADC for a 7.3uW 200mV_{pp}-Linear-Input-Range Neural Recording Front-End

Paper 14.2 Authors: *H. Chandrakumar, D. Markovic*

Paper 14.2 Affiliation: *University of California, Los Angeles, Los Angeles, CA*

[14.7] A Signal-Independent Background-Calibrating 20b 1MS/s SAR ADC with 0.3pm INL

Paper 14.7 Authors: *H. Li[1], M. Maddox[1], M. Coln[1], W. Buckley[2], D. Hummerston[3]*

Paper 14.7 Affiliation: *[1]Analog Devices, Wilmington, MA, [2]Analog Devices, Cork, Ireland, [3]Analog Devices, Newbury, UK*

Subcommittee Chair: *Un-Ku Moon, Oregon State University, Corvallis, OR*

CONTEXT AND STATE OF THE ART

- Micro-power ADCs with high linearity and dynamic range are required in emerging applications such as smart sensors, biomedical imaging, and portable instrumentation.
- Random mismatches in components and circuit nonlinearity have been a fundamental limitation to achieving high linearity, even in advanced IC technologies.
- Innovations in ADC architectures and circuit techniques, including meticulous calibration, help break the performance barrier.

TECHNICAL HIGHLIGHTS

UCLA introduces a continuous-time delta-sigma modulator for closed-loop neural recording with 10x higher bandwidth compared to state-of-the-art front-ends.

- A capacitively-coupled 40nm CMOS continuous-time delta-sigma ADC demonstrates 15.2b-ENOB with only 4.5uW in 5kHz bandwidth.

Analog Devices demonstrates a 20b Nyquist ADC achieving performance comparable to oversampling ADCs.

- With a signal independent background calibration, the 20b 1MS/s pipelined SAR ADC achieves 101.5dB SNDR and 0.3ppm INL 0.18μm CMOS.

APPLICATIONS AND ECONOMIC IMPACT

- Advanced circuit techniques for high accuracy ADCs make many high-precision applications possible and efficient.
- High-precision ADCs do not need factory trimming, thereby reducing manufacturing cost significantly without aging and temperature sensitivity.

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Session 15 Overview: RF PLLs

RF Subcommittee

Session Chair: *Jiayoon Ru, Broadcom, Irvine, CA*

Session Co-Chair: *Jaehyouk Choi, Ulsan National Institute of Science and Technology (UNIST), Korea*

Subcommittee Chair: *Piet Wambacq, imec, Belgium, RF Subcommittee*

This session presents the latest advances in digital and analog PLLs generating frequencies from 1 to 100GHz and covering diverse topics, such as ultra-low-power ADPLLs, FMCW synthesizers, fast-settling bang-bang PLLs, interference-coupling mitigation, type-I sampling PLLs, and mm-wave ADPLLs.

- In Paper 15.1, Tokyo Institute of Technology presents an ultra-low-power all-digital fractional-N PLL in 65nm CMOS. The rms jitter of 0.53ps is achieved at 2.44GHz with the power consumption of 0.98mW. The corresponding FOM is -246dB.
- In Paper 15.2, Infineon Technologies describes a 20-to-24GHz digital bang-bang PLL in 65nm CMOS for mm-wave FMCW radars. The 19.7mA fractional-N PLL, having 213fs jitter and a –58dBc fractional spur, synthesizes fast chirps with a 36μs period and a 200MHz peak-to-peak frequency range.
- In Paper 15.3, University of Michigan describes a 38GHz digital fractional-N FMCW chirp synthesizer using a bandpass delta-sigma TDC to enable >1MHz PLL bandwidths with an in-band PN of –85dBc/Hz at a 100kHz offset. The chip fabricated in 40nm CMOS generates a 9MHz/μs-slope and 824kHz$_{rms}$-error triangular-chirp signal with a 500MHz bandwidth, while consuming 68mW.
- In Paper 15.4, Politecnico di Milano presents a 3.7-to-4.1GHz digital bang-bang PLL adopting a background frequency-aid technique. Over a 364MHz frequency hop, the 65nm-CMOS fractional-N PLL has coarse (within 40MHz) settling time of 2.9μs and fine (within 1kHz) settling time of 180μs. The rms jitter is 183fs with a current consumption of 4.4mA, leading to an FOM of –247.5dB.
- In Paper 15.5, University of Southern California presents a 3-to-5GHz digital frequency synthesizer to mitigate simultaneous interference coupling to DCO and reference paths. Implemented in 65nm CMOS and consuming 21.3mW, the proposed PLL mitigates the increase in the noise floor and spectral spurs due to PA and oscillator mutual pulling by 12 and 22.5dB, respectively.
- In Paper 15.6, University of British Columbia describes a frequency synthesizer, which comprises an all-digital frequency-locked loop and a type-I integer-N PLL with an LC VCO. The synthesizer occupies a 0.01mm^2 area in 65nm CMOS and achieves 185fs$_{rms}$ jitter while consuming 1.1mW, corresponding to an FOM of –254dB across 4.6 to 5.6GHz.
- In Paper 15.7, Columbia University describes a dividerless PLL architecture, i.e. a reference-sampling PLL. The 65nm-CMOS integer-N PLL achieves an rms jitter of 110fs at 2.55GHz, while consuming 3.5mW. The corresponding FOM is –253.5dB, and the reference spur is lower than –67dBc.
- In Paper 15.8, Hong Kong University of Science and Technology presents a W-band ADPLL employing a wide-band DCO and a delta-sigma TDC. The 65nm-CMOS integer-N PLL achieves a frequency-tuning range from 82 to 108GHz and 10MHz phase noise between –106 and –110dBc/Hz, while consuming 35.5mW.

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Session 15 Highlights: RF PLLs

[15.1] A 0.98mW Fractional-N ADPLL Using 10b Isolated Constant-Slope DTC with FOM of -246dB for IoT Applications in 65nm CMOS

Paper 15.1 Authors: *H. Liu, D. Tang, Z. Sun, W. Deng, H. C. Ngo, K. Okada*

Paper 15.1 Affiliation: *Tokyo Institute of Technology*

[15.6] A 0.01mm² 4.6-to-5.6GHz Sub-Sampling Type-I Frequency Synthesizer with –254dB FOM

Paper 15.6 Authors: *A. Sharkia, S. Mirabbasi, S. Shekhar*

Paper 15.6 Affiliation: *University of British Columbia*

Subcommittee Chair: *Piet Wambacq, imec, Leuven, Belgium, RF Subcommittee*

CONTEXT AND STATE OF THE ART

- Phase noise (jitter), power consumption, and silicon area are the three essential CMOS-frequency-synthesizer metrics that always cause a design dilemma.
- Advent of the era of IoT demands low-phase-noise PLLs consuming ultra-low power and using compact silicon area.

TECHNICAL HIGHLIGHTS

0.98mW ultra-low-power ADPLL with 525fs_{rms} jitter

- In Paper 15.1, Tokyo Institute of Technology presents an ultra-low-power all-digital fractional-N PLL in 65nm CMOS. The rms jitter of 0.53ps is achieved at 2.44GHz with the power consumption of 0.98mW, corresponding to an FOM of -246dB.

0.01mm² LC-based compact PLL with 185fs_{rms} jitter

- In Paper 15.6, University of British Columbia describes a 65nm CMOS frequency synthesizer, comprising of an all-digital frequency-locked loop and a Type-I PLL with an LC VCO, occupying 0.01mm² area. The synthesizer achieves 185fs_{rms} jitter with 1.1mW power consumption, corresponding to an FOM of –254dB across a 4.6-to-5.6GHz frequency range.

APPLICATIONS AND ECONOMIC IMPACT

- PLLs concurrently achieving low power consumption and low phase noise are presented for future IoT and 5G systems.
- These PLLs will be the best choice for ultra-low-power wireless connectivity solutions.

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Session 16 Overview: Advanced Optical and Wireline Techniques

Wireline Subcommittee

Session Chair: *Azita Emami, Caltech, Pasadena, CA*

Session Co-Chair: *Andrew Joy, Cavium, Northampton, UK*

Subcommittee Chair: *Frank O'Mahony, Intel, Hillsboro, OR*

Electrical and optical links continue to provide challenges that cannot be overcome by process technology advances alone. The ingenuity of the designer is a major contribution, and this is clearly demonstrated by the papers in this session. The first is an invited paper that reviews state-of-the-art optical interconnects in scalable, high-density standards-based switching fabrics for networking systems and cloud computing. The second paper describes the first electrical domain solution to the non-linear dispersion for both transient and adiabatic chirp of directly modulated lasers. This is followed by a paper that describes the first optical burst-mode receiver with rapid power on/off functionality for a data rate of 56Gb/s and a power efficiency of 2.2pJ/b in always-on mode.

The next three papers demonstrate the benefits of time domain modulation and equalization techniques as an alternative to conventional voltage-domain modulation. The first utilizes integrated pulse width modulation to equalize consecutive-bit ISI from 3 to 16Gb/s achieving 1.6-3.1pJ/b. The second encodes data based on pulse width and location within a fixed-length frame in order to signal at 20Gb/s with 4.53pJ/b. The third uses phase difference modulation to overcome reflections in a 7.8Gb/s/pin, 1.96pJ/b link for multi-drop memory applications. The next paper addresses the short reach interface requirements at 56Gb/s and achieves a 2.25pJ/b power efficiency at 56Gb/s. This is followed by a 1.15pJ/b/pin ground-referenced single-ended link at 25Gb/s in 16nm CMOS for multi-die package communication spanning up to 80mm. The final paper describes a digitally pre-distorted PAM-4 modulation technique for contactless communication at 20Gb/s over a 127GHz carrier consuming 3.98pJ/b.

- In Paper 16.1, Axalume describes the use of optical interconnects in scalable, high-density standards-based switching fabrics for networking systems and cloud computing. It discusses datacenter switches of approximately 25Tb/s capacity with the use of optical interconnects to improve density, efficiency, and latency.
- In Paper 16.2, Korea Advanced Institute of Science & Technology presents a 28Gb/s electronic dispersion compensation technique for directly modulated lasers (DMLs). The dual lane transceiver is fabricated in a 40nm CMOS process, and consumes 236mW at 28Gb/s.
- In Paper 16.3, IBM Research describes a 56Gb/s optical receiver in 16nm CMOS FinFet technology with rapid power on/off functionality. It achieves a 6.8ns wake-up time while consuming always-on and off powers of 126mW and 8mW, respectively.
- In Paper 16.4, Oregon State University presents a 3-16Gb/s wireline transceiver in 65nm CMOS with clock domain equalization using integrated pulse width modulation (iPWM) encoding. The proposed transceiver can compensate 27dB loss at 10Gb/s with an efficiency of 1.8pJ/b.
- In Paper 16.5, Korea Advanced Institute of Science & Technology (KAIST) presents a 20Gb/s serial link transceiver in 40nm CMOS, which employs a framed-pulsewidth modulation (FPWM) scheme. It achieves a total throughput of 20Gb/s while keeping the minimum pulse width to the equivalent of 15Gb/s.
- In Paper 16.6, Pohang University of Science and Technology proposes a 7.8Gb/s/pin 1.96pJ/b phase-difference-modulation transmitter for highly-reflective memory interfaces. It demonstrates ISI suppression capability of a 14-tap DFE by overcoming 10 in-band notches.
- In Paper 16.7, Xilinx presents a 56Gb/s NRZ short reach wireline transceiver in 16nm FinFET technology. The transceiver achieves better than 1e-15 BER over a channel with 8dB loss at 28GHz while consuming 126mW at 56Gb/s.
- In Paper 16.8, Nvidia describes a 25Gb/s/pin ground-referenced single-ended serial link in 16nm CMOS that communicates off-package over 80mm of low-cost PCB and package interconnect. It achieves a link energy efficiency of 1.15pJ/b, and uses an adaptive digital regulator to compensate for process and temperature variations.
- In Paper 16.9, Jet Propulsion Laboratory (JPL) presents a digitally pre-distorted PAM-4 transceiver for contactless communications. It achieves 20Gb/s of data with a 127GHz carrier over 1mm air gap while consuming 79.5mW.

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Session 16 Highlights: Advanced Optical and Wireline Techniques

[16.7] A 126mW 56Gb/s NRZ Wireline Transceiver for Synchronous Short-Reach Applications in 16nm FinFET

Paper 16.7 Authors: *Marc Erett[1], Declan Carey[1], James Hudner[1], Ronan Casey[1], Kevin Geary[1], Pedro Neto[1], Mayank Rajy[2], Scott MacLeod[3], Hongtao Zhang[2], Arianne Roldan[2], Hongyuan Zhao[4], Ping-Chuan Chiang[4], Haibing Zhao[4], KeeHian Tan[4], Yohan Frans[2], Ken Chang[2]*

Paper 16.7 Affiliation: [1]Xilinx, Cork, Ireland, [2]Xilinx, San Jose, CA, [3]Acacia Communications, San Jose, CA, [4]Xilinx, Singapore, Singapore

Subcommittee Chair: *Frank O'Mahony, Intel, Hillsboro, OR, Wireline Subcommittee*

CONTEXT AND STATE OF THE ART

- Thanks to the speed increase in serial link communications, transceivers dedicated to chip-to-chip interconnections are becoming more and more demanding in terms of area and power consumption. Synchronous high speed interface standards have been recently proposed that target chip-to-chip communications across <10dB loss PCB traces. To meet this demand, this year's conference reports a 56Gb/s NRZ short-reach wireline transceiver implemented in a 16nm FinFET CMOS technology that uses a quad-rate clocking architecture and near-ground voltage-mode signaling.

TECHNICAL HIGHLIGHTS

- **NRZ Wireline Transceiver for 56Gb/s Synchronous Short Reach Applications in 16nm FinFET.**
  In Paper 16.7, Xilinx reports an 8-lane 56Gb/s NRZ transceiver for short reach links based on a near-ground voltage-mode transmitter output driver and an ILO-based delay adjustment for per-lane deskewing receiver. Channel loss equalization is based on transmitter-side sub-UI de-emphasis and a receiver-side single-stage continuous-time linear equalizer. The transceiver achieves 50% lower area and power consumption than state-of-the-art published solutions for the same application profile.

APPLICATIONS AND ECONOMIC IMPACT

- Transceivers operating up to 56Gb/s at minimum power and area will be critical for next-generation package-to-package integration, including tight electrical and optical integration.

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Session 17 Overview: Technologies for Health and Society

Technology Directions Subcommittee

Session Chair: *Patrick P. Mercier, University of California, San Diego, La Jolla, CA*

Session Co-Chair: *Long Yan, Samsung Electronics, Korea*

Subcommittee Chair: *Makoto Nagata, Kobe University, Japan, Technology Directions*

Advances in sensors, low-power circuits, and integration technologies are helping to revolutionize industries ranging from agriculture to healthcare. This session highlights innovations in connected sensors for improved food production, diagnostic imaging, physiochemical sensing, and neurophysiology. The first paper is an invited paper, and describes how advances in sensors, circuits, and algorithms can help improve the efficiency of food production. The second paper demonstrates a multi-camera capsule endoscope with integrated high-throughput communications. The next three papers describe sensing systems that are powered from and/or measure chemical parameters in gas for industrial applications, or in bodily fluids for healthcare applications. Subsequent papers demonstrate advances in transcranial communications, optoelectronic neural recorders, multi-modal wearable brain imagers, and closed-loop neural implants with integrated support vector machine classifiers.

- In Invited Presentation 17.1, Fujitsu presents a multifaceted overview of current challenges in agriculture and food production industries. The presentation then discusses how advances in sensors, integrated circuit technologies, wireless networks, artificial intelligence algorithms, and robotics can help make these industries more efficient.
- In Paper 17.2, KAIST presents a capsule endoscope supporting 360° visual angle by 4-Cameras and 80Mb/s body channel communication (BCC) transceiver for 4fps, VGA resolution image transmission. With the help of reconfigurable BCC receivers distributed on the human body, real-time localization of the capsule at sub-cm accuracy is demonstrated.
- In Paper 17.3, the University of California, San Diego demonstrates a wireless biosensing system powered directly by a Glucose/Lactate biofuel cell without a DC-DC converter. Operating at 0.3V, the presented chip includes an duty-cycled maximum power point tracker, a 180nW 64dB SNR passive ΔΣ ADC, and a 30pJ/b 920MHz transmitter.
- In Paper 17.4, Analog Devices describes an electrochemical impedance spectroscopy (EIS) SoC for electrochemical gas detection. It features 0.28mΩ sensitivity and 105dB dynamic range which has 5x better sensitivity and 10dB higher dynamic range compared to state-of-the-art.
- In Paper 17.5, the University of Toronto and the Toronto Western Hospital present a 12-channel potentiostat IC sensing K+ ions concentration in vivo by computing the impedance on the surface of biofouling-resistant label-free potassium-sensitive chemically functionalized microelectrodes. The 50nW, 5kHz-BW opamp-less ΔΣ ADC performs 19.5fJ/conv at an ENOB of 8bits, and is validated in a mouse model.
- In Paper 17.6, the University of California, Berkeley, demonstrates a wireless transceiver designed for transcranial applications. Utilizing off-chip 10x10mm^2 coupled inductors, the 65nm transceiver achieves a data rate of up to 200Mb/s with a bit error rate as low as 5x10^{-11} across scalp and skull; at a transmit power of 300uW, an energy efficiency of 1.5pJ/bit is achieved.
- In Paper 17.7, Cornell University presents a 330x90um^2 opto-electronic wireless system for neural recording applications. A 0.18μm CMOS chip is powered by an AlGaAs diodes that doubles as a PV cell and an LED, the latter of which is used for wireless telemetry of recorded neural data.
- In Paper 17.8, imec demonstrates an active sensing ASIC that supports simultaneous measurement of near-infrared spectroscopy (NIRS), electroencephalography (EEG), and electrical impedance tomography (EIT). Use of a silicon photomultiplier reduces the power needed for NIRS sensing, resulting in total ASIC power of 665μW.
- In Paper 17.9, the University of Toronto, the Krembil Neuroscience Center, the Toronto Western Hospital, and Princeton University present a neural interface SoC used for closed-loop control of neurological disorders. A 32-channel analog front-end captures data using an artifact-tolerant architecture, and classifies neural data with an integrated decaying-memory support vector machine before deciding when to activate a digitally charge-balanced neurostimulator.

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Session 17 Highlights: Technologies for Health and Society

[17.2] 4-Camera VGA-Resolution Capsule Endoscope with 80Mb/s Body-Channel Communication Transceiver and Sub-cm Range Capsule Localization

Paper 17.2 Authors: *J. Jang, J. Lee, K.-R. Lee, J. Lee, M. Kim, Y. Lee, J. Bae, H.-J. Yoo*

Paper 17.2 Affiliation: *KAIST, Daejeon, Korea*

Subcommittee Chair: *Makoto Nagata, Kobe University, Kobe, Japan, Technology Directions*

CONTEXT AND STATE OF THE ART

- Capsule endoscope supporting full 360º high-quality images with wireless telemetry is highly desirable for accurate but painless diagnoses of diseases in digestive tract.
- Although, capsule endoscopes with limited visual angle of view and/or without wireless telemetry have been previously demonstrated; this is the first realization of a fully integrated capsule endoscope with wireless telemetry supporting 4fps 360º VGA resolution image.

TECHNICAL HIGHLIGHTS

360º VGA resolution wireless capsule endoscope allows the patients to have an endoscopy outside of clinical settings

- In Paper 17.2, KAIST presents a capsule endoscope supporting 360º visual angle by 4 cameras and 80Mb/s body channel communication (BCC) transceiver for 4fps VGA-resolution image transmission. With the help of reconfigurable BCC receivers distributed on the human body, real-time localization of the capsule at sub-cm accuracy is demonstrated.

APPLICATIONS AND ECONOMIC IMPACT

- Wireless capsule endoscope increases the patient's autonomy and reduces healthcare costs significantly by facilitating cloud-based remote patient monitoring.

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[17.3] A 0.3V Biofuel-Cell-Powered Glucose/Lactate Biosensing System Employing a 180nW 64dB SNR Passive $\Delta\Sigma$ ADC and a 920MHz Wireless Transmitter

Paper 17.3 Authors: *A.F. Yeknami, X. Wang, S. Imani, A. Nikoofard, I. Jeerapan, J. Wang, P.P. Mercier*

Paper 17.3 Affiliation: *University of California, San Diego, La Jolla, CA*

Subcommittee Chair: *Makoto Nagata, Kobe University, Kobe, Japan, Technology Directions*

CONTEXT AND STATE OF THE ART

- Wearable and implantable glucose sensors conventionally require a bulky battery and DC-DC converters to power electronic readout circuits.
- Powering directly from low-voltage energy-harvesting sources without a DC-DC converter requires sophisticated circuits that reliably operate at very low voltages.

TECHNICAL HIGHLIGHTS

Self-powered glucose sensing: a wireless chip extracts energy from a glucose biofuel cell and wirelessly reports glucose concentration without a battery

- In Paper 17.3, the University of California, San Diego demonstrates a wireless biosensing system powered directly by a Glucose/Lactate biofuel cell without a DC-DC converter or battery.
- Operating at 0.3V, the presented chip includes an duty-cycled maximum power point tracker, a 180nW 64dB SNR passive ΔΣ ADC, and a 30pJ/b 920MHz transmitter.

APPLICATIONS AND ECONOMIC IMPACT

- Diabetes is projected to affect 522 million people worldwide by 2030. Many of these patients require frequent monitoring of glucose levels, yet conventional technology requires invasive blood draws and large cumbersome power sources.
- The multi-billion-dollar glucometer market can potentially benefit from self-powered glucose sensors that eliminate bulky batteries and DC-DC converters.
- Low-voltage instrumentation, including ADCs and transmitters, can also be potentially valuable to other low-power IoT applications.

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[17.9] A Recursive-Memory Brain-State Classifier with 32-Channel Track-and-Zoom $\Delta^2\Sigma$ ADCs and Charge-Balanced Programmable Waveform Neurostimulators

Paper 17.9 Authors: *G. O'Leary[1], R. Pazhouhandeh[1], D. Groppe[2], T.A. Valiante[3], N. Verma[4], R. Genov[1]*

Paper 17.9 Affiliation: *[1]University of Toronto, Canada ; [2]Krembil Neuroscience Center, Toronto, Canada ; [3]Toronto Western Hospital, Toronto, Canada; [4]Princeton University, Princeton, NJ*

Subcommittee Chair: *Makoto Nagata, Kobe University, Kobe, Japan, Technology Directions*

CONTEXT AND STATE OF THE ART

- Neural interface SoCs are used for closed-loop control of neurological disorders.
- The state-of-the-art in such SoCs are pushing towards increasingly rich feature sets for enhancing the specificity of therapeutic and abortive stimulations.

TECHNICAL HIGHLIGHTS

Brain State Classifier with 32-Channel Programmable Waveform Neurostimulators

- In Paper 17.9, researchers from University of Toronto, Krembil Neuroscience Center, Toronto Western Hospital and Princeton University present a 32-channel analog front-end that captures data using an artifact-tolerant architecture, and classifies neural data with an integrated decaying-memory support vector machine before deciding when to activate a digitally charge-balanced neurostimulator.
- The paper exploits a rich feature set including spectral energy, phase-locking, and cross-coupling parameters to enhance brain state classification.

APPLICATIONS AND ECONOMIC IMPACT

- Electroceuticals and neuromodulators represent areas of increasing investment by the pharmaceutical and medical device industry.
- The resulting devices are having a great impact in enhancing the quality of life for patients suffering from drug-resistant diseases especially those of the central nervous system.

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Session 18 Overview: Adaptive Circuits & Digital Regulators

Digital Circuit Techniques Subcommittee

Session Chair: *Dennis Sylvester, University of Michigan, Ann Arbor, MI*

Session Co-Chair: *Koji Hirairi, Sony LSI Design, Kanagawa, Japan*

Subcommittee Chair: *Edith Beigne, CEA-LETI, Grenoble, France, Digital Circuits Subcommittee*

This session focuses on circuits that detect and adapt to various types of process-voltage-temperature-aging (PVTA) variations, along with the latest progress in digital low-dropout (LDO) voltage regulators. The presented adaptive circuits demonstrate rapid and accurate voltage-droop detection to perform instruction throttling, clock period stretching via use of a critical-path replica within the phase-locked loop (PLL) and (buck) voltage regulator, and closed-loop continuous-body-bias for temperature, process, and aging compensation. There are five digital LDO papers that introduce a range of new techniques, such as an analog-assisted NMOS power transistor, a beat-frequency-based adaptive-sampling scheme, and the replacement of traditional power-transistor devices with a switched-capacitor resistor. These papers also describe a distributed LDO array that improves IR drop and response time, as well as an LDO that is designed to minimize pass-through of voltage ripple from a preceding switching regulator.

- In Paper 18.1, IBM describes a new set of techniques to improve latency in voltage-droop mitigation, including slope calculation and unit-to-unit communication, that double the performance gains over their previous-generation design. They also describe a new method to estimate voltage noise in a large processor using local activity detectors. These techniques are validated on their latest 14nm enterprise class processor.
- In Paper 18.2, the University of Washington presents a combined buck converter and PLL design in 65nm that uses a programmable canary-based oscillator to reduce the impact of supply droop on timing margin. Combined with all-digital autonomous switching between continuous- and discontinuous-conduction modes, the design reduces margin by 90% and offers 95% peak converter efficiency across 0.6-1.0V.
- In Paper 18.3, CEA-LETI and STMicroelectronics describe a low-overhead compensation unit that provides continuous and body-bias values to reduce leakage at fixed frequency across process/temperature/aging variation in 28nm FDSOI technology. The unit is 92× smaller and 4× lower power than prior work in body-bias generation, while offering 100μs response time across a wide supply voltage range of 0.35-1V.
- In Paper 18.4, the University of Macau presents a digital LDO design that exploits an NMOS power device for intrinsic response to output voltage droops, and employs a high-pass analog path with a voltage-doubled NAND gate to increase conductance during load transients. Together, these techniques enable a 5.1fs speed FoM in a 0.0055mm^2 28nm LDO that provides 20mA output current with 50mV minimum dropout.
- In Paper 18.5, the University of Minnesota and Cisco describe a new approach to balancing the demands of response time (speed) and quiescent current (power) in a digital LDO. An adaptive sampling frequency is generated via a beat-frequency quantizer. The resulting 0.0374mm^2 design in 65nm improves settling time by 25× and voltage droop by 5× over a fixed sampling frequency design and uses a small 40pF output capacitor.
- In Paper 18.6, the Hong Kong University of Science and Technology presents a 3×3 mesh of analog-assisted LDOs that work together to supply 500mA to an unevenly distributed load. Using interleaved phases for clocking, the 9 LDOs work together to improve response speed. The design is fabricated in 65nm CMOS process and employs a 0.9nF on-chip capacitor.
- In Paper 18.7, the University of California San Diego describes a fully digital LDO that uses a switched-capacitor resistance to replace the PMOS switch array in conventional digital LDOs. The 65nm CMOS design achieves 99.3% peak current efficiency at 3mA I_{LOAD}, 34.3ps speed FoM and less than 1.5mV voltage ripple in steady state.
- In Paper 18.8, National Chiao Tung University presents a fully digital LDO in 40nm using a non-linear switch control technique to improve current efficiency by decreasing quiescent current and reducing switching power consumption with variable-switching frequency control. It achieves peak current efficiency of 99.8% at 20mA I_{LOAD}, under 10uA quiescent current, 6mV voltage ripple, and 40mV droop (1.3μs transient response time) on a 1-to-20mA load step.

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Session 18 Highlights: Adaptive Circuits & Digital Regulators

[18.1] Droop Mitigation Using Critical-Path Sensors and an On-Chip Distributed Power-Supply Estimation Engine in the z14™ Enterprise Processor

Paper 18.1 Authors: *C. Vezyrtzis[1], T. Strach[2], P. Chuang[1], P. Lobo[3], R. Rizzolo[4], T. Webel[2], P. Owczarczyk[4] A. Buyuktosunoglu[1], R. Bertran[1], D. Hui[4], S. Eickhoff[4], M. Floyd[5], G. Salem[6], S. Carey[4], S. Tsapepas[4], P. Restle[1]*

Paper 18.1 Affiliation: *[1]IBM Research, Yorktown Heights, NY; [2]IBM STG, Boeblingen, Germany, [3]IBM STG, Bangalore, India; [4]IBM STG, Poughkeepsie, NY; [5]IBM STG, Austin, TX; [6]IBM STG, Essex Junction, VT*

CONTEXT AND STATE OF THE ART

- Large current draw in high-performance processors leads to droops on power supply rails, necessitating margining and hence, degraded performance.
- Innovations in supply voltage droop mitigation therefore enhance performance and energy efficiency in data center/cloud computing applications.

TECHNICAL HIGHLIGHTS

- **IBM demonstrates two novel voltage droop detection techniques to improve the response time for droop mitigation enhancing the z14™ performance.**
- The z14™ integrates two novel techniques for mitigating the impact of voltage droops on performance. One technique detects voltage droops by continuously tracking critical-path-monitor (CPM) delay changes, as well as CPM measurements from neighboring cores to trigger core instruction throttling to reduce the current demand, and thus the droop magnitude. The second technique employs a distributed on-chip cycle-by-cycle-accurate (CBCA) voltage estimation engine based on core activity counters. The voltage droop mitigation scheme with the CPM detectors enables a 4% processor frequency improvement. The CBCA voltage estimation engine accurately tracks the effect of a voltage droop on CPM delay, indicating the potential of replacing the CPM with the estimator to trigger the instruction throttling in future implementations.

APPLICATIONS AND ECONOMIC IMPACT

- Datacenter operating costs, dominated by energy costs, drive the need to improve energy efficiency in high-performance processors.
- Robust operation and peak performance for ultra-high-reliable data compute centers are crucial for many business applications, including machine learning and in financial industries.

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Session 19 Overview: Sensors and Interfaces

Analog Subcommittee

Session Chair: *Man-Kay Law, University of Macau, China*

Session Co-Chair: *Taeik Kim, Samsung Electronics, Hwaseong, Korea*

Subcommittee Chair: *Kofi Makinwa, Delft University of Technology, Delft, The Netherlands, Analog Subcommittee*

This session highlights the advances in state-of-the-art temperature, current, physical and chemical sensors. Three energy-efficient CMOS temperature sensors with the best figures of merit down to 34fJ·K^2 are reported. Two current sensors (Papers 4 and 5) are presented, one demonstrating a high room-temperature gain accuracy with a ±4A input range, while the other shows a 160dB DR biosensor readout with 7ppm INL. An energy-efficient pressure-sensing system (Paper 6) and a high-resolution readout IC (Paper 7) are also reported. An energy-efficient CO_2 sensor achieving 2× better resolution (94ppm) and >10× lower energy consumption (12mJ/meas) than the prior art is also described (Paper 8).

- In Paper 19.1, Intel Advanced Design describes a hybrid temperature sensor using subthreshold NMOS devices and parasitic PNPs. It enables single-element remote sensing with a small size (0.00021mm^2) and achieves 3× better Resolution-FOM of 0.54nJ·K^2 using a 22nm FinFET process.
- In Paper 19.2, Delft University of Technology presents the first resistor-based CMOS temperature sensor capable of operating over the full military range (-55°C to 125°C). It achieves state-of-the-art energy efficiency of 32fJ·K^2 with 3× smaller area.
- In Paper 19.3, Yonsei University describes a highly compact resistor-based CMOS temperature sensor for dense thermal monitoring in nanometer semiconductor processes. The proposed PPF-based FLL shows 13× smaller area and 15× higher resolution-FOM when compared to similar prior art.
- In Paper 19.4, Delft University of Technology presents a current sensor that supports a ±4A range with 0.05% gain error at room temperature. It achieves a resolution of 150µA$_{rms}$ in a conversion time of 2ms while consuming 10.9µA, which is 10× more energy efficient than the state-of-the-art.
- In Paper 19.5, the University of California, San Diego presents an accurate current measurement with wide dynamic range and high linearity for biosensor readouts. With an asynchronous Hourglass ADC, the system achieves 7ppm INL and 160dB DR.
- In Paper 19.6, the University of Michigan describes a duty-cycled bridge-to-digital converter for a small battery-operated pressure sensing system. By heavily duty-cycling the bridge sensor's excitation voltage, the system requires 6000× less excitation power. It consumes 2.5nJ/conversion and achieves 49.2dB SNR and 10.6pJ/conv-step FOM.
- In Paper 19.7, Seoul National University presents a fully-integrated gain-programmable read-out IC with a maximum resolution of >21b. With the proposed system chopping technique utilizing an on-chip reconfigurable digital filter, the system achieves a low 1/f corner <100µHz and a maximum FOM that is 5.3dB higher than previous work.
- In Paper 19.8, Delft University of Technology presents a CMOS-compatible thermal-conductivity-based CO_2 sensor using a high-resolution phase-domain delta-sigma modulator to sense the thermal time constant of a hot tungsten wire. The sensor achieves a CO_2 sensor resolution of 94ppm while dissipating only 12mJ per measurement.

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Session 19 Highlights: Sensors and Interfaces

[19.4] A ±4A High-Side Current Sensor with 25V Input CM Range and 0.9% Gain Error from -40ºC to 85ºC Using an Analog Temperature Compensation Technique

Paper 19.4 Authors: *Long Xu, Johan Huijing, Kofi Makinwa*

Paper 19.4 Affiliation: *Delft University of Technology, Delft, The Netherlands*

[19.1] An 8b Subthreshold Hybrid Thermal Sensor with ±1.07ºC Inaccuracy and Single-Element Remote Sensing Technique in 22nm FinFET

Paper 19.1 Authors: *Cho-Ying Lu[1], Surej Ravikumar, Amruta D Sali[1], Matthias Eberlein[2], Hyung-Jin Lee[1]*

Paper 19.1 Affiliation: [1]*Intel, Hillsboro, OR,* [2]*Intel, Neubiberg, Germany*

Subcommittee Chair: *Kofi Makinwa, Delft University of Technology, Delft, The Netherlands, Analog*

CONTEXT AND STATE OF THE ART

- Temperature sensors are scaling down to enable more local temperature sensing in silicon, which is needed in highly dense technologies. By reducing the remote sensing to one element only connected with one wire, the overhead of adding temperature sensing is reduced to the bare minimum.
- Current measurement systems become more and more important for controlling and protecting battery-powered devices and transport. Increasing the accuracy and common-mode input range are key to enabling high-side measurement capabilities. Reduction of the power consumption of the measurement chain while increasing the accuracy enables longer battery lifetimes.

TECHNICAL HIGHLIGHTS

Fully integrated 4A CMOS current sensor with 25V common-mode range

- In Paper 19.4 Delft University of Technology presents a current sensor that supports a ±4A range with 0.05% gain error at room temperature. It achieves a resolution of $150\mu A_{rms}$ in a conversion time of 2ms while consuming 10.9µA, which is 10× more energy efficient than state of the art.

Ultra-small remote temperature sensor enabling distributed monitoring in 22nm FinFET technology

- In Paper 19.1 Intel Advanced Design describes a hybrid temperature sensor using subthreshold NMOS and parasitic PNP transistors. It enables single-element remote sensing ($0.00021mm^2$) and achieves 3× better resolution-FOM of $0.54nJ{\cdot}K^2$ using a 22nm FinFET process.

APPLICATIONS AND ECONOMIC IMPACT

- Distribution of temperature sensors in highly dense devices provides information for thermal protection or performance optimization.
- Enabling more accurate current-sensing techniques enables better protection of the battery, guaranteeing a longer lifetime.

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Session 20 Overview: Flash Memory Solutions

Memory Subcommittee

Session Chair: *Ki-Tae Park, Samsung Electctonics, Hwaseong, Korea*

Session Co-Chair: *Yan Li, Western Digital, Milpitas, CA*

Subcommittee Chair: *Leland Chang, IBM, Yorktown Heights, NY*

Continued proliferation of semiconductors for a smarter society drives the evolution of flash memory technologies towards higher density, lower power consumption, and lower cost. This year, a new generation of 3D NAND Flash memory with up to 96-stacked word-line layers is introduced. For the first time, a memory with over 1Tb density is demonstrated using a 4b/cell 3D NAND technology. An ultra-low latency flash controller with a new high-speed 3D NAND is proposed in order to fill a large performance gap between DRAM and Flash memories.

- In Paper 20.1, Toshiba and Western Digital present a 512Gb 3b/cell 3D NAND Flash with an advanced 96-stacked WL-layer technology. A start bias control scheme designed for 3D NAND is proposed to enhance program performance by 7% and a new smart on-chip V_{th}-tracking read that can support program suspend function is also presented.

- In Paper 20.2, Samsung presents an ultra-low latency Flash controller using a high-performance 3D NAND that supports a 15μs-latency SSD, which is over 3-5 times faster than a conventional SSD. To provide such a high-performance gain, a split DMA architecture and an advanced suspend/resume DMA operation are proposed.

- In Paper 20.3, Samsung presents a 1Tb NAND Flash in 64 stacked layers by using a 4b/cell technology. It achieves a 5.63Gb/mm^2 areal density; the highest density ever. In order to control tight V_{th} distributions at 12MB/s, a new fast unselect precharging scheme and a slow bit bypass scheme are proposed.

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Session 20 Highlights: Flash Memory Solutions

[20.1] A 512Gb 3b/Cell 3D Flash Memory on a 96-Word-Line-Layer Technology

Paper 20.1 Authors: *Hiroshi Maejima[1], Kazushige Kanda[1], Manabu Sato[1], Toshifumi Hashimoto[1], Xu Li[1], Bushnaq Sanad[1], Susumu Fujimura[1], Yuuki Shimizu[1], Kenichi Abe[1], Tadashi Yasufuku[1], Junji Musha[1], Takatoshi Minamoto[1], Hiroshi Yoshihara[1], Mizuho Yoshida[1], Katsuaki Sakurai[1], Takahiro, Yamashita[1], Hicham Haibi[1], Kazuhiko Satou[2], Tohru Tategami[3], Teruo Takagiwa[1], Takahiro Sugimoto[1], Fumihiro Kono[1], Masatsugu Ogawa[1], Yusuke Ochi[1], Naoaki Kanagawa[1], Mitsuhiro Abe[1], Tomoharu Hashiguchi[1], Masatsugu Kojima[1], Makoto Matsuda[3], Hikaru Mochizuki[3], Satoshi Inoue[1], Yasuhiro Suematsu[2], Kenro Kubota[2], Taichi Wakui[2], Yoshihiko Shindo[1], Takahiro Shimizu[1], Akihiro Imamoto[1], Naoki Kobayashi[1], Makoto Miakashi[1], Kouichirou Yamaguchi[1], Dong He[1], Weihan Wang[1], Hiroe Minagawa[1], Tomoko Nishiuchi[1], Susumu Ozawa[1], Jumpei Sato[1], Naohito Morozumi[1], Ryo Fukuda[1], Yuui Shimizu[1], Hao Nguyen[4], Kwang-Ho Kim[4], Ken Cheah[4], Yee Koh[4], Feng Liu[4], Venky Ramachandra[4], Srinivas Rajendra[4], Steve Choi[4], Keyur Payak[4], Namas Raghunathan[4], Spiros Georgakis[4], Hiroshi Sugawara[4], Seungpil Lee[4], Takuya Futatsuyama[1], Koji Hosono[1], Noboru Shibata[1], Toshiki Hisada[1], Tetsuya Kaneko[1], Hiroshi Nakamura[1]*

Paper 20.1 Affiliation: *[1]Toshiba Memory, Yokohama, Japan, [2]Toshiba Memory Systems, Yokohama, Japan, [3]Toshiba Information Systems, Kawasaki, Japan, [4]SanDisk, Milpitas, CA*

[20.2] A Flash Memory Controller for 15µs Ultra-Low-Latency SSD Using High-Speed 3D NAND Flash with 3µs Read Time

Paper 20.2 Authors: *Jin-Hyeok Choi, Wooseong Cheong, Chanho Yoon, Seonghoon Woo, Kyuwook Han, Daehyun Kim, Chulseung Lee, Youra Choi, Shine Kim, Dongku Kang, Geunyeong Yu, Jaehong Kim, Jaechun Park, Ki-Whan Song, Ki-Tae Park, Sangyeun Cho, Hwaseok Oh, Daniel DG Lee, Jaeheon Jeong*

Paper 20.2 Affiliation: *Samsung Electronics, Hwaseong, Korea*

[20.3] A 1Tb 4b/Cell 64-Stacked-WL 3D NAND Flash Memory with 12MB/s Program Throughput

Paper 20.3 Authors: *Seungjae Lee, Chulbum Kim, Minsu Kim, Sungmin Joe, Ki-Tae Park*

Paper 20.3 Affiliation: *Samsung Electronics, Hwaseong, Korea*

Subcommittee Chair: *Leland Chang, IBM, Yorktown Heights, NY, Memory*

CONTEXT AND STATE OF THE ART

- The three papers in this session are all front-runners in three different directions in fast-evolving flash memory technologies.
- One paper showcases the most advanced 3D NAND technology with the world's first 96 layers with TLC. Another paper achieved the world's highest density QLC flash memory. The 3rd paper provides a microcontroller solution to the world's fastest SLC NAND.

TECHNICAL HIGHLIGHTS

- [20.1] Toshiba and Western Digital present a 512Gb 3b/cell 3D NAND Flash with an advanced 96-stacked WL layer technology.
- [20.2] Samsung presents an ultra-low latency Flash controller using the fastest performance 3D NAND, which supports a 15µs latency SSD that is over 3-5 times faster than a conventional SSD.

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- [20.3] Samsung presents a 1Tb 3D NAND Flash using 4b/cell that achieves a 5.63Gb/mm^2 areal density; the highest density ever.

APPLICATIONS AND ECONOMIC IMPACT

- 96-layer 3D NAND demonstrates continued physical scaling and cost reduction in the Flash memory industry. The logical scaling to QLC gives an extra cost reduction. Cheaper NAND Flash will continue to fuel its application in data centers, mobile devices and other storage applications.
- The SSD based on fast NAND provided comparable performance to the Intel Optane SSD. This fast media will fill a gap between Flash and DRAM in computer hierarchy and will fuel high-performance applications.

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Session 21 Overview: Extending Silicon and its Applications

Technology Directions Subcommittee

Session Chair: *Jan Genoe, imec, Belgium*

Session Co-Chair: *Frederic Gianesello, STMicroelectronics, France*

Subcommittee Chair: *Makoto Nagata, Kobe university, Japan, Technology Directions*

This session includes six papers from the Technology Directions subcommittee at ISSCC 2018. The first two papers present advances in mixed signal processing for machine learning, the third paper describe a 32GHz mechanical resonator achieved for the first time in 14nm FinFET technology, the fourth paper reviews 10Gb/s Si Photonics transceiver targeting 1Tb/s/mm^2 die-to-die communication, the fifth paper describes an innovative sensor to detect laser fault injection attack on a cryptographic core in order to avoid any information exposure and the final paper presents an injection locked VCO array targeting ESR application.

- In Paper 21.1, KU Leuven University presents a highly-configurable non-linear mixed-signal interface for sensor systems enabling energy-efficient and application-tunable translation from analog to non-linear digital. The work achieves 90nm IC proof-of-concept demonstrating up to 33kS/s operation and 50% data-reduction while preserving 9.5b resolution in the region-of-interest
- In Paper 21.2, Columbia University presents a voice activity detector using analog signal processing and a digital deep neural network classifier for feature extraction. Ultra-low power operation of 380nW is achieved (9.4× improvement) while delivering mean speech/non-speech hit-rate of 85.4%.
- In Paper 21.3, MIT, Purdue University and Globalfoundries present a 32GHz Resonant-Fin Transistors in 14nm FinFET Technology. A periodic array of fins forms a slow-wave structure that achieves confinement of mechanical vibrations in the FEOL.
- In Paper 21.4, CEA-LETI and ST Microelectronics present a 10Gb/s Si-photonic transceiver for 1Tb/s/mm^2 die-to-die optical networks. A 10Gb/s 150µW Si-photonic Transceiver with 120µs lock-time has been obtained through digitally-supervised analog micro-ring wavelength stabilization.
- In Paper 21.5, Kobe University, The University of Electro-Communication and Nara Advanced Institute of Technology present a 286F^2/Cell distributed bulk-current sensor that protects against laser fault injection attacks by securely flush erasing the code. The erasing is in the nanosecond order and the overall overhead is only 28%.
- In Paper 21.6, Ulm University and Helmholtz-Zentrum Berlin für Materialien und Energie present an array of eight injection locked VCOs for ESR spectroscopy operating around 13GHz. By using injection locking, this circuit enables a 10-fold increase in sensitive volume and a 10-fold improvement in noise frequency floor.

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Session 21 Highlights: Extending Silicon and its Applications

[21.1] Mixed-Signal Programmable Non-Linear Interface for Resource-Efficient Multi-Sensor Analytics

Paper 21.1 Authors: *Komail Badami, Juan-Carlos Pena Ramos, Steen Lauwereins, Marian Verhelst*

Paper 21.1 Affiliation: *KU Leuven, Leuven, Belgium*

Subcommittee Chair: *Makoto Nagata, Kobe University, Kobe, Japan, Technology Directions*

CONTEXT AND STATE OF THE ART

- Analog signal processing is a powerful technique that enables power-efficient compression of sensor signals and reduces the power consumption required for signal processing.
- Current mixed-signal non-linear interfaces are not programmable, thus providing some scalability to be able to adapt the circuit performance to various use cases is a desirable feature.

TECHNICAL HIGHLIGHTS

Mixed-Signal Programmable Interface for Resource-Efficient Multi-Sensor Analytics

- In Paper 21.1. KU Leuven presents, for the first time, a highly configurable non-linear mixed-signal interface for sensor systems enabling energy-efficient and application-tunable translation from analog to non-linear digital domain.
- The work demonstrates a proof-of-concept in 90nm CMOS demonstrating up to 33kS/s operation and 50% data-reduction while preserving 9.5b resolution in the region-of-interest.

APPLICATIONS AND ECONOMIC IMPACT

- Analog signal processing targeting low-power IoT applications.

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[21.2] A 1µW Voice Activity Detector using Analog Feature Extraction and Digital Deep Neural Network

Paper 21.2 Authors: *Minhao yang, Chung-Heng Yeh, Yiyin Zhou, Joao Oedro Cerqueira, Aurel Lazar, Mingoo Seok*

Paper 21.2 Affiliation: *Columbia University, New York, NY*

Subcommittee Chair: *Makoto Nagata, Kobe University, Kobe, Japan, Technology Directions*

CONTEXT AND STATE OF THE ART

- Voice activity detectors are used to provide a compelling user interface for wearable and mobile devices.
- Prior arts were targeting high sensitivity and consequently power consumption was not optimal.

TECHNICAL HIGHLIGHTS

Voice Activity Detector using Analog Feature Extraction and Digital Deep Neural Network

- In Paper 21.2, Columbia University presents a voice activity detector using analog signal processing and a digital deep-neural-network classifier for feature extraction.
- Ultra-low-power operation of 380nW is achieved (9.4× improvement) while delivering a mean speech/non-speech hit-rate of 85.4%.

APPLICATIONS AND ECONOMIC IMPACT

- Low-power wearable and mobile devices using a voice user interface.

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[21.4] A 10Gb/s Si-Photonic Transceiver with 150µW 120µs-Lock-Time Digitally Supervised Analog Microring Wavelength Stabilization for 1Tb/s/mm² Die-to-Die Optical Networks

Paper 21.4 Authors: *Y.Thonnart[1], J.L.Gonzalez-Jimenez[1], G.Waltener[1], R.Polster[1], O.Dubray[1], M.Zid[1], F.Lepin[1], S,Bernabe[1], S.Menezo[1], G.Pares[1], O.Castany[1], L. Boutafa[1], P.Grosse[1], B.Charbonnier[1], C.Baudot[2]*

Paper 21.4 Affiliation: [1]*CEA-LETIT-MINATEC, Grenoble, France,* [2]*STMicroelectonices, Crolles, France*

Subcommittee Chair: *Makoto Nagata, Kobe University, Kobe, Japan, Technology Directions*

CONTEXT AND STATE OF THE ART

- The strong temperature-dependence of the microrings for WDM (wavelength-division-multiplexing) systems requires temperature robustness by a fine-tuning of wavelength.

TECHNICAL HIGHLIGHTS

Silicon-photonic Transceiver for high Die-to-Die Optical Networks

- In Paper 21.4, CEA-LETI-MINATEC presents a high density and highly stable 3D-stacked CMOS-on-Si-photonic transceiver chip
- A 10Gb/s Si-photonic transceiver for Die-to-Die WDM optical communications, consist of 4 RX modulator driver and 2 RX receiver, achieves a 120µs wavelength lock-time by digitally-supervised analog closed loop stabilization.

APPLICATIONS AND ECONOMIC IMPACT

- The wavelength-locked electro-optical die-to-die communication networks pave the realization of unlimited high-performance computation applications.

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Session 22 Overview: Gigahertz Data Converters

Data Converter Subcommittee

Session Chair: *Kostas Doris, NXP Semiconductors, Eindhoven, The Netherlands*

Session Co-Chair: *Jan Westra, Broadcom Ltd, Bunnik, The Netherlands*

Subcommittee Chair: *Un-Ku Moon, Oregon State University, Corvallis, OR*

Extensive calibrations, the use of FinFET technology and architectural innovations continue to push the bandwidth and dynamic range envelopes of high-speed data converters. This session covers gigahertz data converters covering resolutions from 8b up to 16b and sampling rates up to 72GS/s.

In the first paper, an ADC designed in 14nm CMOS extends hierarchical time interleaving techniques combined with high-speed low-power SAR ADCs and extensive calibrations to enable a record sampling rate for 8-bit converters with only 235mW power dissipation.

In the second paper, a Nyquist DAC designed in 16nm CMOS combines a current source calibration scheme with dynamic element matching to push the boundaries of linearity across the whole Nyquist range.

Finally, a hybrid DAC introduces a bandpass Delta Sigma modulator architecture with pre-distortion techniques for agile signal generation of RF carrier signals up to 6GHz.

- In Paper 22.1, IBM presents a 24-72GS/s 8b ADC in 14nm CMOS that achieves 30dB SNDR at Nyquist. This ADC employs hierarchical interleaving with 16 parallel sampling switches each driving 4 sub ADCs. The 64 asynchronous 8b SAR ADCs use separate comparators per bit and are extensively calibrated for offset, gain and timing errors.

- In Paper 22.2, Broadcom presents a 16b 6GS/s Nyquist DAC in 16nm FinFET technology. Utilizing calibration and Dynamic Element Matching, this DAC achieves an IMD <-90dBc up to 1.9GHz and SFDR >80dBc up to 900MHz, occupying an area of 0.52mm^2, while consuming 350mW.

- In Paper 22.3, the University of Southern California presents a 16b 12GS/s bandpass Delta-Sigma DAC in 65nm CMOS able to tune to the center frequency up to 6GHz. A timing and amplitude error correction scheme combined with inverse sinc pre-distortion enables it to achieve an IM3 from -85 to -67dBc up to Nyquist and an SFDR >60dBc at 4.2GHz.

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Session 22 Highlights: Gigahertz Data Converters

[22.1] A 24-to-72GS/s 8b Time-Interleaved SAR ADC with 2.0-to-3.3pJ/conversion and >30dB SNDR at Nyquist in 14nm CMOS FinFET

Paper 22.1 Authors: Lukas Kull[1], Danny Luu[1,2], Christian Menolfi[1], Matthias Braendli[1], Pier Andrea Francese[1], Thomas Morf[1], Marcel Kossel[1], Alessandro Cevrero[1], Ilter Ozkaya[1,3], Thomas Toifl[1]

Paper 22.1 Affiliation: [1]IBM Zurich Research Laboratory, Rueschlikon, Switzerland, [2]ETH Zurich, Zurich, Switzerland, [3]EPFL Lausanne, Switzerland

[22.2] A 16b 6GS/s Nyquist DAC with IMD <-90dBc up to 1.9GHz in 16nm CMOS

Paper 22.2 Authors: Chi-Hung Lin, Koon Lun Jacki Wong, Tae-Youn Kim, Guangxi Ray Xie, Donald Major, Gregory Unruh, Hans Eberhart, Ardie Venes

Paper 22.2 Affiliation: Broadcom, Irvine, CA

[22.3] A 16b 12GS/s Single/Dual-Rate DAC with Successive Bandpass Delta-Sigma Modulator Achieving <-67dBc IM3 Within DC-to-6GHz Tunable Passbands

Paper 22.3 Authors: Shiyu Su and Mike Shuo-Wei Chen

Paper 22.3 Affiliation: University of Southern California, Los Angeles, CA

Subcommittee Chair: *Un-Ku Moon, Oregon State University, Corvallis, OR*

CONTEXT AND STATE OF THE ART

- High-bandwidth data converters, with bandwidths above 1GHz, are required in future communication applications.
- Advanced IC technologies, like 16nm and 14nm FinFET CMOS, allow data converters to push the traditional bandwidth limits and shift traditionally analog functions into the digital domain.
- Extensive calibration, randomization and interleaving techniques break the traditional trade-offs between resolution, noise, area, and power consumption.

TECHNICAL HIGHLIGHTS

- **IBM demonstrates a CMOS 72GS/s ADC that achieves >30dB SNDR at Nyquist consuming 235mW.**
- **The Broadcom 16b 6GS/s DAC achieves an IMD <-90dBc up to 1.9GHz, dissipating 350mW.**
- **USC demonstrates a 16b 12GS/s DAC using bandpass delta-sigma modulation in 65nm CMOS.**

APPLICATIONS AND ECONOMIC IMPACT

- High-bandwidth data converters enable digital implementation of traditionally analog functions such as up-conversion mixing or DFE.
- New techniques and scaled technology help to reduce power consumption and save system cost by reducing area and integrating functions in a single chip.

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Session 23 Overview: LO Generation

RF Subcommittee

Session Chair: *Hyunchol Shin, Kwangwoon University, Seoul, Korea*

Session Co-Chair: *Andrea Bevilacqua, University of Padova, Padova, Italy*

Subcommittee Chair: *Piet Wambacq, imec, Belgium, RF Subcommittee*

The session presents LO-generation systems aimed at 5G communications and sub-mm-wave sensing systems. The first three papers focus on mm-wave CMOS LOs for multiband 5G systems and highlight the importance of injection-locked frequency multipliers and accurate quadrature generation for the 28-to-44GHz band. Then, the session continues with a BiCMOS 301.7-to-331.8GHz source and a 4GHz inverse-Class-F CMOS VCO. A quad-core BiCMOS 15GHz VCO is presented next, while a 7.4-to-14GHz CMOS PLL concludes the session.

- In Paper 23.1, Ulsan National Institute of Science and Technology presents a multiband LO generator for 5G systems covering 5.2-to-6GHz and 25-to-30GHz bands and showing -31.4dBc integrated phase noise and 206fs_{rms} jitter for a 29GHz carrier.
- In Paper 23.2, University of Pavia presents a circuit capable of precise generation of quadrature signals over a wide frequency range for 5G communication systems. Over the 28-to-44GHz frequency range, the circuit achieves a quadrature error of less than 1°.
- In Paper 23.3, University of Electronic Science and Technology of China presents an injection-locked frequency tripler operating from 22.8 to 43.2GHz to support multiband 5G applications. The signal generator achieves -40dBc integrated phase noise at 28GHz with a 41.8mW power consumption.
- In Paper 23.4, University of Michigan, Cornell University, and STMicroelectronics describe a frequency stabilization technique for mm-wave/THz oscillators. The paper presents a BiCMOS 300GHz oscillator having a very stable frequency output without the need for a PLL or an off-chip crystal and providing a peak output power of -13.9dBm across a 302-to-332GHz range.
- In Paper 23.5, University of Macau describes a 4GHz very-low-phase-noise inverse-Class-F CMOS VCO that significantly improves phase noise in $1/f^2$ and $1/f^3$ regions. The VCO exhibits an FOM of 196.2dBc/Hz with a tuning range of 25.5% between 3.5 and 4.5GHz.
- In Paper 23.6, Infineon Technologies and University of Padova present an ultra-low-phase-noise 15GHz quad-core oscillator. Over a 16% tuning range, the phase noise is -124dBc/Hz at a 1MHz offset, and the oscillator FOM is -189dBc/Hz.
- In Paper 23.7, Xilinx describes a 7.4-to-14GHz PLL in a 16nm FinFET process. The design provides 54fs_{rms} jitter, in-band noise of -120dBc/Hz at a 100kHz offset, a -75.5dBc reference spur with the power dissipation of 45 mW.

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Session 23 Highlights: LO Generation

[23.4] A 301.7-to-331.8GHz Source with Entirely On-Chip Feedback Loop for Frequency Stabilization in 130nm CMOS

Paper 23.4 Authors: *C. Jiang[1,2], A. Cathelin[3], E. Afsari[1,2]*

Paper 23.4 Affiliation: *[1]University of Michigan, Ann Arbor, MI, [2]Cornell University, Ithaca, NY, [3]STMicroelectronics, Crolles, France*

[23.5] An Inverse-Class-F CMOS VCO with Intrinsic-High-Q 1st- and 2nd- Harmonic Resonance for $1/f^2$-to-$1/f^3$ Phase Noise Suppression

Paper 23.5 Authors: *C.-C. Lim[1,2], J. Yin[1], P.-I. Mak[1], H. Ramiah[2], R. P. Marins[1,3]*

Paper 23.5 Affiliation: *[1]University of Macau, Macau, China, [2]University of Malaya, Kuala Lumpur, Malaysia, [3]University of Lisbon, Lisbon, Portugal*

Subcommittee Chair: *Piet Wambacq, imec, Belgium, RF Subcommittee*

CONTEXT AND STATE OF THE ART

- Very stable frequency sources operating from a few GHz to mm-waves are critical building blocks for wireless communication and sensing systems. Low-power and low-phase-noise design techniques for Si oscillators have always been needed and challenging.
- A new on-chip frequency-stabilization technique for a very stable 300GHz BiCMOS oscillator and a new phase-noise-reduction technique for a 4GHz CMOS oscillator are proposed in this session.

TECHNICAL HIGHLIGHTS

300GHz oscillator with on-chip frequency-stabilization technique.

- In Paper 23.4, University of Michigan, Cornell University, and STMicroelectronics describe a frequency-stabilization technique for mm-wave/THz oscillators. The design presents a 300GHz oscillator with a very stable frequency output without the need for a PLL or an off-chip crystal. The BiCMOS oscillator provides a peak output power of -13.9dBm across 302 to 332GHz range.

4GHz CMOS VCO with inherent phase-noise suppression.

- In Paper 23.5, University of Macau describes a 4GHz very-low-phase-noise inverse-Class-F CMOS VCO that significantly improves phase noise in $1/f^2$ and $1/f^3$ regions. The VCO exhibits an FOM of 196.2dBc/Hz with a tuning range of 25.5% between 3.5 and 4.5GHz.

APPLICATIONS AND ECONOMIC IMPACT

- Very stable Si-VCO-design techniques pave the way to building low-power low-noise wireless communication transceivers and THz imaging systems.

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Session 24 Overview: GaN Drivers and Converters

Power Management Subcommittee

Session Chair: *Yogesh Ramadass, Texas Instruments, Santa Clara, CA*

Session Co-Chair: *Gerard Villar Pique, NXP Semiconductors, Eindhoven*

Subcommittee Chair: *Axel Thomsen, Cirrus Logic, Austin, TX*

GaN power devices have garnered significant attention for their reduced switching losses leading to small form factor high frequency switching converters. However, issues related to reliable GaN gate drivers, level shifters with high common mode immunity and zero-voltage switching detection remain. This session presents recent advances in gate drivers and ZVS detection schemes for GaN based power converters.

- In Paper 24.1, University of Texas at Dallas describes a 2MHz 150-to-400V isolated phase-shifted full-bridge bus converter using gate-drivers that perform slope-sensing-based ZVS detection. The adaptive dead-time circuitry reduces converter loss by 1.6W and enables 2MHz switching frequency which is 14× better than state of the art for comparable power efficiency.
- In Paper 24.2, Reutlingen University presents a 1.5A GaN gate driver that provides the capability of bipolar/three-level gate drive without the need for any external capacitors. The integrated buffer capacitors enable the gate driver to support 11.6nC gate charge and the ability to drive gate injection GaN transistors.
- In Paper 24.3, University of Texas at Dallas describes a GaN DC-DC converter for automotive application, which employs an isolated gate driver with dead time and duty ratio minimization schemes. The dead-times can be reduced to 0.2ns while supporting a 40V to 3.3V conversion. The on-die ground isolation scheme can handle CMTI rates up to 50V/ns.

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Session 24 Highlights: GaN Drivers and Converters

[24.1] A 2MHz 150-to-400V Input-Isolated DC-DC Bus Converter with Monolithic Slope-Sensing ZVS Detection Achieving 13ns Turn-On Delay and 1.6W Power Saving

Paper Authors: *L. Cong1,2, H. Lee1*

Paper Affiliation: *1University of Texas at Dallas, Richardson, TX 2Texas Instruments, Santa Clara, CA*

Subcommittee Chair: *Y. Ramadass, Texas Instruments, Santa Clara, CA, Power Management*

CONTEXT AND STATE OF THE ART

- Increasing popularity of GaN transistors for high-voltage and high-frequency switching converters with high efficiency.
- Need for robust high-voltage integrated gate drivers that can switch very fast.

TECHNICAL HIGHLIGHTS

- A 2MHz 150-to-400V GaN DC-DC Bus Converter with Adaptive Loss Reduction Control
- In Paper 24.1, University of Texas at Dallas describes a 2MHz 150-to-400V isolated phase-shifted full-bridge bus converter using gate-drivers that perform slope-sensing based ZVS detection. The adaptive dead-time circuitry reduces converter loss by 1.6W and enables 2MHz switching frequency, which is 14× better than state of the art for comparable power efficiency.

APPLICATIONS AND ECONOMIC IMPACT

- Very high-voltage and high frequency switching converters using GaN power transistors.
- Compact power supplies with small form factor.
- Improved power conversion efficiency in automotive, industrial, and offline applications.

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Session 25 Overview: Clock Generation for High-Speed Links

Wireline Subcommittee

Session Chair: *Roberto Nonis, Infineon, Austria*
Session Co-Chair: *Pavan Kumar Hanumolu, University of Illinois, Urbana-Champaign, IL*

Subcommittee Chair: *Frank O'Mahony, Intel, Hillsboro, OR, Wireline Subcommittee*

Clock generation circuits are ubiquitous building blocks in all electronic systems and are the fundamental performance limiters in many of them. This session covers the latest advances in clock generation for high-speed links. The first paper addresses a precision quadrature generator in the latest CMOS process, making use of injection-locking techniques. The second paper presents a technique for generating high-frequency reference clocks by quadrupling the frequency of commonly used, low-cost, crystal oscillators. The third paper demonstrates a fractional PLL that uses reference clock dithering and calibrated dither cancellation in the feedback loop to effectively attenuate fractional spurs. And the final paper describes a digital ring PLL that uses a fast phase correction method and proportional pulse calibration to reduce jitter.

- In paper 25.1 Xilinx presents a combined injection-locked quadrature clock generator and phase interpolator in a 7nm FinFET process. The design achieves a continuous range from 4 to 16GHz with less than 1° quadrature phase error and INL of the phase interpolator <1.5LSB at 16GHz, while dissipating 22.4mW.

- In paper 25.2. University of Illinois presents a crystal oscillator frequency quadrupler in cascade with a 5GHz injection-locked multiplier in 65nm CMOS. The quadrupler and the injection locked multiplier archive $129fs_{rms}$ and $366fs_{rms}$ integrated jitter, respectively, while consuming 1.45mW and 5mW.

- In Paper 25.3, University of Southern California presents a 3-to-5GHz fractional-N digital PLL with a spur reduction technique implemented in 65nm CMOS. The proposed method uses dithering of the reference clock to break the fractional spurs and performs dither cancellation in background. The PLL measures >40dB spur improvement and achieves a worst-case fractional spur of -62.5dBc.

- In Paper 25.4, Ulsan National Institute of Science and Technology (UNIST) presents a fast phase-error correction technique that reduces the impact of oscillator noise on PLL output jitter. Using a TDC with optimally spaced time thresholds, the prototype DPLL achieves $320fs_{rms}$ jitter with an FoM of -242dB.

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Session 25 Highlights: Clock Generation for High-Speed Links

[25.2] A 5GHz 370fs$_{rms}$ 6.5mW Clock Multiplier using a Crystal-Oscillator Frequency Quadrupler in 65nm CMOS

Paper 25.2 Authors: Karim Megawer, Ahmed Elkholy, Mostafa Ahmed, Ahmed Elmallah, Pavan Hanumolu.

Paper 25.2 Affiliation: University of Illinois, Urbana-Champaign, IL

Subcommittee Chair: Frank O'Mahony, Intel, Hillsboro, OR, Wireline Subcommittee

CONTEXT AND STATE OF THE ART

- Low noise clock generation is critical in high-speed serial links. Such clock generators can be implemented using low-noise high-frequency reference clocks, at the expense of the increased cost of the crystal oscillator. This paper provides a means to multiply a crystal oscillator frequency using feedforward techniques, and demonstrates its application in a low-noise injection-locked clock generator.

TECHNICAL HIGHLIGHTS

- **Lowest noise crystal oscillator quadrupler**
  This ring-based clock multiplier uses a crystal oscillator frequency quadrupler and injection locking to achieve low jitter while using a relatively low-frequency reference clock. Fabricated in 65nm CMOS, the prototype clock multiplier achieves 366fs$_{rms}$ jitter at 4.752GHz while operating with a standard 54MHz crystal oscillator, which translates to a multiplication factor of 88. It consumes 6.5mW of power of which 1.5mW is consumed by the crystal oscillator and the quadrupler.

APPLICATIONS AND ECONOMIC IMPACT

- The demonstration of high quality feedforward crystal clock multipliers paves the way to the usage of low-cost crystal oscillators even in high performance applications like multi-GHz high-speed links and RF frequency generation.

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Session 26 Overview: RF Advanced Techniques for Communication and Sensing

RF Subcommittee

Session Chair: *Giuseppe Gramegna, Huawei, Nice, France*
Session Co-Chair: *Hua Wuang, Georgia Institute for Technology, Atlanta, USA*

Subcommittee Chair: *Piet Wambacq, imec, Leuven, Belgium, RF Subcommittee*

The increasing need to improve transmitter efficiency, enhance receiver linearity and robustness, and migrate electronic interfaces closer to the antenna continues to stimulate research in advanced RF techniques. The first paper in this session presents a broadband hybrid-coupler circulator for full-duplex operation. The following two papers demonstrate mm-wave antenna and power amplifier co-integration to increase efficiency and reduce cost. Next, we have three papers that advance power-amplifier architectures for 5G and NB-IoT applications. The three papers towards the end of this session demonstrate techniques for high-linearity receivers. A real-time, near-field THz imager concludes the session.

- In Paper 26.1, Oregon State University presents a balanced hybrid circulator RX that achieves 2.7dB NF, while providing >40dB TX-to-RX baseband isolation across 32MHz BW (56MHz BW for an average of 40dB isolation), and >30dB isolation across 190MHz bandwidth. An on-chip balancing network is not required. The improvement in NF in this work is >2×, and the isolation bandwidth is increased >2.7× compared to state-of-the-art circulator-based RX.

- In Paper 26.2, Georgia Institute of Technology leverages a high-efficiency multi-feed antenna-based active-load-modulation scheme. The paper reports a multiport 65GHz on-chip Doherty radiator in 45nm SOI-CMOS that supports Gb/s modulations and generates 19dBm P_{1dB} with 27.5%/20.1% PAE at 0dB/6dB back-off. The best back-off efficiency enhancement among 60-to-80GHz silicon-based PAs is demonstrated using a new output network.

- In Paper 26.3, the California Institute of Technology demonstrates an integrated PLL with a locking range of 69-to-79GHz that is capable of providing a continuous 35.7dBm EIRP and 24.4dBm of total radiated power with 15.2% DC-to-radiation efficiency. The approach is also scalable and extracts high power levels from low-voltage CMOS transistors by combining power from multiple PAs and lowering the radiator driving impedance.

- In Paper 26.4, Washington State University presents a transformer to correct the AM-PM distortion of a Class-AB PA for 5G applications. The 65nm CMOS PA achieves <0.7 degree AM-PM distortion, 41% PAE, and 15.5dBm P_{out} at 28GHz CW. Tested under a 512/256/64QAM signal with a 20/40/250/340MSym/s data-rate at 28GHz, the PA has a linear PAE at 28GHz of 18.2% for a 64QAM, 340MHz BW signal (P_{avg}=9.8dBm, EVM=-26.4dBc and ACPR=-30dBc).

- In Paper 26.5, Fudan University demonstrates a dual-band high-power digital Doherty PA for cellular NB IoT in 55nm CMOS. The PA reaches 28.9dBm_{peak} P_{out} with 36.8% PAE in the low band and 27dBm_{peak} P_{out} with 25.4% PAE in the high band. For a 12-subcarrier 180kHz NB-IoT signals, P_{out} is 24.4dBm with an average PAE of 29.5% and -21.6dB EVM.

- In Paper 26.6, Georgia Institute of Technology presents a PA that achieves a P_{sat} 1dB bandwidth of 19 to 29.5GHz (43.3%) or S_{21} 3dB BW of 17.7 to 32.3GHz (58.4%) for multiband 5G MIMO. It supports 18Gb/s 64QAM and 8Gb/s 256QAM with >8.7dBm P_{avg}, >16.3% total PAE, and >20% PA PAE under modulation. The design is based on a continuous-mode harmonically tuned linear mm-wave PA that features an ultra-compact on-chip PA output network in only one transformer footprint. The continuous-mode terminations at the fundamental, 2nd, and 3rd harmonics are wideband with no tunable elements or switches.

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- In Paper 26.7, the KU Leuven demonstrates an E-Band direct-conversion subharmonic receiver (SHRX) that achieves 8.3dB noise figure, 12.5GHz RF bandwidth, and -25dBm ICP_{1dB}, while consuming <100mW. The receiver leverages on-chip coupled RTWOs to generate 8 differential phases at $f_{LO}=f_{RF}/4$. It is implemented in a 28nm bulk CMOS technology without an ultra-thick top metal.

- In Paper 26.8, University of California, Berkeley, presents an E-Band mixer-first RX with S_{11}<-10dB, 8-to-12.7dB NF, 19.5-to-25.3dB gain, and -16.8dBm maximum ICP_{1dB} across 70-to-100GHz. The high-input-impedance passive mixer is matched at the RF input using a frequency-translational feedback and a broadband matching network. Power consumption is 12mW.

- In Paper 26.9, the University of Southern California describes a 13th-order CMOS reconfigurable RF bandpass filter that is tunable from 0.8 to 1.1GHz. The IIP3-OOB is +24dBm at a 40MHz offset. The filter has adjustable close-by transmission zeros. The 3dB BW is 30 to 50MHz, tunable, and has a -100dB/100MHz transition-band roll-off that enables close-by blocker rejection.

- In Paper 26.10, University of Wuppertal presents a silicon-based super-resolved real-time terahertz sensing system that includes THz illumination, detection, evanescent field sensing, and readout on a single chip. It comprises of 128 split-ring-resonator-based 0.56THz near-field sensors. Chopping techniques and an integrated lock-in amplifier are employed to achieve 93dB dynamic range (1Hz BW) in an analog readout mode, and 37dB at 28fps in a digital readout mode.

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Session 26 Highlights: RF Techniques for Communication and Sensing

[26.2] A 62-to-68GHz Linear 6Gb/s 64QAM CMOS Doherty Radiator with 27.5%/20.1% PAE at Peak/6dB-Back-off Output Power Leveraging High-Efficiency Multi-Feed Antenna-Based Active Load Modulation

Paper 26.2 Authors: *H. Nguyen, T. Chi, S. Li, H. Wang*

Paper 26.2 Affiliation: *Georgia Institute of Technology, Atlanta, USA*

[26.6] A Continuous-Mode Harmonically Tuned 19-to-29.5GHz Ultra-Linear PA Supporting 18Gb/s at 18.4% Modulation PAE and 43.5% Peak PAE

Paper 26.6 Authors: *T. Li, M. Huang, H. Wang*

Paper 26.6 Affiliation: *Georgia Institute of Technology, Atlanta, USA*

[26.10] A 128-Pixel 0.56THz Sensing Array for Real-Time Near-Field Imaging in 0.13µm SiGe BiCMOS

Paper 26.10 Authors: *P. Hillger[1], R. Jain[1], J. Crzyb[1], L. Mavarani[1], B. Heinemann[2], G. M. Grogan[3], P. Mounaix[4], T. Zimmer[5], U. Pfeiffer[1]*

Paper 26.10 Affiliation: *[1]University of Wuppertal, Wuppertal, Germany*

[2]IHP, Frankfurt (Oder), Germany

[3]Institut Bergonie, Bordeaux, France

[4]CNRS, Talence, France

[5]University of Bordeaux, Talence, France

Subcommittee Chair: ***Piet Wambacq, imec, Leuven, Belgium***, *RF Subcommittee*

CONTEXT AND STATE OF THE ART

- Future mm-wave massive-MIMO systems will extensively employ spectrally efficient modulation schemes with high peak-to-average power levels. This necessitates power-amplifier (PA) architectures that simultaneously support high energy efficiency, high linearity, and Gbit/s modulation speeds. The Doherty power amplifier is a popular choice for mm-wave applications due to its efficiency enhancement in power back-off and high modulation bandwidths. Furthermore, broadband linear PAs with harmonic tuning can achieve superior peak efficiency and linearity.
- Real-time THz sensing arrays with high spatial resolution, low cost, and rapid scanning time are an enabling technology for various applications.

TECHNICAL HIGHLIGHTS

A mm-wave linear radiator with on-antenna Doherty efficiency enhancement at power back off

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- A high-efficiency, multiport antenna-based active-load-modulation scheme is proposed to enhance the peak and back-off efficiency of a mm-wave radiator. A proof-of-concept implementation in 45nm SOI-CMOS at 65GHz supports Gb/s modulations and generates 19dBm P1dB with 27.5%/20.1% PAE at 0dB/6dB back-off. The best back-off efficiency enhancement among 60-to-80GHz silicon-based PAs is demonstrated using an on-antenna Doherty load modulation network.

A wideband harmonically-tuned linear mm-wave PA in CMOS with world-record efficiency

- A continuous-mode harmonically-tuned linear mm-wave PA utilizes an on-chip, compact, one-transformer PA output network to implement continuous-mode wideband terminations at the fundamental, 2nd, and 3rd harmonics with no tunable elements or switches. The PA achieves a P_{sat} 1dB bandwidth of 19 to 29.5GHz (43.3%) or S_{21} 3dB bandwidth of 17.7 to 32.3GHz (58.4%) for multiband 5G MIMO. It supports 18Gb/s 64QAM and 8Gb/s 256QAM with >8.7dBm P_{avg}, >16.3% total PAE, and >20% PA PAE under modulation.

A THz sensing array system-on-a-chip for real-time super-solution near-field imaging

- A silicon-based super-resolved real-time terahertz sensing system includes functions such as THz illumination, detection, evanescent field sensing, and readout on a single chip. It comprises 128 split-ring-resonator-based 0.56THz near-field sensors. Chopping techniques and an integrated lock-in amplifier are employed to achieve 93dB dynamic range (1Hz BW) in an analog readout mode, and 37dB at 28fps in a digital readout mode.

APPLICATIONS AND ECONOMIC IMPACT

- Improving transmitter efficiency while maintaining high linearity and wide modulation bandwidth supports emerging 5G systems, mm-wave communication, and sensing applications. This session presents multiple power amplifier architectures and showcases improving transmitter efficiencies.
- With their non-ionizing nature, real-time THz imaging is a unique technology for sensing applications, such as security screening, non-destructive evaluation, and material characterization.

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Session 27 Overview: Power Converter Techniques

Power Management Subcommittee

Session Chair: Makoto Takamiya, *The University of Tokyo, Japan*

Session Co-Chair: Yen-Hsun Hsu, *Mediatek, Hsin-Chu, Taiwan*

Subcommittee Chair: Axel Thomsen, *Cirrus Logic, Austin, TX*

The session on Power Converter Techniques presents improvements of power density, power efficiency and power dissipation in switched-capacitor, hybrid, linear and inductor-based DC-DC converters and power modulators. The first paper addresses the fully integrated fine-grained rational buck-boost converter with switched capacitor. The next four papers present innovative ideas in inductor-based DC-DC converters including capacitor-assisted hybrid DC-DC converters. This is followed by two high-frequency HPUE-capable envelope-tracking power modulators. An LDO is also presented that achieves good transient response under Hi-Lo-Hi transient stimulus. Finally, the last paper introduces the on-chip resonant-gate-drive SC converter for near-threshold computing.

- In Paper 27.1, Macau University describes an Algorithmic Voltage-Feed-In (AVFI) Topology for systematic rational VCR generation. The converter achieves 84.1% peak efficiency at 13.2mW/mm^2 with 0.22-to-2.4V input, demonstrating a >13× power density improvement.
- In Paper 27.2, Hanyang University presents a current-mode time-domain-controlled buck converter, which eliminates the need for current sensor and prevents sub-harmonic oscillation without slope compensation. This 10MHz current-mode buck converter can provide wide range of output from 0.15V to 1.69V with 1.8V input with peak efficiency of 94.9%.
- In Paper 27.3, the University of Pavia demonstrates a SIMO DC-DC converter generating three supply voltages suitable for a class-D audio amplifier of a car-radio. The circuit withstands the 4-to-40V range of car battery variations and regulates in the range of 4.5 to 27V. Designed using a 0.11µm BCD process, switched at 2.4MHz, the SIMO offers a peak efficiency of 86% at 2.7W of output power with active area of 2.5mm^2.
- In Paper 27.4, KAIST presents a step-up/down converter IC for Li-ion battery management, which embeds 1/2 and 3/2 charge-pumps in buck topology. It is fabricated with a 0.18µm BCD process, achieves 97% maximum efficiency with wide load current range of 0.03 to 1A, and 6µs fast recovery time with hysteretic control.
- In Paper 27.5, KAIST describes a dual-path step-up DC-DC converter with two current paths in an inductor and a flying capacitor in different time-slot. The output ripple voltage is reduced to less than 15mV owing to the continuous output delivery current and furthermore, its right-half-plane zero is alleviated. This converter has peak efficiency of 95.2% even with a DCR up to 200mΩ.
- In Paper 27.6, Mediatek demonstrates an envelope-tracking modulator (ETM) in 0.153µm CMOS for an 80MHz LTE-A transmitter with a dual-mode AC feed-forward Class-AB linear amplifier. This 80MHz ETM achieves -38.1dBc ACLR at 26dBm PA output power and its peak efficiency is 87.1% and 81.2% for 20MHz and 80MHz, respectively.
- In Paper 27.7, Samsung demonstrates a single 2TX SM-IC supporting two independent TXs with Power Class 2. Only one buck-boost is used and shared for both TXs by swapping capacitors, and buck converters are equipped with return-to-battery switching for efficiency and noise. The SM achieves max 84.6% efficiency and -133dBm/Hz noise. The ET-PA of LTE Band 41 reaches 42.7% PAE while delivering 29.4dBm power with -38.2dBc ACLR.
- In Paper 27.8, Mediatek presents an LDO that features a virtual-ground-based dynamic-power-recycling buffer and anti-ringing feed-forward compensation. It achieves 20mV undershoot with the unique short-period H-L-H load transient of flash memory. The near-zero driving dead-zone of the buffer improves transient response while maintaining high current efficiency with 94% power recycling.
- In Paper 27.9, Ohio State University demonstrates a fully-integrated switched-C converter for near-threshold in 45nm SOI. A single 100pH on-chip inductor is used to reduce the switching losses of multiple power FETs, thus maximizing efficiency without sacrificing current density. The converter achieves 70.2% efficiency at 0.92 A/mm^2 and 0.4V output using an area-efficient resonant-gate-drive scheme. It operates from 1V input and occupies 0.3 mm^2, only 5% of which is for the inductor.

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Session 27 Highlights: Power Converter Techniques

[27.4] 97% High-Efficiency 6μs Fast-Recovery-Time Buck-Based Step-Up/Down Converter with Embedded 1/2 and 3/2 Charge-Pumps for Li-Ion Battery Management

Paper 27.4 Authors: *Min-Woo Ko[1], Ki-Duk Kim[1], Young-Jin Woo[2], Se-Un Shin[1], Hyun-Ki Han[1], Yeunhee Huh[1], Gyeong-Gu Kang[1], Jeong-Hyun Cho[1], Sang-Jin Kim[1], Hyung-Min Lee[3], Gyu-Hyeong Cho[1]*

Paper 27.4 Affiliation: *[1]KAIST, Daejeon, Korea, [2]Siliconworks, Daejeon, Korea, [3]Korea University, Seoul, Korea*

[27.5] A 95.2% Efficiency Dual-Path DC-DC Step-Up Converter with Continuous Output Current Delivery and Low Voltage Ripple

Paper 27.5 Authors: *Se-Un Shin[1], Yeunhee Huh[1], Yougmin Ju[1], Sungwon Choi[1], Changsik Shin[1], Young-Jin Woo[1], Mingeong Choi[1], Se-hong Park[1], Young-hoon Sohn[1], Min-woo Ko[1], Young Jo[1], Hyunki Han[1], Hyung-Min Lee[2], Sung-Wan Hong[3], Gyu-Hyeong Cho[1]*

Paper 27.5 Affiliation: *[1]KAIST, Daejeon, Korea, [2]Korea University, Seoul, Korea, [3]Sookmyung Womens' University, Seoul, Korea*

Subcommittee Chair: *Axel Thomsen, Cirrus Logic, Austin, TX, Power Management*

CONTEXT AND STATE OF THE ART

- In mobile devices (e.g. smartphones), DC-DC converters are crucial to bridge the voltage gap between the battery voltage and various ICs. In DC-DC converters, however, the trade-off between the power conversion efficiency and the size exists.
- To solve the trade-off, hybrid converters, where one or two capacitors are added to conventional inductive DC-DC converters, are presented.

TECHNICAL HIGHLIGHTS

- **Adding two capacitors achieves a step-up/down DC-DC converter with high power-conversion efficiency and fast transient.**
- In Paper 27.4, KAIST presents a step-up/down converter IC for Li-ion battery management, which embeds 1/2 and 3/2 charge-pumps in buck topology. Fabricated in a 0.18um BCD process, it achieves 97% maximum efficiency with wide load current range of 0.03 to 1A, and 6μs fast recovery time with hysteretic control.

- **Adding a capacitor achieves a step-up DC-DC converter with high power-conversion efficiency and small-size inductor.**
- In Paper 27.5, KAIST describes a dual-path step-up DC-DC converter with two current paths in an inductor and a flying capacitor in different time-slot. The output ripple voltage is reduced to less than 15mV owing to the continuous output delivery current and furthermore, its right-half-plane zero is alleviated. This converter has a peak efficiency of 95.2% even with a DCR up to 200mΩ.

APPLICATIONS AND ECONOMIC IMPACT

- Mobile devices (e.g. smartphones) with smaller form factor and longer battery life will be achieved thanks to the high efficiency of the DC-DC converters using small-size passive components (e.g. inductors).

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Session 28 Overview: Wireless Connectivity

Wireless Subcommittee

Session Chair: *Howard Luong, Hong Kong University of Science and Technology, Hong Kong, China*

Session Co-Chair: *Kyoohyun Lim, Future Communication IC (FCI), Republic of Korea*

Subcommittee Chair: *Stefano Pellerano, Intel, Hillsboro, OR, Wireless*

Connecting things wirelessly requires optimization from multidisciplinary areas. This session will introduce state-of-the-art wireless transceivers supporting ultra-lower-power IoT and connectivity solutions. In this session, a high-performance WLAN SoC supporting up to 802.11ax 1024QAM will be presented. Then, two-blockers-tolerant high-sensitivity Bluetooth Low-Energy (BLE) transceivers in 65nm and 40nm CMOS will be presented followed by a best-in-class performance all-digital PLL for BLE in 16nm FinFET technology, and an energy-harvesting BLE transmitter in 28nm CMOS. An ultra-low-power wakeup receiver enabling event-driven sensor nodes and an ultrasonic wake-up receiver using a precharged capacitive micro-machined ultrasound transducer will be shown. Finally, a 5.8GHz near-field radio achieving the smallest die size of 116μm×116μm will be presented in this session.

- In Paper 28.1, Toshiba presents a fully integrated 4×4 AP WLAN SoC in 28nm CMOS supporting up to 802.11ax and equipped with frequency-dependent IQ calibration for 1024QAM and an interference analyzer for reliable connection.
- In Paper 28.2, the Tokyo Institute of Technology reports a Bluetooth Low-Energy (BLE) transceiver in 65nm CMOS. The RX consumes 2.3mW with a sensitivity of -94dBm and high blocker tolerance owing to the proposed single-channel demodulation and dynamic range enhancement technique. The single-point polar TX consumes 2.9mW with a 1.89% FSK error.
- In Paper 28.3, imec-Holst center and Renesas Electronics describe a 0.8V 0.8mm^2 Bluetooth 5/BLE digital-intensive transceiver in 40nm CMOS with a 2.3mW phase-tracking RX utilizing a hybrid loop filter for interference resilience. With an ADPLL-based digital FM interface for precise deviation frequency control, the TX delivers 1.8dBm maximum output power, whereas the RX achieves a -92/-95dBm sensitivity at 2Mb/s and 1Mb/s respectively.
- In Paper 28.4, TSMC, Delft University of Technology, and University College Dublin present a 0.45V sub-mW all-digital PLL for BLE modulation and <100ns instantaneous channel hopping using a 32.768kHz reference in 16nm FinFET technology. It performs channel hopping and GFSK modulation in a 2-point manner with extensive DCO calibrations after locking to the center band upon system power-up.
- In Paper 28.5, the University of Macau and Instituto Superior Technico/University of Lisboa describe the implementation of a 0.2V energy-harvesting BLE transmitter in 28nm CMOS with a micropower manager exhibiting 25% system efficiency at 0dBm output. An ultra-low-voltage VCO with a 5.6:1 transformer and Class-E/F2 PA with an HD-3-notching transformer is presented with a passive-intensive type-I PLL with a 5% duty cycle to improve the reference spurs to -47dBc.
- In Paper 28.6, the University of Virginia reports an ultra-low-power wakeup receiver in 0.13μm CMOS, enabling event-driven sensor nodes with automatic offset compensation spending the majority of their time in an “asleep-yet-alert” state. The receiver consumes 7.4nW with a measured sensitivity of -76dBm and -71dBm at the 151.8MHz MURS and 433MHz ISM bands respectively.
- In Paper 28.7, Stanford University implements an ultrasonic wake-up receiver in 65nm CMOS using a precharged capacitive micro-machined ultrasonic transducer. Realized in an area of 14.5mm^2, it achieves -59.7dBm sensitivity with 8nW power consumption.
- In Paper 28.8, the University of California at Berkeley presents a 5.8GHz power-harvesting 116μm×116μm “Dielet” near-field radio in 65nm CMOS with on-chip coil antenna. A hybrid two-tone IM2-IM3 technique is proposed to lock the on-chip oscillator, simultaneously improving the uplink SNR to 42dB and uplink signal-to-transmitter ratio to -28.9dBc at 20MHz.

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Session 28 Highlights: Wireless Connectivity

[28.1] An 802.11ax 4x4 Spectrum-Efficient WLAN AP Transceiver SoC Supporting 1024QAM with Frequency-Dependent IQ Calibration and Integrated Interference Analyzer

Paper 28.1 Authors: *Shusuke Kawai[1], Hiromitsu Aoyama[2], Rui Ito[3], Yutaka Shimizu[3], Mitsuyuki Ashida[3], Asuka Maki[3], Tomohiko Takeuchi[3], Hiroyuki Kobayashi[3], Go Urakawa[3], Hiroaki Hoshino[3], Shigehito Saigusa[3], Kazushi Koyama[4], Makoto Morita[2], Ryuichi Nihei[2], Daisuke Goto[2], Motoki Nagata[3], Katsuyuki Ikeuchi[1], Kentaro Yoshioka[1], Ryoichi Tachibana[3], Makoto Arai[2], Chen-Kong Teh[2], Atsushi Suzuki[2], Hiroshi Yoshida[2], Yosuke Hagiwara[3], Takayuki Kato[2], Ichiro Seto[1], Tomoya Horiguchi[3], Koichiro Ban[1], Kyosuke Takahashi[3], Hirotsugu Kajihara[3], Toshiyuki Yamagishi[3], Yuki Fujimura[3], Kazuhisa Horiuchi[3], Katsuya Nonin[1], Kengo Kurose[3], Hideki Yamada[3], Kentaro Taniguchi[1], Masahiro Sekiya[1], Takeshi Tomizawa[3], Daisuke Taki[3], Masaaki Ikuta[3], Tomoya Suzuki[3], Yuki Ando[3], Daisuke Yashima[1], Takahisa Kaihotsu[1], Hiroki Mori[1], Kensuke Nakanishi[1], Takeshi Kumagaya[1], Yasuo Unekawa[2], Tsuguhide Aoki[1], Kohei Onizuka[1], Toshiya Mitomo[1]*

Paper 28.1 Affiliation: *[1]Toshiba, [2]Toshiba Electronic Devices and Storage, [3]Toshiba Memory, [4]Toshiba Microelectronics, Kawasaki, Japan*

[28.2] An ADPLL-Centric Bluetooth Low-Energy Transceiver with 2.3mW Interference-Tolerant Hybrid-Loop Receiver and 2.9mW Single-Point Polar Transmitter in 65nm CMOS

Paper 28.2 Authors: *Hanli Liu, Zheng Sun, Dexian Tang, Hongye Huang, Tohru Kaneko, Wei Deng, Rui Wu, Kenichi Okada, Akira Matsuzawa*

Paper 28.2 Affiliation: *Tokyo Institute of Technology, Tokyo, Japan*

Subcommittee Chair: *Stefano Pellerano, Intel, Hillsboro, OR, Wireless*

CONTEXT AND STATE OF THE ART

- Gigabit-per-second wireless data-rates and improved network capacity are facilitated with the first fully integrated 802.11ax transceiver SoC.
- IoT applications have pushed for increasing demand of designs of ultra-low-power and wake-up transceivers with lower and lower power consumption.

TECHNICAL HIGHLIGHTS

4×4 1024-QAM WLAN Access-Point Transceiver SOC with integrated interference analyzer

- In Paper 28.1, Toshiba presents a fully integrated 4×4 AP WLAN transceiver SoC in 28nm CMOS for 802.11abgn/ac and ax standards with a novel frequency-dependent (FD) IQ calibration to support 1024-QAM operation with -38.1dB TX EVM and -57.7dBm RX sensitivity @ 5GHz. An integrated interference analyzer ensures a reliable connection in a dense operating environment.

Bluetooth Low-Energy (BLE) Transceiver with 2.3mW Interference-Tolerant Hybrid-Loop Receiver and 2.9mW Single-Point Polar Transmitter

- In Paper 28.2, the Tokyo Institute of Technology describes a Bluetooth Low-Energy (BLE) transceiver in 65nm CMOS. The RX consumes 2.3mW with a high sensitivity of -94dBm and high blocker tolerance owing to the proposed single-channel demodulation and dynamic-range enhancement technique. The TX consumes 2.9mW with a 1.89% modulation error utilizing a single-point polar TX through a wide loop-bandwidth ADPLL.

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APPLICATIONS AND ECONOMIC IMPACT

- The target is wireless applications with data-rates of Gigabits per second with improved network capacity and reliable operation in harsh environments.
- Ultra-low-power and wake-up radios would enable emerging wireless applications, including IoT, biomedical and implantable devices, with extended battery life or even with energy-harvesting technologies.

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Session 29 Overview: Advanced Biomedical Systems

IMMD Subcommittee

Session Chair: *Pedram Mohseni, Case Western Reserve University, Cleveland, OH, USA*

Session Co-Chair: *Nick Van Helleputte, imec, Heverlee, Belgium*

Subcommittee Chair: *Makoto Ikeda, University of Tokyo, Tokyo, Japan, IMMD Subcommittee*

Advances in biomedical circuits and systems are essential technology drivers in addressing critical societal needs to increase the effectiveness and lower the cost of healthcare. This session highlights the latest advances in implantable, high-density, and wearable systems for neural recording, optogenetics, multimodal cell interfacing, and heart-rate monitoring.

- In Paper 29.1, Medtronic introduces the system architecture for a brain coprocessor exploring novel methods for treating neurological disorders.
- In Paper 29.2, the University of Freiburg – IMTEK present a reconfigurable fully immersible deep-brain neural probe with a modular architecture for parallel readout of 144 recording sites in a 11.5mm needle fabricated in 0.18µm CMOS. Each electrode is equipped with 11b ΔΣ-ADC in an area of 70×70µm^2 and features low noise of 8.1µV$_{rms}$ and 13.4µV$_{rms}$ in the frequency bands of the two types of neural signals, local field potentials (1 to 300Hz) and action potentials (0.3 to 10kHz), respectively, and crosstalk of -74.4dB at 1kHz with 39.14µW per recording site.
- In Paper 29.3, imec presents an active microelectrode array (MEA) with 16,384 electrodes and 1,024 channels for multimodal cell monitoring in 0.13µm CMOS. This MEA integrates 6 cell-interfacing modalities, including intracellular recording and fast impedance monitoring in all of the channels, with a total input-referred noise of 7.5µV$_{rms}$ and a total power consumption of 95mW.
- In Paper 29.4, Laval University presents a 0.13µm CMOS IC for simultaneous multichannel optogenetics and electrophysiological brain recording with 10 multimodal recording channels (NEF of 2.30) with ADC, and a 4-channel LED driver circuit. Digitization is done using an in-channel 8.68b ENOB ΔΣ MASH 1-1-1 ADC with on-chip decimation including AFE, with power consumption of 11.2µW per channel.
- In Paper 29.5, Georgia Institute of Technology and Michigan State University present a mm-sized, free-floating, wirelessly powered, implantable, optical stimulating system-on-a-chip (SoC) in 0.35µm CMOS. A 4×4 µLED array is selectively driven with up to 10mA current, and an optimized 3-coil inductive link delivers more than 2mW at 60MHz along with ASK data at 50kb/s to the SoC.
- In Paper 29.6, the University of California San Diego presents a 16-channel 92dB dynamic range, low-noise, low-power neural-recording acquisition system employing predictive digital auto-ranging (PDA) in 0.8V 65nm CMOS. Per-channel ADC with PDA offers a 22dB increase in SNDR and 30× improvement in bandwidth and faster than 1ms recovery to 100mV input differential transient artifacts, with noise below 1µV$_{rms}$ over DC-to-500Hz bandwidth at 32kHz chopping and 1µA supply current.
- In Paper 29.7, DGIST presents a multichannel neural recording amplifier system with 110dB common-mode and 100dB power supply rejection in 0.18µm CMOS. The neural amplifier system achieves a worst-case total CMRR of 80dB at 1kHz and an electrode impedance of 100kΩ.
- In Paper 29.8, KAIST presents a low-power, photoplethysmography (PPG)-based, heart-rate monitoring sensor based on a heart beat locked loop (HBLL) architecture in 0.18µm CMOS. The sensor realizes an effective duty cycle of 0.0175% with heart rate error of less than 2.1bpm, while consuming 43.4µW.

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Session 29 Highlights: Advanced Biomedical Systems

[29.2] A Fully Immersible Deep-Brain Neural Probe with Modular Architecture and a Delta-Sigma ADC Integrated Under each Electrode for Parallel Readout of 144 Recording Sites

Paper Authors: Daniel De Dorigo[1], Christian Moranz[1], Hagen Graf[1], Maximilian Marx[1], Boyu Shui[1], Matthias Kuhl[1], Yiannos Manoli [1,2]

Paper Affiliation: [1]University of Freiburg - IMTEK, Freiburg, Germany, [2]Hahn-Schickard, Villingen-Schwenningen, Germany

Subcommittee Chair: *Makoto Ikeda, University of Tokyo, Tokyo, Japan, IMMD subcommittee*

CONTEXT AND STATE OF THE ART

- Tissue-penetrating probes for high-density deep-brain recording of *in vivo* neural activity provide important tools for neuroscience exploration and disease management.
- Conventional devices need either a large number of interconnects at the base of the probe or allow only a reduced number of electrodes to be read out simultaneously.

TECHNICAL HIGHLIGHTS

- First reported reconfigurable miniaturized probe, with a single 11.5mm-long 70µm-wide needle shank without base.
- Parallel readout of all 144 integrated recording sites.
- Incremental delta-sigma analog-to-digital converters (ΔΣ-ADC) integrated within $70{\times}70\mu m^2$ area under each electrode avoid global routing of noise-sensitive neural signals.
- Smallest external 8-wire interface, including supplies, biases, and digital.

APPLICATIONS AND ECONOMIC IMPACT

- Slim shaft of 70µm from top to bottom can potentially improve neural recording quality and longevity for chronic brain monitoring.
- Chronic recording of neural signals from the brain accelerates understanding of neurological diseases and improves health outcomes.

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Session 30 Overview: Emerging Memories

Memory & TD Subcommittees

Session Chair: *Shinichiro Shiratake, Toshiba Memory, Yokohama, Japan*

Session Co-Chair: *Edoardo Charbon, EPFL, Lausanne, Switzerland*

Subcommittee Chair: *Leland Chang, IBM, Yorktown Heights, NY*

Subcommittee Chair: *Makoto Nagata, Kobe University, Kobe, Japan*

Speed and power are major concerns in today's memory designs, and they are becoming particularly important with the emergence of high-performance computing and deep learning applications.

In this session, multiple new developments in emerging memories will be presented. An 11Mb 40nm CMOS embedded RRAM macro with fast access and improved reliability by means of circuit techniques is proposed. A 28nm CMOS 1Mb MRAM with 2.8ns access time is presented, where circuit techniques are used to save write energy. An embedded 28nm CMOS 32kb 2T2MTJ MRAM is demonstrated achieving a 1.3ns access time through a novel sensing scheme with a sophisticated offset canceling technique. Finally, a novel memory based on crystalline oxide semiconductor FETs, optimized for an embedded deep-learning engine, achieves sub-50ns read/write capability.

- In paper 30.1, TSMC presents an 11Mb embedded RRAM macro fabricated in a 40nm CMOS process. It proposes a new sense amplifier with a 58% faster access speed, and a new write scheme to improve both endurance and retention performance.

- In paper 30.2, the University of Michigan presents a 1Mb STT-MRAM with a 2.8ns read-access time, offering an offset-canceling sense amplifier for fast access and a self-write-termination scheme to save write energy.

- In paper 30.3, National Tsing Hua University presents a 32kb embedded 2T2MTJ MRAM macro with a 1.3ns read-access time. It adopts a continuous-recording-and-enhancement voltage sense amplifier to realize the world's fastest read operation.

- In paper 30.4 the Semiconductor Energy Laboratory proposes a memory comprising of crystalline oxide semiconductor FETs (OSFETs) compatible with CMOS processes. The memory, embedded in a deep learning engine, has a 1kb density enabled by a 60nm OSFET process, which can be read in 45ns and written in 20ns using 97.9pJ and 123pJ.

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Session 30 Highlights: Emerging Memories

[30.1] A N40 256K×44 Embedded RRAM Macro with SL-Precharge SA and Low-Voltage Current Limiter to Improve Read and Write Performance

Paper 30.1 Authors: *Chung-Cheng Chou, Chung-Cheng Chou, Zheng-Jun Lin, Pei-Ling Tseng, Chih-Feng Li, Chih-Yang Chang, Wei-Chi Chen, Y.D. Chih, Tsung-Yung, Jonathan Chang*

Paper 30.1 Affiliation: *TSMC, Hsinchu, Taiwan*

Subcommittee Chair: *Leland Chang, IBM, NY*

Subcommittee Chair: *Makoto Nagata, Kobe University, Kobe, Japan*

CONTEXT AND STATE OF THE ART

- Emerging memory is one of the critical components of today's high-performance computing and edge devices.
- Embedded RRAM is one of the promising candidates due to its compatibility with CMOS processes.

TECHNICAL HIGHLIGHTS

- **TSMC introduces a high-density 11Mb embedded RRAM macro in their 40nm process.**
  Paper 30.1 introduces a 256Kx44 embedded RRAM macro in the TSMC 40nm process. The macro adopts a sense amplifier with a 58% faster access speed and a new write scheme to improve both endurance and retention performance.

APPLICATIONS AND ECONOMIC IMPACT

- Embedded nonvolatile memories in advanced technology nodes can provide critical functionality across a wide range of solid-state circuit applications – from edge devices to cloud servers

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[30.4] A 20ns-Write, 45ns-Read and 1014-Cycle Endurance Memory Module Composed Only of 60nm Crystalline Oxide Semiconductor Transistors

Paper 30.4 Authors: *Shuhei Maeda[1], Satoru Ohshita[1], Kazuma Furutani[1], Takahiko Ishizu[1], Tomoaki Atsumi[1], Yoshinori Ando[1], Daisuke Matsubayashi[1], Kiyoshi Kato[1], Takashi Okuda[1], Masahiro Fujia[2], Shunpei Yamazaki[2]*

Paper 30.4 Affiliation: *[1]Semiconductor Energy Laboratory, Atsugi, Japan, [2]University of Tokyo, Tokyo, Japan*

Subcommittee Chair: *Leland Chang, IBM, NY, USA*

Subcommittee Chair: *Makoto Nagata, Kobe University, Kobe, Japan*

CONTEXT AND STATE OF THE ART

- Accessing memory units quickly using low power is critical for emerging deep learning engines.
- The OSFET technology offers fast and low-energy access of memories, while ensuring full CMOS compatibility.

TECHNICAL HIGHLIGHTS

- **The Semiconductor Energy Laboratory introduces a fast, low power, CMOS compatible OSFET memory.**
  Paper 30.4 presents a 60nm crystalline oxide semiconductor FET (OSFET) technology for fast and low-power storage. The memory, embedded in a deep learning engine, has a 1kb density and can be read in 45ns and written in 20ns, requiring 97.9pJ and 123pJ of energy.

APPLICATIONS AND ECONOMIC IMPACT

- Integrated deep learning has a major impact in everyday life. However, in order to maximize efficiency, deep-learning engines must work in close proximity with memory. The OSFET technology offers a high-speed, low-power solution to implement such functionality.

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Session 31 Overview: Computation in Memory for Machine Learning

Technology Directions and Memory Subcommittees

Session Chair: *Naveen Verma, Princeton University, Princeton, NJ*

Session Co-Chair: *Fatih Hamzaoglu, Intel, Hillsboro, OR*

Subcommittee Chair: *Makoto Nagata, Kobe University, Kobe, Japan, Technology Directions*

Subcommittee Chair: *Leland Chang, IBM, Yorktown Heights, NY, Memory*

Many state-of-the-art systems for machine learning are limited by the memory in terms of the energy they require and the performance they can achieve. This session explores how the bottleneck can be overcome by emerging architectures that perform computation inside the memory array. This necessitates unconventional, typically mixed-signal, circuits for computation, which exploit the statistical nature of machine-learning applications to achieve high algorithmic performance with substantial energy and throughput gains. Further, the architectures serve as a driver for emerging memory technologies, exploiting the high-density and nonvolatility these offer towards increased scale and efficiency of computation. The innovative papers in this session provide concrete demonstrations of this promise, extending well beyond conventional architectures.

- In Paper 31.1, MIT describes a compute-in-memory structure by performing multiplication between an activation and 1-b weight on a bit line, and accumulation through analog-to-digital conversion of charge across bit lines. Mapping two convolutional layers to the accelerator, an accuracy of 99% is achieved on a subset of the MNIST dataset, at an energy efficiency of 28.1TOPS/W.
- In Paper 31.2, UIUC describes a compute-in-memory structure that simultaneously accesses multiple weights in memory to perform 8b multiplication on the bit lines, and introduces on-chip training, via stochastic gradient decent, to mitigate non-idealities in mixed-signal compute. An accuracy of 96% is achieved on the MIT-CBCL dataset, at an energy efficiency of 3.125TOPS/W
- In Paper 31.3, Stanford/UCB/MIT demonstrate a brain-inspired hyperdimensional (HD) computing nanosystem to recognize languages and sentences from minimal training data. The paper uses 3D integration of CNTFETs and RRAM cells, and measurements show that 21 European languages can be classified with 98% accuracy from >20,000 sentences.
- In Paper 31.4, National Tsing-Hua U. implements multiply-and-accumulate operations using a 1Mb RRAM array for a Binary DNN in edge processors. The paper proposes an offset-current-suppressing sense amp and input-aware dynamic-reference current generation to overcome sense-margin challenges. Silicon measurements show successful operation with sub-15ns access time.
- In Paper 31.5, National Tsing-Hua U. demonstrates multiply-and-accumulate operations using a 4kb SRAM for fully-connected neural networks in edge processors. The paper overcomes the challenges of excessive current, sense-amplifier offset, and sensing V_{ref} optimization, arising due to simultaneous activation of multiple word lines. Sub-3ns access speed is achieved with simulated 97.5% MNIST accuracy.

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Session 31 Highlights: Computation in Memory for Machine Learning

[31.3] Brain-Inspired Computing Exploiting Carbon Nanotube FETs and Resistive RAM: Hyperdimensional Computing Case Study

Paper Authors: *T. Wu, H. Li, P.-C. Huang, A. Rahimi, J. M. Rabaey, P. Wong. M. M. Shulaker, S. Mitra*

Paper Affiliation: *Stanford Univ., CA, UCB, CA, MIT, MA*

Subcommittee Chair: *Makoto Nagata, Kobe University, Kobe, Japan, Technology Directions*

Subcommittee Chair: *Leland Chang, IBM, Yorktown Heights, NY, Memory*

CONTEXT AND STATE OF THE ART

- Demonstration of microsystem for compute in memory, based on monolithic integration of CNTFETs and RRAM
- Realization of hyperdimensional computing, a framework looking beyond DNNs, for language classification

TECHNICAL HIGHLIGHTS

Brain-Inspired Computing Exploiting Carbon Nanotube FETs and Resistive RAM:

- For the first time, an end-to-end brain-inspired system is demonstrated in emerging technologies, CNTFETs and RRAMs, monolithically integrated.
- Stanford/UCB/MIT demonstrate a brain-inspired hyperdimensional (HD) computing nanosystem to recognize languages and sentences from minimal training data. The paper uses 3D integration of CNTFETs and RRAM cells, and measurements show that 21 European languages can be classified with 98% accuracy from >20,000 sentences.

APPLICATIONS AND ECONOMIC IMPACT

- Cognitive computing, computer vision, natural-language processing
- Nanotechnology scaling beyond the silicon-CMOS/Moore's-Law roadmap

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ISSCC 2018
TRENDS

Conditions of Publication

PREAMBLE

The Trends to follow serve to capture the context, highlights, and potential impact, of the papers to be presented in each Session at ISSCC 2018 in February in San Francisco

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- From ISSCC's point of view, the phraseology included in the box below captures what we at ISSCC would like your readership to know about this, the 65th appearance of ISSCC, on February 11th to February the 15th, 2018, in San Francisco.

This and other related topics will be discussed at length at ISSCC 2018, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 11 - February 15, 2018,

at the San Francisco Marriott Marquis Hotel.

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HISTORICAL TRENDS IN TECHNICAL THEMES

ANALOG SYSTEMS

ANALOG SUBCOMMITTEE

POWER MANAGEMENT SUBCOMMITTEE

DATA CONVERTERS SUBCOMMITTEE

Analog – 2018 Trends

Subcommittee Chair: *Kofi A. A. Makinwa, Delft University of Technology, Delft, The Netherlands*

The energy consumption of analog systems including sensors, amplifiers, and voltage and frequency references, is being scaled down to meet the demands of today's low-power systems. For example, in the case of integrated temperature sensors, this trend is captured by the movement towards the bottom-right in the plot shown in Figure 1. Fast power-up and power-down of such systems is also necessary to facilitate the use of duty-cycling to achieve even higher energy efficiencies. Together, these trends portend a future in which portable devices can be powered indefinitely from sustainable sources, opening the door to the Internet of Everything (IoE), ubiquitous sensing, environmental monitoring, and medical applications.

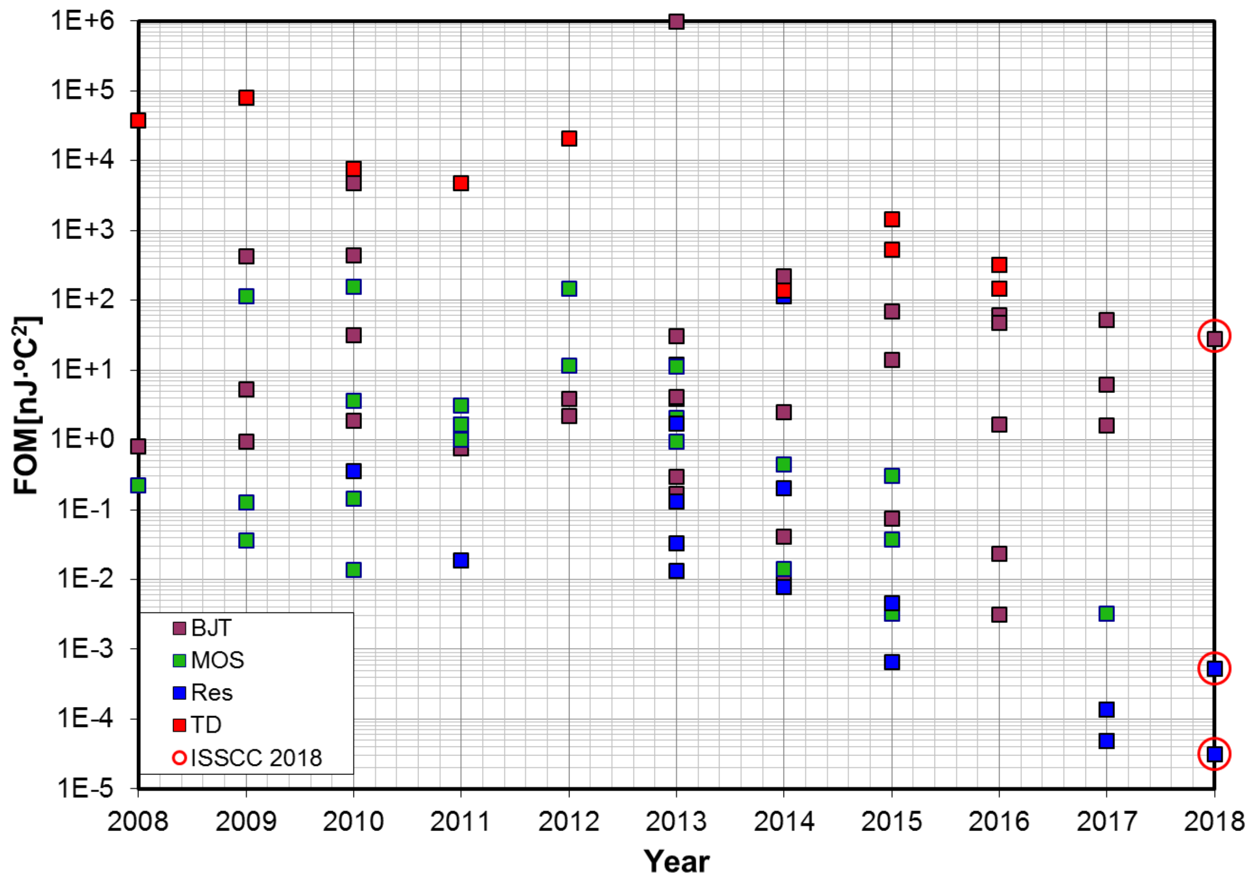

Figure 1 – Trends in the Energy Efficiency of Integrated Temperature Sensors: Resolution FOM versus Time

The stringent clocking requirements of many types of battery-powered mobile and emerging IoE systems pose various challenging requirements to system-level frequency references, including increased frequency stability, low noise, and strict control of temperature coefficient with a limited energy budget. To meet this challenge, the stability of integrated frequency references has been increasing steadily, as shown in Figure 2. This year, a 7MHz CMOS frequency reference was able to achieve a temperature coefficient (TC) of 3.85ppm/°C, the lowest reported so far.

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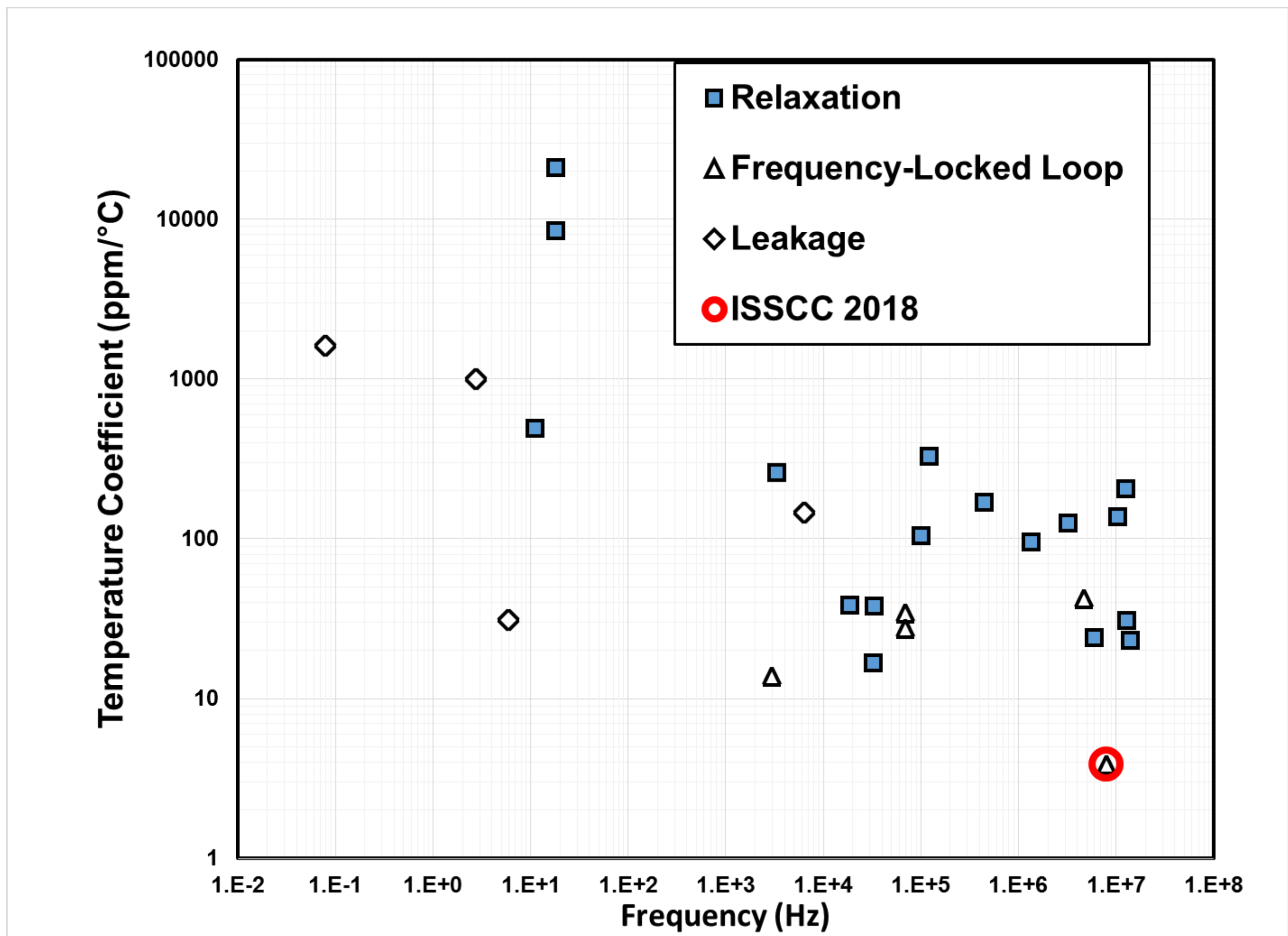

Figure 2 – Trends in the Stability of Integrated Oscillators: Temperature Coefficient versus Frequency.

We also see an increase in the linearity and resolution of amplifiers, for audio and precision amplifications, while at the same time maintaining, or even improving, their power efficiency.

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Power Management – 2018 Trends

Subcommittee Chair: *Axel Thomsen, Cirrus Logic, Austin, TX*

The efficient control, storage, and distribution of energy are worldwide challenges, and are increasingly important areas for analog circuit research. While the manipulation and storage of information is efficiently performed digitally, the conversion and storage of energy is fundamentally performed with analog systems. Therefore, the key technologies for power management are predominantly analog. For example, there is much interest in wireless power transmission for battery-charging applications, ranging from mobile handsets to medical implants: increased performance in wireless power transmission is enabling more-efficient power delivery over longer distances. There is also an explosion of technologies that allow energy to be collected from the environment in novel ways using photovoltaic, piezoelectric, or thermoelectric transducers, with a trend toward the use of multiple sources at the same time. A significant focus here is on analog circuits that are able to harvest sub-microwatt power levels from multiple energy sources at tens of millivolts, to provide autonomy for IoE devices, or to supplement conventional battery supplies in portable devices. To achieve this, the attendant analog circuits must consume extremely low power, so that surplus energy is available to charge a battery or super-capacitor. As can be noted in Figure 1, this trend is captured by movement towards the top-left.

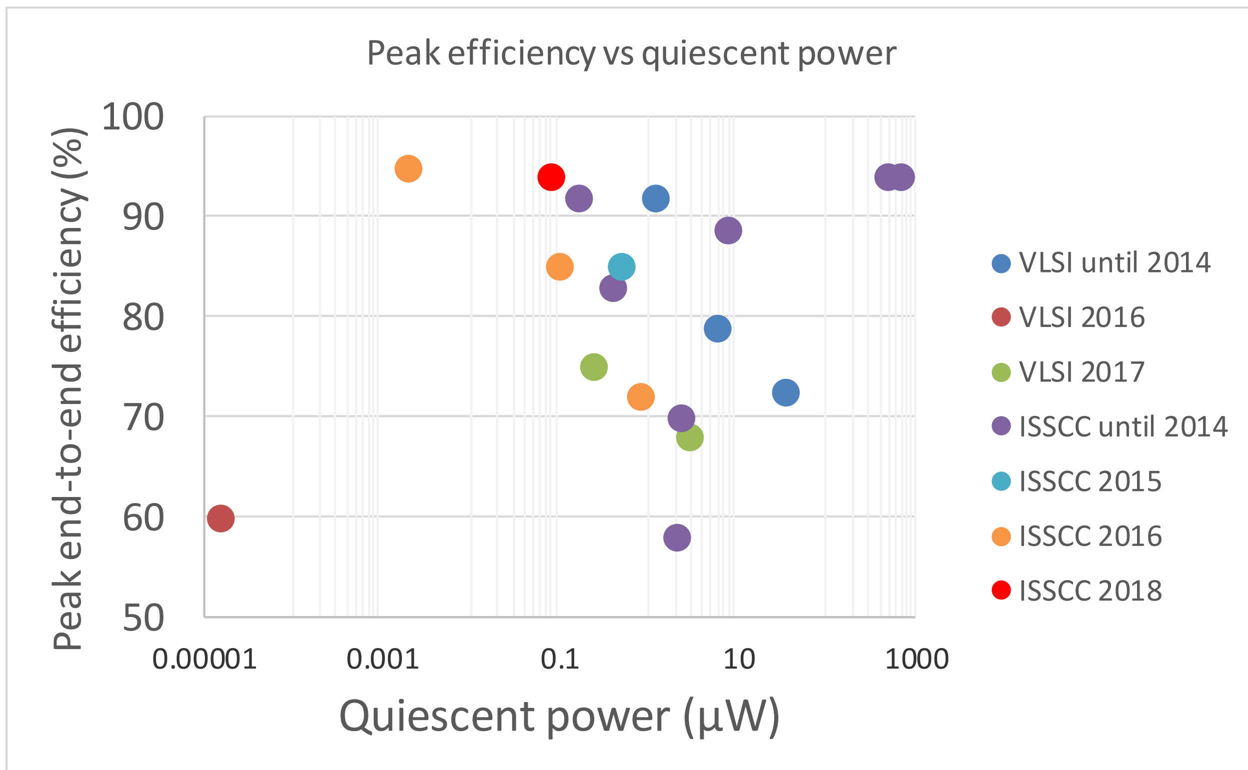

Figure 1 – Comparison of Integrated Energy-Harvesting Systems showing Peak End-to-End Efficiency vs Quiescent Power

Analog circuits also serve to bridge between the digital and the analog real world. Just as with actual bridges, analog circuits are often bottlenecks, and their design is critical to overall performance, efficiency, and robustness. In spite of this, digital circuits, such as microprocessors have driven the market, and semiconductor technology has been relentlessly optimized for digital circuits over the past 40 years to reduce their size, cost, and power consumption. Consequently, analog circuitry has proven increasingly difficult to implement using these modern IC technologies. For example, as the size of transistors decreased, the range of analog voltages they can handle as well as their analog performance have decreased, while the variation observed in their analog parameters has increased.

These aspects of semiconductor technology explain two key divergent trends in analog circuits: One trend is to forgo the latest digital IC manufacturing technology, instead fabricating analog circuits in older technologies, which may be augmented to accommodate the high voltages demanded by increasing markets in medical, automotive, industrial, and high-efficiency lighting applications. However, some other applications dictate full integration of analog and digital circuits together in the most modern digital semiconductor process. For example, microprocessors with multiple cores can reduce their overall power consumption by dynamically scaling operating voltage and frequency in response to time-varying computational demands. For this purpose, DC-DC voltage converters can be embedded alongside the digital circuitry, driving research into the delivery of locally-regulated power supplies with increasing efficiency, decreasing die area,

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and increasing power density. Correspondingly, these latest advances are implemented in the latest low-cost standard CMOS technologies. As can be noted in Figure 2, these trends are captured by movement towards the top-right.

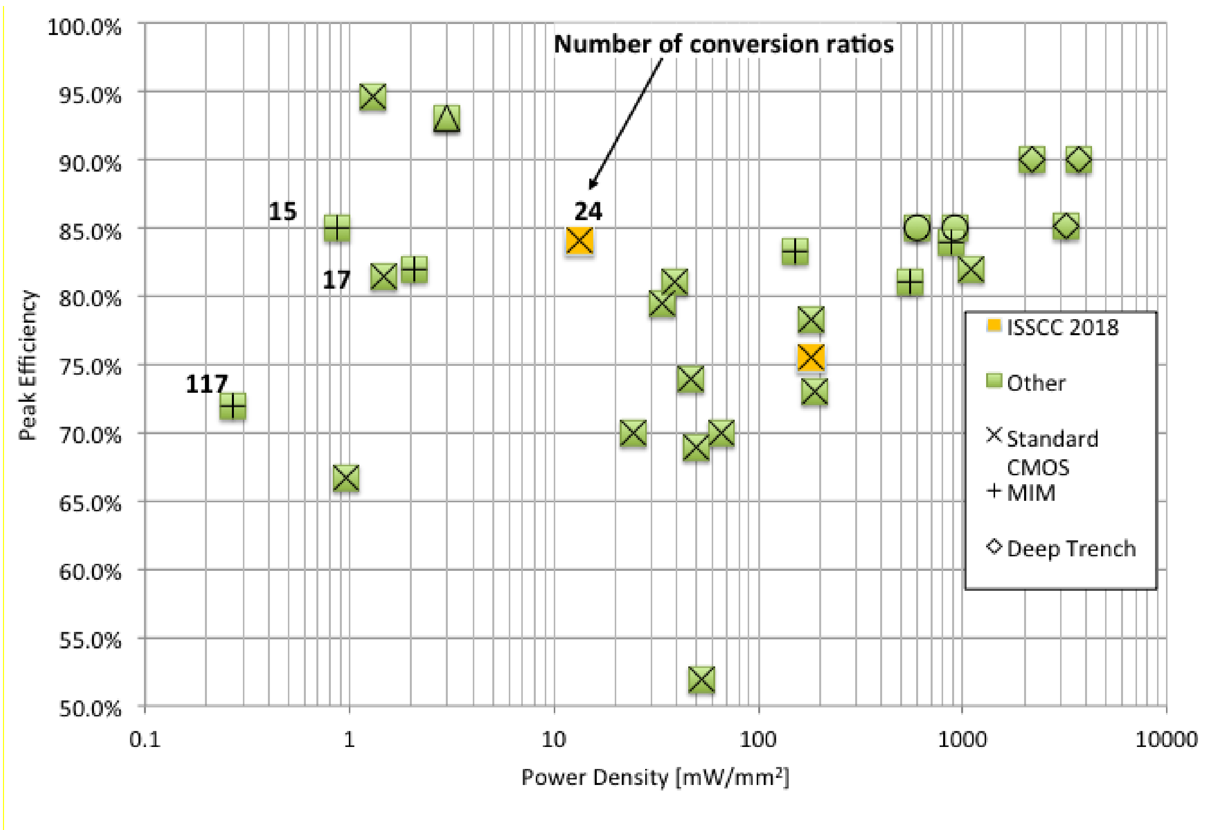

Figure 2 – Comparison of Integrated Switched-Capacitor Power Converters showing Peak Efficiency vs Power Density at Peak Efficiency (Conversion ratio refers to the relationship between output & input voltage)

This year, we see the performance of switched-capacitor power converters with a high number of conversion ratios making a significant step to increase their power density (Figure 2). A high number of conversion ratios are required in applications with high output and/or input voltage ranges, such as needed in IoE.

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Data Converters – 2018 Trends

Subcommittee Chair: *Un-Ku Moon, Oregon State University, Corvallis OR*

Data converters form the key link between the analog physical world and the world of digital computing and signal processing dominating modern electronics. The need to faithfully preserve the signal across domains continues to pressure data converters to deliver more bandwidth and linearity while continuing to increase power efficiency. This year, ISSCC 2018 continues the trend of GHz digital-to-analog converters with excellent linearity and noise performance. In analog-to-digital converters (ADCs) a combination of successive-approximation (SAR) and noise-shaping techniques is used to further improve speed, resolution, and power efficiency.

The three figures below represent traditional metrics which capture innovative progress in ADCs. Figure 1 plots power dissipated relative to the Nyquist sampling rate (P/f_{snyq}), as a function of signal-to-noise and distortion ratio (SNDR), to give a measure of ADC power efficiency. Note that a lower P/f_{snyq} metric represents a more efficient circuit on this chart. For low-to-medium-resolution converters, energy is primarily expended to quantize the signal; thus the overall efficiency of this operation is typically measured by the energy consumed per conversion and quantization step. The dashed trend-line represents a benchmark of 2fJ/conversion-step. Circuit noise becomes more significant with higher-resolution converters, necessitating a different benchmark proportional to the square of signal-to-noise ratio, represented by the solid line. In all figures, designs published from 2009 to 2017 are shown in green and older designs are shown in red, indicating a clear trend towards higher resolution at lower energy-per-conversion. ISSCC 2018 designs are shown in blue, with superior performance moving towards the lower right of Figure 1.

Figure 2 plots signal fidelity vs. the Nyquist sampling rate normalized to power consumption. At low sampling rates, converters tend to be limited by thermal noise, independent of the sampling rate. Higher speeds of operation present additional challenges in maintaining accuracy in an energy-efficient manner, indicated by the roll-off vs. frequency in the dashed line. The past 10 years have resulted in an over 10dB improvement in power-normalized signal fidelity, or a 10× improvement in speed for the same normalized signal fidelity. Of note in this year's ISSCC is that several designs improve upon the thermal-noise-limited efficiency, using a combination of SAR and noise-shaping.

Figure 3 shows achieved bandwidth as a function of SNDR. Sampling jitter or aperture errors coupled with an increased noise bandwidth make achieving both high resolution and high bandwidth a particularly difficult task. While 10 years ago a state-of-the-art data converter showed an aperture error of approximately $1ps_{rms}$, in recent years designs with aperture errors below $100fs_{rms}$ have been published at a wide range of resolutions. ISSCC 2018 further advances the art with the first data converter with an input frequency above 30GHz, using a 64× time-interleaved SAR ADC.

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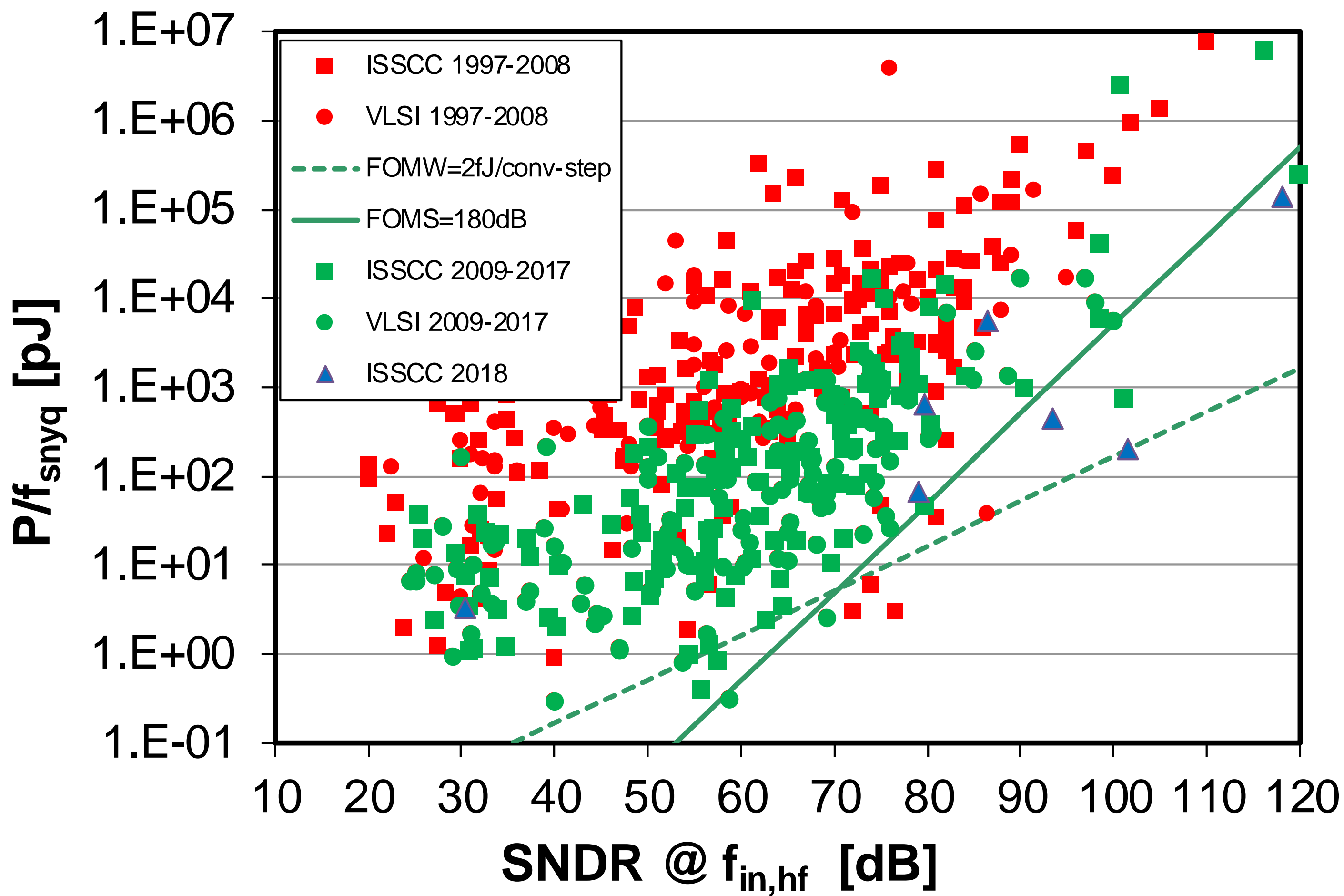

Figure 1: ADC power efficiency (P/f_{snyq}) as a function of SNDR.

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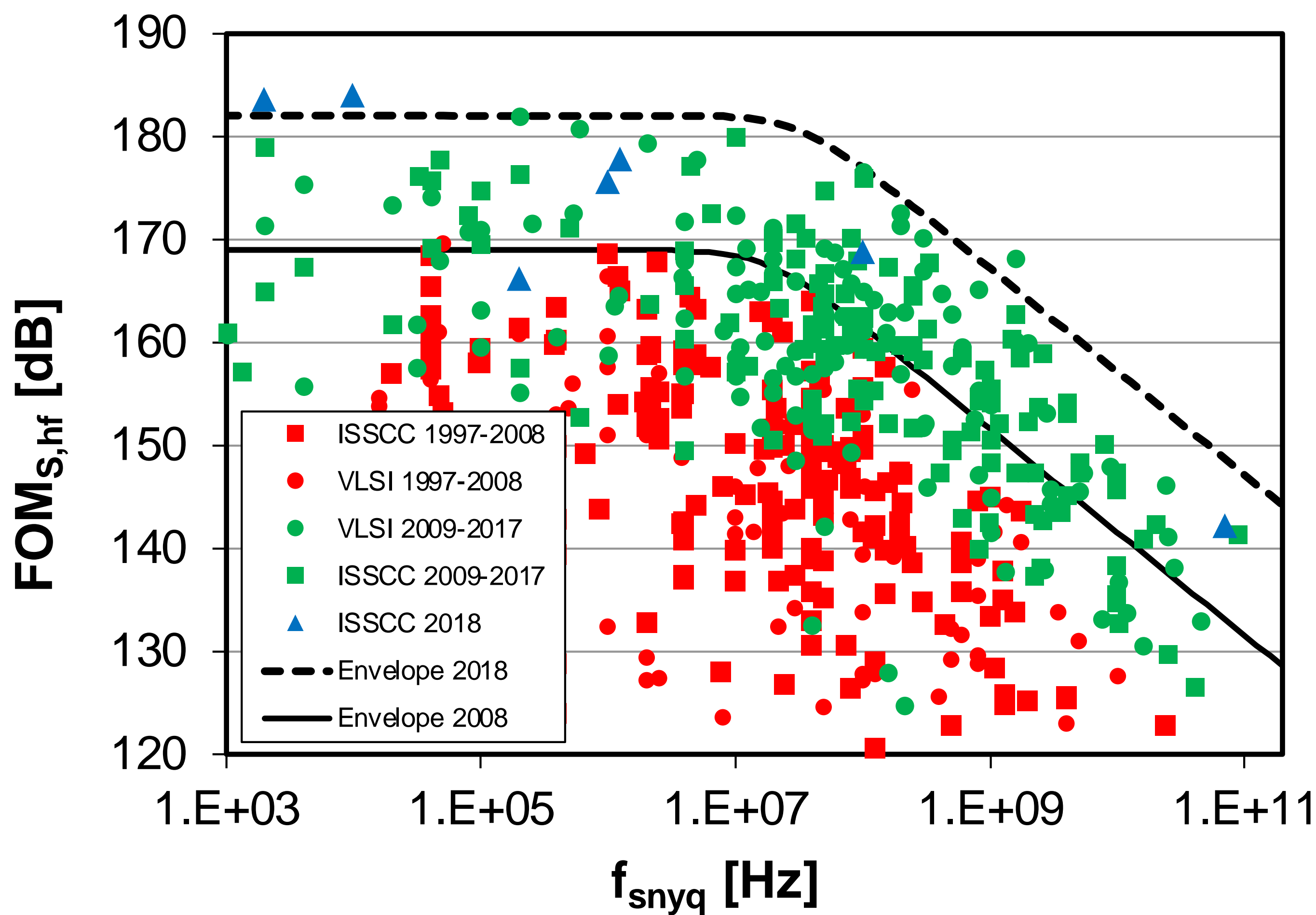

Figure 2: Power normalized noise and distortion vs. the Nyquist sampling rate.

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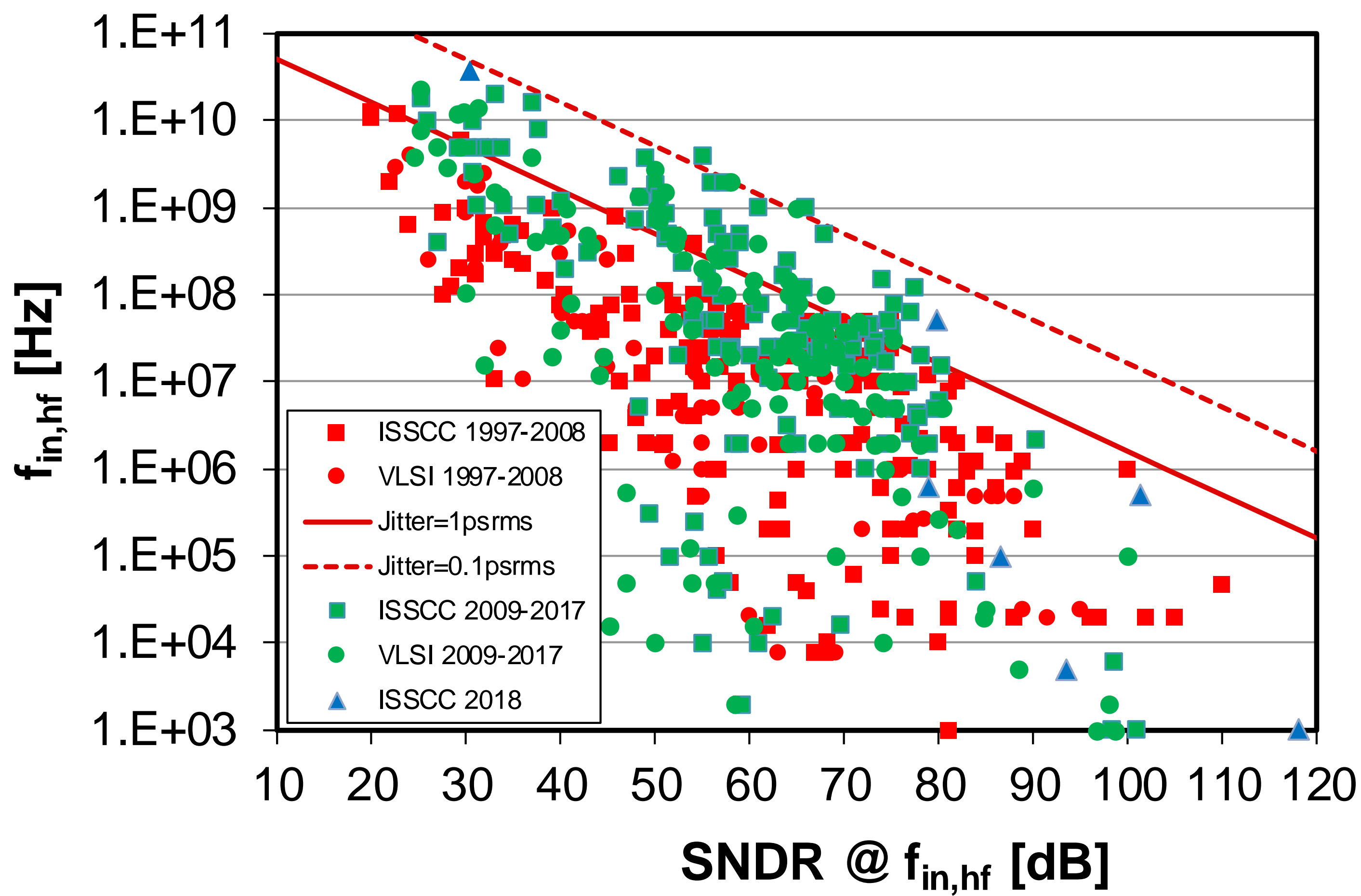

Figure 3: Bandwidth vs. SNDR.

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HISTORICAL TRENDS IN TECHNICAL THEMES

COMMUNICATION SYSTEMS

RF SUBCOMMITTEE – WIRELESS SUBCOMMITTEE

WIRELINE SUBCOMMITTEE

RF Subcommittee – 2018 Trends

Subcommittee Chair: Piet Wambacq, imec, Belgium

Introduction

This year, ISSCC 2018 features ongoing advancements in RF building blocks for broadband communications, mm-wave sensing, and THz imaging. Topics include frequency generation, efficient-transmit and robust-receive techniques for emerging cellular narrowband IoE, full-duplex, 5G massive-MIMO, and backhaul-link systems as well as real-time near-field imaging. Papers showcase advances in voltage-controlled oscillators and wideband mm-wave LO-generation blocks for 5G networks and digitally-intensive frequency synthesizers for communication and chirp-based radar-sensing applications. This document highlights such trends that will be presented at ISSCC 2018.

Frequency Generation and Synthesis: In the area of voltage-controlled oscillators, the trend is toward achieving low phase noise with architectural advancements such as waveform-shaping LC tanks or multicore and multiple-resonator-based circuits. As illustrated in Figure 1, phase noise of oscillators tends to increase at higher carrier frequencies. Achieving lower phase noise requires novel circuit topologies or spending more power. ISSCC 2018 presents a low-voltage inverse-Class-F VCO with 196.2dBc/Hz FOM and a 15GHz BiCMOS VCO with -124dBc/Hz PN at 1MHz offset.

Wideband mm-wave LO-generation building blocks become essential for next-generation broadband communications systems. At ISSCC 2018, injection-locked-frequency-multiplier-based techniques are demonstrated to support multiple bands in the mm-wave region. At sub-THz frequencies, stable sources are critical for imaging systems. ISSCC 2018 will present a BiCMOS 300GHz oscillator with a very stable frequency output with no need for a PLL or an off-chip crystal. The oscillator provides a peak output power of -13.9dBm from 302 to 332GHz.

In the field of frequency synthesizers, ISSCC 2018 will highlight advancements in digital architectures enabling compact-area low-power low-noise implementations. A 653μW fractional-N ADPLL for IoE applications will be presented. By leveraging an isolated constant-slope DTC, it achieves an integrated jitter of 0.53ps at 2.44GHz output with a power consumption of 0.98mW, corresponding to an FOM of -246dB. Another development presented is a frequency synthesizer comprising an all-digital frequency-locked loop and a type-I PLL with an LC VCO, occupying only 0.01mm^2 in 65nm CMOS, achieving -254dB jitter FOM from 4.6-to-5.6GHz output.

An important trend is a rising interest in frequency synthesizers for fully integrated chirp-modulation-based radar systems. At ISSCC 2018, two papers will address this topic: one showing a 23GHz digital bang-bang PLL for fast triangular and sawtooth chirp modulation and the other presenting a 36.3-to-38.2GHz fractional-N FMCW chirp synthesizer with a bandpass delta-sigma DTC.

RF Techniques for Communication and Sensing: At ISSCC 2018, papers will showcase techniques for integrating passive front-end filtering on IC. A 3.4dB NF full-duplex hybrid-coupler circulator with 40dB TX self-interference suppression will be presented. An N-path-filtering-based 13th-order reconfigurable bandpass filter for SAW-less receivers will be described. In the area of THz imaging, a 0.56THz sensing array for real-time near-field imaging in 0.13μm SiGe BiCMOS will be demonstrated.

Improving Output Power and Efficiency of mm-Wave PAs: Output power and power efficiency of silicon-based PAs have been limited due to their lossy output matching and combining networks. This year, several outstanding mm-wave transmitters/PAs which are remarkable both in peak output power and efficiency are presented as plotted in Figure 2. As well, a mm-wave radiator with an on-chip antenna array targeting 77GHz radar, achieves over 27dBm output power in 65nm CMOS. Co-design of a strongly coupled slot-antenna array and associated PAs effectively reduces the PA load impedance achieving efficient spatial power sharing without significant distortion of the desired radiation pattern.

Harmonic impedance tuning is a key to maximizing peak-power efficiency. A 5GHz CMOS PA in 65nm CMOS achieves a record peak PAE of 41% with harmonically tuned Class-F load network. As well, the PA is made highly linear thanks to a novel transformer-based AM-PM correction technique. Another 5G PA realizes wideband impedance matching both at fundamental and harmonic frequencies. It achieves 43.5% peak PAE and 19-to-29.5GHz wide P_{out} 1dB bandwidth.

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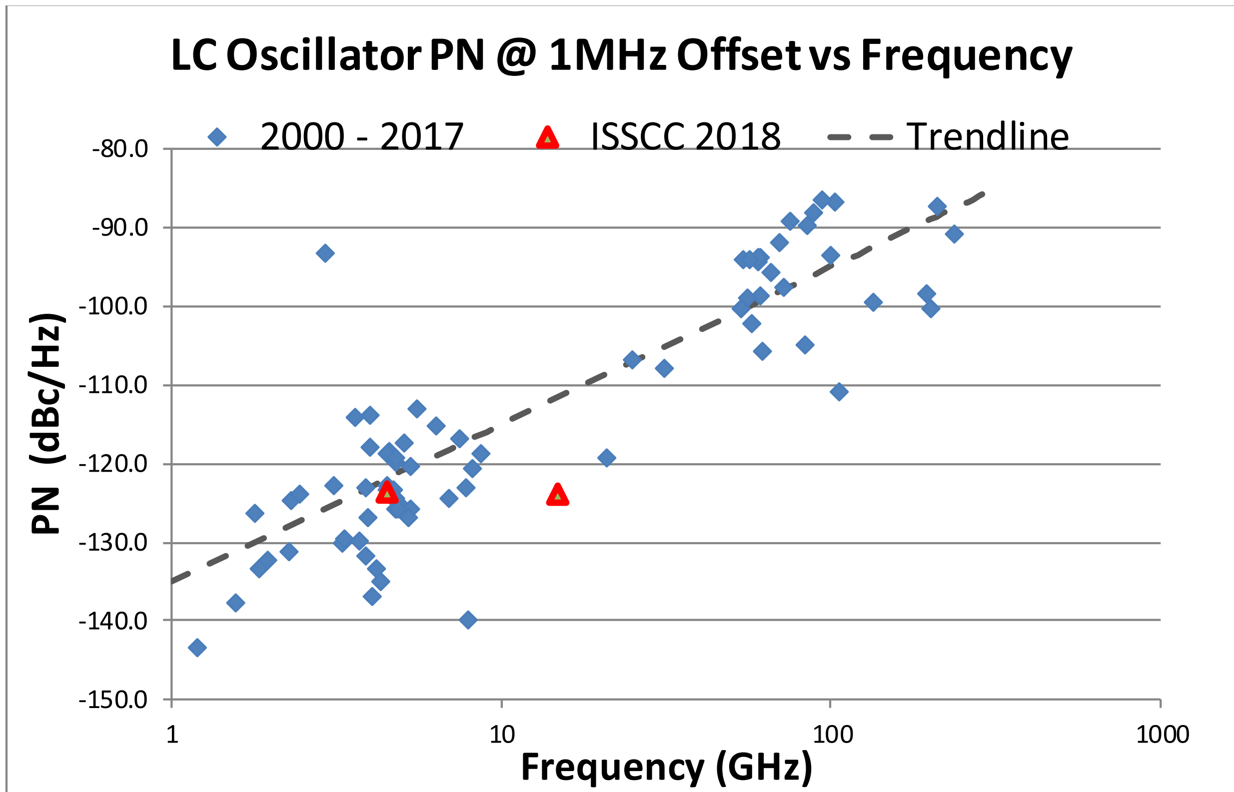

Figure 1: LC oscillator phase noise (PN) @ 1MHz offset versus carrier frequency.

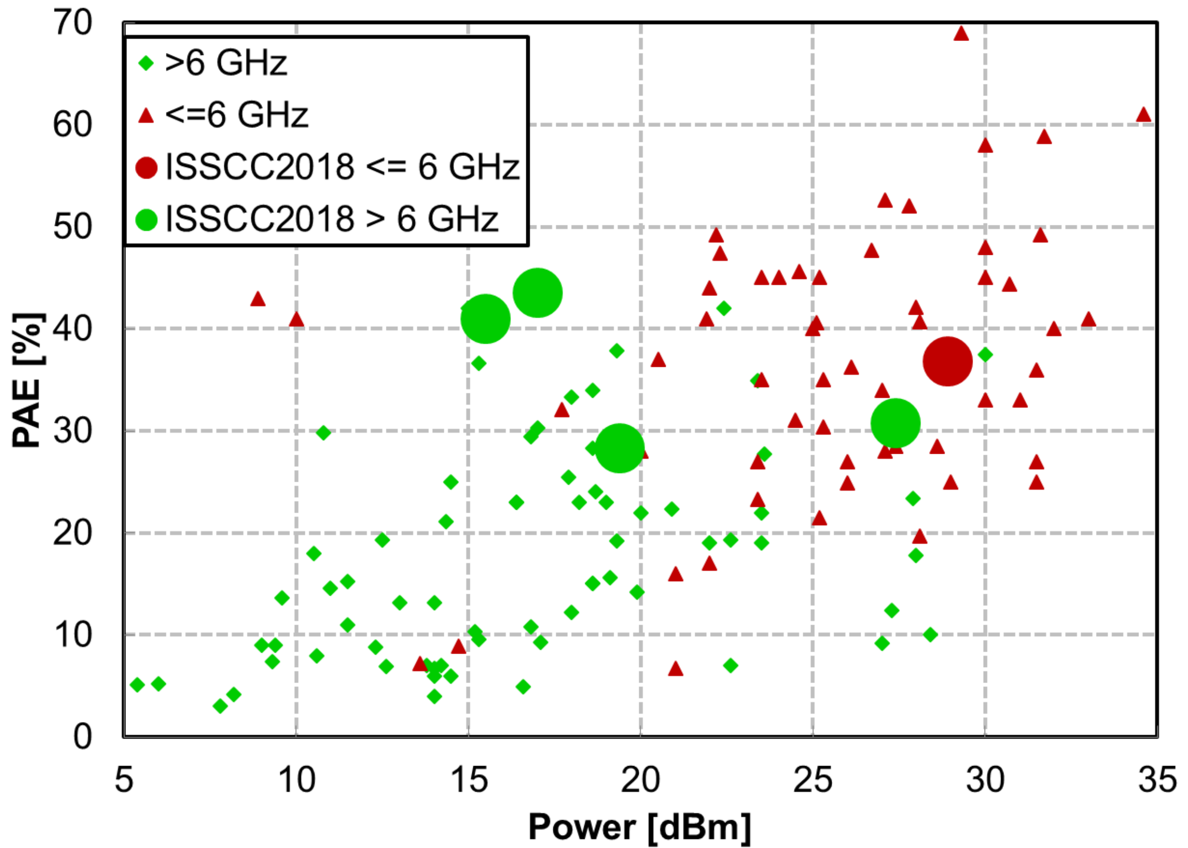

Figure 2: Peak power-added-efficiency (PAE) [%] versus max. output power [dBm] for recent Si-based power amplifiers.

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Wireless – 2018 Trends

Subcommittee Chair: *Stefano Pellerano, Intel, Hillsboro, OR*

The insatiable need for big-data communication calls for transceivers with high throughput. This has been achieved through higher digital modulation, carrier aggregation, MIMO with beamforming or beam steering, and interference detection and cancellation. The crowded cellular spectrum demands transceivers that are both flexible and also exhibit very good linearity. This year, at ISSCC 2018, a 14nm mobile-handset cellular transmitter with CIM3 of -62.6dBc will be demonstrated. Furthermore, a universal 400MHz-to-6GHz full-band-capture macro basestation transceiver will be presented. This enables carriers to deploy a common IC solution in virtually all of the 2G/3G/4G/5G bands.

Scalable mm-wave phased arrays with >100 elements capable of high-resolution beam steering have been developed for >18Gb/s point-to-point links. Further increase in network capacity by exploiting polarization-diversity has been demonstrated through integrated dual-polarization mm-wave MIMO and dual-polarization full-duplex links. Applications for integrated mm-wave radios include automotive radar. For this role, a fully-integrated multi-element radar transceiver has been developed in CMOS, supporting beamforming and MIMO radar.

In the IoE space, Bluetooth Low-Energy (BLE) transceivers continue to achieve lower power consumption and demonstrate new features. These include an energy harvesting BLE transmitter operating from just 0.2V in 28nm CMOS, and a single-crystal BLE transceiver using a 32kHz reference in 16nm FinFET. Wake-up receivers with under 10nW power consumption will be presented at ISSCC 2018. These can be used as an alternative to synchronization to enable long battery life in wireless sensor nodes. For higher-data-rate applications, frequency dependent IQ calibration is used in WLAN to support 802.11ax.

Figure 1 shows mm-wave wireless-data-rate trends over the past 10 years while Figure 2 shows ultra-low-power 2.4GHz and MICS-band wireless receiver sensitivity trends. Figure 3 shows ultra-low-power 2.4GHz and MICS-band wireless transmitter efficiency trends. Because many different techniques are used to design the circuits, there is significant scatter in the graphs. However, in all cases, the arrows show the desired trend directions.

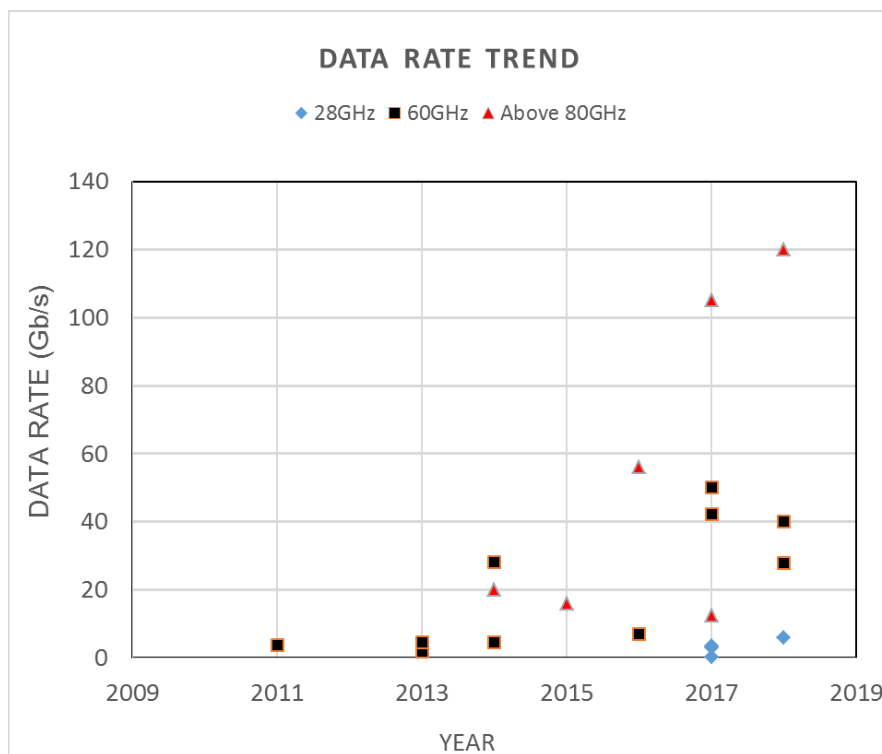

Figure 1: mm-Wave Wireless Data-Rate Trends.

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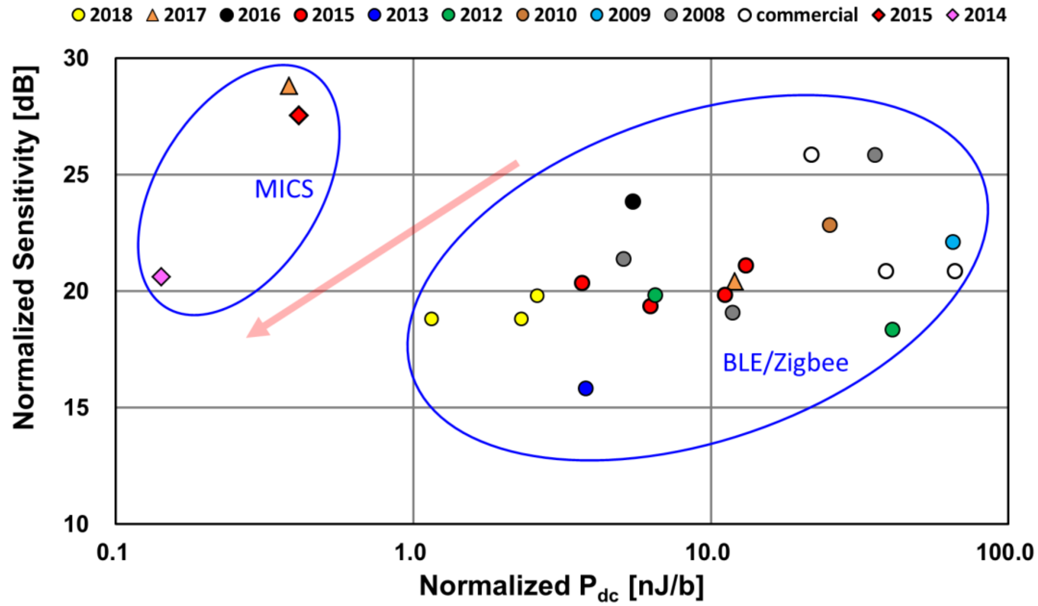

Figure 2: Ultra-Low-Power 2.4GHz and MICS-Band Wireless Receiver Sensitivity Trends.

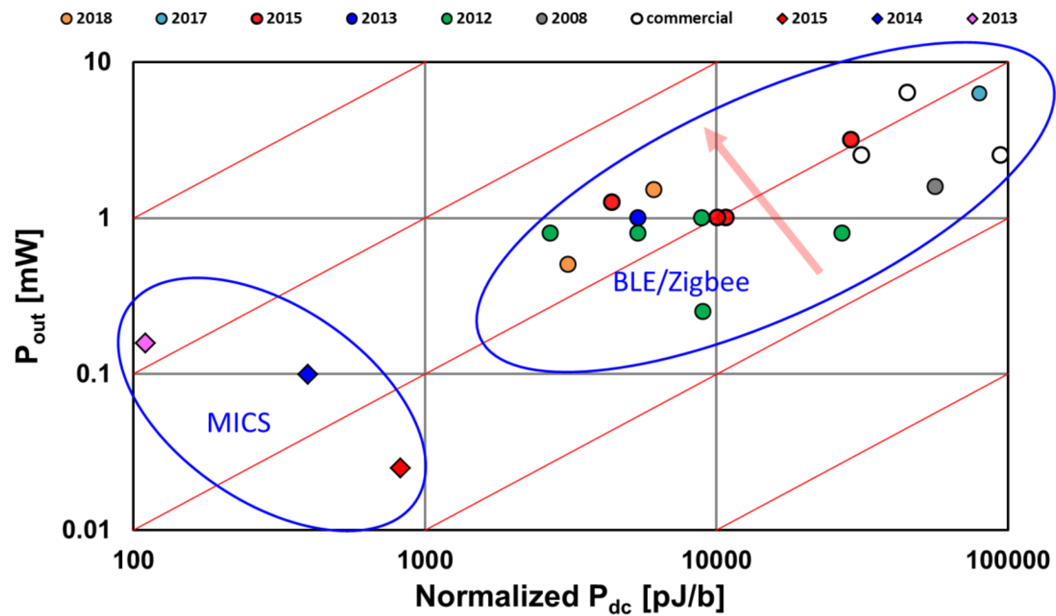

Figure 3: Ultra-Low-Power 2.4GHz and MICS-Band Wireless Transmitter Efficiency Trends.

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Wireline – 2018 Trends

Subcommittee Chair: *Frank O'Mahony, Intel, Hillsboro, OR*

For the past decade, wireline I/O has enabled the incredible scaling of computer systems both large and small, ranging from supercomputers to handheld electronics. During this time, aggregate I/O bandwidth requirements have increased at a rate of approximately 2× to 3× every 2 years. Demand for bandwidth has been driven by applications such as memory expansion, graphics, chip-to-chip fabric, backplane, rack-to-rack, and LAN. In part, this demand has been met by expanding the number of I/O pins per component. As a result, I/O circuitry consumes an increasing amount of area and power on today's chips. But, increasing bandwidth has also been enabled by rapidly accelerating the per-pin data rate. Figure 1 shows that per-pin data rate has approximately doubled every four years across a variety of diverse I/O standards ranging from DDR, to graphics, to high-speed Ethernet. Figure 2 shows that the data rates for published transceivers have kept pace with these standards, enabled in part by process-technology scaling. However, continuing this amazing I/O scaling trend will be thwarted by the future difficulties in transistor scaling. Significant advances in both energy efficiency and signal integrity must be made to enable the next generation of low-power and high-performance computing systems. Papers at ISSCC 2018 include 112Gb/s PAM-4 transmitters in 10nm and 14nm CMOS, and a power-efficient 56Gb/s ADC-based transceiver in 16nm CMOS.

Energy Efficiency and Interconnect Density:
Power consumption of I/O circuits is a first-order design constraint for systems ranging from cell phones to servers. As the pin count and per-pin data rate for I/Os have increased, so has the percentage of total power consumed by I/Os. Technology scaling has enabled increased clock and data rates, and offers improved energy efficiency, especially for digital components. However, simply increasing per-pin baseband data rates with existing circuit architectures and channels is not always a viable path given fixed system power limits. Figure 3 plots the energy efficiency (expressed in mW/Gb/s, which is equivalent to pJ/b) as a function of channel loss for recently reported transceivers. Looking at the most aggressive designs, the data indicates that the scaling factor between link power and signaling loss is slightly less than unity — in particular, that 30dB channel loss corresponds to a roughly 10× increase in pJ/b. Many recent advances have reduced power for high-speed link components through circuit innovation: these include low-power RX equalization (DFE, CTLE), CMOS resonant clocking, low-swing voltage-mode transmission, and links with low-latency power-saving states. At ISSCC 2018, a 112Gb/s PAM-4 transmitter in 10nm CMOS that consumes only 1.16pJ/b will be demonstrated. Furthermore, an 8b DAC-based 112Gb/s PAM-4 transmitter with a power efficiency of 2.55pJ/b will be presented.

Electrical Interconnect:
There has been ever-growing demand for very high-data-rate communication across a wide variety of channels. Some types of channels, especially those related to medium-distance electrical I/O (such as server backplanes), must support high data rates over high-loss channels. For these links, the key to scaling has been improvements in equalization and clock/data recovery. Recent high-speed transceivers use a combination of fully-adaptive equalization methods, including TX FIR, RX CTLE, and DFE, as well as RX FIR and/or IIR FFEs. As a result, recent receivers achieve data rates above 28Gb/s across channels with up to 50dB of loss. At ISSCC 2018, we see examples of transceivers that are starting to extend the equalization range of 56Gb/s wireline communication. One paper describes a 28.05Gb/s multi-standard transceiver that compensates 40dB loss with an energy efficiency of 6pJ/b. Another paper presents a fully adaptive 19-to-56Gb/s transceiver with a 3-to-7b reconfigurable ADC that achieves a power efficiency of 6.4pJ/b over a 7.4dB channel.

Optical Interconnect:
As the demand for higher bandwidth has accelerated and as electrical channel impairments become increasingly severe with per-lane data rates rise, optical interconnects have become an increasingly attractive alternative to traditional electrical wireline interconnects. Optical communication has clear benefits for high-speed and long-distance interconnects since it offers lower channel loss. Circuit-design and packaging techniques that have traditionally been used for electrical wireline are being adapted to enable integrated optical links with extremely low power. This has resulted in rapid progress in optical ICs for Ethernet, backplane, and chip-to-chip optical communication. At ISSCC 2018, a 56Gb/s 128mW burst-mode optical receiver with a rapid wake-up time of 6.8ns will be presented.

Concluding Remarks:
Continuing to aggressively scale I/O bandwidth is essential, but extremely challenging. Thus, innovations that provide higher performance and lower power must continue to be made in order to sustain this trend. Advances in circuit architectures, interconnect topologies, and transistor scaling are together changing how I/O will be done during the next decade. The most exciting and most promising of these emerging technologies for wireline I/O will be highlighted at ISSCC 2018.

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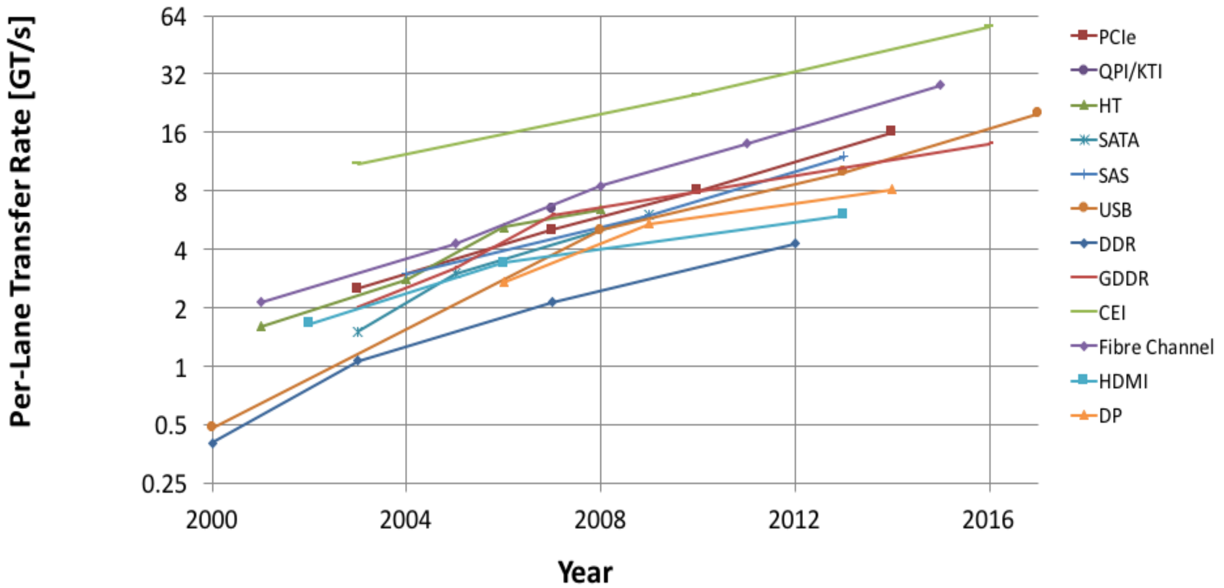

Figure 1: Per-pin data rate vs. Year for a variety of common I/O standards.

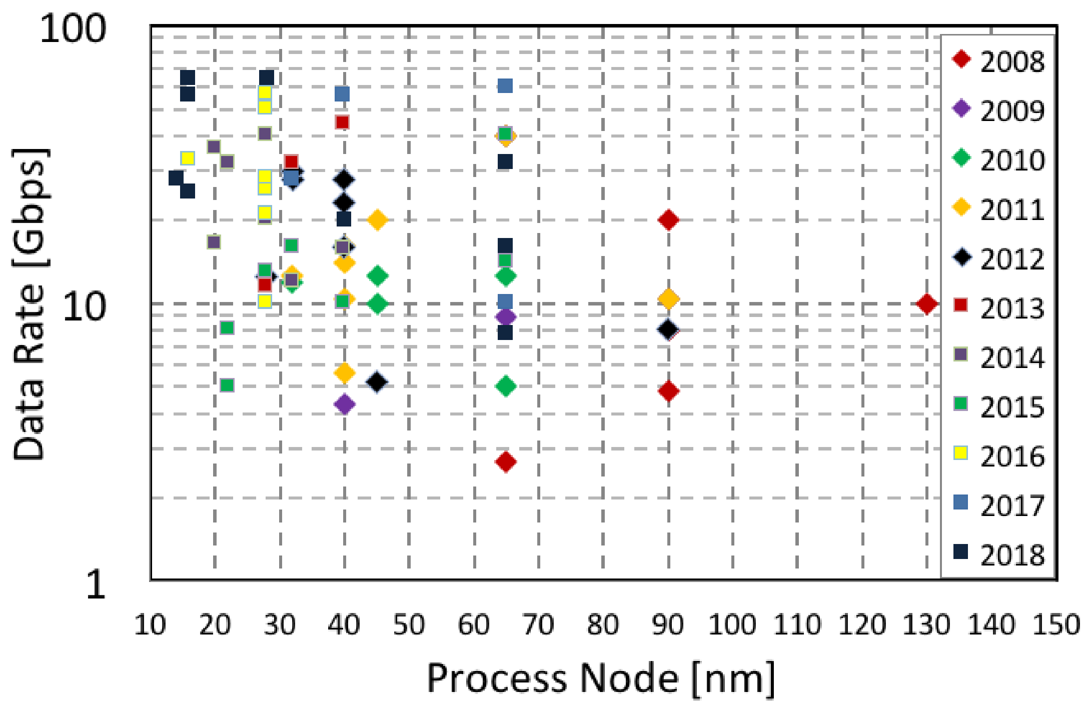

Figure 2: Data-rate vs. process node and year.

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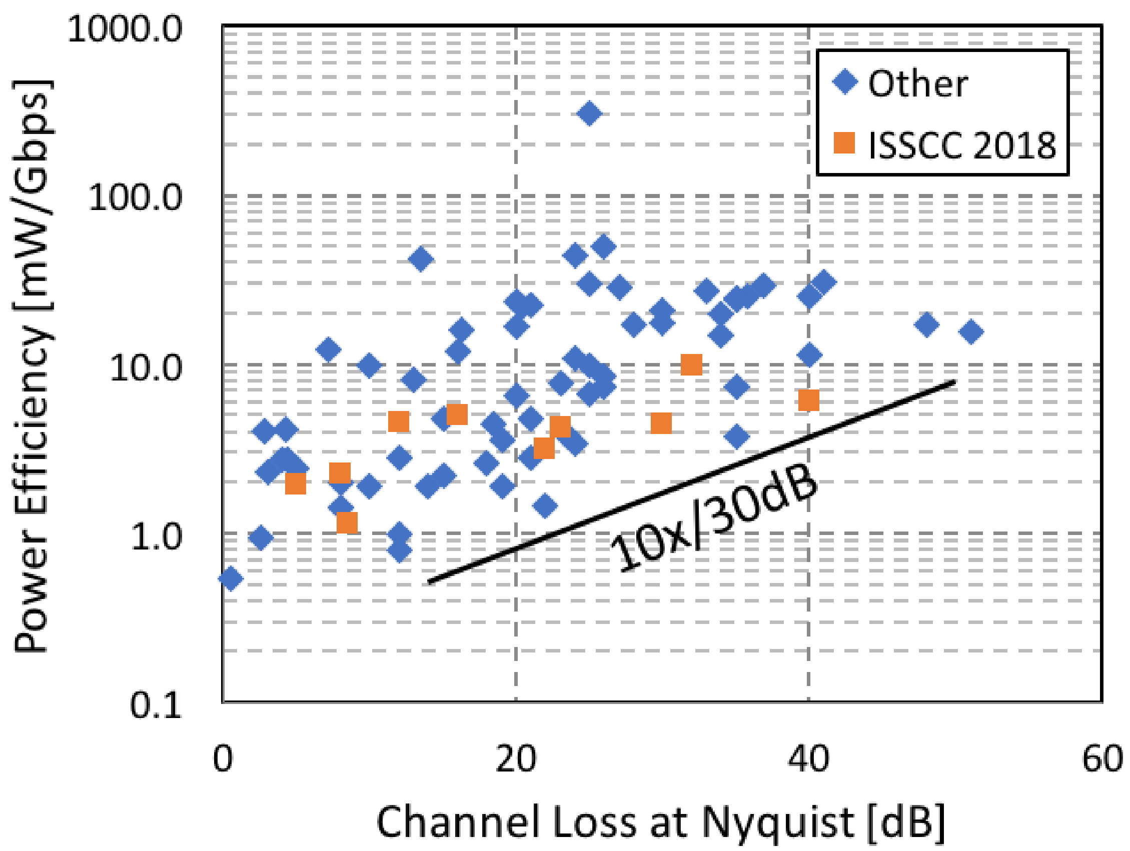

Figure 3: Transceiver power efficiency vs. channel loss.

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HISTORICAL TRENDS IN TECHNICAL THEMES

DIGITAL SYSTEMS

DIGITAL ARCHITECTURES & SYSTEMS SUBCOMMITTEE

DIGITAL CIRCUITS SUBCOMMITTEE

Digital Architectures & Systems (DAS) – 2018 Trends

Subcommittee Chair: Byeong-Gyu Nam, *Chungnam National University, Daejeon, Korea*

The dominant trend in high performance CPUs is the increasing number of processor cores per die and the amount of overall chip memory. For example, at ISSCC 2018, Intel will describe a server-class CPU integrating 28 cores using 14nm tri-gate process technology. The processor has a two-dimensional MESH on-die interconnect fabric serving the cores. Furthermore, multichip modules (MCMs) are emerging as a method by which to continue chip complexity growth, even while traditional process scaling slows down. For example, at ISSCC 2018, AMD will describe an SoC that is architected as a chiplet (incorporating 8 x86 cores) of which 1 to 4 would be configured on an MCM to service multiple markets including servers, mainstream and high-end desktops. Utilizing 14nm FinFET process technology, this chiplet SoC incorporates over 4.8B transistors on a 213mm^2 die. Meanwhile, clock-frequency growth has leveled off and is no longer systematically increasing, requiring more innovation at the architectural level to maintain performance-growth requirements. For example, at ISSCC 2018, IBM will describe a z14™ processor having 50% more L2 cache, 2× the amount of L3 cache, 25% more cores, running at 5.2GHz (which is 200MHz faster than previous designs), while maintaining the same power envelope. It also features significant microarchitectural updates for branch prediction, cache management, and cryptography.

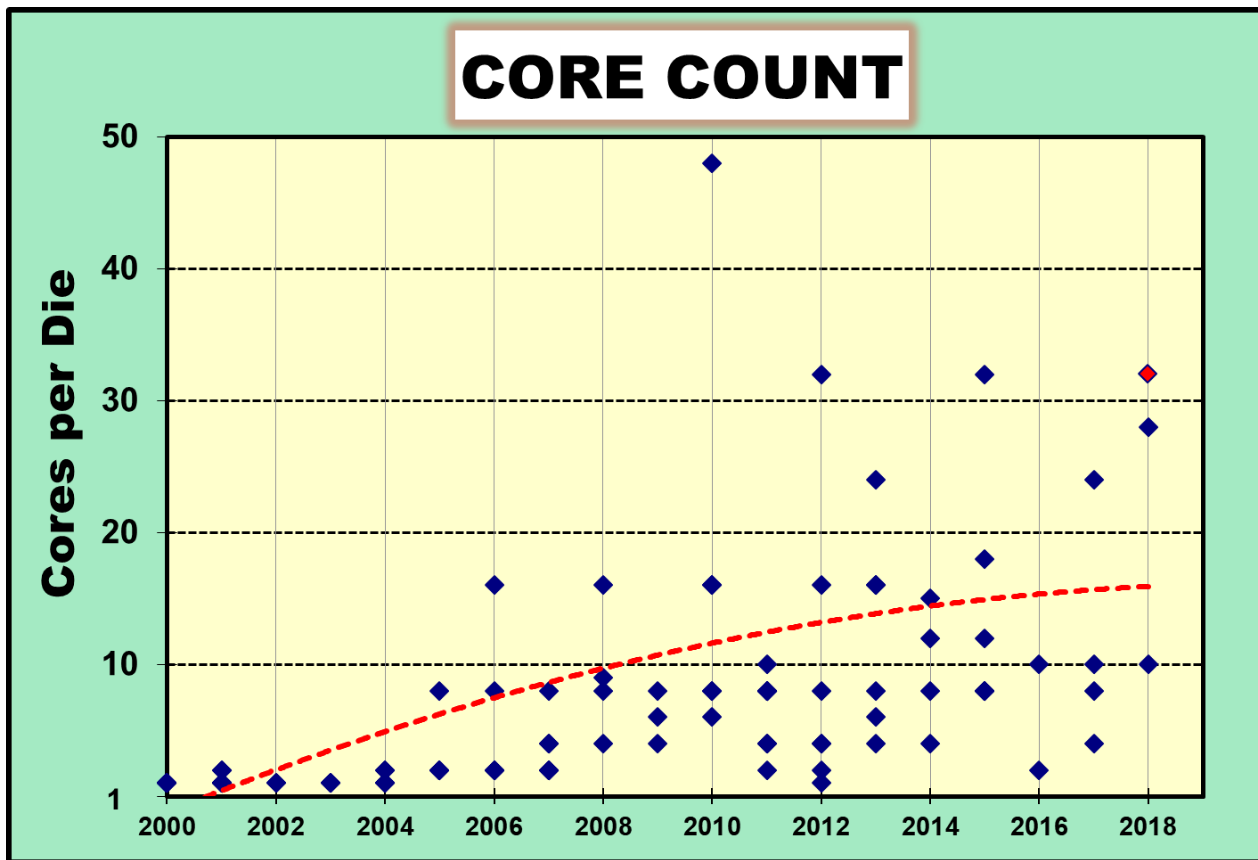

Figure 1: Core-count trends (red diamond designates multi-chip module).

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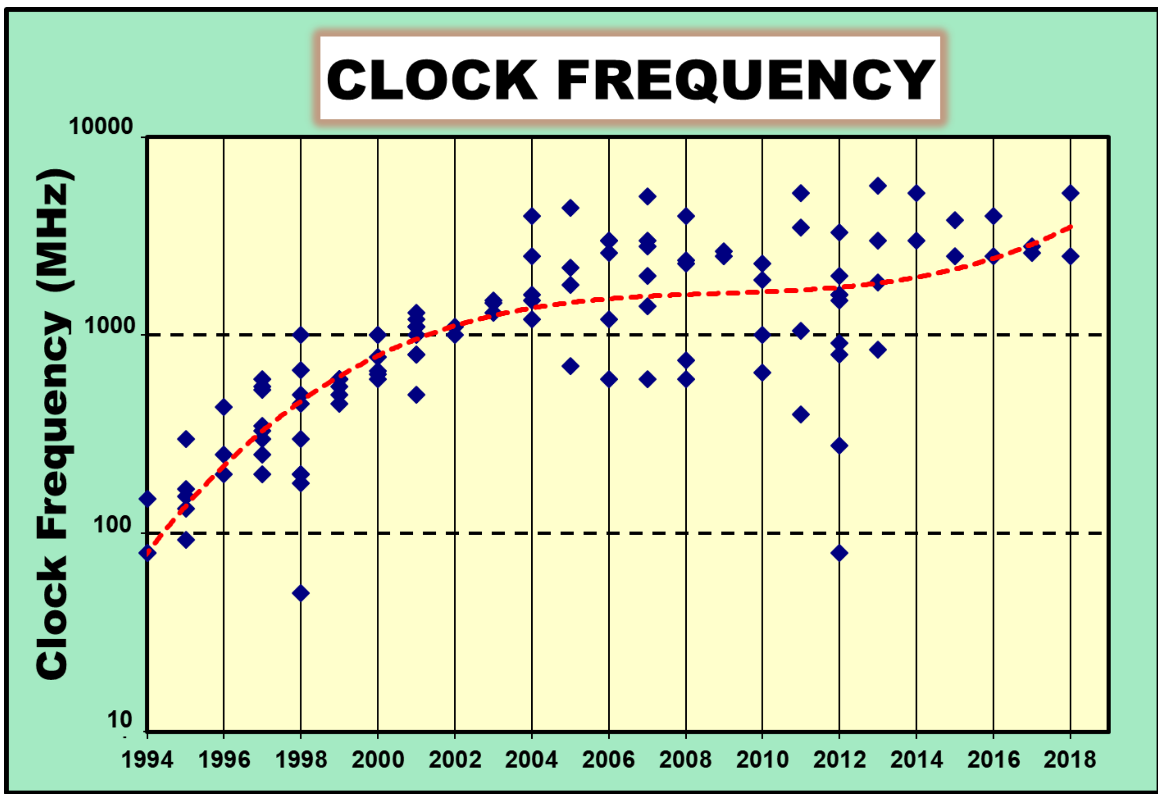

Figure 2: Clock-frequency-scaling trends.

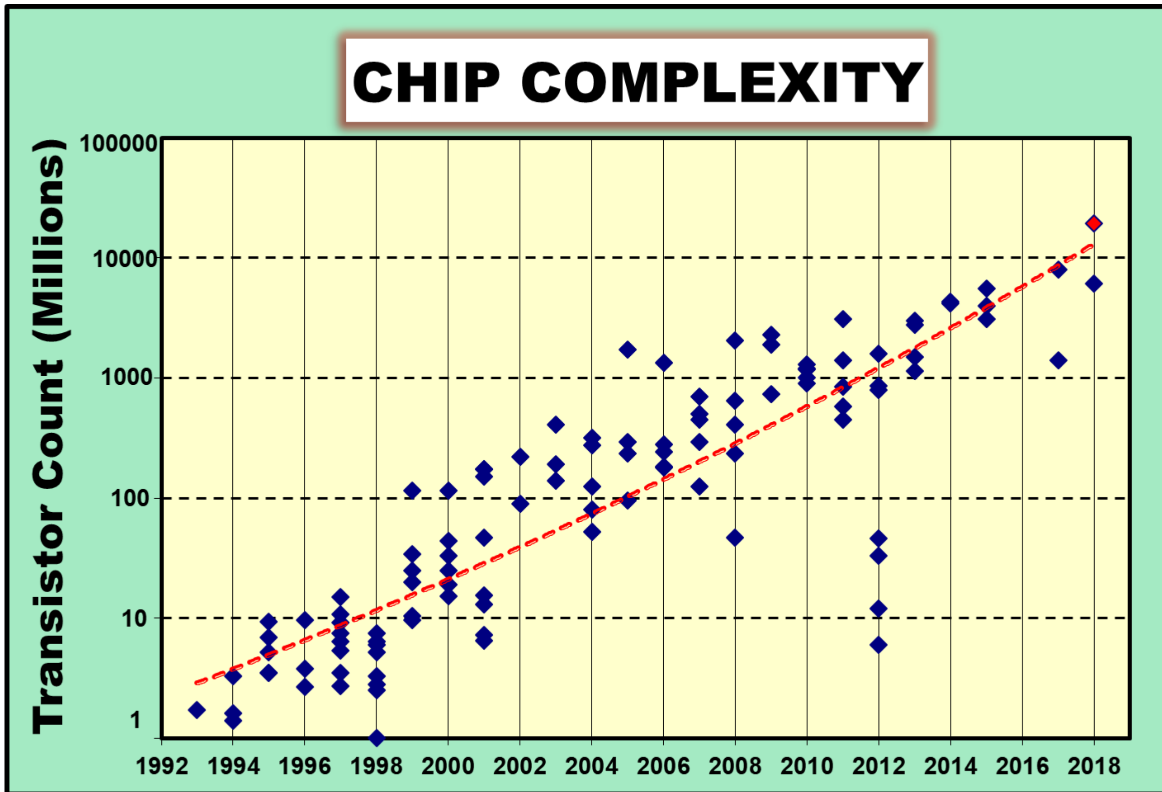

Figure 3: Chip-complexity scaling trends (red diamond designates multi-chip module).

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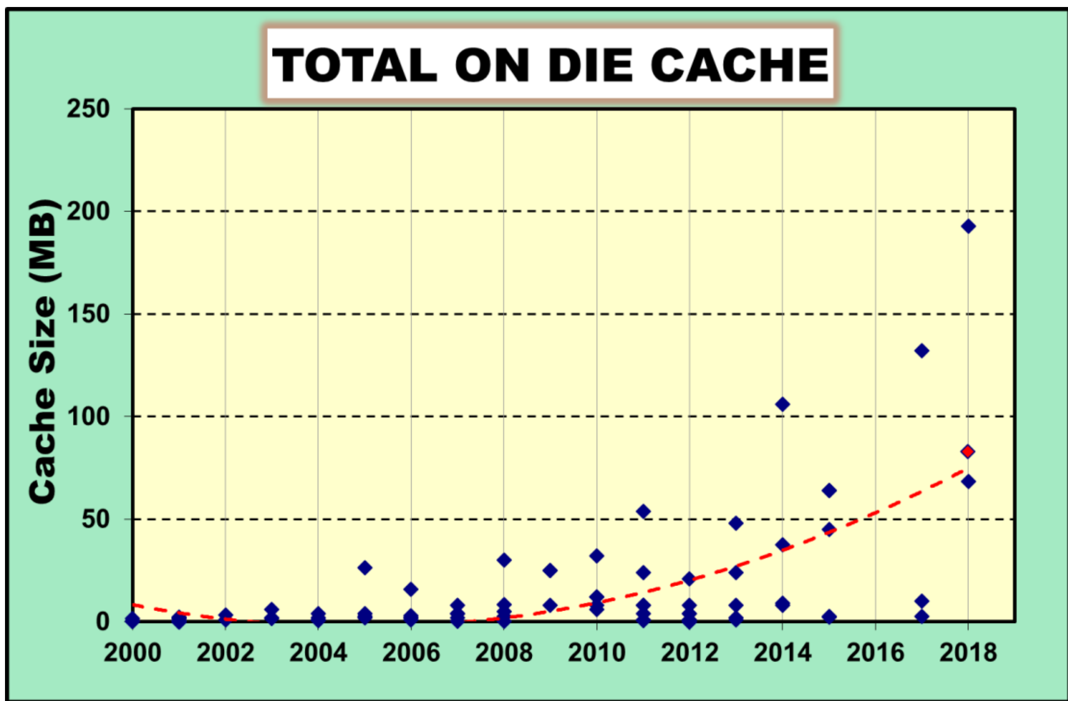

Figure 4: On-die cache-size trends (red diamond designates multi-chip module).

The computational performance of mobile AP (Application Processor) SoCs has historically grown as silicon process technology advances. This year, at ISSCC 2018, the leading SoCs remained in 10nm process technology and hence, did not show significant improvement in performance. Restricted by the slowdown in process-technology advancement, the maximum configuration shown has 8 heterogeneous cores similar to last year.

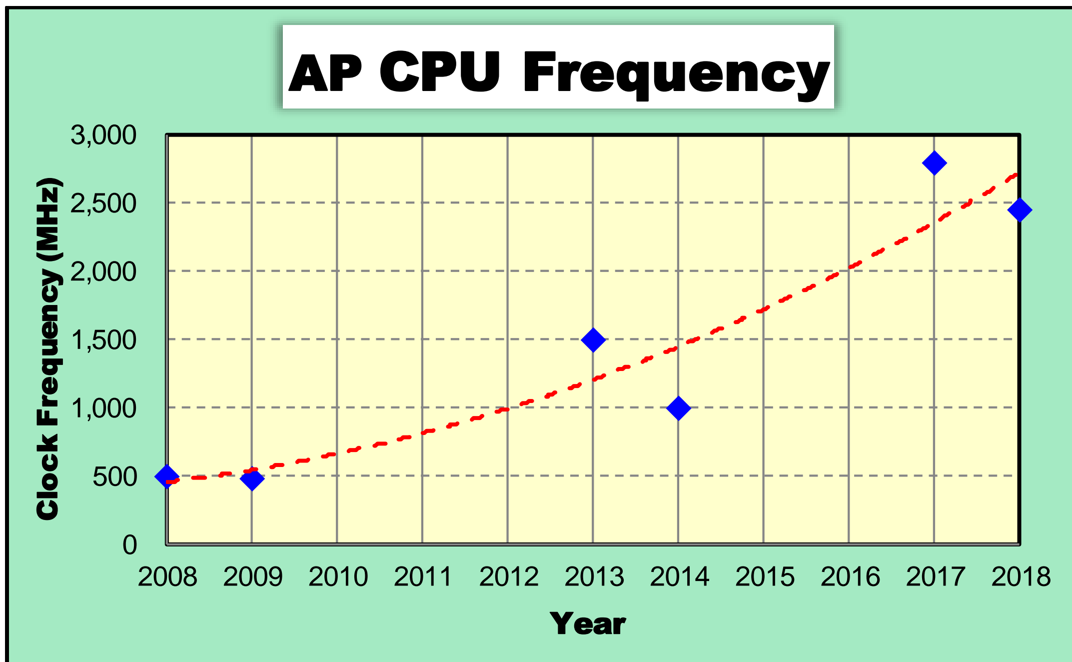

Figure 5: Clock-frequency trends for mobile CPU.

AP SoCs continue to add more features, including multimedia IP cores and accelerators on-chip to enhance functionality. Programmable neural-network processors have appeared in AP SoCs to enhance machine-learning application capabilities. Dedicated neural-network

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accelerators execute machine-learning functions faster and with higher energy efficiency than generic CPUs and GPUs. Neural-network processor units (NNPU) will be adopted in most future AP SoCs, consequently, establishing an important future direction: This will consist of an efficient software solution utilizing heterogeneous computing combining CPUs, GPUs, and NNPUs.

Graphics	OpenGL (ES1.1)	OpenGL/VG/MAX (ES2.0)	AR (Augmented Reality)	VR (Virtual Reality) Vulkan			
Display	VGA	WVGA @ 60fps	SXGA @ 60fps	WQXGA/WQXGA+ @ 60fps	WQXGA/WQXGA+ @ 60fpsx2 (VR)		
Camera	5~8M	10M	16M	20M	24M	12MxDual 360º VR	16MxDual 3D Depth / AR
Image/Video	H.264/AVC (VGA)	H.264/AVC (D1)	H.264/AVC (Full HD)	H.264/MVC H.264/SVC	H.265/VP9	H.265/VP9 HDR	AV1 HDR10+
Audio	AAC	AAC Plus	WMA Dolby 5.1	Dolby TrueHD/Digital+	DSD Dolby Atmos		
Accelerator	FPU	SIMD Multi core (2-4)	Multi core (4-8)	Heterogeneous Multi-Processing	Neural-net Processor		
downlink [Mb/s]	UMTS 0.4- 2	HSPA 1.8 - 7	HSPA+ 7 - 42	LTE 100	LTE-A 150-750	LTE-A 1600	LTE-A 2000
CPU [MIPS]	300 500	500 800	800 2400	2400 6000	6K 12K	12K 100K	13K 112K

CPU [MIPS] (continued): 9K 162K

Years: 2007, 2008, 2009, 2010, 2011, 2012, 2013, 2014, 2015, 2016, 2017, 2018

Figure 6: Application-processor trends in smart phones.

Wired and wireless links continue to increase in bandwidth with a trend of 10× increase in data rate every five years. Changes are modest this year relative to last year, however the 802.11ax standard is close on the horizon. mm-wave and massive MIMO technologies are being actively studied to realize 5G communication. The explosion of IoE devices will require the evolution of narrow-band wide-area networks.

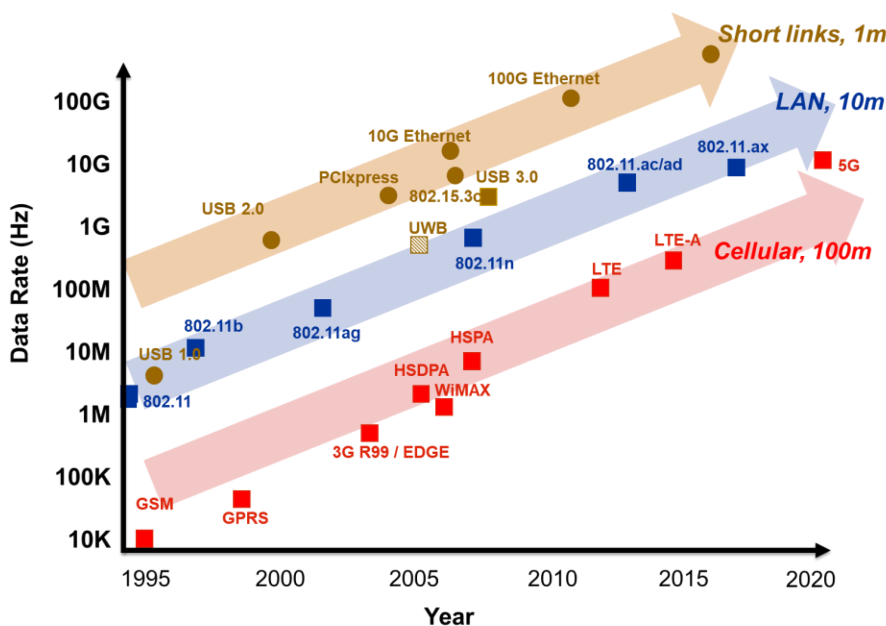

Figure 7: Data-rate trends in wired, wireless, and cellular.

Deep learning is a rapidly evolving topic at ISSCC 2018. The computational complexity of typical deep neural networks impedes their execution on resource-scarce mobile or wearable devices. Last year, several innovative solutions were introduced to enhance throughput and improve energy efficiency, mostly focusing on the efficiency of convolutional neural networks (CNN). The current state-of-the-art still

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faces two significant challenges: 1) A need to improve energy efficiency for ultra-low power applications; and, 2) solutions for efficient execution of fully connected non-convolutional networks.

To realize improved energy efficiency, there is a trend towards reduced-precision networks, with binary networks as the extreme case. Recently, the first binary neural-network accelerator has appeared. This year, ISSCC 2018 pushes peak efficiency to several tens of TOPS/W (digital accelerators) to beyond hundreds of TOPS/W for a mixed-signal implementation. Several papers at ISSCC 2018 treat energy efficiency of fully-connected-network acceleration. In such networks, the bottleneck is the memory load/stores, and as such, innovative solutions include the fabrication of a 3D stack of processing and memory dies, as well as smart-memory interfaces enhancing data reuse. These innovations clearly bring deep neural networks within reach of battery operated devices.

Figure 8 illustrates deep-learning processor efficiency and throughput improvements for CNNs and DNNs presented at ISSCC 2018, as compared to the state-of-the-art in 2017.

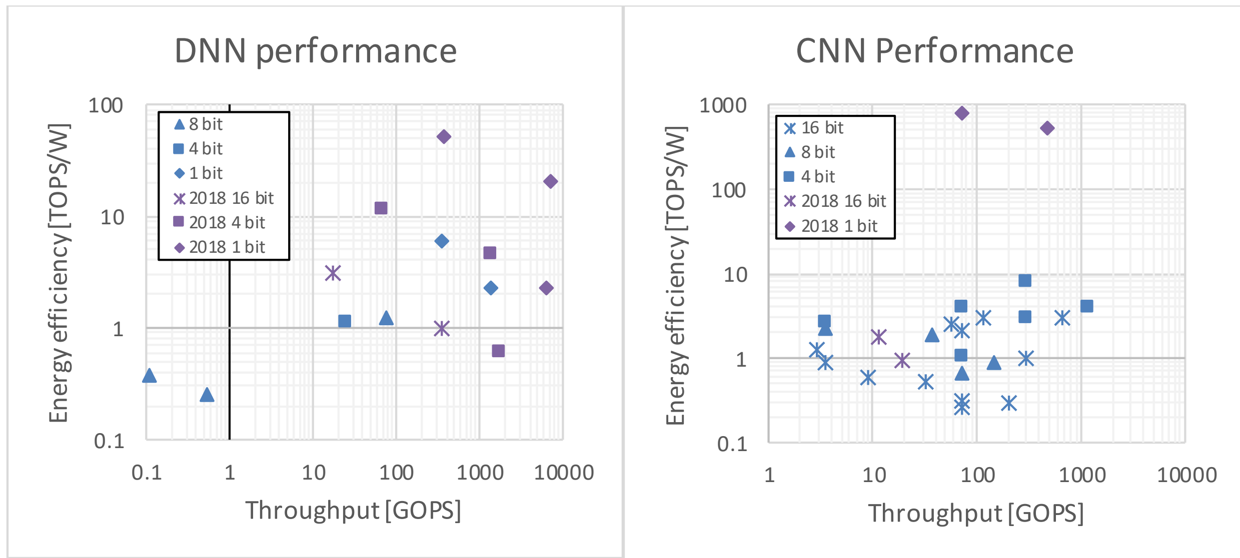

Figure 8: Deep-learning processor throughput and efficiency.

Highlights ISSCC 2018: ISSCC 2018 features the Intel SkyLake-SP Xeon processor, a server class CPU with 28 cores in an 11-metal layer 14nm tri-gate process technology. The Xeon incorporates 6 DDR4 channels capable of 2667GT/s per channel, 10.4GT/s processor-to-processor UPI links and PCI links. IBM presents the next generation z14™ processor fabricated in 14nm. This processor has 50% more L2 cache, 2× the amount of L3 cache, 25% more cores, runs 200MHz faster than previous designs, while maintaining the same power envelope. AMD describes "Zeppelin", an SoC that is architected as a chiplet, configurable with 1-4 chips on an MCM to service multiple markets, including server, mainstream and high-end desktops. It contains 8 x86 cores, 16MB L3 cache, memory and I/O controllers, and integrated Southbridge capabilities. These functions are connected on the SoC and between chips with AMD's new coherent Infinity Fabric.

Hokkaido University proposes stacking its novel MIMD-parallel multi-purpose deep-neural network (DNN) accelerator, with SRAM dies to balance capacity, latency, and bandwidth, and also features a logarithmic-quantized DNN architecture. KAIST presents a DNN accelerator that supports CNNs and RNNs with a single programmable architecture, that outperforms previous hybrid-type CNN-RNN architectures in energy efficiency. Stanford University/KU-Leuven also proposes a CNN mixed-signal inference processor that is an order-of-magnitude more energy efficient than previous work, combining an all on-chip memory, data-parallel architecture, and switched-capacitor circuits.

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Digital Circuits – 2018 Trends

Subcommittee Chair: *Edith Beigne, CEA-LETI, Grenoble, France*

Demand for higher performance across ubiquitous, connected, and energy-constrained platforms ranging from Internet of Everything (IoE) to cloud data-centers continues to drive innovations in all CMOS digital-circuit building blocks, with goals of improving energy-efficient performance, lowering cost/design effort, and enhancing security. Classic technology scaling has slowed and circuit design efforts are exploiting technology features, such as body biasing and passive-device advancements, to enable circuit innovation.

Energy-Efficiency Techniques and Integrated Voltage Regulators: Energy reduction remains a top priority as power density continues to increase. Voltage regulators, while traditionally being off-chip, have increasingly been integrated on-chip to reduce cost. Low-dropout (LDO) linear regulators, switched-capacitor voltage regulators (SCVR), and now, inductor-based buck voltage regulators (LCVR) are integrated in scaled process nodes to enable faster and fine-grain dynamic voltage and frequency scaling (DVFS) of individual functional blocks. In turn, the low voltages supported in DVFS systems necessitate a move from analog-based LDOs to digital implementations. Figure 1 shows the conversion efficiency and current density of these integrated voltage regulators which continues to improve. Variation mitigation has also become a major trend in digital circuits in order to improve robustness and power efficiency across Process, Voltage, and Temperature (PVT). Specific all-digital sensors and adaptive techniques are currently proposed to mitigate these effects on-chip.

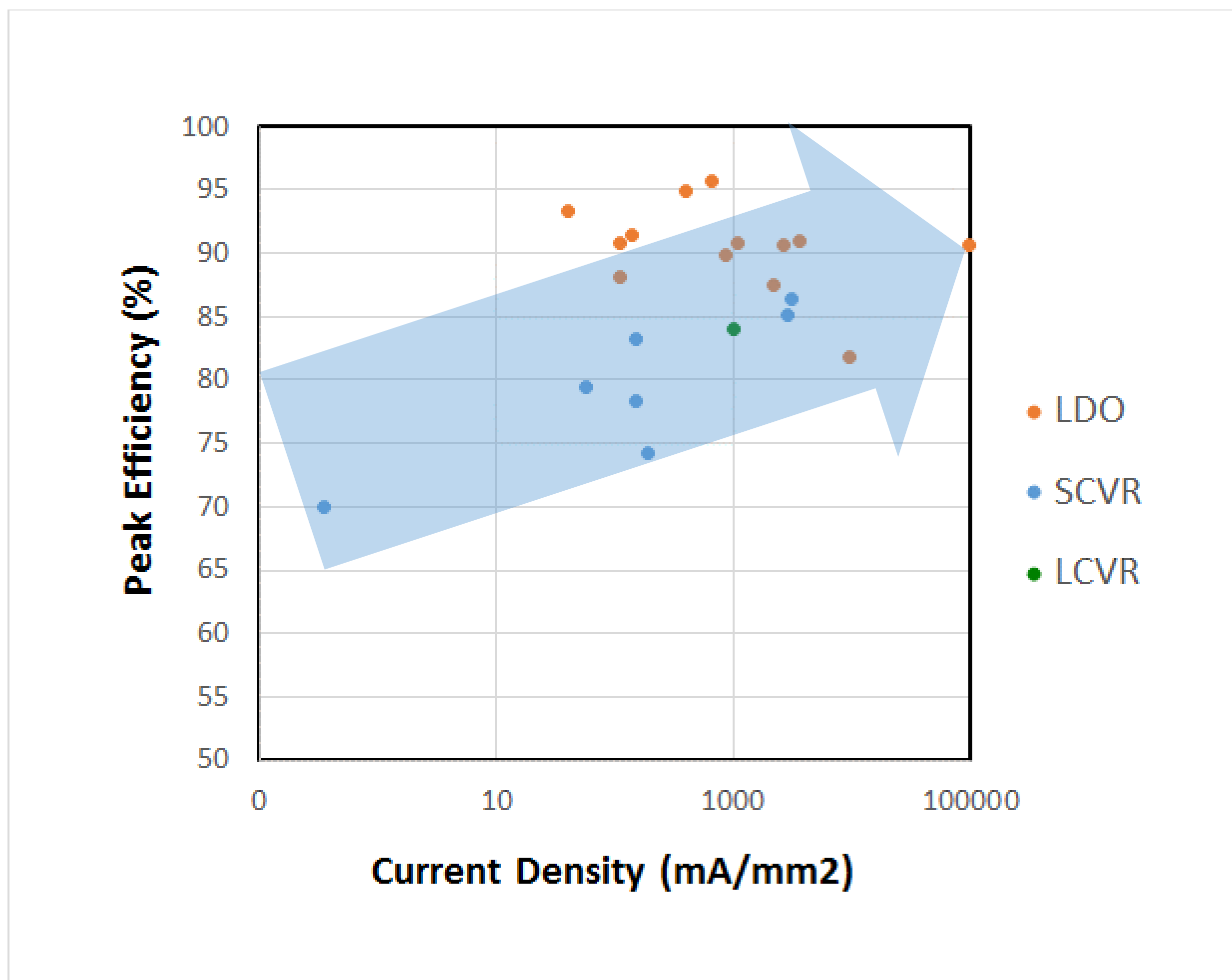

Figure 1. Integrated voltage regulators

Synthesizable Digital PLLs for Low-Jitter Applications: PLL trends include migration from analog to digital to include more functionality, cope with variability, and ease scaling to finer geometries. Demand for compact low-jitter PLLs is increasing. The use of more automated digital design flows (such as synthesis and APR) dramatically reduces development costs, but can degrade jitter, requiring new techniques to compensate. Figure 2 highlights metrics for PLLs and DPLLs published at ISSCC over the past 10 years; the plot shows the relationship between reference (input) frequency and figure-of-merit, demonstrating the tradeoff between cost

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(higher reference frequency) and overall PLL performance.

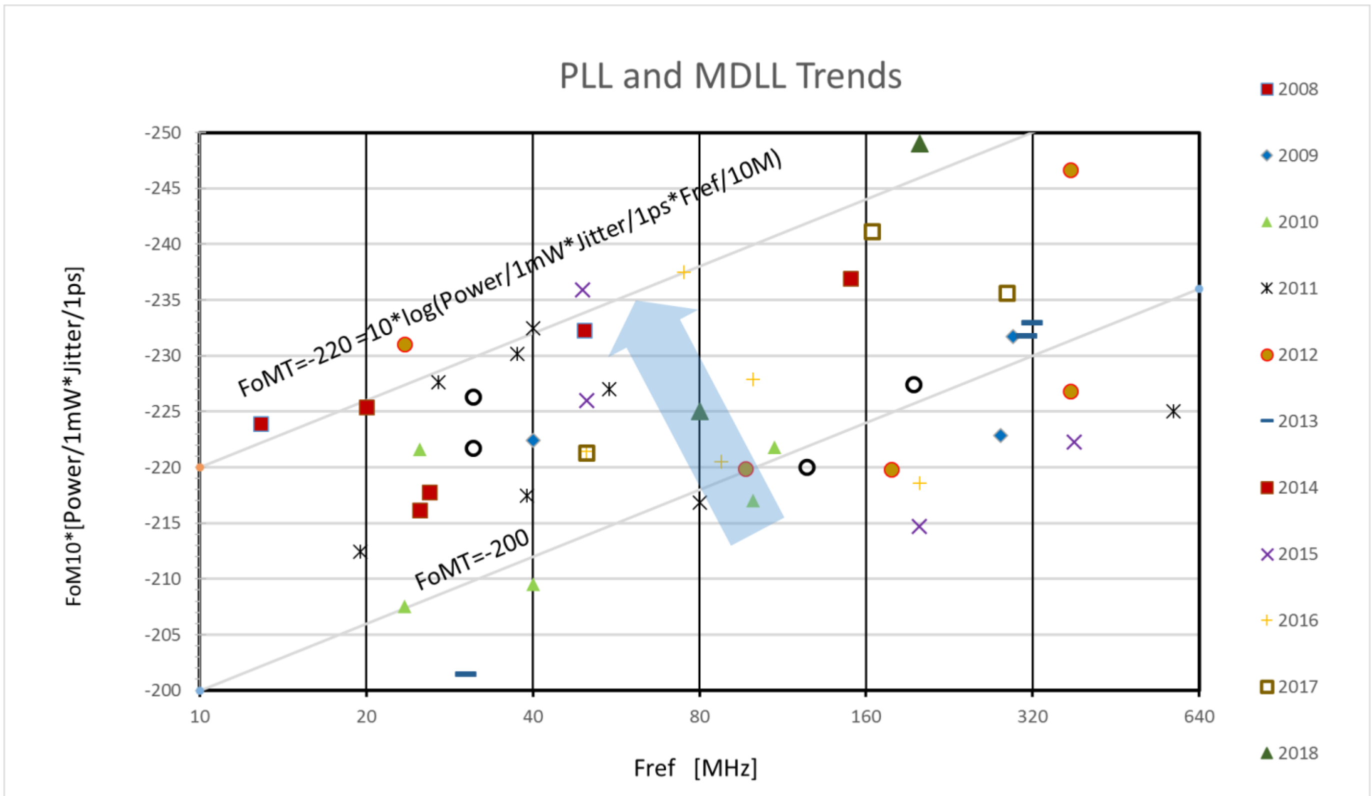

Figure 2. PLL and Multiplying Delay-Locked Loop (MDLL) trends.

Circuits for Hardware Security: With the increasing risk and cost of information theft, hardware-implemented security has become a common circuit component. Though focus on cryptographic implementation continues, cost-effective PUFs (Physically Unclonable Functions) are now a focus area, such as in smart cards and consumer devices. TRNGs (True Random-Number Generators) are also commonly leveraged to strengthen secret key generation in cryptographic applications. Figure 3 illustrates trends in area/bit scaling and bit-error rates for PUFs published recently at ISSCC.

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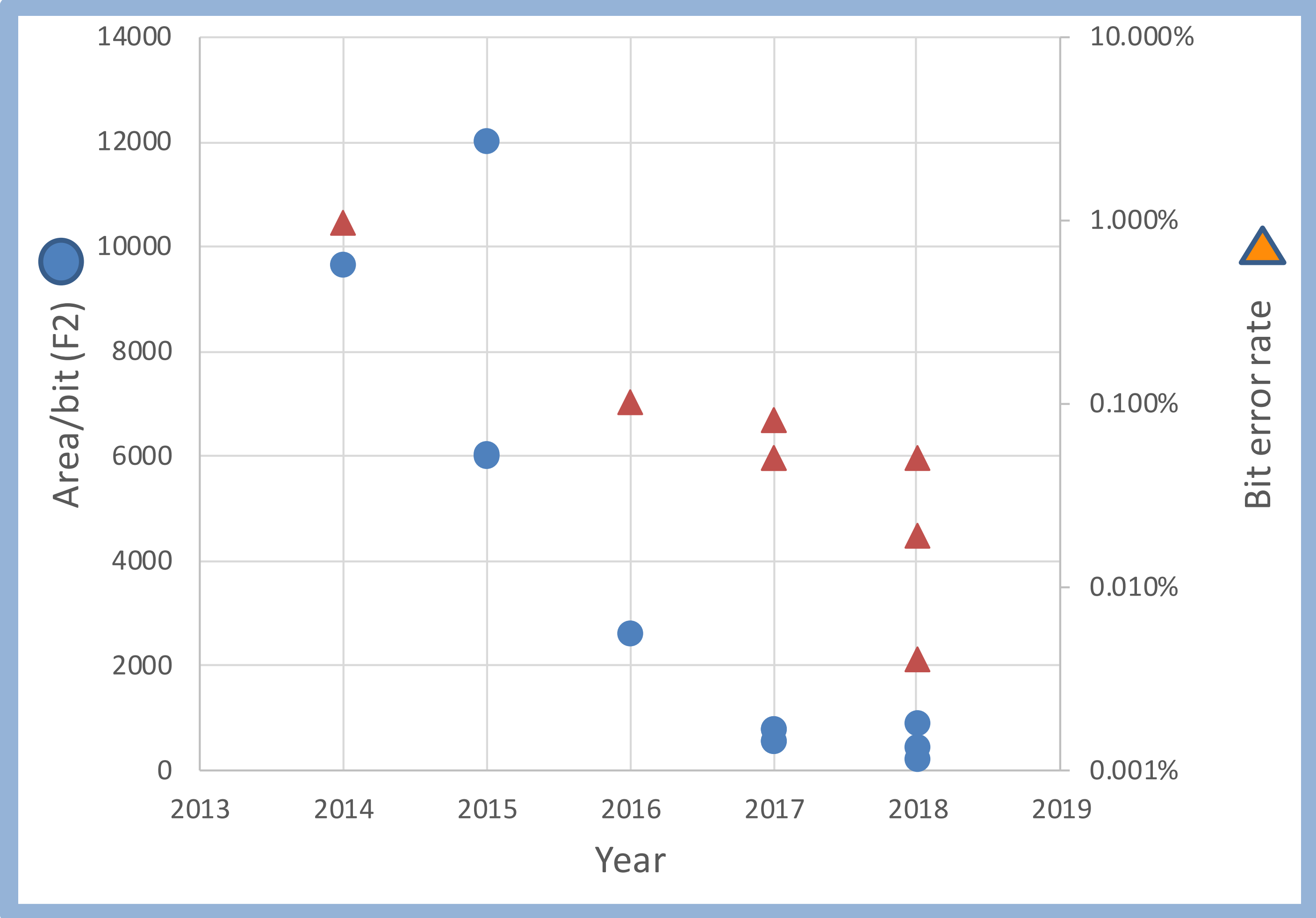

Figure 3. Area/bit and bit-error-rate trends for physically unclonable functions (PUFs).

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Memory – 2018 Trends

Subcommittee Chair: *Leland Chang, IBM, Yorktown Heights, NY, Memory*

The demand for high-density high-bandwidth and low-energy memory systems continues in applications from high-performance computing, to SoCs, to wearables, and IoE. In embedded memory, both record bitcell size SRAM in 7nm and 10nm high-array-density SRAM is shown to be functional at the MByte level. DRAM high-performance memory-interface technologies are enhanced for GDDR6 and HBM; meanwhile record density DRAMs are implemented in 1xnm processes. NAND Flash memory has extended capacity using both bit/cell techniques and number of layers in 3D structures. A new era of compute in memory (CIM) for neural networks is emerging using both SRAM and RRAM. In the meantime, STTRAM progressed to operate at up to 120^0C with 1T1MTJ implementation.

Some current state-of-the-art papers from ISSCC 2018 include:

- A $0.031\mu m^2$ and a $0.026\mu m^2$ SRAM bitcell in 10nm and 7nm, respectively, shown to be functional at a MByte array level.
- A 1Mb 28nm 1T1MTJ STTRAM array with 3.6ns read access time at 120^0C utilizing an offset-cancelled sense amp and in-situ write termination.
- A 16Gb GDDR6 is implemented to operate at 18Gb/s/pin with a per-bit trainable single-ended DFE, ZQ-coded transmitter, and PLL-less clocking.
- A 16Gb LPDDR4X is implemented in a 10nm process with $81mm^2$ die size using in-DRAM ECC, which achieves a data rate of 5Gb/s/pin and self-refresh power of 0.1mW/Gb.
- A 1Tb NAND Flash in 64 stacked layers by using 4b/cell technology with $5.63Gb/mm^2$ areal density.
- A 512Gb 3b/cell 3D flash memory on a 96-word-line-layer technology with string-based start bias control scheme achieves 7% shorter program time.
- Multiple compute in memory implementations for neural networks using SRAM and RRAM.

SRAM: For embedded high-speed applications, SRAM continues to be the memory of choice – from mobile to high-performance servers to internet of everything and compute in memory for neural networks. This year ISSCC 2018 highlights 7nm FinFET bitcells operating at 6GHz and a 10nm SRAM showing $23.6Mb/mm^2$ array density. SRAM arrays are also implemented for product-sum compute in memory operations. Figure1 shows SRAM bit cell area and V_{MIN} scaling trends.

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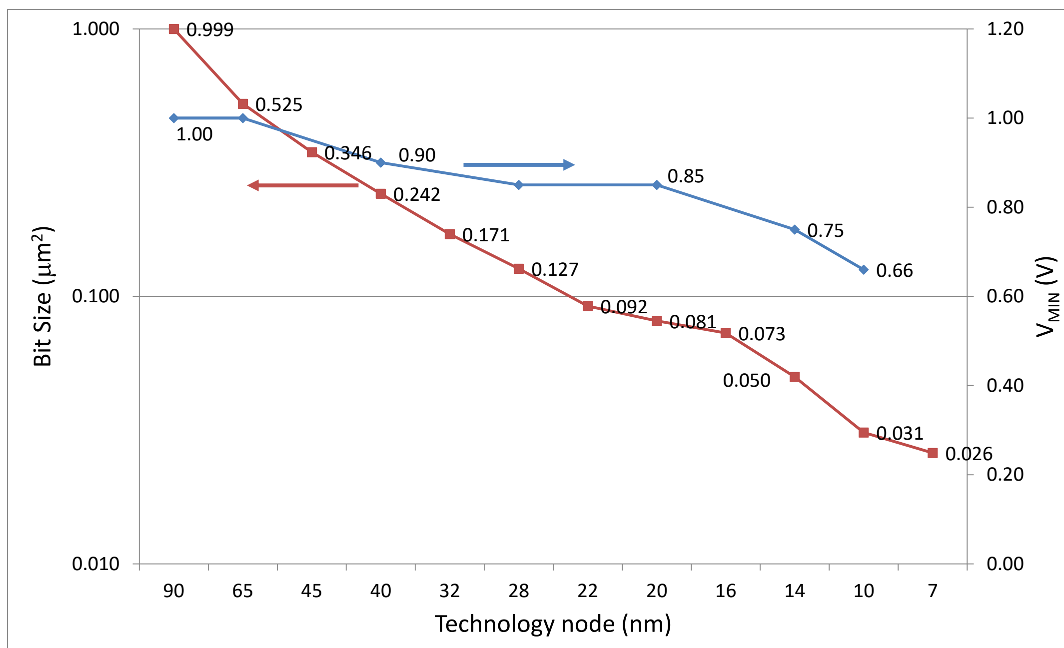

Figure 1 – Bit-cell and V_{MIN} scaling trends for SRAM.

High-Bandwidth DRAM: In order to maintain the optimal memory hierarchy ratio with respect to storage memory, DRAM continues to scale density, form factor, and bandwidth. This year, ISSCC 2018 presents the latest interface-standard benchmarks, including GDDR6, HBM for high-bandwidth, LPDDR4X for low-power applications, and DDR4 for computing with high density. Figure 2 shows DRAM bandwidth scaling over the past decade.

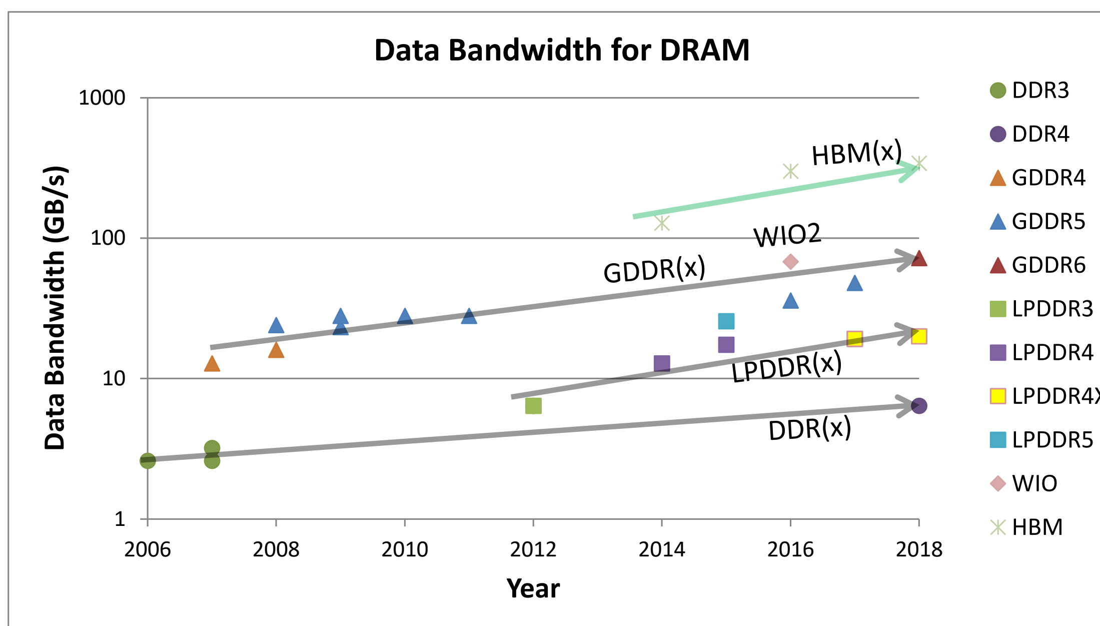

Figure 2 - DRAM data-bandwidth trends.

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Nonvolatile Memories: In the past decade, significant investment has been put into the emerging memories field to find an alternative to floating-gate-based nonvolatile memory. The emerging NVMs, such as phase-change memory (PRAM), ferroelectric RAM (FeRAM), magnetic spin-torque-transfer (STT-MRAM), and Resistive memory (ReRAM), are showing potential to achieve high cycling capability and lower power per bit in read/write operations. Figure 3 highlights 3b/cell(TLC) NAND Flash and 4b/cell(QLC) NAND Flash write throughput. Figure 4 shows a significant increase in NAND Flash capacity from 768Gb to 1Tb at ISSCC 2018. Such high areal densities are achieved through advancements in 3-dimensional vertical bit-cell-stacking technologies.

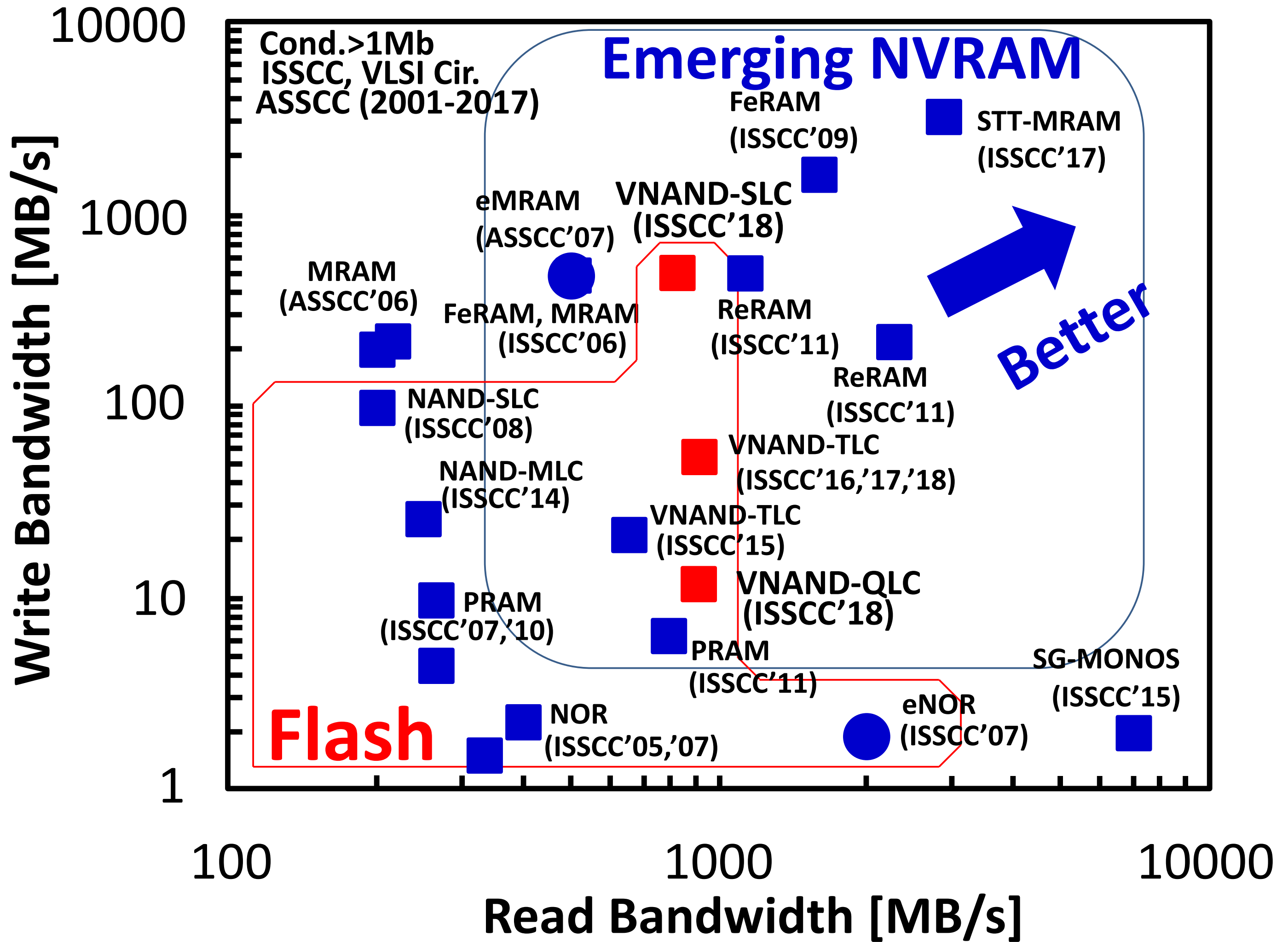

Figure 3 - Read/write bandwidth comparison of nonvolatile memories.

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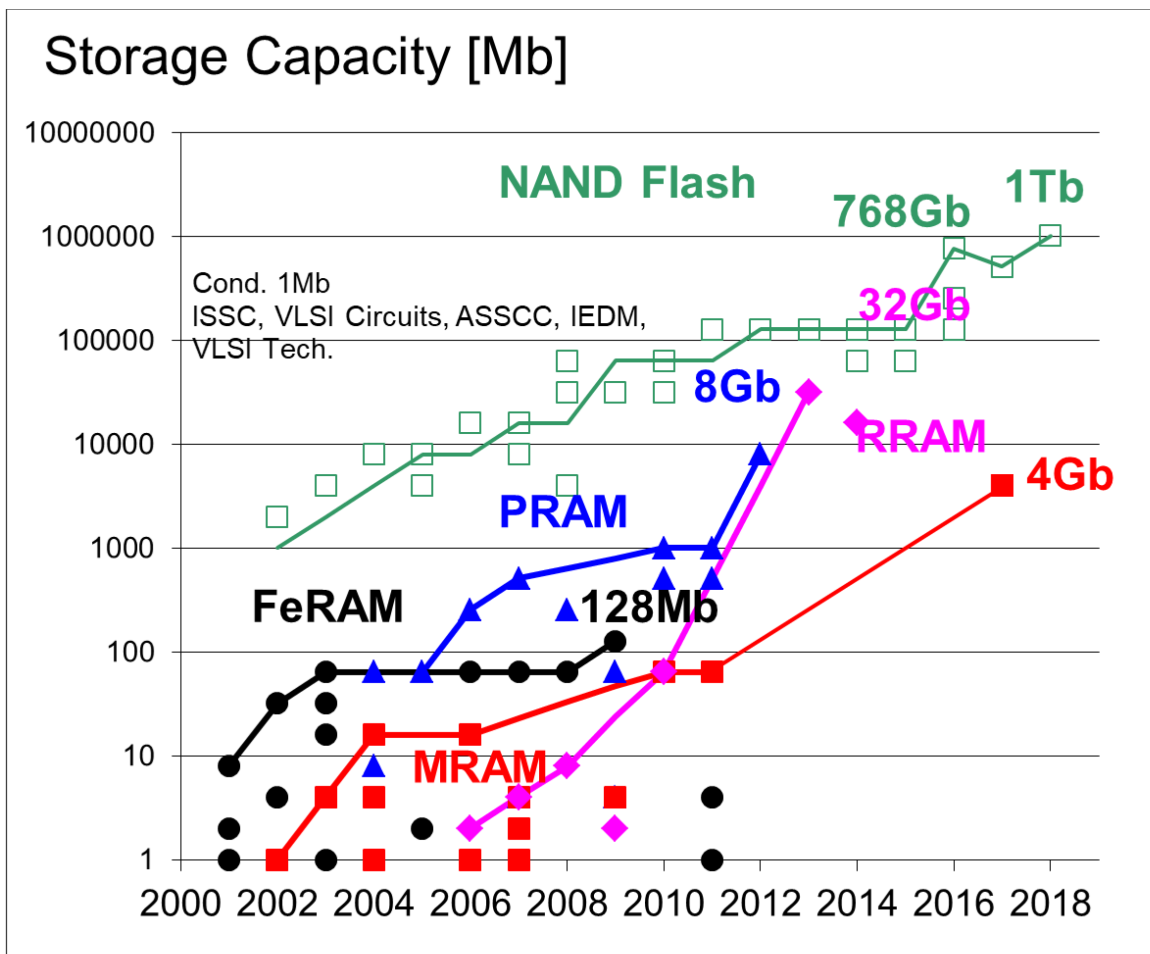

Figure 4 - Memory Capacity Trend of Emerging Nonvolatile Memories

NAND Flash Memory: NAND flash memory continues to advance towards higher density and lower power, resulting in low-cost storage solutions that are replacing traditional hard-disk storage with solid-state disks (SSDs). 3D memory technology has been the mainstream for NAND flash memory in mass-production of semiconductor industries. At ISSCC 2018, a 1Tb 4b/cell achieves 5.63mm^2/Gb areal density and a 512Gb 3b/cell 3D NAND with 96 stacked WL layers will be presented, continuing the trend to satisfy the ever-growing demand for increased density requirements and lower manufacturing costs. Not only higher density, but also higher performance over 57MB/s program throughput and 1.0GB/s read throughput with lower I/O voltage from 1.8V to 1.2V will be presented. Figure 5 shows the observed trend in NAND Flash capacities at ISSCC over the past 15 years.

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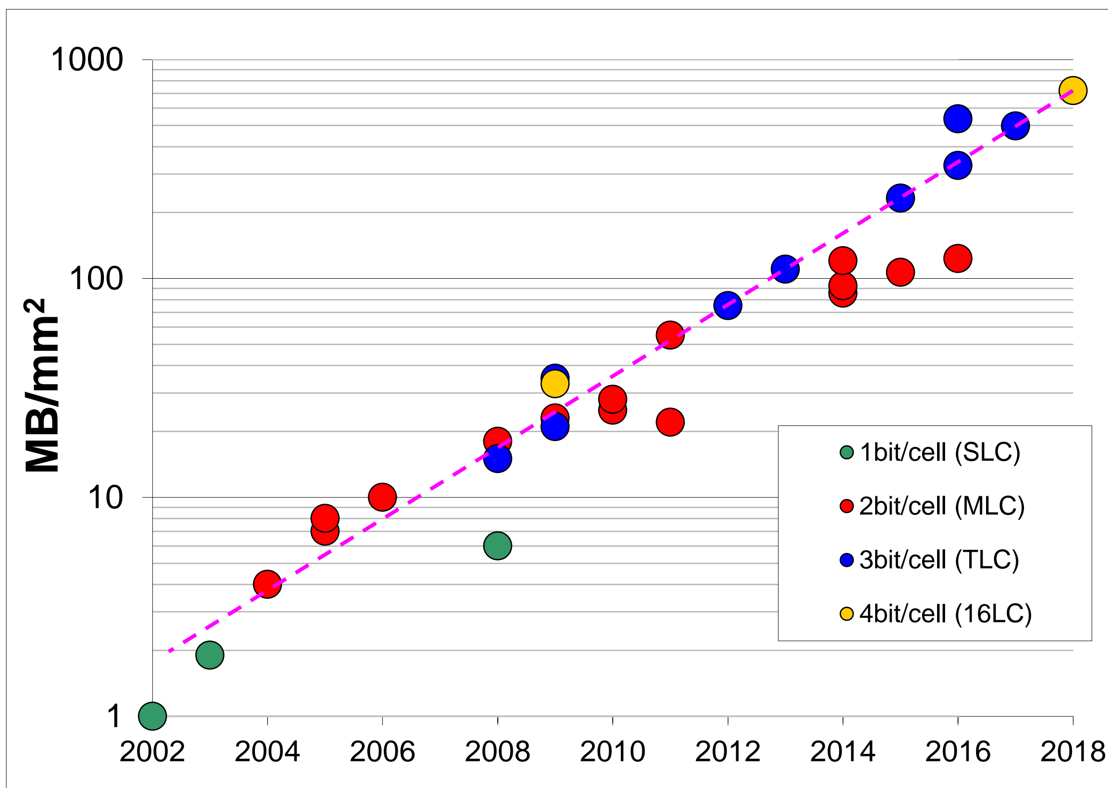

Figure 5 - NAND Flash memory trends.

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HISTORICAL TRENDS IN TECHNICAL THEMES

Innovative Topics

Imagers/MEMS/Medical/Displays Subcommittee

Technology Directions Subcommittee

IMMD – 2018 Trends (Sensors)

Subcommittee Chair: *Makoto Ikeda, University of Tokyo, Tokyo, Japan*

Sensors are a key building block for a wide variety of applications. They collect the data and are an important part of the value chains that are enabling new features. Increasingly, processing is performed at the sensor interface, resulting in ever-more optimized systems.

MEMS inertial sensors (accelerometers and gyroscopes) are key components used in a wide variety of consumer and automotive products, where power consumption and reliability are key requirements. The new FM gyroscope employs rate-chopping to reduce offset drift of the sensor. In addition, fusion of pressure and inertial sensors are shown to enable a personal navigation system for operations in environments without GPS access.

New circuit techniques allow beamforming directly at ultrasound interfaces with reduced power consumption and area. This will enable miniature 3D ultrasound probes.

In an effort to enlarge the application area of touch user interfaces and improve noise immunity, natural handwriting with a stylus is becoming important with a capacitive touch controller. New touch-sensing architectures are being investigated to integrate active stylus and an electrically coupled resonance (ECR) stylus, with both having pressure sensitivity.

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IMMD – 2018 Trends (Medical)

Subcommittee Chair: *Makoto Ikeda, University of Tokyo, Tokyo, Japan*

As illustrated at ISSCC 2018, both sensor and actuator systems for in-body implantable usage continue to evolve toward more robust and energy-efficient operation. New circuit concepts permit recording of weak biopotential signals in the presence of real-life interference and under stringent power and size constraints, paving the way toward autonomous robust systems that combine sensing and actuation as part of a single implantable device. This will allow therapy to be applied directly in closed-loop fashion for treatment of a variety of neurological disorders. Furthermore, technological approaches for multimodal, very-high-density cellular interfacing continue to advance, with new applications in high-throughput drug screening.

The state-of-the-art in biomedical integrated circuits and systems has further advanced this year, at ISSCC 2018 with a larger number of recording channels in neural interfaces (>16K), integration of circuits for combined optogenetics and neurophysiology, increased dynamic range (>90dB), increased common-mode and power supply rejection (>100dB), and improved noise/power efficiency (PEF < 3).

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IMMD – 2018 Trends (Imagers)

Subcommittee Chair: *Makoto Ikeda, University of Tokyo, Tokyo, Japan*

The CMOS-image-sensor business remains one of the fastest-growing segments of the semiconductor industry with double-digit CAGR. Image sensors are required components in most mobile devices, which now include multiple front- and rear-facing cameras. The other applications that continue to drive the demand for image sensors include autonomous driving, smart security, wearables, gaming, VR, AR, IoE, and biomedical.

3D-stacked image sensors have become more popular since they enable increasing on-chip functionality without detracting from image quality. At ISSCC 2018, 6 out of the 10 image sensor papers use a 3D stacking process in order to preserve most of the top layer area for light sensing, while keeping the readout and image-signal-processing circuits on the bottom layer. In one paper, a 14b ADC is stacked under each pixel using a Cu-Cu hybrid bonding technology.

As seen at ISSCC previously, the race to higher resolution and smaller pixels has slowed slightly, but has never stopped. At ISSCC 2018, a 0.9μm pixel with a full-depth deep-trench isolation that reaches a performance level exceeding the current generation 1.0μm pixel in both the saturation level and readout noise will be presented. The broadcasting industry continues to push the array size towards, and beyond, the 8k4k or 33Mpixel resolution, with frame rates exceeding 120fps. At ISSCC 2018, a 33Mpixel 480fps CIS will be presented.

We observe continued development of depth sensors, using either direct or indirect time-of-flight technology, to address the emerging applications in VR, AR, and LiDAR for autonomous driving. Four of the 10 image sensor papers this year at ISSCC 2018 will describe depth-sensing applications. BSI and 3D wafer stacking are now being used. SPADs and SiPDs are being used for direct time-of-flight measurement with extended range imaging up to 200m. Pixel resolution continues to scale for depth sensing beyond 1Mpixel.

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Technology Directions – 2018 Trends

Subcommittee Chair: *Makoto Nagata, Kobe University, Kobe, Japan*

Technology innovations bring the promise of enabling completely new system functionalities or substantially greater efficiency of existing ones. It is significant that harnessing such innovations for the solution of real-world problems requires thinking about technologies in the context of systems. Thus, now, with a focus on silicon engineering in the social world, trends in Technology Directions emphasizes biomedical systems and in-memory computing for machine-learning applications.

Biomedical systems: The human body is an incredibly complex system, yet innovations in medical devices and systems are allowing us to dive deeper into the dynamic inner-workings of the body. Over the past decade, the trend in biomedical-integrated-circuit development has been primarily on building sensors and actuators, and their corresponding electronic instrumentation, that interact with the body in the electrical domain: for example, circuits used for measurement of ECG, EEG, EMG, and so on, or stimulation of neural tissues have all been explored in detail at ISSCC 2018. This trend is continuing, but now the research focus is on enhancing system-level functionality, for example through multi-sensor interfaces that also infer hemodynamic processes, through ultra-miniaturized single-channel implants co-integrated with optical features, or through integration of in-sensor machine learning processors to help classify and use data in closed-loop systems. Machine learning can, in some cases, be an impactful technique to reduce the amount of data that needs to be wirelessly-transmitted, potentially reducing overall system power due to lower radio energy costs.

If in-sensor processing of data is infeasible, either due to energy or other application-level constraints, then wireless transmission of data must be extremely energy efficient so as to minimize the size of the energy source (such as a battery, energy harvester, and so on) in order to fit anatomical size constraints. As a result, another trend in biomedical systems is the design of wireless communication circuits that operate extremely efficiently in the presence of biological tissue. Examples include innovations in body-coupled communication systems that operate in the GI tract as part of a multi-camera capsule endoscope, and transcranial links that operate up to 200Mb/s.

Beyond sensing of physical and electrophysiological parameters, an emerging trend in biomedical systems is to measure physiochemical parameters. Biosensors that respond to glucose, electrolytes, or gasses, can offer new views into the dynamic behavior of freely-behaving biological subjects. In wearable and implantable applications, trends include enabling such functionality at nW-level power consumption, or via bio-energy harvesting that exploits the energy naturally present in many metabolites to be sensed. In very small systems, it may be possible to forgo conventional DC-DC converters if the voltage of biofuel cell energy harvesters is sufficiently large, or if circuits are specifically designed to operate at low supplies (such as 0.3V). In stationary applications, trends include increasing the resolution and dynamic range of correction circuitry to support long-term accurate operation.

Mixed-signal and in-memory computing for machine-learning applications: Machine-learning applications are having broad and substantial impacts on increasing facets of society. In many cases, the applicability of such systems is limited by the energy they require and the performance they can achieve. Addressing these limitations has become a critical trend in Technology Directions. To overcome the limitations faced by traditional architectures, researchers in this area are taking advantage of innovations in unconventional architectures and emerging technologies. This has driven renewed interest and perspectives on mixed-signal computation. Unlike before, where mixed-signal computation was primarily driven by its energy-efficiency in the regime of low-resolution computation, now motivations at the architecture level are raising even greater promise of mixed-signal computation. This is particularly important in the area of memory access, which has been one of the main limitations of current machine-learning systems and sensing, and that represents one of the most vital sources of data on which machine-learning systems are being applied. Consequently, a key trend in Technology Directions has been mixed-signal computation in memory arrays and near sensors. This requires a confluence of circuits, architectures, and algorithms, opening new opportunities and perspectives through which integrated systems will impact society.

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In line with these trends, ISSCC 2018 will feature two sessions representing the latest technological innovations in biomedical systems: One will include an invited presentation on the impact of sensors and electronic systems for food production and agricultural applications. Another will emphasize in-memory computations for machine-learning applications.

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A paper number mentioned in this section follows the convention S.P, where S is the session number and P is the paper number. For example 23.2 will be the second paper in the twenty-third session. You can refer back to the TECHNICAL SESSION OVERVIEWS in this Press Kit for additional details on any given paper. Some of the papers will also be available in the "not-so-technical" SESSION HIGHLIGHTS part of this Press Kit. All sessions and papers are in ascending order in both the Session Overviews and the Session Highlights sections of the Press Kit.

Technical Topics Mapped to Papers

Technical Topic	All papers in the following Sessions
Communication Systems includes Wireless, RF, and Wireline Subcommittees	**4, 6, 9, 15, 16, 23, 25, 26, 28**
Analog Systems includes Analog, Power Management and Data Converter Subcommittees	**3, 8, 14, 19, 22, 24, 27**
Digital Systems includes Memory, Digital Circuits, and Digital Architectures and Systems Subcommittees	**2, 11, 12, 13, 18, 20, 30, 31**
Innovative Topics includes Imagers/MEMS/Medical Devices/Displays and Technology Directions Subcommittees	**5, 7, 10, 17, 21, 29, 30, 31**

Selected Presenting Companies/Institution Mapped to Papers

Chart 4.1

Affiliation	Paper Numbers
Acacia Communications	16.7
Air Force Research Laboratory	27.9
AMD	2.4
ams AG	19.8
Analog Devices	4.1, 9.3, 14.7, 17.4
Arizona State University	31.5
ARM	2.7
Axalume	16.1
Bell Laboratories	4.6
Broadcom	4.2, 15.3, 16.8, 22.2
Brookman Technology	5.6

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California Institute of Technology	10.7, 26.3
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