2015

PRESS KIT

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ISSCC VISION STATEMENT

The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and use to maintain technical currency, and to network with leading experts.

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TABLE OF CONTENTS

1. PREAMBLE
   1.1. FAQ on ISSCC
   1.2. About ISSCC 2015
   1.3. Plenary Session

2. TECHNICAL SESSION OVERVIEWS
   Features 206 papers in 27 sessions

3. NOT-SO-TECHNICAL HIGHLIGHTS
   Features highlights from selected papers

4. INDEX
   4.1. Technical Topics mapped to papers
   4.2. Selected Presenting Company/Institution mapped to papers

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1. PREAMBLE

1.1 FAQ on ISSCC

What is ISSCC?
ISSCC (International Solid-State Circuits Conference) is the **flagship** conference of the IEEE Solid-State Circuits Society. According to the SIA, the Semiconductor industry generated US$290 billion in sales in 2012 and ISSCC continues to be the premier technical forum for presenting advances in solid-state circuits and systems.

Attendance at ISSCC 2015 is expected to be around **3000**. Corporate attendees from the semiconductor and system industries typically represent around **60%** of the attendees. The **62nd ISSCC** will be held at the San Francisco Marriott Marquis on February 22-26, 2015. ISSCC 2015 will kick off with three exciting plenary speakers on Monday, February 23, 2015:

- **Kinam Kim**, President, Samsung Electronics, Kiheung, Korea
- **Willy Sansen**, Professor Emeritus, Katholieke Universiteit Leuven, Leuven, Belgium
- **Sehat Sutardja**, Chairman and CEO, Marvell Technology Group, Santa Clara, CA

What Technical Topics are covered at ISSCC?
The conference covers a spectrum of design approaches in various technical areas and advancements broadly categorized into: (1) Communication Systems, (2) Analog Systems, (3) Digital Systems, and (4) Innovative Topics such as micro-machines and MEMS, imagers, sensors, biomedical devices, as well as forward-looking solutions that may be at least 3 years away from becoming commercial.

Who selects papers to present at ISSCC?
Over 600 submissions are received every year for review by an international team of over 150 scientific and industry experts from the Far-East, Europe and North America. These experts are organized into 10 subcommittees that cover the 4 broad areas described earlier:

- **Communication Systems** includes Wireless, RF, and Wireline subcommittees
- **Analog Systems** includes Analog and Data Converters subcommittees
- **Digital Systems** includes Memory, Energy-Efficient Digital and High-Performance Digital subcommittees
- **Innovative Topics** includes Imagers/MEMS/Medical Devices and Technology Directions subcommittees

What companies are presenting this year at ISSCC?
Companies presenting at the conference include Samsung, Toshiba, IBM, Intel, AMD, Oracle, Qualcomm, ARM just to name a few. A more complete list can be found in the Index.

Are there educational sessions?
ISSCC 2015 features the following educational sessions:

- Ten Tutorials (targeted toward participants that are starting to learn about certain topics)
- Six Forums (targeted toward information sharing amongst experts)
- One Short course (targeted toward education in an annually important evolving field)

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Anything else other than technical and educational sessions?
Here is a complete list of activities at ISSCC 2015:

- Plenary presentations
- Technical sessions (27 distinct sessions)
- Six evening sessions and panels
- Educational sessions featuring:
    - Ten Tutorials
    - Six Forums
    - One Short Course
- Student Research Preview
- Demonstration sessions from academia and industry
- Networking social events
- Author interview sessions
- Women's networking event
- Various university alumni events
- Book display

How do I use this Press Kit?
The Press Kit provides a PREAMBLE section that features this FAQ and other general information. The kit also includes a TECHNICAL OVERVIEW of all 206 papers in all 27 technical session, as well as less technical HIGHLIGHTS of selected papers in every technical session. The Kit includes an INDEX section that maps (a) the 27 technical sessions to the 4 Technical Topics, (b) the 206 papers to their corresponding presenting companies and institutions.

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1.2 ABOUT ISSCC 2015 – Silicon Systems – Small Chips for Big Data

Big Data generated by the Internet of Things (IoT), healthcare, and the web, is changing our lifestyle and our society. Small silicon chips are enabling this change through data sensing, gathering, processing, storing, and networking through wireless and wireline connectivity. Recent silicon-system technologies, including ultra-low-power systems, high-performance circuits and systems, wireless power and data transmission, and 3D IC structures, will open the door to Big-Data applications. Moreover, Big-Data applications such as healthcare, machine learning, and sensor systems, will challenge designers to consider new system architectures requiring advances in circuits and technology. ISSCC 2015 showcases novel circuit and system solutions that open new vistas for society, with opportunities for new lifestyles, all driven by Big-Data technology.

1.3 PLENARY SESSION (Session 1)

The plenary session on the morning of Monday, February 23, 2015, will feature three invited speakers:

- **Kinam Kim**, President of Samsung Electronics, will present "Silicon Technologies and Solutions for the Data-Driven World"
- **Sehat Sutardja**, Chairman and CEO of Marvell Technology Group, will present "The Future of IC Design Innovation"
- **Willy Sansen**, Professor Emeritus at the Katholieke Universiteit Leuven, will discuss "Analog CMOS from 5 Micrometer to 5 Nanometer"

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ISSCC 2015
SESSION OVERVIEWS

CONDITIONS OF PUBLICATION

PREAMBLE

The Session Overviews to follow serve to capture the context, highlights, and potential impact, of the papers to be presented in each Session at ISSCC 2015 in February in San Francisco

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- That you will provide a courtesy PDF of your excerpted press piece and particulars of its placement to press_relations@isscc.net

FOOTNOTE

- From ISSCC's point of view, the phraseology included in the box below captures what we at ISSCC would like your readership to know about this, the 62nd appearance of ISSCC, on February 22nd to the 26th, 2015, in San Francisco.

This and other related topics will be discussed at length at ISSCC 2015, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 22-26, 2015,
at the San Francisco Marriott Marquis Hotel.

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Session 2 Overview: *RF TX/RX Design Techniques*

RF SUBCOMMITTEE

Session Chair: *Ehsan Afshari, Cornell University, Ithaca, NY*
Session Co-Chair: *Minoru Fujishima, Hiroshima University, Hiroshima, Japan*

Subcommittee Chair: *Andreia Cathelin, STMicroelectronics, Crolles, France*

Wireless communication at radio frequencies has made our world a smaller place by enabling us to share ideas and concerns regardless of our geographical location. Innovation in this field makes the technology more accessible and adds more functionality to the existing products. Papers in this session showcase some of the recent advances in RF transmitter and receiver building blocks. The first four lower the noise of receivers and increase their linearity. The next six papers present methods to increase the PAE and output power of integrated power amplifiers for the transmitter blocks.

- In Paper 2.1, UCLA and Broadcom present an inductorless receiver with an integrated RF ring VCO in 28nm CMOS. Their work achieves a 2dB NF across the 0.3-to-3GHz band, while dissipating 55mW at 2GHz.

- In Paper 2.2, imec, Murata, and HiSilicon present an electrical-balance duplexer achieving state-of-the-art linearity and insertion loss performance in an RF CMOS SOI process.

- In Paper 2.3, Nanyang Technological University, the University of Electronic Science and Technology of China and Singapore University of Technology and Design present an SPDT switch that operates from 130 to 180GHz with 3.3dB insertion loss and 23.7dB isolation in 65nm CMOS.

- In Paper 2.4, the University of Macau and Universidade de Lisboa demonstrate a receiver with a 1.5-to-2.9dB NF, +13dBm OB IIP3 and <-16dB S_{11} over a 0.1-to-1.5GHz frequency range. It is fabricated in a 65nm CMOS process with an area of 0.028mm^2, consuming 11mW.

- In Paper 2.5, Nanyang Technological University shows a 2-to-6GHz power amplifier that achieves 19%-to-28.4% PAE, 20.1-to-22.4dBm P_{SAT}, 17.81-to-20.73dBm P_{1dB}, <±2° AM-PM, 23.6±0.8dB gain, and 9.31-to-11.31dBm output power for 256QAM signals with EVM<-32dB.

- In Paper 2.6, The Technical University of Aachen presents a class of power amplifiers, termed as Class-O, which provides high linearity and low voltage stress on the power-amplifying CMOS devices.

- In Paper 2.7, Samsung Electronics shows a hybrid supply modulator that enhances the dynamic range of ET operation by employing adaptive control of both supply voltage and bias current in the linear stage.

- In Paper 2.8, Georgia Institute of Technology and Toshiba present a broadband digital power amplifier with hybrid Class-G Doherty efficiency enhancement in 65nm CMOS. The PA achieves 26.7dBm peak power with 40.2% drain efficiency at 3.71GHz.

- In Paper 2.9, the University of Southern California presents a mm-Wave digital power amplifier with dynamic load modulation using variable impedance transmission lines in a 0.13µm SiGe process. It achieves a peak output power of 28.9dBm with 18.4% peak PAE at 46GHz.

- In Paper 2.10, STMicroelectronics, the University of Bordeaux and CEA-LETI-MINATEC present a PA linearization and efficiency enhancement technique using 28nm CMOS UTBB FD-SOI. In high-gain mode, the 3-stage 60GHz PA reaches 35dB gain and in linearized mode it achieves 21% PAE at 18.2dBm P_{1dB} while consuming 74mW.

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Session 3 Overview:
Ultra-High-Speed Wireline Transceivers and Energy-Efficient Links

WIRELINE SUBCOMMITTEE

Session Chair: *Ken Chang, Xilinx, San Jose, CA*
Session Co-Chair: *Shunichi Kaeriyama, Renesas Electronics, Tokyo, Japan*

Subcommittee Chair: *Daniel Friedman, IBM, Yorktown Heights, NY, Wireline Subcommittee*

Smart phones and their social apps drive tremendous growth of Internet and big data infrastructure. In turn, this spurs the insatiable need for data communication bandwidth between chips. In this context, wireline transceivers that push the limits imposed by process technology—in terms of data-rate, energy efficiency, and ability to support bursty traffic—are extremely critical. This session opens with the presentation of 3 complete 28+Gb/s transceivers addressing the challenges of high channel loss (up to 40dB) and multi-standard support. Two papers then address PAM4 signal generation/transmission for future advanced standards at higher data rates. The session concludes with a paper describing a dynamically enabled digital equalizer employed within an ADC-based link, a paper pushing the limits of rapid on/off operation in burst-mode links, and a final paper exploring calibration techniques enabling aggressive transceiver voltage scaling.

- In Paper 3.1, Broadcom presents a 28Gb/s multi-standard transceiver with data rates up to 28Gb/s in 28nm CMOS. The receiver has a linear equalizer and a 14-tap DFE, while the transmitter uses a source-series terminated driver with a 5-tap FFE. The transceiver compensates a 40dB loss backplane channel at 25.78Gb/s; each 0.62mm^2 TX/RX consumes 295mW.

- In Paper 3.2, Hitachi presents a multi-standard backplane transceiver that uses a 36-tap DFE with a pattern-capture CDR and a pattern-matching adaptive equalizer to cancel reflections due to backplane connectors. The 28nm CMOS chip operates from 0.3 to 28.05Gb/s over a 40dB loss backplane with 2 connectors.

- In Paper 3.3, Xilinx presents a fully-adaptive 0.5-to-32.75Gb/s transceiver embedded in a 20nm CMOS FPGA. The receiver uses a 15-tap DFE while the clocking circuits consist of fractional-N LC PLLs and poly-phase IQ generation circuits. The transceiver achieves BER <10^{-15} over a 10.4 dB loss short-reach channel at 32.75Gb/s and a 27dB loss backplane at 28Gb/s.

- In Paper 3.4, Broadcom presents a 36Gb/s PAM4 transmitter with a clock-generation circuit. The transmitter is based on an 18GS/s 8b DAC achieving 800mV$_{ppdiff}$. Implemented in 28nm CMOS technology, the measured SFDR is 52 and 43dB at 0.7 and 8GHz outputs, respectively. The DAC-based transmitter consumes 84mW from 1 and 1.5V power supplies.

- In Paper 3.5, Intel presents a 0.0279mm^2 NRZ/PAM4 transmitter (TX) operating from 16 to 40 Gb/s in 14nm tri-gate CMOS. The TX includes a feed-forward charge-injected 4:1 serializer and quarter-rate clocking and clock calibration. The TX consumes 195 and 518mW at 28 and 40Gb/s, respectively, in NRZ mode and consumes 141 and 168mW at 33.6 and 40Gb/s in PAM4 mode.

- In Paper 3.6, Texas A&M University presents a 65nm 10Gb/s hybrid ADC-based receiver employing a 3-tap analog FFE embedded inside a 6b asynchronous SAR ADC, as well as a per-symbol dynamically-enabled digital equalizer. Applying the latter technique to the digital 4-tap FFE and 3-tap DFE results in ~30mW savings on a 36.4dB loss channel.

- In Paper 3.7, University of Illinois at Urbana-Champaign presents a 7Gb/s embedded clock burst-mode transceiver to achieve energy proportional operation. Using a fast-locking LC PLL the design achieves effective throughput scaling over a 100× range (7Gb/s to 70Mb/s) while scaling the power by 44× (63.7mW to 1.43mW).

- In Paper 3.8, University of Illinois at Urbana-Champaign presents a source-synchronous transceiver with aggressive supply voltage scaling to achieve energy efficiency ranging from 0.29 to 0.58pJ/b at data rates of 1 to 6Gb/s, as the supply voltage varies from 0.45 to 0.7V. Phase-spacing errors resulting from device mismatches are corrected using self-calibration.

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Session 4 Overview: *Processors*

HIGH-PERFORMANCE DIGITAL SUBCOMMITTEE

Session Chair: *Atsuki Inoue, Fujitsu Labs., Kanagawa, Japan*
Session Co-Chair: *Jinuk Luke Shin, Oracle Corporation, Redwood Shores, CA*

Subcommittee Chair: *Stefan Rusu, Intel, CA, High-Performance Digital Subcommittee*

As compute power is increasingly migrating to large data centers and the cloud, microprocessors face progressively more stringent design constraints. This year's processor session introduces three new "big iron" processors in 22nm/20nm technology providing higher performance and power efficiency. Increasing core counts and cache sizes, with adaptive power management techniques, are applied to optimize performance/W. A high-density microserver computing node is optimized for Big Data and shows its capability in handling a large number of threads. For future intelligent computing, such as deep learning and inference, a specialized processor is demonstrated. Other papers in this session describe adaptive techniques, as well as design optimizations to improve throughput and energy efficiency.

- In Paper 4.1, IBM presents their 678mm^2 System z microprocessor chip implemented in IBM's 22nm SOI, high-κ metal-gate technology with 17 layers of wiring and functional thru 5GHz. The design comprises 8 dual-threaded cores with private 4MB eDRAM L2 cache and a 64MB unified eDRAM L3 cache, joined by a single global clock mesh and connected to high-bandwidth memory, SMP, and embedded PCI IO links.

- In Paper 4.2, Oracle introduces the SPARC M7 processor with 32 S4 cores and 1.6TB/s bandwidth 64MB L3 cache to deliver more than 3.0× throughput performance over its predecessor. The chip, fabricated in 20nm, features an on-chip network (OCN) with 0.5TB/s data bandwidth, 280 SerDes lanes with 18Gb/s line rate and 1TB/s total bandwidth, and adaptive clocking scheme to deliver 2× supply noise guard-band reduction.

- In Paper 4.3, Oracle describes the power management system of the SPARC M7 processor. It comprises 48 on-die digital dynamic power meters, 16 temperature sensors, and a configurable hardware proportional feedback controller which directs actuation techniques, including clock cycle skipping and DVFS, to optimize performance by 17% on a power-constrained workload.

- In Paper 4.4, IBM demonstrates a 36W density-optimized, hot-water cooled microserver compute node based on a 1.8GHz CPU with 48GB DDR3 DRAM achieving peak memory bandwidth of 43.2GB/s. 128 of such nodes are combined in a 34.7L 2U rack for a total of 6TB of memory at 159GB/s/L, along with 10Gb/s Ethernet, SATA, and USB.

- In Paper 4.5, Intel's next-generation Xeon processor features 18 dual-threaded 64b Haswell cores, 45MB L3 cache, 4 DDR4-2133MHz memory channels, 40 8GT/s PCIe lanes and 60 9.6GT/s QPI lanes to achieve a 33% performance boost. The processor has 5.56B transistors on a 22nm tri-gate CMOS die measuring 663.5mm^2. Fully integrated voltage regulator (FIVR) technology enables per-core p-states and independent uncore frequency scaling.

- In Paper 4.6, KAIST presents a 213.1mW, battery-powered processor with 4 deep learning, 2 deep inference cores, and a true random number generator. Manufactured in 65nm CMOS with 3.75M transistors and 8 wiring layers on 10mm^2, it achieves 411.3GOPS peak performance at 200MHz, taking ~20ms for object recognition at 640×480 resolution.

- In Paper 4.7, Intel presents an adaptive and resilient register file with in-situ timing margin and error-detection techniques to tolerate within-die voltage droop, temperature and aging. The chip demonstrates 409GOPS/W operation in 22nm tri-gate CMOS to achieve 21% throughput and 67% energy-efficiency improvement with 6.4-to-12.8% area and 0.2-to-0.3% power overheads.

- In Paper 4.8, AMD presents their next-generation APU, Carrizo, which includes the latest x86 core, Excavator. Implemented in a 28nm HKMG process, the SoC occupies 244.62mm^2 with more than 3.1B transistors. The core realized a 23% area reduction and a 40% power reduction compared to the previous core design. The architectural improvements and power management innovations enable a reduction of typical energy use by more than 50%.

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Session 5 Overview: *Analog Techniques*

ANALOG SUBCOMMITTEE

Session Chair: *Xicheng Jiang, Broadcom, Irvine, CA*
Session Co-Chair: *Ed van Tuijl, University of Twente, Enschede, The Netherlands*

Subcommittee Chair: *Axel Thomsen, Silicon Laboratories Inc. Austin, TX, Analog*

This year's session on Analog Techniques continues to defy simple categories. This session illustrates the diversity and vigor of modern analog circuitry. The rise of wearable devices and Internet of Things (IoT) leads to the emergence of nano-power designs of references, oscillators and many other blocks. New frontiers of precision, power, and performance are established.

- Paper 5.1 from Analog Devices presents an auto-zero and chopper operational amplifier with 6.8nV/√Hz PSD in 0.18μm BCDMOS. The chopper op-amp employs 800kHz interleaved clocks, moving the majority of the switching PSD up to 4.8MHz, above the op-amp's unity gain frequency of 3.2MHz. The maximum input bias current is 200pA. It achieves 152dB CMRR and 1.2V/μs slew rate.

- Paper 5.2 by Delft University of Technology presents a ΔΣ ADC with an improved capacitively-coupled high voltage chopper. It achieves ±30V input common-mode voltage range, 110dB SNR and 8μV maximum offset. The sensing AFE consumes 505μW from a 5V supply.

- Paper 5.3 by National Taiwan University presents a continuous two-channel capacitively-coupled instrumentation amplifier using an orthogonal frequency chopping technique and only one active amplifier. It achieves 26nV/√Hz input-referred noise, –83.2dB crosstalk and consumes 27μA from a 3V supply.

- Paper 5.4 by PsiKick Inc. presents a 32nW bandgap reference from a 0.5V supply voltage. It achieves 75 ppm/°C over a temperature range of 0 to 80˚C and 3% untrimmed 3σ process variation.

- Paper 5.5 by University of Twente presents a 450MHz inverter based, 3rd-order Butterworth gm-C filter in 28 nm UTBB FD-SOI technology. The cut-off frequency and filter shape are kept constant over a supply ranging from 0.7V-to-1V, while maintaining linearity above 1dBV without any requirement for Q-tuning and supply voltage turning. It achieves 6.1nV√Hz input noise, and dissipates less than 5.6mW.

- Paper 5.6 by Georgia Institute of Technology presents a fully digital LDO that uses adaptive control and fine grained clock gating to enable >90% current efficiency across a 50× load current range. The design also introduces a technique to enable 8× reduction in transient time in response to large voltage droops.

- Paper 5.7 by Pohang University of Science and Technology presents a bandgap reference circuit with a PTAT generated by leakage current. No start-up circuit is needed. The BGR is fabricated in 0.35μm CMOS and consumes 29nW from a 1.4V supply.

- Paper 5.8 by Infineon Technology presented a digitally assisted single-point-trim CMOS bandgap reference. The key idea is to keep the analog bandgap core simple and only compensate non-PTAT related effects by using chopping techniques. A 3σ inaccuracy of ±0.08% from –40°C to +120°C is achieved. The temperature drift is 7ppm/°C.

- Paper 5.9 by Texas Instruments presents a 24MHz crystal oscillator and a 31.25kHz derived sleep timer for a single crystal wireless node application. A dedicated state machine enables mode transitions without losing clock pulses. It achieves 9ppm/V of frequency variation with voltage and consumes 37μW in sleep mode.

- Paper 5.10 by Institute of Microelectronics Singapore presents a 4.7MHz CMOS reference clock oscillator for SoCs with severely digital noise contaminated supply and ground. It employs a fully differential supply- and ground-regulating frequency-locked loop architecture, a differential period detector with a supply-insensitive period reference, and a differential integrator generating a virtual ground. It achieves –22dB power-supply-noise rejection and consumes 53μW from a 1.7V supply.

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Session 6 Overview: *Image Sensors and Displays*

IMMD SUBCOMMITTEE

Session Chair: *Yusuke Oike, Sony, Atsugi, Japan*
Session Co-Chair: *Young-Sun Na, LGE, Seoul, Korea*

Subcommittee Chair: *Makoto Ikeda, University of Tokyo, Tokyo, Japan, IMMD Subcommittee*

The session presents recent advancements in the field of image sensors and capacitive touch-sensing displays. The session starts with 3 papers on image sensors, including demonstrations of a back-illuminated stacked image sensor with highly parallel multi-sampling ADCs, the first 35mm-format image sensor for 8K video, and a low-power image sensor with a switchable "always-on" mode for mobile and wearable devices. The next 2 papers present a high-speed burst-mode image-acquisition system for scientific phenomena, and an event-driven motion detection system that uses in-pixel non-volatility analog memory for security applications. The latter part of the session presents recent achievements in the area of capacitive touch-sensing displays. This includes the first system where passive/active styluses and multi-fingers can simultaneously touch a 60-inch display. Another paper presents a system where touch is extended into to the 3rd dimension for mobile applications. A 6b-resolution pen pressure sensor that uses a passive resonant stylus is introduced that can replace conventional costly Electro-Magnetic-Resonance-based touch systems.

- In Paper 6.1, Sony presents a 1/1.7-inch 20Mpixel back-illuminated stacked CMOS image sensor. The sensor achieves 1.3e-rms random noise with multiple sampling using double 12b ADCs at 16Mpixel 120fps readout with visually lossless data compression in addition to 20Mpixel 30fps readout.

- In Paper 6.2, NHK Science & Technology Research Laboratories and Forza Silicon present a 133Mpixel 60fps 12b image sensor for 8K video. The pixel size in 0.18μm technology is 2.45×2.45μm^2. Front-end multiplexing analog readout circuitry and column-parallel successive approximation register ADCs are used.

- In Paper 6.3, Samsung presents an always-on image sensor that enables smart sensing in addition to a photograph-shooting mode. Switchable always-on and photo-shooting modes are implemented using dynamic voltage-scaling and reconfigurable ADC circuits. The sensor has 640×480 pixels and consumes 45.5μW at 15fps in the always-on mode.

- In Paper 6.4, Shizuoka University presents a CMOS image sensor fabricated in a 0.11μm process with 5×3 apertures. The sensor performs single-shot and burst-readout image acquisition at a frame rate of 200Mfps employing image reproduction based on compressive sensing.

- In Paper 6.5, Semiconductor Energy Lab and the University of Tokyo propose a 240×160-pixel vision sensor with a motion-capturing function. The sensor has in-pixel non-volatile analog memory employing 0.5μm CAAC-IGZO FET/0.18μm p-ch Si FET technology to obtain differential data in a reference frame. It consumes 25.3μW at 60fps in a motion capture mode.

- In Paper 6.6, Sharp presents a mutual capacitance touch-sensing architecture that achieves multiple active/passive styluses and multi-finger touch sensing at the same time through 60-inch and 13-inch displays, respectively.

- In Paper 6.7, UCLA presents a 3D touch sensor SoC that uses an oscillator-based bootstrapped and correlated double sampling architecture for mobile application. The 2.3mW 11cm 3D sensing system with with 1cm resolution is achieved with small die area of 2mm^2.

- In Paper 6.8, KAIST and Samsung present a pen pressure sensitive capacitive touch system with passive resonant stylus that can replace costly EMR-based systems. The multi-TX scanning and charge demodulating integrator scheme achieves 49dB SNR with 1mmϕ 6b resolution pen pressure sensing.

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Session 7 Overview: *Non-Volatile Memory Solutions*

MEMORY SUBCOMMITTEE

Session Chair: *Fatih Hamzaoglu, Intel, Hillsboro, OR*
Session Co-Chair: *Takashi Kono, Renesas Electronics, Hyogo, Japan*

Subcommittee Chair: *Joo Sun Choi, Samsung, Hwasung, Korea, Memory Subcommittee*

Strong demand for high-density low-power and reliable non-volatile Memory (NVM) Solutions continues to enable data centers, advanced automotive control, and wearables. In ISSCC 2015, a new 64Gb MLC Flash in 15nm CMOS technology is optimized for low power. Another 128Gb V-NAND with 3b/cell is introduced at 1Gb/s I/O rate. A high-speed 28nm embedded SG-MONOS Flash technology is developed for automotive industry. Aside from memory technology, system level innovations are critical to achieve high-speed reliable NVM solutions. A frequency-boosting interface chip is shown to stack 16-die 128Gb Flash at 1GB/s interface. An SSD controller is implemented for high-speed and reliable enterprise-level SSD with TLC Flash. As SRAM and DRAM scaling faces serious challenges, high-speed emerging memories needed to continue area and cost reduction. Two Mb level STTRAM macro papers are shown to achieve sub-10ns read speed, potentially replacing SRAM and DRAM.

- In Paper 7.1, Toshiba presents a 64Gb MLC NAND Flash memory developed in 15nm CMOS technology. 30MB/s program throughput and 533Mb/s data transfer rate are achieved even at 1.8V V_{CC} by an optimized datapath design. New design features are introduced to reduce current peak and BL discharging time.

- In Paper 7.2, Samsung presents world's first 128Gb TLC vertical NAND (V-NAND) Flash memory with 32 stacked WL layers. High-speed program (HSP) and data pre-processing technique enable t_{PROG} of 700µs and endurance over 5K program/erase cycles. 1Gb/s I/O rate is realized by the proposed multiple circuit techniques.

- In Paper 7.3, Renesas Electronics presents 28nm embedded SG-MONOS Flash macros for automotive uses. 200MHz random read and 2MB/s write throughput at T_j = 170°C with sufficient TDDB lifetime and suppressed RF noise are achieved by introducing 4 circuit techniques.

- In Paper 7.4, Samsung presents a sensing scheme for 8Mb STTRAM Macro to achieve 9ns sense speed with 200% TMR and 4% MTJ resistance sigma. Adjacent bitcells share the source line, and reference cell pairs are shared among 128 data columns for high density. Less than 2mA can be sensed at 1.5V periphery voltage.

- In Paper 7.5, Toshiba presents design techniques to optimize STTRAM array active and idle power, as well as read-disturb reduction. Equalized and hierarchical bitline is shown to reduce bitcell disturb, and multi-level dynamic periphery power down is implemented on 1Mb Macro to achieve 72µJ/MHz read and 166µJ/MHz write power with 3.5ns/3ns read/write time in 2T2MTJ fashion.

- In Paper 7.6, Samsung presents a frequency boosting interface chip (F-Chip) to alleviate SSD interface speed bottleneck. 2Tb NAND Flash MCP with 1GB/s toggle DDR interface is accomplished by incorporating the proposed F-Chip into the NAND MCP including a 16-die stacked 128Gb NAND flash.

- In Paper 7.7, Chuo U presents three SSD controller techniques for high speed and reliable enterprise-level SSD. Fast low-density parity-check (LDPC) reduces the read latency of 1Xnm TLC NAND Flash SSD by 83%. Dynamic V_{TH} optimization and auto data recovery reduce the NAND flash bit-error rate (BER) by 80% and 17%, respectively.

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Session 8 Overview: *Low-Power Digital Techniques*

ENERGY-EFFICIENT DIGITAL

Session Chair: *Victor Zyuban, IBM Research, Yorktown Height, NY*
Session Co-Chair: *Peter Nilsson, Lund University, Lund, Sweden*

Subcommittee Chair: *Stephen Kosonocky, AMD, Fort Collins, CO, EED*

Energy efficiency is becoming the main design driver for both small embedded microcontrollers, as well as multicore platforms. This session presents a wide range of low-power digital-design techniques implemented in complete ultra-low-power microcontrollers for the Internet-of-Things (IoT), as well as in SoC building blocks exploiting fine-grain DVFS. The record-low power operation of the presented ARM and TI cores will prolong battery life in many IoT applications and enable energy-harvesting operations. These papers achieve both low-active power consumption, as well as incorporating techniques for efficient full-state retention. On the SoC side, innovative on-chip voltage and frequency regulation techniques enable operation across a wide range of supply voltages and PVT variations. This enables operation at reduced voltages and lower power. Novel voltage regulators increase energy efficiency and reduce voltage droops on the power rails caused by variations in the current consumptions of the cores.

- In Paper 8.1, ARM presents an 11.7pJ/cycle subthreshold ARM Cortex M0+ WSN processing subsystem in 65nm 1.2V CMOS, occupying 1.28mm^2. Retention power of 80nW is one order of magnitude lower than previous sub-threshold designs below 180nm. The ultra-low-voltage sub-system comprises an ARM Cortex-M0+, an ultra-low-voltage high-density SRAM, synthesized boot ROM, an AES-128 accelerator, and specific interfaces.

- In Paper 8.2, the University of Michigan presents a battery-less 295pW 1.19mm^2 32b Cortex M0+ processor and a 256B memory at 0.55V. It proposes a new logic implementation referred to as dynamic leakage-suppression logic, consuming 10fW of active power per gate. The core was operational when directly powered by a 0.09mm^2 bulk silicon solar cell.

- In Paper 8.3, Texas Instruments presents a 10.5µA/MHz microcontroller in a 90nm flash process running at 16MHz with single-cycle code accesses from a flash memory. To maintain low retention leakage, MTCMOS sequential cells and adaptive forward-body-bias schemes are used.

- In Paper 8.4, STMicroelectronics presents a near-threshold SoC embedding a 26pJ/cycle 0.272mm^2 SPARC V8 processor at 0.45V exploiting forward body biasing in a 28nm UTBB FDSOI technology. An AVS scheme is incorporated, comprising a 0.33V/0.45V dual-mode switched-capacitor DC-DC converter, a timing monitoring system, and a 1.51pJ/cycle open-loop clock multiplier.

- In Paper 8.5, Qualcomm presents a 16nm FinFET CMOS auto-calibrating adaptive clock distribution system recovering the F_{MAX} loss from V_{DD} droops, while eliminating the overheads from tester calibration. It enables in-field low-latency tuning of the dynamic variation monitor across a wide range of PVT variations, with throughput gains from 13% to 30% for a 10% V_{DD} droop relative to supply voltages ranging from 0.6-0.9V.

- In Paper 8.6, Intel presents a fully integrated, digitally controlled voltage regulator, which is a hybrid of an LDO and a switched capacitor to supply current to a 22nm graphics execution core. Compared to a shared-rail implementation, the 2.6x1.3mm^2 (core plus test area) regulator enables 82% reduction in core energy consumption, while operating at a voltage of 0.38V, and achieves a 67% energy reduction, while operating at 0.84V.

- In Paper 8.7, Intel presents a dual-mode digital power gate and linear voltage regulator implemented in 14nm CMOS, operable from 0.4-1V, in 0.041mm^2, capable of delivering up to 3A to a microprocessor core, while achieving over 99% regulator efficiency and a 60mV dropout voltage.

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Session 9 Overview: *High-Performance Wireless*

WIRELESS SUBCOMMITTEE

Session Chair: Li Lin, Marvell, Santa Clara, US
Session Co-Chair: Chun-huat Heng, National Univ. of Singapore, Singapore

Subcommittee Chair: *Aarno Pärssinen, University of Oulu, Oulu, Finland, Wireless*

State-of-the-art wireless systems implemented in low-cost, deep-submicron CMOS processes support a wide range of applications including 2/3/4G cellular and 802.11a/b/g/n/ac. This session includes a multiband GSM/EDGE/HSPA+/TDSCDMA/LTE transceiver, the first reported single-chip HSPA transceiver with fully-integrated 3G CMOS power amplifiers, a transmitter with10b 128MS/s incremental-charge-based DAC achieving -155dBc/Hz out-of-band noise, a digital quadrature transmitter based on the IQ cell sharing, a 5.3GHz 16b 1.75GS/s wideband RF Mixing-DAC achieving IMD<-82dBc up to 1.9GHz, an LTE SAW-less transmitter using 33% Duty-Cycle LO signals for harmonic suppression, and a 28nm CMOS digital fractional-N PLL LO with -245.5dB FOM for 802.11abgn/ac radio.

- In Paper 9.1, Broadcom presents a $13mm^2$, 40nm SAW-less TX 2G/HSPA+/TDSCDMA/LTE Cat4 transceiver. It operates from 0.7GHz to 2.7GHz and supports free-running XO operation and 32kHz RTC generation. 36/65mA in 3G/LTE20 B1, -50dBm TX/-60dBm RX is achieved. TX LTE20 E(UTRA) ACLR is less than -40(-43)dBc and NF is better than 2.5dB.

- In Paper 9.2, Intel, DMCE and AVL present an HSPA transceiver with on-chip integrated 3G power amplifiers in a standard 65nm CMOS technology without additional metal stack options or process tunings, to enable real low-cost monolithic system integration. The achieved performance shows that watt-level PA integration is possible and leads to a significant size and cost benefit for applications like M2M.

- In Paper 9.3, imec and Vrije Universiteit present a charge-based architecture for nanoscale CMOS RF transmitters. Its incremental-based charge-domain operation provides out-of-band filtering for both thermal and quantization noise. With a 128MS/s 10b DAC configuration, it achieves -45dB ACLR and -155dBc/Hz out-of-band noise at 45MHz offset from a 1GHz modulated carrier, while consuming 41mW and core area of $0.25mm^2$.

- In Paper 9.4, Marvell presents a 28nm CMOS local oscillator circuit for dual-band 802.11 a/b/g/n/ac radio with a low-noise integrated XTAL oscillator, a fractional-N digital PLL with background doubler duty cycle error correction, non-periodic DCO dithering and compensation, and a frequency tripler. The fractional-N PLL achieves 0.17ps rms jitter while consuming 9.5mW, leading to a record FOM of -245.5dB.

- In Paper 9.5, Pohang University and Samsung present a digital quadrature transmitter suitable for SDR application. Three-level LO shape for time independent multiplexing and disabling cell technique is adopted. The dynamic range of output power is from -20.2dBm up to 13.86dBm, and the PAE of the transmitter at the peak power/average power is 40.43%/29.1%.

- In Paper 9.6, Eindhoven University of Technology and Integrated Device Technology present a mixing-DAC architecture with local mixing per current cell, multi-level cascoding with double bleeding currents and elevated bulk voltage, supply-isolated LO driver, and sort-and-combine calibration. A 65nm CMOS chip achieves IMD<-82dBc and SFDRRB300MHz>75dBc (SFDR in a Reduced Bandwidth) up to f_{out}=1.9GHz. SFDRRB>68dBc is measured up to 5.3GHz.

- In Paper 9.7, MediaTek presents an LTE transmitter using 33% duty-cycle LO signals for harmonic suppression. It achieves <-70dBc CIM3 and meets the Band-13 PSB emission without external filter. The RX band noise at 30MHz offset of -159.4dBc/Hz satisfies the SAW-less requirement. The TX core circuit occupies an area of $0.93mm^2$ in 40nm CMOS and consumes 216mW at Band-13 maximum output power.

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Session 10 Overview: *Advanced Wireline Techniques and PLLs*

WIRELESS SUBCOMMITTEE

Session Chair: *Gerrit den Besten, NXP Semiconductors, Eindhoven, The Netherlands*
Session Co-Chair: *Nicola Da Dalt, Infineon Technologies, Villach, Austria*

Subcommittee Chair: *Daniel Friedman, IBM, Yorktown Heights, NY, Wireline*

How many Gb/s can you suck through a straw? Can we make a smartphone out of Lego-like blocks? To answer these questions and more, this session presents several unconventional approaches for data links in emerging applications. The session also includes innovations in transceiver techniques for more conventional communication links as well as advances in PLL design. The session includes a plastic waveguide link with an on-chip coupler, a non-contact interface, techniques for multi-drop memory buses, and 14-nm designs. The final three papers describe new approaches in injection-locked clock multipliers and fractional-N PLLs.

- In Paper 10.1, Keio University presents an area efficient non-contact 6Gb/s interface for modular smartphones that bridges 5mm distance. Realized in 65nm CMOS, the design consumes 6pJ/b while achieving excellent EMI robustness.

- In Paper 10.2, KU Leuven, presents a full plastic fiber link which transports up to 12.7Gb/s using a 120GHz carrier FSK modulation and achieving an energy efficiency of 1.8pJ/b. This full link solution includes 40nm CMOS transceiver ICs, a TX integrated coupler, an RX bond-wire based antenna, and the fiber.

- In Paper 10.3, EPFL Lausanne demonstrates a channel-matched multi-tone link for memory-bus applications that suffer from notches in the transfer function due to stub reflections. The transceiver is implemented in 40nm CMOS and achieves 7.5Gb/s while consuming 1pJ/b.

- In Paper 10.4, Samsung presents a duo-binary equalizing front-end for a binary link combined with a 5-tap DFE to adaptively remove pre- and post-cursor ISI without a high-boosting CTLE for a reflective memory channel. The DFE receiver implemented in 45nm CMOS operates at 5.8Gb/s and consumes 2.45pJ/b.

- In Paper 10.5, Intel presents a 5.9pJ/b 10Gb/s serial link with improved lock-point Mueller-Muller CDR in 14nm tri-gate CMOS. The transceiver can deal with 24dB channel loss, occupies 0.065mm^2 and is 60% smaller than the smallest comparable link.

- In Paper 10.6, IBM presents a 14nm FinFET 16Gb/s receiver with CTLE and 2-tap speculative DFE capable of handling 30dB channel loss and consuming 2pJ/b. The CTLE provides programmable active peaking with up to 8.8dB gain boost at 8GHz.

- In Paper 10.7, University of Illinois presents a 65nm CMOS LC-based injection-locked clock multiplier at 6.75 to 8.25GHz, achieving 190fs$_{rms}$ integrated jitter while consuming 2.25mW power. The multiplier employs a digital frequency-tracking loop, ensuring robust operation across PVT variations.

- In Paper 10.8, MediaTek presents a low-area fractional-N PLL in 40nm CMOS achieving fractional spurs below -70dBc and reference spurs below -87dBc. The PLL generates 2GHz from a 26MHz reference with 9.1mW. A switched-capacitor loop filter improves charge-pump noise and linearity and provides cancellation of ΔΣ modulator quantization noise.

- In Paper 10.9, IBM presents a 13-to-28GHz hybrid analog/digital fractional-N PLL in 32nm CMOS SOI. The design employs a highly digital self-calibrating ΔΣ noise cancellation system to significantly improve out-of-band phase noise. The PLL occupies 0.24mm^2 and consumes 31mW.

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Session 11 Overview:
Sensors and Imagers for Life Sciences
IMMD SUBCOMMITTEE

Session Co-Chair: *Sam Kavusi, Robert Bosch, Palo Alto, CA*
Session Co-Chair: *Makoto Ikeda, University of Tokyo, Tokyo, Japan*

Subcommittee Chair: *Makoto Ikeda, the University of Tokyo, Tokyo, Japan, IMMD Subcommittee*

Life sciences applications require imaging in different modalities, e.g., fluorescence, positron imaging, near-IR, with higher sensitivity, higher speed, and smaller form factor. This session includes two papers that achieve significant milestones in fluorescence lifetime imaging with low picosecond resolution. Two other papers describe advances in positron emission tomography and functional near-IR medical imaging. Another major accomplishment is the demonstration of time-correlated photon counting with 14GS/s throughput. Finally, an intriguing technique for improving CMRR in neural recording, an enabling multi-modal cell-based drug screening assay platform, and a consumer oriented ultrasound body fat sensor, enable advances in their respective fields.

- In Paper 11.1, KAIST presents a portable brain imaging system based on a multi-channel functional near-IR IC in time for the 20th anniversary of this technique. The system contains 10 channel receivers and 8 channel transmitters that drive the VCSELs and consumes 143mW.

- In Paper 11.2, Shizuoka University presents a fluoresence lifetime image sensor with 10.8ps time resolution and 256×512 spatial resolution. The sensor employs lock-in pixels enabled by a 2-stage lateral electric field charge-transfer technique.

- In Paper 11.3, Fondazione Bruno Kessler presents a sub-nanosecond time-gated single-photon imager with analog counting, and programmable time-gating width and delay. The 160×120 imager with 25μm pixels and a fill factor of 21% allows for 486fps lifetime imaging acquisition.

- In Paper 11.4, TU Delft presents a PVTB-compensated 432-column parallel endoscopic time-of-flight sensor incorporating 67,392 SPADs. The chip achieves 48 timestamps per SiPM utilizing 432 TDCs.

- In Paper 11.5, University of Edinburgh and STMicroelectronics present a time-correlated single-photon-counting chip utilizing SPADs and direct-to-histogram TDCs. The design achieves 71.4ps resolution, over an 18.8ns dynamic range, with 14GS/s throughput.

- In Paper 11.6, National University of Singapore presents a neural amplifier system with 90dB CMRR employing inverter-based OTAs with common-mode feedback through supply rails. The chip is fabricated in 65nm CMOS.

- In Paper 11.7, Georgia Institute of Technology presents a multi-modal CMOS sensor array for cell-based drug screening. Voltage, impedance, optical shadow, and temperature are measured on a 2D array. The effect of a cardiac pharmacological agent on a human cardiomyocyte cellular assay is monitored on the die surface.

- In Paper 11.8, UC Berkeley and UC Davis present an integrated ultrasound imaging system for body fat composition measurement. A level-shifter free of crow-bar current driving a 17.5pF load at 8MHz achieves 89% efficiency yielding 2.6μJ per measurement.

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Session 12 Overview:
Inductor-Based Power Conversion

ANALOG SUBCOMMITTEE

Session Chair: *Makato Takamiya, University of Tokyo, JAPAN*
Session Co-Chair: *Dragan Maksimovic, University of Colorado, Boulder, CO*

Subcommittee Chair: *Axel Thomsen, Silicon Labs, Austin, TX, Analog*

Efficient Inductive-based power conversion from one voltage to another voltage is one of the fundamental analog tasks needed by the electronic world. It is an area that targets diverse applications with the goal of maintaining efficiency, while meeting the requirements of the load or source. This session begins with five DC-DC buck converters and a LED driver. Several techniques including a fixed switching frequency control, a time-based control, an analog-digital hybrid control, an error-based control, and an energy recycling technique are shown.

The second part of the session is dedicated to circuits for inductive wireless power transmission. A highly integrated system and several techniques to increase the power transmission efficiency versus distance and load variations are shown.

- In Paper 12.1, KAIST presents a hysteretic buck converter employing quasi-inductor current emulator (QICE) with reset operation. This converter achieves fast-step load transient responses. The switching frequency is fixed within 0.2% of 1MHz and the maximum efficiency reaches 95.5%.

- In Paper 12.2, University of Illinois at Urbana-Champaign and Qualcomm present time-based control techniques to generate automatically synchronized and inherently duty-cycle matched multi-phase PWM signals. A 1.8V prototype achieves 87% peak efficiency while consuming 90µA quiescent current at 30MHz switching frequency.

- In Paper 12.3, University of Michigan presents a PWM buck converter providing 1V and 35µA-to-4mA for implantable biomedical systems. Adaptive power gating and hybrid analog-digital hybrid control to achieve 86.3% peak efficiency at 1.4mA, and over 80% efficiency from 45µA-to-4mA load.

- In Paper 12.4, RWTH Aachen University presents a capacitor-free single-inductor 4-channel all-digital integrated DC-DC LED driver in a 0.18µm technology. Based on the use of laterally double-diffused DMOS transistors, up to 1A LED current is generated from up to 24V input voltage.

- In Paper 12.5, KAIST presents a controller for single-inductor multiple-output DC-DC buck converters, which achieves high efficiency and improved cross-regulation. In a prototype having 10 independently regulated output voltages, peak efficiency of 88.7% is achieved down to 5mA output current.

- In Paper 12.6, National Chiao Tung University and Realtek Semiconductor present an output-independent gate-drive approach for single-inductor multiple output buck converters. In targeting tablet applications, a peak efficiency of 90% is achieved for output voltages between 1.2V and 3.3V.

- In Paper 12.7, Pennsylvania State University and Georgia Institute of Technology present a Q-modulation technique in the receiver for 2MHz, 1.4W wireless power transfer to compensate for variations in the load resistance and coupling distance in 0.35µm CMOS.

- In Paper 12.8, Hong Kong University of Science and Technology presents a primary equalizer in the transmitter for 13.56MHz, 234mW wireless power transfer to extend the coupling and load ranges in 0.35µm CMOS. The maximum total efficiency is 62.4%.

- In Paper 12.9, Samsung Electronics, U-blox, and Georgia Institute of Technology present a fully integrated 6W wireless power receiver at 6.78MHz compatible with A4WP standard in 130nm BCD process. The maximum receiver efficiency is 84.6%.

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Session 13 Overview: *Energy-Efficient RF Systems*

RF & WIRELESS SUBCOMMITTEES

Session Chair: *Ali Afsahi, Broadcom, San Diego, CA*
Session Co-Chair: *Jan van Sinderen, NXP Semiconductors, Eindhoven, The Netherlands*

Subcommittee Chair: *Andreia Cathelin, ST Microelectronics, Crolles, France, RF Subcommittee*

There is an increasing demand for energy efficient and very small wireless solutions for different applications such as IoT, wearable and wireless sensors. The papers presented in this session focus on various circuit and architecture techniques to demonstrate highly integrated low-power RF systems. Four papers present BLE RF system solutions. The other four papers demonstrate very-low-power techniques like receiver-based FLL, wake-up radio, extreme low duty-cycle regimes and RF energy harvesting.

- In Paper 13.1, KAIST and Samsung Advanced Institute of Technology present a receiver-based FLL, consuming only 227uW while having a sensitivity of -83dBm for receiving 1Mb/s OOK signals.

- In Paper 13.2, Holst Centre / imec, Eindhoven University of Technology and Renesas Electronics present a 40nm RF SoC for WPAN in 40nm CMOS. The digital-intensive RF architecture is fully compliant with BLE PHY/Data-link/MAC and achieves 3.7mW RX and 4.4mW TX power consumption.

- In Paper 13.3, Dialog Semiconductor presents a 55nm BLE SoC transceiver with fully integrated matching network and RX-TX switch. It achieves blocking performance >35 dB better than required by the standard.

- In Paper 13.4, Renesas Electronics presents a 40nm BLE transceiver with -94dBm sensitivity. Its integrated matching network is also used as a notch filter in RX mode to achieve -55dBc image rejection.

- In Paper 13.5, STMicroelectronics, the University of Lille and the University of California at Berkeley present a 2.4GHz low-data-rate wake-up receiver for ultra-low power and compact Wireless Sensor Nodes with -97dBm sensitivity and only 99uW power consumption.

- In Paper 13.6, the University of Toronto presents a sub-mW BLE receiver front-end operating under 0.8V. The receiver shows NF of 15.8dB, IIP3 of -17dBm, image rejection of 30dB and sensitivity of -82dBm.

- In Paper 13.7, MIT presents a 2.4GHz TX that is optimized for extremely low duty-cycle regimes, achieving 30× reduction in sleep-mode power. The output power is 10.9dBm with total TX efficiency of 43.7%.

- In Paper 13.8, Tokyo Institute of Technology presents a 5.8GHz RF-powered transceiver that achieves 2.5Mb/s, 32-QAM modulation while consuming 113uW.

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Session 14 Overview:
Digital PLLs and SoC Building Blocks
HIGH-PERFORMANCE DIGITAL SUBCOMMITTEE

Session Chair: *Anthony Hill, Texas Instruments, Dallas, TX*
Session Co-Chair: *Hiroo Hayashi,Toshiba, Kawasaki, Japan*

Subcommittee Chair: *Stefan Rusu, Intel, Santa Clara, CA, High-Performance Digital Subcommittee*

The nine papers in this session highlight developments in clock generation, sensors, and security. Digital PLL solutions are presented in FinFET technology, improved power supply noise and jitter, and synthesized fractional-N functionality. Papers in this session also present solutions for on-die power and aging sensors for reliable operation, and address security with innovations in device authentication using physically unclonable functions.

- In Paper 14.1, the Tokyo Institute of Technology presents a 0.048mm^2 0.8V, 3mW fully synthesizable fractional-N all-digital PLL, with a soft injection-locking technique and cascading topology. The PLL is designed and fabricated in 65nm CMOS achieving a 3.6ps integrated jitter at a carrier of 1.5222GHz and a -224.2dB FOM with output frequency of 0.8-1.7GHz from an input reference clock of 50-400MHz.

- In Paper 14.2, the University of Michigan presents a 40nm all-digital physically unclonable function (PUF), based on oscillation collapse. This chip has 5.5×10^{28} challenge-response pairs. BER is estimated at $<10^{-8}$ across -25-125°C and 0.7-1.2V with average inter-chip Hamming distance of 0.5007, an effective throughput of 1.6Mb/s, efficiency of 17.75pJ/b, and occupying 845μm^2.

- In Paper 14.3, the National University of Singapore presents a 65nm physically unclonable function (PUF) for secure key generation and chip identification with energy down to 15fJ/b. Concerning the uniqueness of PUF keys, the average ratio of inter-chip to intra-chip Hamming distance is >140. Native unstable bits are <2% at nominal conditions and >6% across 0.7-1.0V and 25-85°C. This PUF consumes 25μm^2 in 65nm CMOS.

- In Paper 14.4, KAIST presents a reference-frequency-multiplied all-digital PLL, with low reference spur. Implemented in 65nm CMOS operating at 1V, the prototype PLL at 5GHz achieves an integrated RMS jitter of 701.7fs from 100Hz-40MHz, with a power of 9.52mW on an area of 0.228mm^2, with an in-band phase noise of -95.8dBc/Hz at 100kHz, and out-band phase noise of -130.6dBc/Hz at 10MHz.

- In Paper 14.5, TSMC presents a 0.029mm^2 16nm FinFET fractional-N 0.25-to-4GHz ADPLL with spread-spectrum clocking. The multicore technique and coarse-tuning adjustor achieve a resolution of 133KHz, frequency tuning range of 529MHz, phase noise of -120dBc/Hz, 1.22ps integrated jitter and -228.6 FOM, while operating across 0.52-0.8V. This PLL consumes a total power of 9.3mW at 200MHz.

- In Paper 14.6, ARM presents a power delivery monitor embedded in a dual-core Cortex-A57 28nm SoC with fully integrated on-chip digital storage oscilloscope, VCO-based ADC, triggering and analysis engine, and programmable synthetic current load. The power monitor can obtain 2.24GS/s with -0.4/+0.6 to -0.9/+0.7 LSB accuracy and 3.3mV resolution. The power density monitor operates between 0.8-1.0V in 0.0775mm^2.

- In Paper 14.7, Columbia University presents a monitoring technique for NBTI in SRAM register files by sensing bitcell PMOS V_t. V_t is sensed directly (in-situ) and robustly across temperature and voltage variation with <20% in-field error, improving cross-voltage and temperature errors by 3.2-5×. Techniques to generate recovery vectors are proposed for rebalancing PMOS skews in bitcells and improving V_{MIN}. This monitor is implemented in 65nm and operates from 0.6-0.9V and 20-80°C.

- In Paper 14.8, Samsung presents a 14nm FinFET 0.8V, 0.009mm^2, 30-to-2000MHz 2nd-order ΔΣ analog bang-bang digital PLL. DCO phase noise is improved by 2.78dB using a self-switching technology and PVT tolerance is achieved with a foreground automatic frequency calibration (AFC) loop. The PLL dissipates 2.06mW at 2GHz at 0.8V with an integrated jitter of 18.8ps and a FOM of -211.38dB.

- In Paper 14.9, UCLA presents a low-noise fractional-N all-digital PLL in 65nm CMOS. The 0.23mm^2 ADPLL operates at 1V and produces an Fout of 2.6-3.9GHz, achieves -110.6dBc/Hz in-band phase noise, consuming 11.5mW of power with a -242dB FOM. It has a fractional spur of -63.1dBc, a phase noise of -118dBc/Hz at 1MHz and a bandwidth of 700kHz with RMS jitter of 226fs at 1KHz and 240fs at 100MHz.

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Session 15 Overview: *Data-Converter Techniques*

DATA CONVERTERS SUBCOMMITTEE

Session Chair: *Seung-Tak Ryu, KAIST, Daejeon, South Korea*
Session Co-Chair: *Matt Straayer, Maxim Integrated, Chelmsford, MA*

Subcommittee Chair: *Boris Murmann, Stanford University, Stanford, CA, Data Converters*

The demands for low power and increased bandwidth continue to be a primary motivation for ADCs. However, the system requirements also present demands on the ADC that can drive design choices at the architectural level. This session demonstrates multiple design techniques for realizing high-performance data converters targeted at a variety of applications and process technologies. Papers in this session include high-performance continuous-time delta-sigma ADCs, a PVT-insensitive TDC implemented in 14nm FinFET technology, and new buffering techniques for both reference voltages and input signals. These papers represent multiple advances in capability for low-power, wide-bandwidth, and high-performance data converters.

- In Paper 15.1, MIT and MediaTek present a ΔΣ modulator in 28nm LP CMOS that utilizes a 3-1 continuous-time Sturdy-MASH architecture to achieve aggressive noise shaping with a 50MHz bandwidth. It is clocked at 1.8GHz and achieves 85.2dB SFDR and 74.6dB SNDR while consuming 78mW.

- In Paper 15.2, MediaTek presents a continuous-time self-coupling (CTSC) ΔΣ modulator with residual ELD compensation and DAC linearity enhancement techniques. The ADC achieves an SNDR of 90.4dB with a 2.2MHz bandwidth. It is implemented in 55nm CMOS and consumes 4.5mW.

- In Paper 15.3, University of Twente, Delectronics, and Teledyne DALSA present a ΔΣ audio DAC with a 2-path approach that reduces out-of-band noise to below -60dBFS, allowing for a very small area and power-efficient implementation. Fabricated in 0.08mm^2 of 0.18µm CMOS, the dynamic range and THD+N are measured at 115dB (A-Weighted) and -103dB, respectively.

- In Paper 15.4, TU Eindhoven presents a 10b 80kS/s SAR ADC in 65nm CMOS with a 0.62V reference-voltage generator (RVG). To save power, the RVG is operated at 10% duty cycle, and a bi-directional dynamic comparator is employed. The ADC achieves 56.6dB SNDR and 65.0dB SFDR at Nyquist with an efficiency of 2.4fJ/conversion-step.

- In Paper 15.5, Samsung presents a low-power and PVT-variation-tolerant TDC featuring stochastic phase interpolation and 16× spatial redundancy. The converter architecture leverages 14nm FinFET CMOS technology to achieve high linearity and 1ps resolution without any calibration.

- In Paper 15.6, MIT presents a virtual ground reference buffer approach for switched-capacitor circuits that significantly relaxes key op-amp specifications including unity-gain bandwidth, noise, and open-loop gain. The technique is demonstrated with a 12b 250Ms/s pipeline ADC in 65nm CMOS that achieves 67dB SNDR with 49.7mW power consumption.

- In Paper 15.7, Stanford University and NXP Semiconductors present a 14b 35MS/s SAR ADC in 40nm CMOS with a loop-embedded input buffer that consumes only 23% of the total ADC power. The buffer uses a source follower (SF) topology whose nonlinearities are cancelled by the SAR algorithm, achieving 99dB SFDR despite the small amount of invested power.

- In Paper 15.8, Texas Instruments presents a 14b 500MS/s pipelined ADC in 0.18µm BiCMOS SiGe targeted for wireless infrastructure applications. Track-and-hold enhancements and extended amplifier settling time are used to achieve over 90dB SFDR at low frequency and over 80dB up to 500MHz inputs.

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Session 16 Overview:
Emerging Technologies Enabling Next-Generation Systems
TECHNOLOGY DIRECTIONS SUBCOMMITTEE

Session Chair: *Jan Genoe, imec, Leuven, Belgium*
Session Co-Chair: *Koichi Nose, Renesas Electronics, Tokyo, Japan*

Subcommittee Chair: *Eugenio Cantatore, Eindhoven University of Technology, Eindhoven, The Netherlands, Technology Directions*

New materials and technologies are opening exciting possibilities for next-generation systems and applications. These novel technologies may enable new form factors or new sensing modalities, or they may lead to lower power consumption or high voltage switching efficiencies, which cannot be achieved using existing standard CMOS processes. The papers in this session give insight into the latest advances in these emerging technologies, and offer a valuable overview of the systems and applications, which may enter the mainstream in the near future.

- In Paper 16.1, INES, Festo, and IMS CHIPS present an ultra-thin (20μm) bendable CMOS stress sensor (2×10b digital output for stress along both axis), where both the analog and digital parts of the circuit are compensated for stress and temperature. The application is demonstrated on a robotic gripper.

- In Paper 16.2, Princeton University presents a thin-film image sensing and detection system based on a-Si photoconductors and embedded TFT classifiers. These TFT classifiers in the large area system reduce the total signals required for detection by 9× before connecting to an external CMOS IC.

- In Paper 16.3, imec, TNO and KULeuven present how NFC tags, realized using amorphous IGZO transistors on flexible foil, can be powered by commercial NFC readers. The NFC data rates obtained exceed by 22× the state-of-art of existing technologies on foil and the tags are compliant to ISO15693.

- In Paper 16.4, University of Tokyo and Osaka University present a fever-alarm armband with a size of 30×18cm^2. Solar cells power the armband from indoor lighting, a temperature detector monitors the underarm temperature of a patient, and a PVDF speaker produces a sound to alert a nurse whenever a predefined threshold temperature is exceeded.

- In Paper 16.5, ASYGN and APIX analytics present an integrated circuit for a Nano-ElectroMechnical System (NEMS) for attogram gravimetric sensing applications. A NEMS-array driving and readout IC fabricated in a 28nm CMOS process provides the required performance for attogram-level mass measurements (10MHz-to-1GHz driving frequencies and 10V drive voltage). The silicon area is 0.9mm^2 and requires 68mW of power.

- In Paper 16.6, Seoul National University, Kyung Hee University and Chonnam National University present a biosensor chip comprising a CMOS-CNT(carbon nanotube) sensor array with a padless structure which can be used for direct bare-die measurements in low-cost medical applications. The chip is fabricated using a 0.35μm standard CMOS process and it operates under 150mW maximum power.

- In Paper 16.7, the University of Texas and Texas Instruments present a 20V, 8.4W, 20MHz four-phase GaN DC-DC converter. The half-bridge gate driver IC with a 4ns propagation delay uses a dynamic level shifter and an active bootstrap switch.

- In Paper 16.8, the Massachusetts Institute of Technology presents the first 1GHz monolithic GaN MMIC MEMS-based oscillator based on a 268×214μm^2 Lamb-mode resonator, which achieves a FOM up to 205.9dBc/Hz FOM using only 1mW of power.

- In Paper 16.9, Semiconductor Energy Laboratory and University of Tokyo present a 128kb 4b/cell memory using c-axis aligned crystalline In-Ga-Zn oxide (CAAC-IGZO) FETs deposited on top of CMOS. In the 32768-cell memory, the 3σ distribution width of the read voltages is 47mV, and 16 non-overlapping distributions are obtained.

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Session 17 Overview:
Embedded Memory and DRAM I/O

MEMORY SUBCOMMITTEE

Session Chair: *Leland Chang, IBM, Yorktown Heights, NY*
Session Co-Chair: *Takefumi Yoshikawa, Panasonic, Kyoto, Japan*

Subcommittee Chair: *Joo Sun Choi, Samsung Electronics, Gyeonggi, Korea, Memory*

Demand for smaller and lighter personal devices with increasing functionality in the cloud drives advancements in both embedded memory technology and high-speed DRAM interfaces. Lower power through voltage reduction and increased performance through higher memory density and bandwidth are key enablers. This year's conference highlights 14nm FinFET technologies with the smallest bit cells achieved to date for both SRAM – at 0.05µm^2 – and embedded DRAM – at 0.01747µm^2. A new assist technique to drive V_{MIN} reduction and novel bit cells for both 2-port SRAM and TCAM applications are also presented. In addition, two area-efficient techniques to boost DRAM bandwidth are reported.

- In Paper 17.1, Intel presents an 84Mb embedded SRAM fabricated in 14nm FinFET technology featuring the smallest bit cells to date at 0.050µm^2 for high density and 0.058µm^2 for low voltage. 1.5GHz operation at 0.6V is demonstrated.

- In Paper 17.2, TSMC presents a new 16nm 8T bit cell to address read-disturb problems in two-port applications. Taking advantage of the relative PMOS-to-NMOS transistor drive ratio in FinFET technology, traditional NMOS write transistors in the bit cell are replaced with PMOS transistors.

- In Paper 17.3, National Tsing Hua University presents a novel dual-split-control approach to improve the read/write margins of a 6T bit cell. A V_{MIN} improvement of 280mV is demonstrated in 28nm technology. Additionally, a figure of merit is proposed to quantify read/write margin improvements.

- In Paper 17.4, IBM presents a 1.1Mb embedded DRAM in 14nm FinFET technology for high-performance microprocessor caches. The 0.01747µm^2 cell features a deep-trench capacitor and a thick-oxide FinFET access device. An array access time of 1.0ns is demonstrated.

- In Paper 17.5, National Tsing Hua University presents a dense ternary content-addressable-memory (TCAM) realized using a multi-level, non-volatile ReRAM cell. A search time of <1ns and energy/bit/search of 0.51fJ are achieved.

- In Paper 17.6, Korea University presents an area-efficient transmitter and receiver for mobile DRAM interfaces beyond LPDDR4. Using a combined RX/TX active area of 0.01mm^2, 10.5Gb/s/pin single-ended data transmission has been achieved through a 10cm FR4 PCB trace.

- In Paper 17.7, Samsung presents a 25nm 16Gb DDR4 SDRAM with a compact DLL architecture and hybrid DCC to address power noise in a 4-H TSV stack. Stable operation of 2.67Gb/s/pin at 1.2V is demonstrated in an active area of 0.012mm^2.

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Session 18 Overview:
SoCs for Mobile Vision, Sensing, and Communications

ENERGY-EFFICIENT DIGITAL SUBCOMMITTEE

Session Chair: *Mike Polley, Samsung, Richardson, TX*
Session Co-Chair: *Paul Liang, MediaTek, Taiwan*

Subcommittee Chair: *Stephen Kosonocky, AMD, Fort Collins, CO, Energy-Efficient Digital Subcommittee*

SoCs presented in this session highlight recent energy-efficient architectures and design techniques enabling new capabilities to be added to power-sensitive systems. Machine vision processing brings object recognition and visual analytics for human-machine interfaces and vehicular applications. Smart multi-dimensional sensing systems achieve highest reported efficiency for monitoring humans and our environment. New video and communication processors demonstrate energy-efficient and cost-effective designs that implement the newest standards.

- In Paper 18.1, KAIST presents a two-chip gaze-activated object recognition system for head-mounted display applications. A 16mm^2 65nm CMOS chip operating down to 0.7V delivers 151.3GOPS at 131mW for gaze recognition. A 10mm^2 65nm CMOS chip operating down to 0.7V operates on 720p 30fps video to achieve object recognition in only 75mW, or 2.7nJ/pixel.

- In Paper 18.2, Toshiba presents a multicore SoC for high-performance object recognition in automotive applications. A 105.6mm^2 40nm CMOS device operating at 1.1V achieves 1.9TOPS performance in 3.4W.

- In Paper 18.3, KAIST presents an ultra-low-power recognition processor for mobile and wearable vision applications. The 2mm^2 65nm CMOS device operating at 0.5V achieves 93.5% recognition accuracy at 54µW power dissipation, offering 9.5× better power efficiency than previous state-of-the-art.

- In Paper 18.4, Princeton University presents a matrix-multiplying ADC that combines data conversion, feature extraction, and classification. The system is trained with machine learning techniques and achieves an overall energy savings of up to 23× compared to conventional systems. The device is implemented in 130nm CMOS operating at 1.2V.

- In Paper 18.5, UCLA presents a sparse-approximation (SA) engine to aggregate compressively sampled biomedical signals. The 5.13mm^2 SA engine in 40nm CMOS operating down to 0.45V achieves a 44-to-202× improvement in energy efficiency over prior hardware designs.

- In Paper 18.6, MediaTek presents a first 4k HEVC video codec supporting diverse formats. The 2.16mm^2 core in 28nm CMOS operating at 0.9V decodes 4k HEVC 60fps video at 126.73mW, 0.5nJ/pixel.

- In Paper 18.7, the University of Michigan presents a minimum mean-squared error (MMSE)-nonbinary LDPC iterative detector-decoder that achieves 1.38Gb/s. The 2.4mm^2 65nm CMOS detector and decoder at 0.5V consumes a lowest-reported 9.7pJ/b and 6.9pJ/b/iteration.

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Session 19 Overview: *Advanced Wireless Techniques*

WIRELESS SUBCOMMITTEE

Session Chair: Stefano Pellerano, Intel Corporation, OR, USA
Session Co-Chair: Koji Takinami, Panasonic, Japan

Subcommittee Chair: *Aarno Pärssinen, University of Oulu, Oulu, Finland; Wireless*

Latest advances in state-of-the-art wireless systems implemented in low-cost, deeply scaled CMOS technologies have demonstrated a wide range of applications: reconfigurable receivers with interference cancellation to support coexistence, FDD and even full-duplex, compressed sampling for rapid interferer detection and UWB/mm-wave ranging. This session opens with three papers demonstrating self-interference cancellation techniques in modern receivers and reconfigurability in SDR for carrier aggregation. A rapid interferer detection technique based on compressed sampling is demonstrated in the fourth paper. The fifth paper describes innovative HCI healing techniques applied to a 60GHz transceiver. The last two papers demonstrate two ranging applications based on UWB and mm-Wave with techniques to reduce power consumption and TX-to-RX crosstalk.

- In Paper 19.1, Columbia University presents a 1-to-1.7GHz receiver with a reconfigurable self-interference cancellation technique in 65nm CMOS that supports >>20MHz cancellation BW. Under the same-channel full-duplex (SC-FD) mode, 2dBm in-band IIP3 and 68dBm in-band IIP2 are achieved while consuming 63-to-69mW.

- In Paper 19.2, The University of Twente presents a 0.15-to-3.5GHz self-interference-cancelling receiver in 65nm CMOS that supports the in-band full-duplex application. It achieves up to 87dB effective SFDR in 16.25MHz bandwidth.

- In Paper 19.3, the University of Southern California presents a reconfigurable SDR in 65nm CMOS that supports multi-channel intra-band carrier aggregation using only one frequency synthesizer. The carrier frequency ranges from 0.5 to 3GHz and NF is 4.8dB.

- In Paper 19.4, Columbia University presents a quadrature analog-to-information converter (QAIC) for rapid interferer detection over a wide instantaneous bandwidth by exploiting blind bandpass sub-Nyquist compressed sampling. The QAIC front-end is implemented in 65nm CMOS in 0.43mm^2 and consumes 81mW from a 1.1V supply, enabling to scan from 2.7GHz to 3.7GHz with 20MHz RBW in 4.4μs.

- In Paper 19.5, Tokyo Institute of Technology presents the first 60GHz CMOS transceiver with HCI damage-healing technique for a longer lifetime. The transceiver achieves 7Gb/s in 16QAM with 214mW and 184mW in transmitting and receiving modes, respectively.

- In Paper 19.6, Yonsei University presents a real-time sampling IR-UWB receiver using time-extension method that allows digitizing a short pulse with 20Gs/s with a low-speed 100MHz ADC to lower power consumption. Implemented in 65nm CMOS, the chip demonstrates ranging accuracy of 1.9mm with maximum radio range of 2.1m with the power efficiency of 71.04nJ per detection step.

- In Paper 19.7, imec, Vrije Universiteit and Panasonic present a 79GHz PMCW radar transceiver that integrates a TX-to-RX spillover cancellation loop, achieving 15dB of suppression to reduce required ADC resolution. Implemented in 28nm CMOS, the transceiver achieves 11dBm TX output power, 35dB RX gain and NF < 7dB while consuming 260mW in a total die area of 2.72mm^2.

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Session 20 Overview: *Energy Harvesting and SC Power Conversion*

ANALOG SUBCOMMITTEE

Session Chair: *Makoto Nagata, Kobe University, Kobe, Japan*
Session Co-Chair: *Stefano Stanzione, IMEC/Holst Centre, Eindhoven, The Netherlands*

Subcommittee Chair: *Axel Thomsen, Silicon Laboratories Inc., Austin, TX, Analog*

The efficient control, storage, and distribution of energy are worldwide challenges, and are increasingly important areas of analog circuit research. Switched-capacitors are becoming a valuable alternative to inductive converters even for large power levels (on the order of several Watts) with high efficiency and extremely fast transient response. The session starts with 5 papers on switched-capacitor converters, ranging from large conversion ratio, large power and Dynamic Voltage Scaling. On the other hand, both battery-powered and battery-less wireless sensing applications can be enabled by harvesting energy from various energy sources. The second part of the session focuses on energy harvesting techniques and in particular on Maximum Power Point Tracking, energy recycling and zero current detection for photovoltaic, electrostatic, and electromagnetic energy sources.

- In Paper 20.1, KU Leuven and NXP Semiconductors present a highly efficient high-voltage conversion step-down switched-capacitor DC-DC converter. Using only 5 flying capacitors, the switched-capacitor converter achieves maximum 95.5% efficiency when stepping down from 37.2V to 3.3V while delivering 70mW.

- In Paper 20.2, Dartmouth College presents a 3-phase resonant switched-capacitor converter using PCB trace inductors. The switched-capacitor converter delivers up to 7.0W at 0.92W/mm^2 with 1.1nH inductors embedded in a flip-chip circuit board.

- In Paper 20.3, ETH Zurich and IBM Research Zurich presents a feedforward controlled switched-capacitor voltage regulator for reducing the output voltage droop during the transient load step. The voltage droop is reduced from more than 76mV down to 30mV with the feedforward control.

- In Paper 20.4, Hong Kong University of Science and Technology and University of Macau present a 123-phase ring-shaped switched capacitor converter for fast-DVS applications. With 123 ring-shaped topology, a 40MHz converter can achieve 3ns response time and 3.5mV ripple voltage without using a GHz clock.

- In Paper 20.5, Hong Kong University of Science and Technology and University of Macau present a parasitic insensitive topology for a fully integrated step-down switched-capacitor converter. The converter delivers 0.5-to-0.7V output voltage and can provide 11% efficiency improvement to 79.5%.

- In Paper 20.6, IMTEK and HSG-IMIT present an efficient and fully autonomous electromagnetic energy harvester interface. With sensorless conduction angle controlled maximum power point tracking, the system achieves 90% peak efficiency with 4.7μW start-up power.

- In Paper 20.7, Texas A&M University presents a charge pump based energy harvester interface with a two-dimensional maximum power point tracking algorithm, tuning both switching frequency and conversion ratio. Advantages of this topology are the wide input range (0.45-to-3V) and the large power efficiency (up to 89%).

- In Paper 20.8, Holst Centre, imec and OMRON present a fully autonomous high input voltage (up to 60V) electrostatic energy harvester interface. Thanks to the asynchronous control, exclusively based on current sensing, the DC-DC converter can start operating from 1μW available power and reaches a peak end-to-end efficiency of 85%.

- In Paper 20.9, National Cheng Kung University presents a single-inductor dual-input for photovoltaic energy harvesting. Thanks to the energy-recycling mechanism, the converter reaches 93% peak power efficiency with an active area of 0.5mm^2.

- In Paper 20.10, National Chiao Tung University presents a photovoltaic energy harvesting system based on a digital buck converter. The proposed self-tracking digital zero current detection and the tri-mode control strategy achieves 92% peak efficiency with a wide output power range of 50nW to 10mW.

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Session 21 Overview:
Innovative Personalized Biomedical Systems

TECHNOLOGY DIRECTIONS SUBCOMMITTEE

Session Chair: *David Ruffieux, CSEM, Neuchâtel, Switzerland*
Session Co-Chair: *Antoine Dupret, LIST-Leti, Saclay, France*

Subcommittee Chair: *Eugenio Cantatore, Eindhoven University of Technology, Eindhoven, The Netherlands*

Advanced biomedical systems-on-chip combined with miniaturized sensors and actuators offer new perspectives in the field of low-cost, portable, connected or self-monitored healthcare applications. Such technologies enable early diagnosis and personal therapy outside of a traditional clinical environment, increasing the autonomy and level of comfort of the patient.

This session presents innovative personalized biomedical circuits and systems spanning from low-level front-ends to complete SoC-based integrated platforms for low power, portable, point-of-care diagnosis and therapy. Applications cover physiological signals acquisition and processing, (tele)monitoring and mental health management via closed-loop electrical stimulations, and portable systems for biological compound analysis.

- In Paper 21.1 KAIST presents a dual-mode high-speed/healthcare BCC transceiver in 65nm CMOS. In high speed mode, the transmitter achieves up to 80 Mb/s at 79pJ/b, using 40/160 MHz dual bands or full duplex operation at 40Mb/s. In the 13.56MHz low data rate healthcare or wake-up mode, the power consumption of the receivers drops down to 42.5µW, while achieving 72dBm sensitivity and 60dB interference rejection.
- In Paper 21.2, Eindhoven University of Technology presents a record low 3nW signal acquisition IC integrating an amplifier with 2.1NEF and a 10b 1kS/s 1.5fJ/step ADC suitable for ECG measurement. With an area of 0.20mm^2 in 65nm CMOS, the chip operates reliably from 0-to-85°C at 0.5-to-0.7V while keeping ultra-low power consumption.
- In Paper 21.3, the University of Virginia and the University of Michigan present a PV/TEG-powered WSN achieving 75% end-to-end peak conversion efficiency. The 0.13µm, 13.5mm^2 SoC consumes only 6.5µW and combines flexible sensing interfaces, a 7.8kb/s WU receiver, a 187.5kb/s 4GHz UWB transmitter and a 2.3µW fine-grained power and clock-gated MCU/DSP versatile digital section operated in sub-threshold.
- In Paper 21.4, Case Western Reserve University presents a 10mm^2 61-to-94mW microfluidic-CMOS platform with 3D-capacitive sensor and fully integrated RF impedance measurement for “palmtop” dielectric spectroscopy in 0.35µm CMOS. The ASIC measures both the real and complex relative permittivity of the fluid in ranges, respectively, 1 to 94 and 0 to 465 with <2% error, over a frequency spanning 9MHz-to-2.4GHz.
- In Paper 21.5, National Taiwan University presents a portable gas-chromatography microsystem for volatile organic compounds detection. With the help of a MEMS pre-concentrator and separation column, the <1mA, 3V, 0.35µm 3.3×3.6mm^2 SOC integrating a CMOS gas detector, a low-noise read-out front-end and a micro-controller unit is able to detect analyte concentration levels down to 15ppb.
- In Paper 21.6, National Taiwan University, National Taiwan University Hospital, and Chang Gung University present a 9mm^2, 3V, 2.6mW, 0.35µm CMOS microfluidic SoC for blood screening immunoassay. The SOC micro-controller unit assists blood filtration through a nanoporous aluminium oxide membrane, biomolecular conjugation with antibodies attached to magnetic beads, electrolytic pumping, magnetic flushing and threshold detection based on Hall sensor array read-out analysis.
- In Paper 21.7, University of Applied Sciences of Southern Switzerland and OCULOX Technology present a circadian and cardiac intraocular piezoresistive pressure sensor measurement system achieving an unprecedented accuracy of 0.036mbar. The 2mm^2, 1.2mW, 0.35µm CMOS ASIC combining a sensor read-out and a 13.56MHz telemetry unit permits the monitoring of the retinal vascular system health.
- In Paper 21.8, Masdar Institute of Technology presents a non-invasive, 16-channel EEG, dual linear support vector machine-based SOC capable of closed-loop seizure detection and suppression after stimulation. The 0.18µm CMOS 25mm^2 SOC consumes 2.7µJ per classification, achieves a seizure detection with an average sensitivity, specificity and latency of 95.7%, 98% and 1s, respectively.
- In Paper 21.9, KAIST presents a robust mental health management system relying on multi-modal EEG, near-infrared hemoencephalography and heart rate variability signal acquisition, data processing, accurate classification and localized transcranial electrical stimulation in real time. The ASIC, integrated in a 0.11µm CMOS process, measures 3.4mm x 2.2mm and dissipates 24mW.

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Session 22 Overview: *High-Speed Optical Links*

WIRELINE SUBCOMMITTEE

Session Chair: *Azita Emami,* California Institute of Technology, Pasadena, CA
Session Co-Chair: *Hyeon-Min Bae,* KAIST, Daejong, Korea

Subcommittee Chair: *Daniel Friedman, IBM Research, Yorktown Heights, NY, Wireline Subcommittee*

Cloud computing is not in the clouds but in very real data centers with significant and growing networking and data communication needs. Data center scale computing demands interconnect solutions that support very high data-rates with ultra-low-power consumption at distances of 10m and greater. Because electrical links cannot meet the distance and density targets demanded by this application, demand for innovations in low-cost optical links to enable high-data-rate power-efficient solutions is strong. This session's nine papers highlight advances in hybrid integrated silicon photonics and electronics supporting rates of 25Gb/s and beyond, report a complete link for WDM, and present enhanced opto-electronic building blocks. The remaining papers describe high-voltage/high-speed drivers for ring and MZM modulators, low-power optical receivers, and clocking techniques for parallel optical links.

- In Paper 22.1, IBM presents a burst-mode optical receiver in 32nm SOI CMOS that uses digital control loops to perform TIA DC-offset calibration in 12.5ns and achieve phase lock in 18.5ns. The sensitivity of the 4.4pJ/b receiver is -10.9dBm (BER $<10^{-12}$) at 25Gb/s.

- In Paper 22.2, Fujitsu presents a hybrid integrated electrical-optical interface. The electronics chip in 28nm CMOS is integrated with silicon-photonic chip using a mixed pitch bumping technology. The carrier-injection ring modulator and the TIA operate at 25Gb/s consuming 2.9 and 2.0pJ/b, respectively.

- In Paper 22.3, Caltech presents an injection-locking method in a quadrature ring oscillator to achieve 4 to 11GHz of locking range. This technique is used to generate accurate clock phases for a 4-channel optical receiver using a forwarded clock. The receiver, implemented in 28nm FDSOI, achieves efficiency of 153fJ/b at 32Gb/s.

- In Paper 22.4, Texas A&M University presents a 24Gb/s hybrid-integrated microring receiver. A thermal tuning loop stabilizes the microring drop filter resonance wavelength. The source-synchronous receiver with LC injection-locked oscillator achieves -10dBm of sensitivity.

- In Paper 22.5 IMEC presents a ring-based 4×20Gb/s WDM transceiver using hybrid flip-chip integration of 40nm CMOS and a thermally tunable WDM Si photonics chips. The transceiver consumes 1.9pJ/b with an extra 7.1mW/nm thermal tuning power per channel.

- In Paper 22.6, Oregon State University presents a Si-photonics microring modulator WDM transmitter in 65nm CMOS. The transmitter incorporates a 2-tap asymmetric FFE for enhanced eye opening while achieving 4.4V output swing. A dynamic thermal tuning loop in the transmitter ensures robust operation by compensating for thermally-induced wavelength fluctuations.

- In Paper 22.7, Fujitsu presents a 4×25.78Gb/s optical transceiver IC in 0.13µm SiGe BiCMOS that occupies $6mm^2$ and consumes 650mW. The CDRs, which are tightly integrated to enable a channel pitch of 250µm, are designed to be robust against inter-VCO coupling.

- In Paper 22.8, Fujitsu presents a VCSEL driver IC with four 24-to-35Gb/s reference-less CDRs implemented in 0.13µm SiGe BiCMOS. One technique used by the parallel CDRs to achieve 250µm channel pitch is implementing an analog-domain phase interpolator in each lane. The phase rotator occupies $0.25mm^2$ and consumes 260mW power.

- In Paper 22.9, STMicroelectronics presents a 1310nm 25Gb/s silicon photonics Mach-Zehnder-based transmitter in 65nm CMOS. The transmitter, which employs a traveling wave modulator scheme, achieves a 6dB extinction ratio while consuming 275mW.

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Session 23 Overview: *Low-Power SoCs*

HIGH-PERFORMANCE DIGITAL SUBCOMMITTEE

Session Chair: *Andy Charnas, NVIDIA, Santa Clara, CA*
Session Co-Chair: *Youngmin Shin, Samsung, Hwasung, Korea*

Subcommittee Chair: *Stefan Rusu, Intel, Santa Clara, CA, High-Performance Digital Subcommittee*

As demands for performance continue to grow, even for embedded processors, SoCs designers must continue to develop energy-efficient solutions to fit into their required electrical and thermal envelopes. This session includes 3 papers that focus on achieving high performance with low power and energy-efficient techniques. Two papers present the latest mobile chips from Samsung and MediaTek, which use heterogeneous octa-core ARM CPUs. The paper from National Taiwan University, presents a depth-estimation processor that estimates full HD depth maps at 30fps from up to 5 stereo views of an image, while consuming only 611mW.

- In Paper 23.1, Samsung presents a mobile application processor with the latest ARM-v8 64b CPUs and a new hexa-core ARM-Mali GPU, implemented in Samsung's 20nm LP 9 layer metal process. The high-performance CPU cluster, with four ARM A57s, has a shared 2MB L2 data cache and operates at 1.9+GHz, and the low-power CPU cluster, with four ARM A53s, has a shared 256KB L2 data cache and operates up to 1.3GHz. Due to power optimizations, the fast 64b CPU consumes only 25% more power than the previous 32b CPU. The A57 area is 14mm^2; the A53 area is 4mm^2; and the area of the GPU complex is 25mm^2.

- In Paper 23.2, National Taiwan University presents a depth-estimation processor for light-field video applications. At 215MHz, it delivers five-view 1080p depth information at 30fps, while consuming 611mW at 0.9V. The stripe-buffering scheme employed reduces DRAM bandwidth by 67% and the four-bank processing architecture improves throughput by 4×. The chip occupies 4.69×4.69mm^2 in 40nm CMOS.

- In Paper 23.3, MediaTek presents a highly integrated smartphone SoC, with heterogeneous octa-core ARM-v7 32b CPU cores (A7 and A17), an LTE cellular modem, and high-performance 3D graphics. The A17 CPU operates at 2.5GHz. Optimized for power-efficiency, it contains a fully integrated power switch, which controls 5 power modes, including forward body bias and a fast adaptive retention mode with 50% lower leakage compared to active mode. The 89mm^2 SoC is fabricated in 28nm high-κ CMOS.

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Session 24 Overview: *Secure, Efficient Circuits for IoT*

TECHNOLOGY DIRECTIONS SUBCOMMITTEE

Session Chair: Chris Nicol, Wave Semiconductor, Campbell, CA
Session Co-Chair: Shinichiro Mutoh, NTT, Atsugi, Japan

Subcommittee Chair: Eugenio Cantatore, Eindhoven University of Technology, Eindhoven, The Netherlands

While the Internet of Things (IoT) is a recent phenomenon in the consumer electronics market, such exciting developments are frequently the result of decades of microelectronics research presented at ISSCC. In this session we address the security and efficiency issues that must be addressed before IoT devices can be deployed in a ubiquitous manner. IoT devices require advanced security mechanisms that protect the private data contained within them from cryptanalytic and physical attacks. This session includes four papers that present demonstrations of security, power and context-aware voice-activated circuitry, an emerging computing paradigm inspired by magnetic spin interactions, and a low power, low cost backplane interconnect.

- In Paper 24.1, KU Leuven presents the circuit level challenges for securing IoT devices. It provides an overview of the challenges of public key systems – both in today's technology and in the future quantum computing era. It outlines circuits that are used to prevent physical attack as well as Physically Uncloneable Functions that essentially provide per-device fingerprinting to further increase security.

- In Paper 24.2, KU Leuven presents a power and context aware acoustic sensor front-end architecture. Acoustic signal classification is initially done in a coarse but very power efficient manner. As more information is gathered about the nature of the signals, more precise but higher power classifications are enabled. This hierarchical wake-up enables power efficient always-on devices.

- In Paper 24.3, Hitachi presents a form of natural computing where a problem is mapped into an Ising model, which utilizes the behavior of magnetic spins. In this computing paradigm the magnetic spin interactions achieve an energy minimum – thereby converging to a solution.

- In Paper 24.4, Keio University and Japan Aerospace Exploration Agency present a 6.5Gb/s shared communications bus using electromagnetic connectors. This approach substantially reduces the power consumption, form factor and cost of high-speed connectors for use in satellite processing systems. The presented techniques can be applied to any backplane computing system in data servers as well as transport systems such as in aircrafts and automobiles.

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Session 25 Overview: RF Frequency Generation from GHz to THz

RF SUBCOMMITTEE

Session Chair: *Payam Heydari, University of California, Irvine, CA*
Session Co-Chair: *Taizo Yamawaki, Hitachi Ltd., Tokyo, JAPAN*

Subcommittee Chair: *Andreia Cathelin, STMicroelectronics, Grenoble, France*

Frequency generation circuits are ubiquitous building blocks in communication, sensing, and imaging systems. This session covers the latest advances in frequency generation, targetting reduction of noise, chip area, and power consumption in frequency synthesizers and VCOs. The session includes an E-band phase-locked-based frequency synthesizer that employs passive scaling to increase loop-filter capacitance, a phase-locked-based transmission array at 320GHz frequency, and a highly stable thin-film-based acoustic resonator achieving a stability of ±3 ppm from 0 to 90°C. Two papers describe techniques for reducing the effects of flicker noise in oscillators, another describes quantization noise cancellation in a fractional-N PLL, and another reduces PLL noise by manipulating impulse sensitivity and noise modulating functions of transistors. One paper addresses all-digital PLL design using voltage-mode digitization, and another describes inductorless PLL design to reduce power consumption.

- In Paper 25.1, UC San Diego and Analog Devices present a highly digital 3.5GHz fractional-N PLL with quantization noise cancellation using a dual-mode ring oscillator. It exhibits -93, -126, and -151dBc/Hz at 100kHz, 1MHz, and 20MHz offsets respectively.

- In Paper 25.2, Tokyo Institute of Technology presents an all-digital PLL that employs a voltage-domain digitization realized using an ADC. The PLL achieves an in-band phase noise of -112dBc/Hz and an rms jitter of 380fsec at 2.2GHz.

- In Paper 25.3, Broadcom presents an LC VCO that uses a common-mode resonance at twice the oscillation frequency to reduce the impact of flicker noise. A 3GHz prototype VCO exhibits -139.7dBc/Hz at 1MHz offset.

- In Paper 25.4, Delft University of Technology presents another technique based on setting up a trap for higher harmonics to lower the flicker noise contribution on the oscillator phase noise. The 4GHz VCO prototype achieves -123.4dBc/Hz at 1MHz offset.

- In Paper 25.5, Cornell University, MIT and STMicroelectronics present a 320GHz phase-locked-based 16-transmitter array in a 0.13μm SiGe process. The radiator achieves DC-to-RF efficiency of 0.54% and an EIRP of 22.5dBm.

- In Paper 25.6, HKUST and Hong Kong University of Science and Technology present a CMOS E-band PLL with passive scaling of the loop filter to increase the filter's effective capacitance. The core PLL occupies 0.6mm^2 of chip area with its loop filter taking 0.12mm^2 of this area. It exhibits better than -91.7dBc/Hz of phase noise at 1MHz offset.

- In Paper 25.7, UCLA presents a CMOS inductorless 2.4GHz frequency synthesizer that can achieve locked phase noise of -114dBc/Hz at 10MHz offset with 4mW of power consumption.

- In Paper 25.8, Sharif University of Technology and Cornell University present a CMOS 2.4GHz VCO that achieves low phase noise by manipulating the ISF and NMF of transistors. The VCO achieves -128.4dBc/Hz phase noise at 1MHz offset.

- In Paper 25.9, the University of Washington presents a CMOS 750MHz thin-film bulk acoustic resonator (FBAR) that achieves a stability of ±3 ppm from 0 to 90°C. A new temperature sensor is implemented that achieves 1.75mK resolution at 100msec sensing.

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Session 26 Overview: *Nyquist-Rate Converters*

DATA CONVERTERS SUBCOMMITTEE

Session Chair: *Hae-Seung Lee, Massachusetts Institute of Technology, Cambridge, MA*
Session Co-Chair: *Seng-Pan U, University of Macau, Macau, China*

Subcommittee Chair: *Boris Murmann, Stanford University, Stanford, CA, Data Converters*

Innovative circuit and architecture techniques are the driving force in improving the efficiency of high-speed Nyquist-rate data converters. In this session, creative approaches including new amplifier topologies, a wide variety of calibration schemes to remove errors resulting from finite gain, insufficient settling, and timing skew, as well as energy efficient data conversion techniques are presented.

- In Paper 26.1, the University of Michigan and Samsung present a SAR-assisted 2-stage pipeline ADC that employs a fully differential ring amplifier. Built in a 65nm technology, the converter achieves 71.5dB SNDR and 6.9fJ/conversion-step FoM at 50MS/s from a 1.2V supply.

- In Paper 26.2, Holst Centre/imec and TU Eindhoven present background calibration for capacitor mismatch in a SAR ADC. The capacitor mismatch is measured by switching the DAC code to its redundant counterpart in an optional extra clock cycle. Utilizing 2 comparators for better power efficiency, the converter achieves 5.5fJ/conversion-step FoM at 6.4MS/s.

- In Paper 26.3, Broadcom presents a resolution-configurable pipeline ADC for a 10GBASE-T receiver. The resolution can be reduced to 10b for short cable lengths to achieve lower power consumption in the receiver. Aided by residue amplifier gain calibration, a peak ENOB of 9.54 is achieved at 800MS/s.

- In Paper 26.4, KAIST and Samsung introduce a 1.6GS/s 10b Flash-assisted 2× time-interleaved SAR ADC where each channel consists of a 4b folding-Flash and 6 SAR ADCs. With background offset and timing skew calibration, the ADC achieves 9 ENOB with energy efficiency of 21fJ/conversion-step.

- In Paper 26.5, the University of Macau presents a 6b 5GS/s converter that interleaves 3b/cycle SAR ADCs with simplified hardware, leading to 39fJ/conversion-step FoM without timing skew calibration. A boundary-detection-code-overriding scheme improves the ADC's metastability rate.

- In Paper 26.6, Broadcom demonstrates a 28nm CMOS 10b pipelined/SAR hybrid ADC operating at 5GS/s. The ADC combines a 2.5b 2-way interleaved MDAC and 8b 8-way interleaved SAR ADCs with over-range calibration loops to allow SHA-less operation. The ADC consumes 150mW power including input and reference buffers.

- In Paper 26.7, KAIST and Samsung introduce a 2.6b/cycle, 4× time-interleaved SAR ADC with a power-gating technique that turns off hardware blocks after respective bit decisions are made, resulting in an energy efficiency of 30.4fJ/conversion-step at 1.7GS/s in 45nm CMOS.

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Session 27 Overview: *Physical Sensors*

IMAGERS, MEMS, MEDICAL AND DISPLAYS SUBCOMMITTEE

Session Chair: *Ralf Brederlow, Texas Instruments, Freising, Germany*
Session Co-Chair: *Michiel Pertijs, Delft University of Technology, Delft, The Netherlands*

Subcommittee Chair: *Makoto Ikeda, University of Tokyo, Tokyo, Japan*

This session presents recent achievements in the area of inertial, pressure, capacitance, magnetic, and temperature sensors. The first 3 papers are pushing power consumption, dynamic range, and drift of inertial sensors, enabling electronic stability control for new levels safety in the automotive sector and always-on navigation in mobile consumer devices. These presentations are followed by a fully integrated, small-form-factor tire pressure sensor. An innovative, energy-efficient read-out circuit for resonant sensors is followed by 2 presentations on energy- and area-efficient capacitance-to-digital converters. The session concludes with papers reporting a thermal-diffusivity-based temperature sensor for thermal monitoring, and a fluxgate-based magnetic-to-digital converter for contactless current sensing.

- In Paper 27.1, Robert Bosch presents a 3-axis gyroscope for electronic stability control with continuous self-test. The system shows a 20dB higher dynamic range and strongly improved offset drift compared to state-of-the-art sensors.
- In Paper 27.2, the National University of Singapore and Nanjing University of Science and Technology demonstrates a MEMS accelerometer for inertial navigation applications with a record-low bias instability of 0.4μg. Its resolution of 1.2μg/√Hz is the highest reported to date.
- In Paper 27.3, Robert Bosch introduces a gyroscope architecture for consumer applications that reduces offset drift and consumes 3× less power than the state of the art.
- In Paper 27.4, the University of Washington and Avago Technologies describe a sensor principle enabling a sub-mm^3 wireless pressure sensor for tire-pressure monitoring, more than 100× smaller than current systems.
- In Paper 27.5, TU Delft introduces a read-out circuit for resonant sensors capable of measuring resonance frequency and quality factor at 7.8× lower energy consumption than state-of-the-art systems.
- In Paper 27.6, the University of Michigan demonstrates a concept for capacitance-to-digital conversion that enables record-low energy efficiency and die size.
- In Paper 27.7, TU Delft presents a capacitance-to-digital converter based on period modulation that employs several design innovations to reduce size and energy consumption.
- In Paper 27.8, TU Delft introduces a highly digital thermal-diffusivity-based temperature sensor for use in SoC thermal monitoring. The sensor is the smallest for designs above 32nm.
- In Paper 27.9, Texas Instruments describes an integrated fluxgate read-out sensor for contactless current sensing. It digitizes the magnetic field at 750× higher bandwidth than state-of-the-art systems.

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ISSCC 2015
SESSION HIGHLIGHTS

CONDITIONS OF PUBLICATION

PREAMBLE

The Session Overviews to follow serve to capture the context, highlights, and potential impact, of the papers to be presented in each Session at ISSCC 2015 in February in San Francisco

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- From ISSCC's point of view, the phraseology included in the box below captures what we at ISSCC would like your readership to know about this, the 62nd appearance of ISSCC, on February 22nd to the 26th, 2015, in San Francisco.

This and other related topics will be discussed at length at ISSCC 2015, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 22-26, 2015, at the San Francisco Marriott Marquis Hotel.

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Session 2 Highlights: RF TX/RX Design Techniques

2.1 A Highly Linear Inductorless Wideband Receiver with Phase and Thermal Noise Cancellation

Hao Wu[1,2], Hooman Darabi[2], David Murphy[2], and M.-C. Frank Chang[1]
[1]University of California, Los Angeles, CA, [2]Broadcom Corporation, Irvine, CA

Context and State of The Art

- As there is no off-chip RF filtering available in a true Software-Defined-Radio (SDR), SDR receivers typically suffer from two fundamental issues when subject to large out-of-band blockers: gain compression and reciprocal mixing.
- Recently developed techniques based on passive mixers only address the first issue.

Technical Highlights

An inductorless receiver achieves a 2dB NF across the 0.3-to-3GHz band, while dissipating 55mW at 2GHz

- In Paper 2.1, UCLA and Broadcom present an inductorless receiver with an integrated RF ring VCO in 28nm CMOS, a new architecture with phase and thermal noise cancellation to address the shortcomings of current systems.

Applications and Economic Impact

- Compact and low-cost software-defined radio.
- Applicable to next generations of advanced solutions for cellular and connectivity.

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Session 3 Highlights:
Ultra-High-Speed Wireline Transceivers & Energy-Efficient Links

3.1 A 28Gb/s Multi-Standard Serial-Link Transceiver for Backplane Applications in 28nm CMOS

Bo Zhang, Karapet Khanoyan, Hamid Hatamkhani, Haitao Tong, Kangmin Hu, Siavash Fallahi, Kambiz Vakilian, Anthony Brewster
Broadcom, Irvine, CA

3.5 A 16-to-40Gb/s Quarter-Rate NRZ/PAM4 Dual-Mode Transmitter in 14nm CMOS

Jihwan Kim, Ajay Balankutty, Amr Elshazly, Yan-Yu Huang, Hang Song, Kai Yu, Frank O'Mahony
Intel, Hillsboro, OR

CONTEXT AND STATE OF THE ART

- In ISSCC 2014, a 28Gb/s transceiver implemented in 28nm CMOS capable of equalizing channel loss of up to 33dB while consuming 560mW power was presented. This year a lower power 28 Gb/s backplane transceiver in 28nm CMOS with better equalization performance is reported – specifically, 295mW to equalize up to 40dB of loss.
- Historically, NRZ has been the de facto standard for high-speed signaling, but challenges for data-rates beyond 32Gb/s have driven renewed interest in multi-level modulation. This year, a dual-mode NRZ/PAM4 transmitter implemented in 14nm tri-gate CMOS and operating up to 40Gb/s is reported.

TECHNICAL HIGHLIGHTS

Broadcom presents the lowest-power CMOS 28Gb/s transceivers over high-loss channels

- In Paper 2.1, Broadcom describes a multi-standard 28Gb/s transceiver in 28nm CMOS consuming 295mW at 25.78Gb/s per channel over 40dB loss of channels. The receiver has a linear equalizer and a 14-tap DFE. The transmitter uses a source-series terminated driver with a 5-tap FFE. The PLL has a tuning range of 20 to 29GHz with $0.23ps_{rms}$ jitter measured at 28.125GHz. The RX is measured at BER $<10^{-12}$ with a 23% eye margin.

Intel presents PAM4 Transmitters in 14nm tri-gate CMOS

- In Paper 2.5, Intel reports a quarter-rate NRZ/PAM4 dual-mode SerDes transmitter (TX) operating from 16 to 40Gb/s. The TX includes a feed-forward charge injected 4:1 serializer and quarter-rate clocking with duty-cycle/quadrature-error detection/correction circuits. The TX is fabricated in 14nm CMOS.

Applications and Economic Impact

- The demonstration of complete transceivers and energy-efficient equalizers operating at over 28+Gb/s is critical to extending the high speed signaling roadmap that supports and enables big data infrastructure.
- The realization of PAM4 transmitters demonstrates an alternative path for data rates higher than 32Gb/s.
- The demonstration of ultra-high data rate transmitters in 14nm tri-gate CMOS shows the feasibility of realizing high-speed I/O components in deeply scaled processes.

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Session 4 Highlights: Processors

4.1 22nm Next-Generation IBM System z Microprocessor

J. Warnock[1], B. Curran[2], G. Fredeman[2], Y. Chan[2], S. Carey[2], G. Salem[3], F. Schroeder[4], F. Malgioglio[2], G. Mayer[4], C. Berry[2], M. Wood[2], Y.-H. Chan[2], M. Mayo[2], C. Nagarajan[5], T. Werner[4], L. Sigal[6], R. Nigaglioni[7], J. Zitz[8], M. Ziegler[6], R. Puri[6], D. Malone[2], R, D. Wendel[4], D. Plass[2]
[1]IBM Systems and Technology Group (STG), Yorktown Heights, NY, [2]IBM STG, Poughkeepsie, NY,
[3]IBM STG, Williston, VT, [4]IBM STG, Boeblingen, Germany, [5]IBM STG, Bangalore, India,
[6]IBM Research, Yorktown Heights, NY, [7]IBM STG, Austin, TX,[8]IBM STG, Hopewell Junction, NY

4.2 A 20nm 32-Core 64MB L3 Cache SPARC M7 Processor

Penny Li, Jinuk Luke Shin, George Konstadinidis, Robert Masleid, Francis Schumacher, Venkat Krishnaswamy, Hoyeol Cho, Sudesna Dash, Heechoul Park, Dawei Huang, Wenjay Hsu, Vijay Srinivasan, Changku Hwang, Curtis McAllister
Oracle Corporation, Redwood Shores, CA

Context and State of the Art

- Exploding data growth and analytics requirements continue to demand a higher level of thread/core/memory integration to handle "Big Data" in data centers.
- Solutions to deliver cost-effective servers drive more sophisticated power management, as well as larger caches, and integration of components that historically were off chip, for today's power-constrained data centers.
- Increased pervasiveness of "Cloud Computing" raises the demand for low-power architectures that can scale out to many cores in dense form factors.

Technical Highlights

- **The latest 678mm^2, 22nm System z processor from IBM takes on Big Data challenges, with 8 multi-threaded cores and 64MB of L3 cache joined to high-bandwidth memory, SMP, and PCI interfaces**
  - IBM presents their 678mm^2 System z microprocessor chip implemented in IBM's 22nm SOI, high-κ metal-gate technology with 17 layers of wiring and functional thru 5GHz. The design comprises 8 dual-threaded cores with private 4MB eDRAM L2 cache and a 64MB unified eDRAM L3 cache, joined by a single global clock mesh and connected to high-bandwidth memory, SMP, and embedded PCI IO links.

- **Oracle announces the next-generation SPARC M7 featuring 32 cores with 1.6TB/s bandwidth 64MB L3 cache, an integrated database accelerator, to achieve a 3.0× performance improvement compared to its predecessor.**
  - The SPARC M7 processor with 32 S4 cores and 1.6TB/s bandwidth 64MB L3 cache to deliver more than 3.0× throughput performance over its predecessor. The chip, fabricated in 20nm, features an on-chip network (OCN) with 0.5TB/s data bandwidth, 280 SerDes lanes with 18Gb/s line rate and 1TB/s total bandwidth, and adaptive clocking scheme to deliver 2× supply noise guard-band reduction.

Applications and Economic Impact

- The IBM and Oracle processors represent two major aspects of processor development: extreme performance for Big Data handling and power efficiency for cloud computing. These higher levels of performance and energy efficiency in ever smaller form factors will extend our abilities towards increasing multimedia social computing to scientific and medical applications, such as understanding human genomes. Businesses will be able to consolidate workloads, increasing their data-processing capabilities and enabling lower cost to consumers.
- These processors represent a new level of integration, and innovative circuit techniques to deliver significantly better performance and capabilities. These efficient engines will enable servers to handle the most challenging technical applications and help to meet the needs for the world's growing cloud computing ecosystem.

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Session 5 Highlights: Analog Techniques

5.1 A 60V Auto-zero and Chopper Operational Amplifier with 800kHz Interleaved Clocks and Input Bias Current Trimming

Yoshinori Kusuda
Analog Devices, San José, CA

Context and State of the Art

- High-voltage op-amps connect industrial and automotive sensors to complex digital signal processing.
- High-frequency chopping enables high accuracy and high bandwidth.

Technical Highlights

Fully-integrated 60V input common-mode range amplifier enables on-chip sensor read-out in industrial applications

- In paper 5.1 Analog Devices presents a chopper op-amp with 800kHz interleaved clocks, moving the majority of the switching PSD up to 4.8MHz, above the op-amp unity gain frequency of 3.2MHz. The 800kHz clock frequency is 2.4× faster than previous work. It uses a novel trimming method achieving 10× input bias current reduction. Maximum input bias current is reduced from 2nA to 200pA by post production trimming, using on-chip charge mismatch compensation circuit.

Applications and Economic Impact

- Analog design techniques, such as chopper stabilization, lead to high levels of integration and high performance, enabling industrial applications in the internet of things.

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Session 5 Highlights: Analog Techniques

5.5 A Forward Body Bias Tuned 450MHz Gm-C 3rd Order Low-Pass Filter in 28nm UTBB FD-SOI with >1dBVp IIP3 over a 0.7 - 1V supply

J. Lechevallier[1,2], R. Struiksma[1], H. Sherry[2], A. Cathelin[2], E. Klumperink[1], B. Nauta[1]
[1]University of Twente, Enschede, The Netherlands, [2]STMicroelectronics, Crolles, France

Context and State of the Art

- FD-SOI is one of the candidate technologies for next-generation high performance SoC.
- Accurate filters with low-power consumption are key blocks for communication systems.
- Filters with wide tuning range are required for multi-standard software defined radio receivers.

Technical Highlights

28nm FD-SOI technology shows its potential for high-performance analog design

- In paper 5.5 STMicroelectronics and University of Twente present a new forward-body-bias filter with a new tuning mechanism. The filter maintains filtering shape, cut-off frequency and linearity over a wide supply range.

Applications and Economic Impact

- Moore's law often introduces difficulties and challenges for analog designers. Scaling generally does not apply to analog circuits and performance might be degraded. However, this paper proves that new technologies such as FD-SOI can also offer opportunities for reducing power consumption and enhancing performance of key analog blocks, making them suitable for SoC integration.

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Session 6 Highlights: Image Sensors and Displays

6.2 133Mpixel 60fps CMOS Image Sensor with 32-Column Shared High-Speed Column-Parallel SAR-ADCs

R. Funatsu[1], S. Huang[2], T. Yamashita[1], K. Stevulak[2], J. Rysinski[2], D. Estrada[2], S. Yan[2], T. Soeno[1], T. Nakamura[1], T. Hayashida1, H. Shimamoto[1], B. Mansoorian[2]
[1]NHK Science & Technology Research Laboratories; [2]Forza Silicon

6.8 A Pen Pressure Sensitive Capacitive Touch System Using Passive Resonant Stylus

C.B. Park[1], S.H. Park[1], K.D. Kim[1], S.H. Park[1], Y.H. Huh[1], G.H. Cho[1], S.S. Park[2], J.W. Park[2], B.H. Kang[2],
[1]KAIST, Daejeon, Korea; [2]Samsung, Gyeonggi, Korea

Context and State of the Art

- 8K ultrahigh-definition television (UHDTV) systems have been promoted to realize next-generation highly realistic broadcasting.
- Today's touch-screen displays are extending their modes of operation: simultaneous multi-finger touch and active/passive sensing are being introduced. The first 6-bit pen pressure sensing with passive resonant stylus without any special layer, such as EMR (Electro Magnetic Resonant) touch system, is introduced.

Technical Highlights

NHK Science & Technology Lab reports the first 35-mm format image sensor for 8K video

- In Paper 6.2, NHK Science & Technology Research Lab and Forza Silicon present a 133Mpixel 60fps 12b image sensor for 8K video. The pixel size in 0.18μm technology is 2.45×2.45μm^2. Front-end multiplexing analog readout circuitry and column-parallel successive approximation register ADCs are used.

KAIST introduces a pen pressure sensing system with passive resonant stylus that achieves 49dB SNR with 1mmΦ 6-bit resolution

- In Paper 6.8, KAIST and Samsung present a pen pressure sensitive capacitive touch system with passive resonant stylus that can replace costly EMR-based systems. The multi-TX scanning and charge demodulating integrator scheme achieves 49dB SNR with 1mmϕ 6b resolution pen pressure sensing.

Applications and Economic Impact

- New high-frame-rate and high-resolution imaging devices are enabling cameras for the evolution towards 8K UHDTV broadcasting. The full-size image format provides high sensitivity and dynamic range. There will be a push for further R&D and commercialization in areas related to UHDTV (imaging, data transmission, and displays) in order to deliver highly realistic and sensational video content to the home.
- Pen pressure sensitive capacitive touch system with passive resonant stylus can replace the costly EMR-based systems, which need an additional layer under the display module. By combining this with 3D touch sensing, we foresee that lighter and realistic 3-dimentional mobile applications will emerge.

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Session 7 Highlights: Non-Volatile Memory Solutions

7.2 A 128Gb 3b/Cell V-NAND Flash Memory with 1Gb/s I/O Rate

J-W. Im, W-P. Jeong, D-H. Kim, S-W. Nam, D-K. Shim, M-H. Choi, H-J. Yoon, D-H. Kim, Y-S. Kim, H-W. Park, D-H. Kwak, S-W. Park, S-M. Yoon, W-G. Hahn, J-H. Ryu, S-W. Shim, K-T. Kang, S-H. Choi, J-D. Ihm, Y-S. Min, I-M. Kim, D-S. Lee, J-H. Cho, O-S. Kwon, J-S. Lee, M-S. Kim, S-H. Joo, J-H. Jang, S-W. Hwang, D-S. Byeon, H-J. Yang, K-T. Park, K-H. Kyung, J-H. Choi
Samsung, Hwasung, Korea

7.3 A 28nm Embedded SG-MONOS Flash Macro for Automotive Achieving 200MHz Read Operation and 2.0MB/s Write Throughput at T_j of 170°C

Y. Taito, M. Nakano, H. Okimoto, M. Hosoda, D. Okada, T. Ito, T. Kono, K. Noguchi, H. Hidaka, T. Yamauchi
Renesas Electronics, Japan

Context and State of the Art

- Non-volatile memory cost-per-bit scaling is crucial for systems such as wearables, IoT, and data centers.
- The highest density 3D NAND Flash published to date is 128Gb 2b/cell (MLC) NAND with 24 stacked WL layers.
- Stacking higher and storing more bits per cell are needed for next-generation non-volatile memories.

- The most advanced technology node of embedded Flash macros to date is 40nm.
- Advances in automotive technology, such as sophisticated real-time engine controls for higher fuel-efficiency and advanced driver assistance systems (ADAS), are expanding the application range of embedded flash memory (eFlash).
- Automotive Flash requires faster random access, shorter rewrite time and larger memory capacity in eFlash, and robust operation under extremely high junction temperature (T_j) of 170°C.

Technical Highlights

Samsung presents the world's first 128Gb 3b/cell V-NAND device with 32 stacked WL layers

- [7.2] Fastest t_{PROG} of 700µs in a TLC NAND by introducing high-speed program (HSP) and data pre-processing technique.
- [7.2] 1Gb/s I/O rate by applying multiple techniques including an open-loop duty-cycle corrector and dynamic bandwidth control scheme.

Renesas presents the world's first 28nm embedded Flash macros using SG-MONOS technology.

- [7.3] 200MHz random read at T_j = 170°C with more than 10× longer TDDB lifetime of WL drivers achieved by the combination of 28nm SG-MONOS memory array and temperature-adjusted overdrive wordline (WL) voltage control.
- [7.3] High write throughput of 2.0MB/s by using source-side injection (SSI) programming with negative back-bias.

Applications and Economic Impact

- [7.2] Future Flash memory scaling is expected to continue via vertical WL-stack and TLC. Samsung's V-NAND can replace existing NAND Flash chips.
- [7.3] eFlash is crucial for automotive applications, IoT, wearables and SoCs. SG-MONOS scaling beyond 4Xnm is challenging and Renesas Electronics 28nm chip shows that scaling continues.

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Session 8 Highlights: Low-Power Digital Techniques

8.1 An 80nW Retention 11.7pJ/cycle Active Subthreshold ARM Cortex-M0+ Subsystem in 65nm CMOS for WSN Applications

J. Myers, A. Savanth, D. Howard, R. Gaddh, P. Prabhat, D. Flynn
ARM Ltd, Cambridge, UK

8.3 A 10.5µA/MHz at 16MHz Single-Cycle Non-Volatile Memory-Access Microcontroller with Full State Retention at 108nA in a 90nm Process

V. Singhal, V. Menezes, S Chakravarthy, M. Mehendale
Kilby Labs, Texas Instruments, Bangalore, India

Context and State of the Art

- The internet-of-things (IoT) promises to connect 50 billion devices by 2020. The event-driven, bursty nature of local compute tasks for data aggregation and analysis in these ubiquitous nodes demands micro-controllers that provide both very low retention power and low energy per operation.
- Current state-of-the-art IoT microcontrollers consume more than 100µA/MHz full system active power and >1µA retention power.

Technical Highlights

Highest reported energy efficiency ARM and TI IoT micro-controllers, offering an order of magnitude lower full state retention power and lowest active energy

- In Paper 8.1, ARM introduces a Cortex M0+-based sub-threshold processor in 65nm CMOS, scaling from 29kHz with 850nW active power at 250mV, to 66MHz at 900mV, while enabling 80nW CPU and SRAM state retention.
- In Paper 8.3, Texas Instruments exploits adaptive body bias in a 90nm 3V Flash process with an MSP430-based processor to achieve 10.5µA/MHz at 16MHz, and full state retention of the CPU and SRAM, consuming 108nA.

Applications and Economic Impact

- The ability to network compact devices with embedded CPU and memory resources enables IoT applications in very diverse fields. Wearable computing will enable both advanced lifestyle monitoring, as well as remote patient monitoring, reshaping the health care market. Additionally, industrial and infrastructure monitoring will increase the efficiency of factories, logistic processes and smart buildings. IoT devices will produce data for Big Data analysis in the cloud, in application areas such as crowd sourcing and wide knowledge extraction.
- Cisco predicts there will be 50 billion devices connected to the Internet by 2020 with the potential economic impact of IoT estimated at $2 trillion to $7 trillion per year by 2025. Gartner and IDC forecast similar mind boggling markets.

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Session 9 Highlights: High-Performance Wireless

9.2 A Single-Chip HSPA Transceiver with Fully-Integrated 3G CMOS Power Amplifiers

José Moreira[1], Stephan Leuschner[1], Nenad Stevanovic[1], Harald Pretl[2], Peter Pfann[1], Ronald Thueringer[1], Martin Kastner[1], Christian Proell[2], Andreas Schwarz[2], Florian Mrugalla[1], Jimena Saporiti[2], Umut Basaran[3], Andreas Langer[1], Tobias D. Werth[1], Timo Gossmann[1], Boris Kapfelsperger[1], Johann Pletzer[2]
[1]Intel Mobile Communications, Neubiberg, Germany, [2]DMCE, Linz, Austria, [3] AVL,Gebze Kocaeli, Turkey

9.7 An LTE SAW-less Transmitter Using 33% Duty-Cycle LO Signals for Harmonic Suppression

Yen-Horng Chen, Neric Fong, Bing Xu, Caiyi Wang
MediaTek, Hsinchu, Taiwan

Context and State of The Art

- Fully integrated HSPA devices have been published and in the market place prior to now. Integration of power amplifiers has not been published until now.
- Similarly, 2/3/4G cellular transceivers needed very tight filtering requirements in order to meet tight emission requirements.

Technical Highlights

A fully digital polar modulator and a single-stage linear PA (9.2)

- In Paper 9.2, RX sensitivity of <-110dBm for 23.5 dBm of output power is achieved at the antenna connector. Coupling from the PA output to the RX inputs as well as from the DC/DC converter to the RX does not produce any significant degradation.

An LTE transmitter uses 33% duty-cycle LO signals for harmonic suppression (9.7)

- In Paper 9.7, <-70dBc CIM3 is achieved, meeting the Band-13 PSB emission without external filter.

Applications and Economic Impact

- Higher cellular integration leads to lower bill-of-material and smaller footprint for both 3G and 4G.
- Simplification of the overall system complexity.
- Ability for concurrent receive and transmit operations, while being on the same die.

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Session 10 Highlights: Advanced Wireline Techniques and PLLs

10.2 An FSK Plastic Waveguide Communication Link in 40nm CMOS

Wouter Volkaerts, Niels Van Thienen, Patrick Reynaert
KU Leuven, ESAT/MICAS, Leuven, Belgium

Context and State of the Art

- Several decades of electrical link innovation have enabled very high data-rate links that were considered impossible in the past. However, physical limitations in loss limit the distance over which copper-based interconnect can operate efficiently.
- For longer distance transmission optical communication is the traditional solution, but the difficulty and cost of integrating optics remain daunting barriers – especially for moderate distance applications of several meters.

Technical Highlights

KU Leuven presents a plastic link transmitter and receiver operating up to 12.7Gb/s

- Coupling to and transporting data through a plastic waveguide using a modulated >100GHz RF signal enables a much lower cost solution since it requires no external components and can be realized in a completely standard CMOS process.
- This paper presents a full plastic fiber link solution, including a 40nm CMOS TX with an on-chip dipole coupler, a 40nm RX with a bond-wire based antenna, and the plastic fiber. The link uses FSK modulation of a 120GHz carrier to achieve data rates of up to 12.7Gb/s at an energy efficiency of 1.8pJ/b.

Applications and Economic Impact

- The server racks within large data centers often require interconnects of several meters in length, and would directly benefit from such a low-cost solution.
- Since such a waveguide based link does not require galvanic connection to the IC, applications such as automotive interconnect that require stringent isolation levels would be well served by this approach as well.

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Session 11 Highlights: Sensors and Imagers for Life Sciences

11.4 A 67,392 SPAD PVTB-Compensated Multi-Channel Digital SiPM with 432 Column-Parallel 48ps 17b TDCs for Endoscopic Time-of-flight PET

E. Carimatto[1], S. Mandai[1], E. Venialgo[1], T. Gong[2], G. Borghi[3], D. Schaart[4], E. Charbon[1,2]
[1]Delft University of Technology, Delft, Netherlands; [2]Ecole Polytechnique Federale Lausanne, Lausanne, Switzerland

Context and State of the Art

- Positron Emission Tomography (PET) scanners compatible with Magnetic Resonance Imaging (MRI) open the way to new frontiers in the field of cancer diagnostics. In order to cope with the high magnetic field, a solid-state solution must be used instead of the traditional Photomultiplier Tube (PMT)s.

Technical Highlights

Delft demonstrates 432 columns of single-photon sensors with <1.8% optical crosstalk enabling a new level of performance in PET/MR

- This design has one of the best TDC accuracies (48ps) and levels of parallelism (432 columns), which allows for exceptional image quality.
- The system is robust to temperature variations.

Applications and Economic Impact

- Minimizing the dosage of radioactive tracers is an active area of clinical research and can possibly be achieved in part by using this miniaturized endoscopic sensor.
- CMOS silicon photomultipliers (SiPM) will replace PMTs, allowing higher spatial and energy resolution, better time resolution and lower cost. This opens the way to low-cost and high-performance diagnostic PET systems for pre-clinical, and eventually clinical, applications.
- Precision and personalized medicine asks for companion diagnostic tests and molecular imaging, ultimately leading to better and cheaper healthcare.

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Session 12 Highlights:
Inductor-Based Power Conversion

12.5 An Error Based Controlled Single-Inductor 10-Output DC-DC Buck Converter with High Efficiency at Light Load Using Adaptive Pulse Modulation

Min-Yong Jung, Sang-Hui Park, Jun-Suk Bang, Dong-Chul Park, Se-Un Shin, Gyu-Hyeong Cho
KAIST, Korea

Context and State of the Art

- Reducing the number of large external components, especially inductors, is a very important issue for power management ICs.
- Single-Inductor Multiple-Output (SIMO) converter is an excellent candidate to provide powers with small volume and low cost.

Technical Highlights

KAIST presents a Single-Inductor 10-Output DC-DC Buck Converter with high light-load efficiency featuring a hybrid topology of switching converter and linear regulator

- In Paper 12.5, KAIST presents a SIMO Buck converter with 10 outputs. Each output has its own switching frequency according to its load condition, thereby stable light load operation can be maintained with high efficiency. It features a hybrid topology composed of a current mode switching converter and a class-AB amplifier to balance the inductor current.

Applications and Economic Impact

- The SIMO solution can be utilized in many systems requiring multiple outputs, alleviating the need for high-cost and bulky external inductors in the system. The resulting reduction in cost and size provides a more attractive solution for portable systems.

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Session 12 Highlights: Inductor-Based Power Conversion

12.7 A Power-Management ASIC with Q-Modulation Capability for Efficient Inductive Power Transmission

Mehdi Kiani[1], Byunghun Lee[2], Pyungwoo Yeon[2], Maysam Ghovanloo[2]
[1]Pennsylvania State University, University Park, PA; [2]Georgia Institute of Technology, Atlanta, GA

Context and State of the Art

- There are increasing needs for higher performance in wireless power transmission enabling more efficient power delivery over longer distance.

Technical Highlights

Pennsylvania State University and Georgia Institute of Technology introduce a new Q-modulation technique for adaptive inductive power transmission

- In Paper 12.7, Pennsylvania State University and Georgia Institute of Technology present a Q-modulation power management IC with automatic load transformation capability, increasing power transmission efficiency by compensating variations in load and coupling distance.

Applications and Economic Impact

- The use of inductive power transmission is expected to see an explosive growth over the next decade as engineers try to cut the last cord from mobile electronics, small home appliances, and even electric vehicles. The increased power transfer efficiency over longer distance with small overhead in size and volume will enable the rapid growth of this wireless market.

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Session 13 Highlights: Energy-Efficient RF Systems

13.3 A 10mW Bluetooth Low-Energy Transceiver with On-Chip Matching

J. Prummel, J. Willms, M. Ancis, M. Papamichail, R. Todi, W. Aartsen, W. Kruiskamp, J. Haanstra, E. Opbroek, S. Rievers, P. Seesink, H. Woering, C. Smit
Dialog Semiconductor, 's-Hertogenbosch, The Netherlands

13.5 A -97dBm-Sensitivity Interferer-Resilient 2.4GHz Wake-Up Receiver Using Dual-IF Multi-N-Path Architecture in 65nm CMOS

C. Salazar[1], A. Kaiser[2], A. Cathelin[1], J. Rabaey[3],
[1]STMicroelectronics, [2]University of Lille, [3]University of California at Berkeley

Context and State of The Art

- Low power radios and their associated wake-up radios are essential building blocks for autonomous wireless applications, requiring innovation in both architecture and circuit design techniques.
- A fully integrated autonomous wireless solution is needed that allows direct operation from battery or USB power.

Technical Highlights

A 55nm Bluetooth Low Energy SoC transceiver with fully integrated matching network and RX-TX switch achieves blocking performance >35 dB better than required by the standard (13.3)

- The BLE radio features a fully integrated antenna matching network and achieves a -94dBm receiver sensitivity level. It also achieves blocking performance 35dB better than required by the standard. Transmit output power is programmable from -20dBm up to 0dBm.
- The total chip includes Link Layer Processor (LLP) with AES-128 encryption engine, ARM Cortex M0 microprocessor, 84KB ROM, 42KB RAM, 8KB Retention RAM and 32KB OTP, a 10b general-purpose SAR-ADC, 32kHz real time clock (either crystal or <500ppm internal RC), Quadrature Decoder, SPI I^2C and UART interfaces.
- The IC features an integrated BUCK/BOOST DC-DC converter to operate directly from Lithium coin cells or alkaline batteries. In total it consumes 10mW in TX and 11mW in RX operation.
- The transceiver is fabricated in TSMC standard 55nm CMOS technology (1P6M), occupies 5.9mm^2 and is available in a 2.4×2.4mm^2 32-pin WLCSP or 48-pin QFN package.

A 2.4GHz low-data-rate wake-up receiver for ultra-low power and compact Wireless Sensor Nodes with -97dBm sensitivity and only 99uW power consumption (13.5)

- This wake-up radio operates at 2.4GHz and presents a sensitivity of -97dBm for 10kb/s and 10^{-3} BER, from a 0.5V supply.
- OOK modulation has been chosen for its energy efficiency, while the use of a cascaded multi-layer N-path filtering approach provides best-in-class interferer rejection, while avoiding expensive off-chip components such as BAW or crystals.
- The receiver is integrated in 65nm CMOS, occupies an active area of 0.0576mm^2 and consumes 99uW. The die is flip-chipped in a compact BGA package together with SMD components.

Applications and Economic Impact

- In the context of IoT, wearable and wireless sensor- connected devices, extreme low cost, low power and compact radio solutions are mandatory to create the network nodes.
- These low-power sensor networks are the last mile of big-data global solutions.

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Session 14 Highlights:
Digital PLLs and SoC Building Blocks

14.2 A Physically Unclonable Function with BER $<10^{-8}$ for Robust Chip Authentication Using Oscillator Collapse in 40nm CMOS

Kaiyuan Yang, David Blaauw, Dennis Sylvester
University of Michigan, Ann Arbor, MI

14.3 15fJ/b Static Physically Unclonable Functions for Secure Chip Identification with <2% Native Bit Instability and 140× Inter/Intra PUF Hamming Distance Separation in 65nm

Massimo Alioto, Anastacia Alvarez, Wenfeng Zhao
National University of Singapore, Singapore, Singapore

Context and State of the Art

- Security is a growing concern in semiconductor chips. Ensuring the authenticity of the chips being placed in today's systems is critical and a number of components have been proposed in the literature, including true random number generators, power attack avoidance, and physically unclonable functions (PUFs).
- Counterfeit chips are becoming more common as rogue organizations seek backdoor methods to gain access to user data.
- Physically unclonable functions (PUFs) are a proposed method for chip authentication. A PUF maps an input code to an output code uniquely for each manufactured chip – a digital fingerprint if you will. Use of such a technique enables a system to validate that the chip is not counterfeit, thus helping secure user data.

Technical Highlights

The University of Michigan proposes a low-error small, low-power PUF.

- In Paper 14.2, the University of Michigan proposes a PUF with error rate of $<10^{-8}$ across process, voltage, and temperature variation. The low-error PUF enables simpler systems through elimination of complex calibration schemes.

The National University of Singapore proposes a PUF that can be easily integrated into a chip.

- In Paper 14.3, the National University of Singapore proposes two different physically unclonable functions and an architecture which removes a need for manual placement and connection of these functions. This eases integration and improves the reach of the technology to more design teams and chips.

Applications and Economic Impact

- Improving our ability to authenticate chips is critical to maintaining security in modern complex electronic systems. Counterfeit silicon is becoming more prevalent, enabling back-door access to user data.
- Building lower-power, more robust PUFs will expand their application. Specifically, more low-power, very small systems will be able to integrate PUFs and provide authentication to halt counterfeiting without an onerous increase in chip power or reduction in features.
- Simplifying the use and inclusion of PUFs in chips will hasten the expansion of the authentication technology.

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Session 15 Highlights: Data-Converter Techniques

15.2 A 4.5mW CT Self-Coupled ΔΣ Modulator with 2.2MHz BW and 90.4dB SNDR Using Residual ELD Compensation

C. Ho, C. Liu, C. Lo, H. Tsai, T. Wang, Y. Lin,
MediaTek, Hsinchu City, Taiwan

15.5 A 0.6V 1.17ps PVT-Tolerant and Synthesizable Time-to-Digital Converter Using Stochastic Phase Interpolation with 16× Spatial Redundancy in 14nm FinFET Technology

S. Kim, W. Kim, M. Song, J. Kim, T. Kim, H. Park
Samsung Electronics, Hwaseong, Korea

Context and State of the Art

- In order to relax the analog front-end filter design for wireless communication applications, a high-dynamic-range ADC is required with low power consumption to prolong battery life. Continuous-time delta-sigma modulators combine excellent power efficiency with high resolution and inherent anti-aliasing filtering.
- The advanced 14nm FinFET CMOS technology node offers state-of-the-art digital circuit performance, high speed, small area, and low leakage. A major challenge of designing mixed-signal circuits in smaller feature size technologies is to guarantee high yield under severely varying PVT corners.

Technical Highlights

MediaTek demonstrates a 4.5mW continuous-time delta-sigma modulator with 90dB SNDR in 2.2MHz bandwidth

- In Paper 15.2, MediaTek presents a continuous-time self-coupling (CTSC) ΔΣ modulator with residual ELD compensation and DAC linearity enhancement techniques. The ADC achieves an SNDR of 90.4dB with a 2.2MHz bandwidth. It is implemented in 55nm CMOS and consumes only 4.5mW.

Samsung Electronics reports the first TDC synthesized with 3D FinFET transistors in 14nm technology

- In Paper 15.5, Samsung Electronics presents a stochastic time-to-digital converter (TDC) architecture in 14nm FinFET technology containing 2^{14} delay cells, achieving 1.17ps resolution at 100MS/s, consuming 0.78mW and occupying 0.035mm^2. Performance is robust over corners, temperature (-25 to 125°C) and supply voltage (0.6 to 1.0V).

Applications and Economic Impact

- The increasing resolution and power efficiency of continuous-time delta-sigma modulators further increases the integration level of wireless receiver systems. At the same time, power consumption is lowered to improve battery life for next-generation mobile devices.
- The stochastic TDC architecture demonstrates the feasibility of designing high-precision mixed-signal circuits in a very advanced 14nm FinFET technology node. The performance is shown to be robust over severely varying process, voltage and temperature corners. These features are key in enabling future wireless integrated systems.

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Session 16 Highlights:
Emerging Technologies Enabling Next-Generation Systems

16.1 An Ultra-Thin Flexible CMOS Stress Sensor Demonstrated on an Adaptive Robotic Gripper

Yigit Mahsereci[1], Stefan Saller[2], Harald Richter[3], Joachim Burghartz[3]
[1]Institut fuer Nano- und Mikroelektronische Systeme (INES), Stuttgart, Germany, [2]*Festo AG&Co. KG,* [3]*IMS CHIPS, Stuttgart, Germany*

16.2 A Large-area Image Sensing and Detection System Based on Embedded Thin-film Classifiers

Warren Rieutort-Louis, Tiffany Moy, Zhuo Wang, Sigurd Wagner, James C. Sturm, Naveen Verma
Princeton University, Princeton, NJ

Context and State of the Art

- Wearable electronics and sensing electronics for robotics require large area sensing with mechanical flexibility.
- Large area electronics enables deployment of sensors which span dimensions on the order of a few meters.
- The poor quality of transistors available in the large area technologies makes high quality sensing a significant issue.

Technical Highlights

An ultra-thin bendable CMOS stress sensor for robotic gripper with stress compensation on sensitive analog/digital circuitry

- In Paper 16.1, INES, Festo AG and IMS CHIPS present an ultra-thin (20µm) bendable CMOS stress sensor (2×10b digital output for stress along both axis), where both the analog and digital parts of the circuit are compensated for stress and temperature. The application is demonstrated on a robotic gripper.

First demonstrated thin-film image sensing and classification system based on a-Si photoconductors and TFT classifiers

- In Paper 16.2, Princeton University presents a thin-film image sensing and detection system based on a-Si photoconductors and embedded TFT classifiers. These TFT classifiers in the large area system reduce the total signals required for detection by 9× before connecting to an external CMOS IC.

Applications and Economic Impact

- The ultra-thin chips have the potential to become part of hybrid systems on foil with applications in wearable electronics, robotics, medical diagnostics and flexible displays.

- High-quality image detection can be performed directly using thin-film transistors. This enables applications that perform sensing on scales of up to a few meters, such as X-ray imagers.

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Session 16 Highlights: Emerging Technologies Enabling Next Generation Systems

16.5 A NEMS-array Control IC for Sub-attogram Gravimetric Sensing Applications in 28nm CMOS Technology

Nicolas Delorme[1], Christophe Le Blanc[1], Alessandro Dezzani[1], Mickaël Bely[1], Alexandre Ferret[1], Simon Laminette[1], Jérôme Roudier[1], Eric Colinet[2]
[1]ASYGN, Montbonnot Saint Martin, France, [2]Apix Analytics, Grenoble, France

Context and State of the Art

- Existing solutions for gravimetric sensing employ discrete electronic boards and specialized lab instruments making them bulky.
- NEMS arrays are a viable candidate for gravimetric applications such as gas sensing, mass spectrometry and biochemical analysis due to their ultra-small form factor and excellent sensitivity.

Technical Highlights

First integrated circuit for driving and readout of NEMS array in 28nm CMOS

- In Paper 16.5, ASYGN and APIX analytics present an integrated circuit for a Nano-ElectroMechnical System (NEMS) for attogram gravimetric sensing applications. A NEMS-array driving and readout IC fabricated in a 28nm CMOS process provides the required performance for attogram-level mass measurements (10MHz-to-1GHz driving frequencies and 10V drive voltage). The silicon area is $0.9mm^2$ and requires 68mW of power.

Applications and Economic Impact

- The proposed system is designed to replace discrete electronics and dedicated lab instruments, providing the form factor, power and cost reduction necessary for mass-market applications.

- It paves the way towards the full integration of a comprehensive hand-held gas chromatography system.

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Session 17 Highlights: Embedded Memory and DRAM I/O

17.1 A 0.6V, 1.5GHz 84Mb SRAM Design in 14nm FinFET CMOS Technology

Eric Karl, Zheng Guo, James Conary, Jeffrey Miller, Yong-Gee Ng, Satyanand Nalam, Daeyeon Kim, John Keane, Uddalak Bhattacharya, Kevin Zhang
Intel, Hillsboro, OR

17.4 A 14nm 1.1Mb Embedded DRAM Macro with 1ns Access

Gregory Fredeman, Donald Plass, Abraham Mathews, Kenneth Reyer, Thomas Knips, Thomas Miller, Elizabeth Gerhard, Dinesh Kannambadi, Chris Paone, Dongho Lee,
Daniel Rainey, Michael Sperling, Michael Whalen, Steven Burns
IBM, Poughkeepsie, NY

Context and State of the Art

- SRAM is the main barrier to logic scaling.
- Since the demonstration of 22nm FinFET products at the ISSCC in 2012, 2nd generation FinFET products are now being developed.
- High-speed eDRAM is an important alternative to SRAM in certain applications to meet unabated growth in demand for high-bandwidth high-capacity on-chip memory.
- This year, IBM demonstrates an embedded DRAM in their leading edge 14nm FinFET technology to bridge the capacity and bandwidth gap.

Technical Highlights

Intel demonstrates a 14nm SRAM with the smallest bit cell reported to date

- In Paper 17.1, Intel presents an 84Mb embedded SRAM fabricated in 14nm FinFET technology featuring the smallest bit cells to date at 0.050µm^2 for high density and 0.058µm^2 for low voltage. 1.5GHz operation at 0.6V is demonstrated.

IBM introduces first 14nm eDRAM for high-performance microprocessor caches

- In Paper 17.4, IBM presents a 1.1Mb embedded DRAM in 14nm FinFET technology for high-performance microprocessor caches. The 0.01747µm^2 cell features a deep trench capacitor and a thick oxide FinFET access device. An array access time of 1.0ns is demonstrated.

Applications and Economic Impact

- Demonstrates FinFET transistor scaling to 14nm node with extremely aggressive bit cell density.
- This technology and the innovative circuit techniques enable low-voltage operation to enable smaller and lighter personal devices with increasing functionality in the cloud.
- Demonstrates eDRAM in 14nm FinFET technology
- With more than 50% of the transistors used for on-chip memory in current high-performance microprocessors, eDRAM represents a key enabler for future high-bandwidth computing.

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Session 18 Highlights: SoCs for Mobile Vision, Sensing, and Communications

18.1 A 2.71nJ/Pixel 3D-Stacked Gaze-Activated Object-Recognition System for Low-Power Mobile HMD Applications

I. Hong, K. Bong, D. Shin, S. Park, K. Lee, Y. Kim, H.-J. Yoo
KAIST, Daejeon, Korea

18.2 A 1.9TOPS and 564GOPS/W Heterogeneous Multi-Core SoC with Color-Based Object Classification Accelerator for Image-Recognition Applications

J. Tanabe, S. Toru, Y. Yamada, T. Watanabe, M. Okumura, M. Nishiyama, T. Nomura, K. Oma, N. Sato, M. Banno, H. Hayashi, T. Miyamori
Toshiba, Kawasaki, Japan

Context and State of the Art

- Head-mounted delays are gaining traction in gaming and other forms of wearable devices. Consumers are demanding more natural user interfaces for head-mounted display applications.
- Computing is increasingly used in automotive applications to improve vehicle safety and ease the burden on drivers.

Technical Highlights

A gaze recognition system for wearable devices – KAIST shows the way!

- KAIST presents a gaze recognition system for wearable electronics. A gaze image sensor and object recognition processor are 3D stacked together, achieving 151.3GOPS and 2.71nJ/pixel energy consumption.

Toshiba presents an advanced driver-assistance system (ADAS), capable of detecting pedestrians and other objects, implemented in a heterogeneous multi-core SoC.

- This 40nm SoC achieves 1.9TOPS, 564GOPS/W and a 99.65% pedestrian detection rate using four color-based feature descriptors. Power-efficient design enables the chip to operate with passive cooling in a high-temperature automotive environment.

Applications and Economic Impact

- The next generation of wearable devices demands more natural user interfaces, while drawing low power consumption. Gaze-activated user interfaces which automatically detect the eye's focus are the way forward.
- As the demand for safe driving grows, advanced driver-assistance systems need higher detection rates for obstacles in a vehicle's path, and lower false positive rates. High-performance and low-power chips for advanced driver-assistance systems have the potential to reduce accident rates and save lives.

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Session 19 Highlights: Advanced Wireless Techniques

19.1 Reconfigurable Receiver with >20MHz Bandwidth Self-Interference Cancellation Suitable for FDD, Co-existence and Full-Duplex Applications

J. Zhou, T.-H. Chuang, T. Dinc, H. Krishnaswamy
Columbia University, New York, NY

19.2 A Self-Interference-Cancelling Receiver for In-Band Full-Duplex Wireless with High SFDR under Cancellation of Strong TX leakage

D.-J. Broek, E. Klumperink, B. Nauta
University of Twente, Enschede, The Netherlands

19.3 Reconfigurable SDR Receiver with Enhanced Front-End Frequency Selectivity Suitable for Intra-Band and Inter-Band Carrier Aggregation

R. Chen, H. Hashemi
University of Southern California, Los Angeles, CA

Context and State Of The Art

- New wireless standards and the push for higher wireless network capacity require architecture and circuit-level innovations in modern transceivers. Self-interference cancellation is required for concurrent transmission and reception in the same frequency band and to help coexistence of different radios operating in nearby bands.

- Software-Defined-Radio (SDR) receivers introduce great flexibility in radio front-ends and can be exploited to aggregate carriers from different frequency bands as required from the latest wireless communication standards.

Technical Highlights

- **Reconfigurable receiver with wideband self-interference cancellation addresses FDD systems, full-duplex communication and radio co-existence**
  In Paper 19.1, Columbia University presents a 1-to-1.7GHz receiver with a reconfigurable self-interference cancellation technique in 65nm CMOS that supports >>20MHz cancellation BW. Under the same-channel full-duplex (SC-FD) mode, 2dBm in-band IIP3 and 68dBm in-band IIP2 are achieved while consuming 63-69mW.

- **A highly linear receiver with cancellation of strong TX signal paves the way to full-duplex communication**
  In Paper 19.2, the University of Twente presents a 0.15-to-3.5GHz self-interference cancelling receiver in 65nm CMOS that supports the in-band full-duplex application. It achieves up to 87dB effective SFDR in 16.25MHz bandwidth.

- **SDR receiver with reconfigurable frequency selectivity targets carrier aggregation in modern cellular transceivers**
  In Paper 19.3, the University of Southern California presents a reconfigurable SDR in 65nm CMOS that supports multi-channel intra-band carrier aggregation using only one frequency synthesizer. The carrier frequency ranges from 0.5 to 3GHz and NF is 4.8dB.

Applications and Economic Impact

- Reconfigurable SDR receivers and self-interference cancellation techniques can enable advanced wireless communication techniques such as carrier aggregation, full-duplex or frequency-division multiplexing in low-cost, low-power, mobile devices.
- Interference cancellation techniques applied to transceivers can mitigate radio coexistence issues and enable tighter integration at lower cost and smaller form factor.

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Session 20 Highlights: Energy Harvesting and SC Power Conversion

20.2 A Variable-Conversion-Ratio, 3-Phase Resonant Switched Capacitor Converter with 85% Efficiency at 0.91W/mm^2 using PCB Trace Inductors

C. Schaef, K. Kesarwani, J. Stauth
Dartmouth College, NH

20.3 A Feedforward Controlled On-Chip Switched-Capacitor Voltage Regulator Delivering 10W in 32nm SOI CMOS

T. M. Andersen[1,2], F. Krismer[1], J. W. Kolar[1], T. Toifl[2], C. Menolfi[2], L. Kull[2], T. Morf[2], M. Kossel[2], M. Brändli[2], P. A. Francese[2]
[1]ETH Zurich, Switzerland, [2]IBM Research Zurich, Switzerland

Context and State of the Art

- The growing demand for both performance and battery life in portable consumer electronics requires small, efficient, and powerful power management circuits, without the need for external components.
- SC DC-DC converters can be realized in small, fully-integrated form-factors, that do not require costly external components. However, their maximum output power and efficiency so far have not been competitive with traditional inductor-based circuits.

Technical Highlights

SC DC-DC converters reach the 10W output power level, while maintaining more than 85% efficiency without external components

- In Paper 20.2, Dartmouth College presents a 7W, 3-phase, resonant SC DC-DC converter, implemented in 0.18µm bulk CMOS with 1.1nH inductors embedded in a flip-chip circuit board. The converter can provide granular step-up/down capability around the nominal conversion ratio while maintaining high efficiency.
- In Paper 20.3, IBM and ETH Zurich present a 10W, 64-phase, on-chip SC DC-DC converter for multi-core microprocessor power delivery systems, implemented in a 32nm SOI CMOS technology. The adopted feed-forward control strategy reduces the voltage droop and, thereby, the voltage overhead of the microprocessor core, significantly decreasing the overall microprocessor power consumption.

Applications and Economic Impact

- SC DC-DC converters capable of delivering more than 1W power can be used for a wide range of voltage-regulation applications. The highly integrated solution reduces the number of external components and, hence, the system cost and size.
- SC DC-DC converters alleviate the need for a high-cost external inductor in the system. The resulting reduction in size provides a more attractive solution for portable systems with small form factors.

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Session 21 Highlights: Innovative Personalized Biomedical Systems

21.2 A 3nW Signal Acquisition IC Integrating an Amplifier with 2.1 NEF and a 1.5fJ/conv.step ADC

P. Harpe, H. Gao, R. van Dommele, E. Cantatore, A. van Roermund
Eindhoven University of Technology, Eindhoven, The Netherlands

Context and State of the Art

- In wireless or self-powered miniature biomedical sensor applications, the 'always on' signal acquisition front-end will typically dominate the overall system power consumption.
- Previous signal acquisition front-ends for biomedical applications presented at ISSCC have reported power consumption in the range of several 10s to several 100s of nW.

Technical Highlights

A fully-integrated signal acquisition front end shows state of the art performance while achieving an overall power consumption of only 3nW

- In Paper 21.2, Eindhoven University of Technology presents a record low 3nW signal acquisition IC integrating an amplifier with 2.1NEF and a 10b 1kS/s 1.5fJ/step ADC suitable for ECG measurement. With an area of 0.20mm^2 in 65nm CMOS, the chip operates reliably from 0-to-85°C at 0.5-to-0.7V while keeping ultra-low power consumption.

Applications and Economic Impact

- Such ultra-low power consumption will enable biomedical signal acquisition systems to operate from energy scavenging devices with very small form factor, which may deliver only a few nanowatts of power.
- Truly-autonomous biomedical sensing systems have the potential to support personalized and sustainable healthcare delivery.

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Session 21 Highlights:
Innovative Personalized Biomedical Systems

21.7 A 0.036mbar Circadian and Cardiac Intraocular Pressure Sensor for a Smart Implantable Lens

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[1]University of Applied Sciences of Southern Switzerland (SUPSI),
[2]Oculox Technology, Lugano, Switzerland

Context and State of the Art

- High intraocular pressure (IOP) is the main risk factor for glaucoma, which is a leading cause of irreversible blindness.
- Lowering IOP is the optimal therapy to prevent or reduce the progression rate of glaucoma, however measurement of IOP today is a complex task carried out by trained eye-care professionals.

Technical Highlights

A smart implantable intraocular lens with state of the art sensitivity enabling for the first time the continuous measurement of both circadian (CiIOP) and cardiac (CaIOP) intraocular pressures

- In Paper 21.7, University of Applied Sciences of Southern Switzerland and OCULOX Technology present a circadian and cardiac intraocular piezoresistive pressure sensor measurement system achieving an unprecedented accuracy of 0.036mbar. The 2mm^2, 1.2mW, 0.35µm CMOS ASIC combining a sensor read-out and a 13.56MHz telemetry unit permits the monitoring of the retinal vascular system health.

Applications and Economic Impact

- The continuous measurement of circadian and cardiac IOP will enable the physician to determine the optimal medication for a given patient, as well as monitoring the patient's compliance to the prescribed therapy.
- This development has the potential to reduce the numbers of persons suffering from visual impairment due to high-IOP-induced glaucoma, improving their quality of life and reducing the associated healthcare costs.

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22.2 A 25Gb/s Hybrid Integrated Silicon Photonic Transceiver in 28nm CMOS and SOI

Yanfei Chen, Masaya Kibune, Akinori Hayakawa, Tomoyuki Akiyama, Shigeaki Sekiguchi, Hiroji Ebe, Tomoyuki Akahoshi, Suguru Akiyama, Shinsuke Tanaka, Takasi Simoyama, Ken Morito, Takuji Yamamoto, Toshihiko Mori, Yoichi Koyanagi, Hirotaka Tamura
Fujitsu Laboratories, Kawasaki, Japan

Context and State of the Art

- High-speed optical signaling already plays a crucial role in data center interconnect solutions. Silicon photonics technology offers a key potential path toward expanding the role of optics. Critical challenges limiting the competitiveness of Si photonics as compared to traditional optical and electrical alternatives include integration/packaging and practical realizations of compact high-data-rate modulator designs.
- Hybrid Si photonic designs to date have relied on wirebond assembly, with no path to massively scaled packaging solutions.
- Si photonic transmitter solutions have leveraged large Mach-Zehnder modulators, with limited progress in complete solutions for >25Gb/s per channel rates for the more compact ring-based modulators.

Technical Highlights

Fujitsu presents a high-speed silicon photonics based transmitter and receiver

- Fujitsu demonstrates a hybrid integrated interface based on a mixed pitch bumping technology that embeds the photonic die within a build-up layer (substrate).
- Micro bumps are used for connection to the photonics; C4 bumps are used for power supply and electrical I/O.
- Demonstrates the highest data rate for a carrier injection ring modulator.

Applications and Economic Impact

- Aggregate bandwidth between processors is extending into the Tb/s range, where bandwidth density can become the bottleneck. Low-cost, ultra-high speed optical interconnects using silicon photonics have the potential to achieve the required data rate density.

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Session 23 Highlights: Low-Power SoCs

23.1 20nm High-κ Metal Gate Heterogeneous 64b Quad-Core CPUs and Hexa-Core GPU for High-Performance and Energy-Efficient Mobile Application Processor

Jungyul Pyo, Youngmin Shin, Hoi-Jin Lee, Sung-il Bae, Min-su Kim, Kwangil Kim, Ken Shin, Yohan Kwon, Heungchul Oh, Jaeyoung Lim, Dong-wook Lee, Jongho Lee, Inpyo Hong, Kyungkuk Chae, Heon-Hee Lee, Sung-Wook Lee, Seongho Song, Chung-Hee Kim, Jin-Soo Park, Heesoo Kim, Sunghee Yun, Uk-Rae Cho, Jae Cheol Son, Sungho Park
Samsung Electronics, Hwasung, Korea

23.3 A Highly Integrated Smartphone SoC Featuring a 2.5GHz Octa-Core CPU with Advanced High-Performance and Low-Power Techniques

Hugh Mair, Gordon Gammie, Alice Wang, Sumanth Gururajarao, Ichiro Lin, HsinChen Chen, Wuan Kao, Anand Rajagopalan, Wei-Zheng Ge, Rolf Lagerquist, Syed Rahman, CJ Chung, Simon Wang, Lee-Kee Wong, Yi-Chang Zhuang, Kent Li, Jidong Wang, Minh Chau, Yijing Liu, Daniel Dia, Mark Peng, Uming Ko
MediaTek, Austin, TX

Context and State of the Art

- To achieve higher performance and energy efficiency within power and thermal limits for mobile SoCs, innovative circuit and design techniques are required.
- Today's mobile users demand ever higher performance, necessitating the use of multiple cores.
- To keep power in check, heterogeneous multiprocessing is applied to match application usage with core capabilities.

Technical Highlights

Samsung's first 20nm 64b processor with two quad-core ARM-v8 CPUs and integrated hexa-core GPU for mobile applications, enabling heterogeneous multi-processing.

- Samsung presents a mobile application processor with the latest ARM-v8 64b CPUs and a new hexa-core ARM-Mali GPU, implemented in Samsung's 20nm LP 9 layer metal process. The high-performance CPU cluster, with four ARM A57s, has a shared 2MB L2 data cache and operates at 1.9+GHz, and the low-power CPU cluster, with four ARM A53s, has a shared 256KB L2 data cache and operates up to 1.3GHz. Due to power optimizations, the fast 64b CPU consumes only 25% more power than the previous 32b CPU. The A57 area is $14mm^2$; the A53 area is $4mm^2$; and the area of the GPU complex is $25mm^2$.

A 28nm smartphone SoC featuring a 2.5GHz octa-core ARM-v7 CPU leveraging body biasing for power management, with integrated LTE modem.

- MediaTek presents a highly integrated smartphone SoC, with heterogeneous octa-core ARM-v7 32b CPU cores (A7 and A17), an LTE cellular modem, and high-performance 3D graphics. The A17 CPU operates at 2.5GHz. Optimized for power-efficiency, it contains a fully integrated power switch, which controls 5 power modes, including forward body bias and a fast adaptive retention mode with 50% lower leakage compared to active mode. The $89mm^2$ SoC is fabricated in 28nm high-κ CMOS.

Applications and Economic Impact

- Heterogeneous multi-core CPUs have expanded from their use in desktops and laptops into smart phones and tablets, and 64b mobile processors are now available.
- The market for mobile SoCs is predicted to be 5× larger than the traditional PC market by 2017, according to 2013 IDC Worldwide Smart Connected Device Tracker forecast data. These SoCs must satisfy mobile market needs for high performance and low power, and consumer desires for long battery life. Competition is fierce in the global smartphone market, estimated to be $150 billion in 2014.

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Session 24 Highlights: Secure, Efficient Circuits for IoT

24.1 Circuit Challenges from Cryptography

I. Verbauwhede, J. Balasch, S. Sinha Roy, A. Van Herrewege
KU Leuven, Heverlee, Belgium

Context and State of the Art

- Cryptographic algorithms require large keys (>256b) to protect private information. The keys themselves must be protected from various forms of physical attacks.
- Attackers benefit from Moore's law: Large computers can be used to 'break' cryptographic algorithms in IoT chips.
- Quantum computers are able to solve mathematically 'hard' problems and break public key algorithms.
- Defending IoT devices from these attacks is increasingly difficult, increases the cost and is a real circuit challenge.

Technical Highlights

This paper provides a spectrum of state-of-art circuit techniques for implementing cryptographic algorithms in low cost chips for IoT

- In Paper 24.1, KU Leuven presents the circuit level challenges for securing IoT devices. It provides an overview of the challenges of public key systems – both in today's technology and in the future quantum computing era. It outlines circuits that are used to prevent physical attack as well as Physically Uncloneable Functions that essentially provides per-device fingerprinting to further increase security.

Applications and Economic Impact

- Security is well known to be a major problem for the IT industry. The economic impact of security breaches in cloud-based, big-data and IoT systems is particularly significant.
- Security is a critical issue for the deployment of IoT; integrated security measures must be low cost and yet effective.
- Protecting against security attacks by those who will have access to quantum computers requires post-quantum cryptographic algorithms and circuit implementations.

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Session 24 Highlights: Secure, Efficient Circuits for IoT

24.2 Context-Aware Hierarchical Information-Sensing in a 6µW 90nm CMOS Voice Activity Detector

K. Badami, S. Lauwereins, W. Meert, M. Verhelst,
KU Leuven, Leuven, Belgium

Context and State of the Art

- Context aware systems need to be always on, and therefore need to maximize information capture in a very energy efficient way.
- At the lower levels of the hierarchy, very low power but coarse classifications can be enabled. Subsequent classifications that are more precise but more power hungry are enabled as required.

Technical Highlights

Always-on context aware device uses hierarchical classification to minimize use of energy intensive operations, until such operations are needed. It exploits analog feature extraction and mixed-signal embedded classification

- In Paper 24.2, KU Leuven presents a power and context aware acoustic sensor front-end architecture. Acoustic signal classification is initially done in a coarse but very power efficient manner. As more information is gathered about the nature of the signals, more precise but higher power classifications are enabled. This hierarchical wake-up enables power efficient always-on devices.

Applications and Economic Impact

- Voice activity detection will become a pervasive need in mobile and non-mobile applications.
- These devices will enter into different modes of operation based on voice commands.
- Voice will be one of many signals that context aware devices need to respond to.

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24.3 20k-Spin Ising Chip for Combinational Optimization Problem with CMOS Annealing

M. Yamaoka, C. Yoshimura, M. Hayashi, T. Okuyama, H. Aoki, H. Mizuno
Hitachi, Tokyo, Japan

Context and State of the Art

- Novel paradigms, different from the traditional Von Neumann architecture, are needed for improved efficiency in computation.
- The Ising model, a model to express the behavior of magnetic spins, can be exploited to solve optimization problems exploiting its convergence properties.

Technical Highlights

A computing paradigm using magnetic spin interactions solves problems with substantial reduction in power

- In Paper 24.3, Hitachi presents a form of natural computing where a problem is mapped into an Ising model, which utilizes the behavior of magnetic spins. In this computing paradigm the magnetic spin interactions achieve an energy minimum – thereby converging to a solution.

Applications and Economic Impact

- New computing paradigms need to be investigated as alternatives to the Von Neumann architecture.
- This is particularly true for special classes of problems such as pattern recognition where classical architectures offer diminishing benefits as problem size increases.

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Session 25 Highlights: RF Frequency Generation from GHz to THz

25.5 320GHz Phase-Locked Transmitter with 3.3mW Radiated Power and 22.5dBm EIRP for Heterodyne THz Imaging Systems

Ruonan Han[1,2], Chen Jiang[1], Ali Mostajeran[1], Mohammad Emadi[1], Hamidreza Aghasi[1], Hani Sherry[1], Andreia Cathelin[3], Ehsan Afshari[1]
[1]Cornell University, Ithaca, NY, [2]MIT, Cambridge, MA, [3]STMicroelectronics, France

Context and State of The Art

- Scalable 338GHz 2D array radiators and 0.53THz reconfigurable source array in CMOS and BiCMOS have been reported in ISSCC 2014.
- EIRP and output power need to be improved.

.

Technical Highlights

A 320 GHz phased-locked-based transmitter array with 22.5 dBm EIRP in SiGe BiCMOS process is reported.

- In Paper 25.5, the use of phase-locking to synchronize all the source elements achieves record-breaking EIRP and higher output power. The output radiation is, for the first time, phase-locked by an integrated PLL operating at 80 GHz (i.e., 4th sub-harmonic).

Applications and Economic Impact

- This paper demonstrates an integrated solid-state radiator with high ERIP and output power at terahertz frequencies.
- It can be used for future generations of miniature terahertz imagers and spectrometers.

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Session 26 Highlights: Nyquist-Rate Converters

26.1 A 1mW 71.5dB SNDR 50MS/s 13b Fully Differential Ring Amplifier Based SAR-Assisted Pipeline ADC in 65nm CMOS

Y. Lim, M. Flynn
University of Michigan, Ann Arbor, MI

26.4 A 21fJ/conversion-step 9 ENOB 1.6GS/s 2× Time-Interleaved FATI SAR ADC with Background Offset and Timing-Skew Calibration in 45nm CMOS

B. R. S. Sung[1], D. S. Jo[1], I. H. Jang[1], D.S. Lee[2], Y. S. You[2], Y. H. Lee[2], H. J. Park[2], S. T. Ryu[1]
[1]KAIST, Daejeon, Korea;, [2]Samsung Electronics, Yongin, Korea

Context and State of the Art

- Low-power Analog-to-Digital Converters (ADCs) are key building blocks in modern electronics. The power efficiency of an ADC can be measured by the energy consumed per conversion step (Walden figure of merit (FoM)).
- Pipelined converters continue to improve, but due to the power required for precision amplification, their FoM has never dropped below 10fJ/conversion-step for an SNDR greater than 70dB.
- Likewise, the FoM of ADCs with a conversion rate greater than 1GS/s is limited by process technology and has never dropped below 30fJ/conversion-step.

Technical Highlights

University of Michigan demonstrates record-setting power efficiency of 6.9fJ/conversion-step for a pipelined ADC

- This 13b 50MS/s ring amplifier based SAR-assisted pipeline ADC with a new switching technique achieves a Walden FoM of 6.9fJ/conversion-step without calibration and achieves an SNDR of 71.5dB.

KAIST and Samsung report a 1.6GS/s 9ENOB ADC featuring 21fJ/conversion-step FoM

- This FATI (Flash-Assisted Time-Interleaved) SAR ADC was implemented in 45nm CMOS and operates at 1.6GS/s conversion speed with a Walden FoM of 21fJ/conversion-step. The design leverages a folding flash sub-ADC topology for low power.

Applications and Economic Impact

- These ADCs with innovative circuit techniques enable low-power wideband communication systems and meet the needs for the world's growing cloud computing ecosystem. Furthermore, these designs are compatible with integration in large systems-on-chip (SoCs) using advanced CMOS technologies.

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Session 27 Highlights: Physical Sensors

27.1 A 3-Axis Gyroscope for Electronic Stability Control with Continuous Self-Test

G. Balachandran[1], V. Petkov[1], T. Mayer[2] and T. Balslink[2]
[1]Robert Bosch, Palo Alto, CA
[2]Robert Bosch, Reutlingen, Germany

Context and State of the Art

- Gyroscopes are increasingly used in automotive and consumer applications for motion detection. In automotive applications, gyroscopes are used for roll-over detection and for stability control. Consumer applications include camera stabilization and in-door navigation.

Technical Highlights

Automotive gyroscope that achieves 20dB better dynamic range and 9× lower offset drift compared to the state of the art will enable higher levels of safety in next-generation cars

- In Paper 27.1, Robert Bosch presents an automotive gyroscope with self-test capability that meets stringent electronic stability control specifications for car safety. The gyroscope has a 10× better dynamic range and a 9× lower offset drift with temperature than state-of-the-art devices.

Applications and Economic Impact

- The new device enables Electronic Stability Control systems, which are mandated for new vehicles in many countries and lead to a higher level of safety for next-generation cars.

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ISSCC 2015
TRENDS

CONDITIONS OF PUBLICATION

PREAMBLE

The Session Overviews to follow serve to capture the context, highlights, and potential impact, of the papers to be presented in each Session at ISSCC 2015 in February in San Francisco

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> This and other related topics will be discussed at length at ISSCC 2015, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 22-26, 2015, at the San Francisco Marriott Marquis Hotel.

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ANALOG SYSTEMS

ANALOG SUBCOMMITTEE
DATA CONVERTERS SUBCOMMITTEE

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Analog – 2015 Trends

Subcommittee Chair: *Axel Thomsen, Silicon Laboratories, Austin, TX*

The efficient control, storage, and distribution of energy are worldwide challenges, and are increasingly important areas of analog circuit research. While the manipulation and storage of information is efficiently performed digitally, the conversion and storage of energy is fundamentally performed with analog systems. Therefore, the key technologies for power management are predominantly analog. For example, there is much interest in wireless power transmission for battery charging applications, ranging from mobile handsets to medical implants: increased performance in wireless power transmission is enabling more efficient power delivery over longer distances. There is also an explosion of technologies that allow energy to be collected from the environment via photovoltaic, piezoelectric, or thermoelectric transducers, with a trend toward the use of multiple sources at the same time. A significant focus here is on analog circuits that are able to harvest sub-microwatt power levels from multiple energy sources at tens of millivolts, to provide autonomy for remote sensors, or to supplement conventional battery supplies in mobile devices. To achieve this, the attendant analog circuits have to consume extremely low power, so that some energy is left over to charge a battery or super-capacitor. Similarly, the power consumption of analog instrumentation amplifiers, oscillators, and audio power amplifiers is being scaled down to meet the demands of these low-power systems. Fast power-up and -down is also desired from these circuits to permit high energy-efficiency during intermittent operation. Together, these technologies will lead to devices powered indefinitely from sustainable sources, opening the door to internet of things, ubiquitous sensing, environmental monitoring, and medical applications.

Analog circuits also serve as bridges between the digital world and the analog real world. Just like actual bridges, analog circuits are often bottlenecks and their design is critical to overall performance, efficiency, and robustness. Nevertheless, since digital circuits, such as microprocessors, drive the market, semiconductor technology has been optimized relentlessly over the past 40 years to reduce their size, cost, and power consumption. Analog circuitry has proven increasingly difficult to implement using these modern IC technologies. For example, as the size of transistors has decreased, the range of analog voltages they can handle as well as their analog performance have decreased, while the variation observed in the analog parameteres has increased.

These aspects of semiconductor technology explain two key divergent trends in analog circuits. One trend is to forgo the latest digital IC manufacturing technologies, instead fabricating analog circuits in older technologies, which may be augmented to accommodate the high voltages demanded by increasing markets in medical, automotive, industrial, and high-efficiency lighting applications. Other applications dictate full integration of analog and digital circuits together in the most modern digital semiconductor processes, including FinFET and FDSOI technologies. For example, microprocessors with multiple cores can reduce their overall power consumption by dynamically scaling operating voltage and frequency in response to time-varying computational demands. For this purpose, DC-DC voltage converters can be embedded alongside the digital circuitry, driving research into the delivery of locally-regulated power supplies with increasing efficiency, decreasing die area, and increasing output power, but without requiring external components. These trends are captured by movement towards the top-right in the plot below with a concurrent increase of the output power level.

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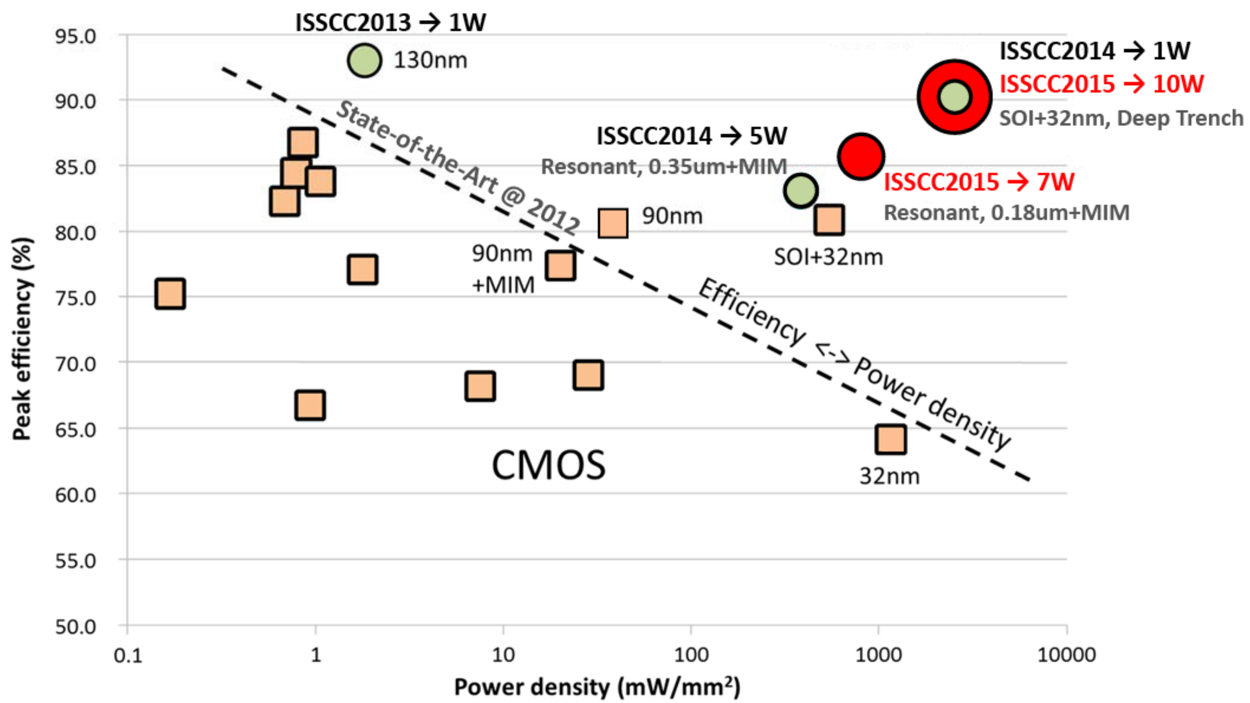

Comparison of Integrated Switched-Capacitor Power Converters from ISSCC papers showing Peak Efficiency vs Power Density and Output Power. Recent advances achieve much higher power density and output power without sacrificing efficiency (see the top right quadrant).

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Data Converters – 2015 Trends

Subcommittee Chair: *Boris Murmann, Stanford University, Stanford, CA*

Data converters serve as key building blocks in virtually all electronic systems, and serve to bridge the analog physical world to the digital circuitry prevalent in modern integrated circuits. Key metrics such as linearity, bandwidth, and power efficiency continue to be the dominant drivers for innovation, as evidenced by the data converters presented at ISSCC 2015. Also, for the first time, we see a converter in 14nm FinFET technology. This design leverages the integration density of this technology to realize a process-voltage-temperature (PVT) tolerant Time-to-Digital Converter using 2^{14} delay elements.

Figure 1 below is a survey of ADC power efficiency expressed as power dissipated relative to the effective Nyquist rate (P/f_{snyq}), and as a function of signal-to-noise and distortion ratio (SNDR). For low-to-medium-resolution converters, energy is primarily expended to quantize the signal and the overall efficiency of this operation is typically measured by the energy consumed per conversion and quantization step. The dashed trend-line represents a benchmark of 5fJ/conversion-step. Higher-resolution converters face the additional burden of overcoming circuit noise, necessitating a different benchmark proportional to the square of signal-to-noise ratio, represented by the solid line. Contributions at ISSCC 2015 are highlighted by the colored squares representing various converter architectures, and contributions from previous years are marked by smaller markers. Delta-Sigma, pipeline and SAR ADCs at various SNDR design points continue to push the limits of energy efficiency. (Note that a lower P/f_{snyq} metric represents a more efficient circuit on this chart.)

Figure 2 shows energy per conversion-step vs. the Nyquist sampling rate. This figure elucidates the difficulty of maintaining good efficiency at higher speeds of operation. Nevertheless, advances in circuit innovations embodied in leading-edge technologies have resulted in new benchmarks in energy efficiency across the entire spectrum of conversion rates.

Figure 3 plots achieved bandwidth as a function of SNDR. Sampling jitter or aperture errors make the combination of high resolution and high bandwidth a particularly difficult task. Nonetheless, in 2015, we see many examples achieving excellent results in this metric across a wide range of SNDR and bandwidths utilizing several different converter architectures.

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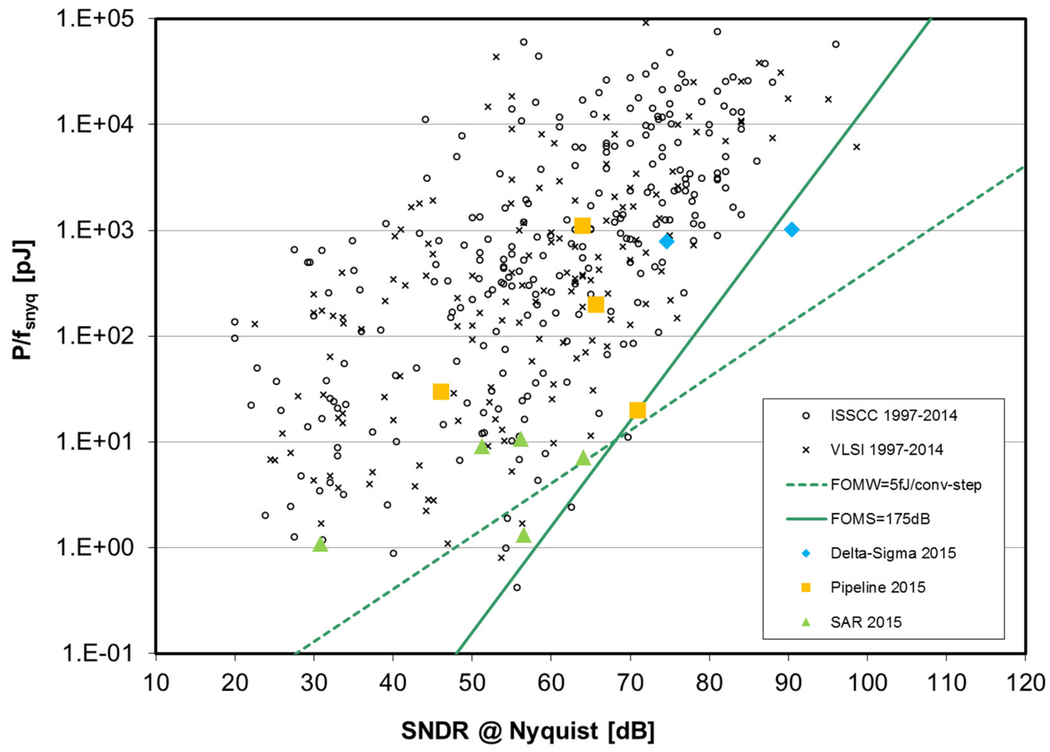

Figure 1: ADC power efficiency (P/f_{snyq}) as a function of SNDR

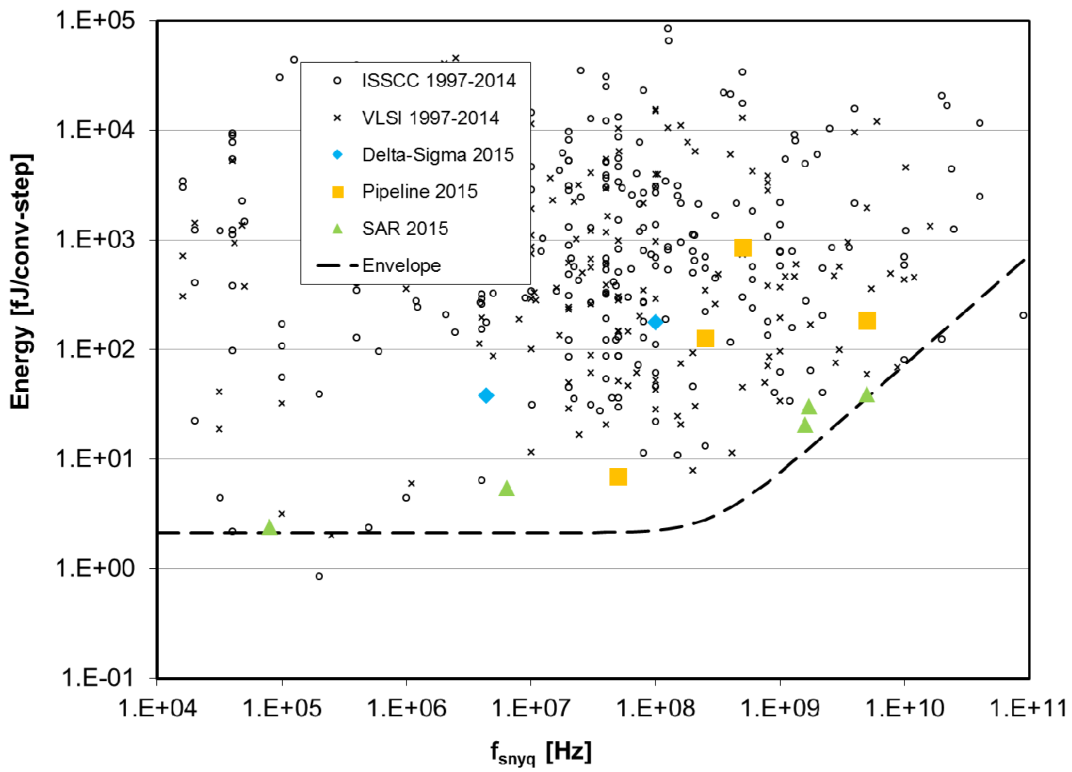

Figure 2: Energy per conversion-step vs. the Nyquist sampling rate

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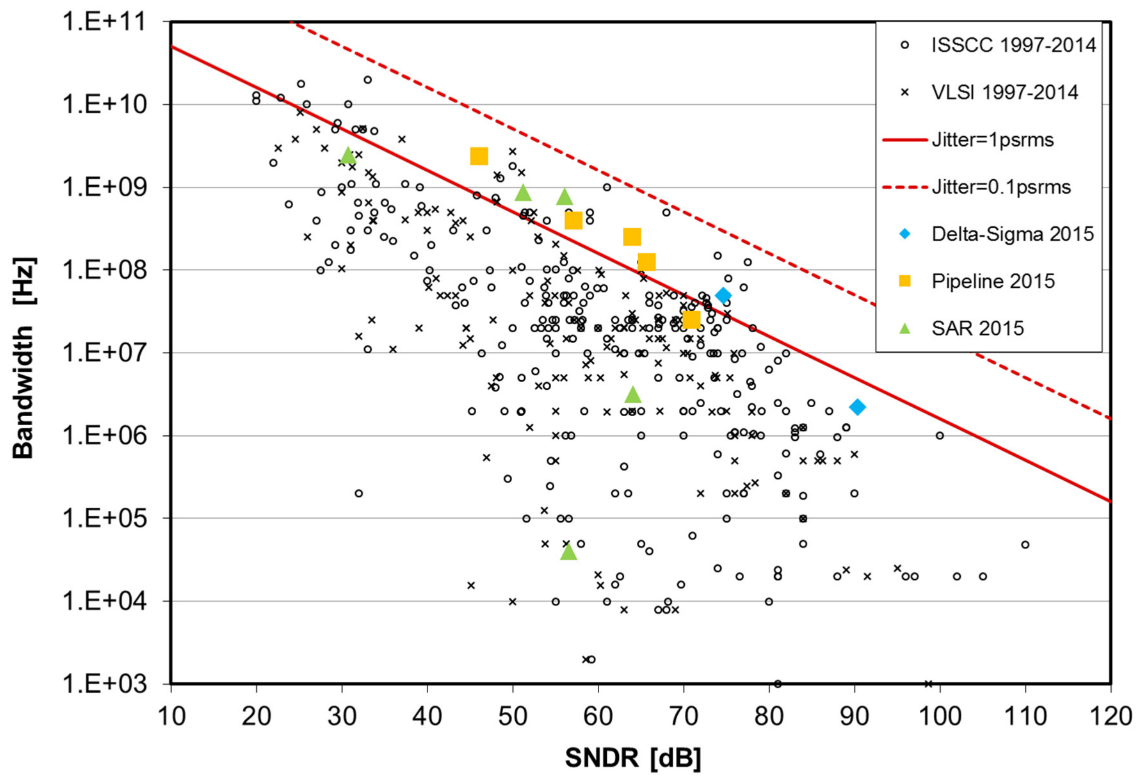

Figure 3: Bandwidth vs. SNDR

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INDICATORS – HISTORICAL TRENDS IN TECHNICAL THEMES

COMMUNICATION SYSTEMS

RF SUBCOMMITTEE - WIRELESS SUBCOMMITTEE
WIRELINE SUBCOMMITTEE

RF Subcommittee – 2015 Trends

Subcommittee Chair: *Andreia Cathelin, STMicroelectronics, Crolles, France*

Introduction
This year has shown increased innovation, integration, and technical maturity across the radio frequency (RF) bands from a few GHz to beyond 300GHz. This includes wireless communication which has made our world a smaller place by enabling us to share ideas and concerns regardless of our geographical location. This document outlines such emerging RF trends that will be covered at the 2015 ISSCC conference. Papers showcase some of the recent advances in RF transmitter and receiver building blocks, with an ongoing drive towards higher output power with better energy efficiency, lower noise and increasing levels of integration. This trend can be seen in all areas of RF design, from cellular and wireless sensors up to mm-Wave/THz sources.

Energy efficiency: There is an increasing demand for energy efficient and very small wireless device solutions for different applications such as IoT, wearable and wireless sensors. The trend is toward highly integrated low-power RF systems. Very low power techniques like receiver-based FLL, wake-up radio, extreme low-duty-cycle regimes and RF energy harvesting have been demonstrated this year.

RF Transmitters and Receivers: RF techniques for transceivers have made significant progress to enable energy and cost-efficient wireless communication systems. For cellular RF, a new class of PA is proposed for high linearity and low voltage stress. In addition, a silicon-based duplexer breaking the +70 dBm IIP3 barrier and a hybrid supply modulator that enhances the dynamic range of envelope-tracking (ET) are realized. For wideband radios spanning across a few GHz, an inductorless receiver with as low as 2dB NF and a Class-AB PA achieving near 30% PAE with >22 dBm P_{sat} are presented. It is observed that utilization of digitally-intensive PA design techniques and body bias in SOI process technology for mm-Wave building blocks have grown significantly. At the same time, the operating frequency bandwidth coverage is also broadened.

Power delivery: There is a continued trend in increasing the output power by means of power combining techniques with improved efficiency, trying to circumvent the low breakdown voltages of nanoscale CMOS. Implementing RF PAs for 3G/4G standards are in particular challenging due to the amplification of signals with high peak-to-average-ratio. The trend is to reach a high degree of linearity with novel linearization techniques using active feedback without pre-distortion for LTE signals. Wideband power amplifiers are further needed to reach higher data-rates. This demands output matching networks that can provide an optimum load impedance over at a larger fractional RF bandwidth. The conference will show a first implementation of PAs supporting modulations such as 256QAM with a PAE reaching 28% over an octave of bandwidth. There is also a continued interest in improving envelope tracking by modulating the supply voltage of power amplifiers to further increase the battery lifetime in mobile LTE applications. Techniques that can enhance the dynamic range of envelope tracking with adaptive control of both the PA supply voltage and the bias currents achieve record PAE performance with lowest power dissipation.

New PA design methodologies presented at this year's conference indicate that future PA architectures may have to combine multiple techniques to further improve the performance of both CMOS and SiGe amplifiers. For instance, different modes of operation such as Class-G are combined with Doherty to enhance the efficiency without mitigating RF bandwidth at around 3.7GHz. Such approaches achieve substantial efficiency enhancements at power back-off. The combination of multiple design techniques also shows first PA implementations at mm-Wave frequencies that have the potential to soon bridge the 1-Watt barrier with good PAE efficiency. This is enabled with novel dynamic load-line modulation techniques using variable impedance transmission lines. A digital Class-E architecture for instance has shown up to 29dBm at 46GHz. Another avenue towards efficient linear power amplification is to leverage advanced technologies such as 28nm CMOS FD-SOI using body biasing. This extra biasing flexibility allows the combination of parallel transistors to operate in different classes by adjusting their threshold voltage individually. First 60GHz WiGig implementations reach 21% PAE at 18.2dBm at P_{1dB}. The trend to simultaneously optimize power and efficiency is indicated in Figure 1 for mm-Wave PAs implemented in CMOS.

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Frequency generation: Frequency generation circuits are ubiquitous building blocks. The race to reduce phase noise, chip area, and power consumption for synthesizers and VCOs is never ending. Utilizing circuit techniques to suppress the impact of flicker noise on phase noise, as well as employing a capacitance scaling technique to decrease PLL filter size are becoming popular. Very low phase noise is achieved and the VCO Figure-of-Merit (FOM) has reached a new record. The trend towards better performing VCOs is shown in Figure 2, where the VCOs FOM versus oscillation frequency is continuously improving. With an attempt to remove the bulky quartz crystal, a highly stable thin-film-based reference frequency generator is reported, attaining a stability of ±3 ppm from 0 to 90°C. At the THz frontier a phase-locked-based transmitter array has been demonstrated with sufficiently high output power beyond 300GHz, enabling numerous practical terahertz applications that require coherent radiation. The output power versus frequency for the trend in mm-Wave and sub-mm-Wave sources is given in Figure 3.

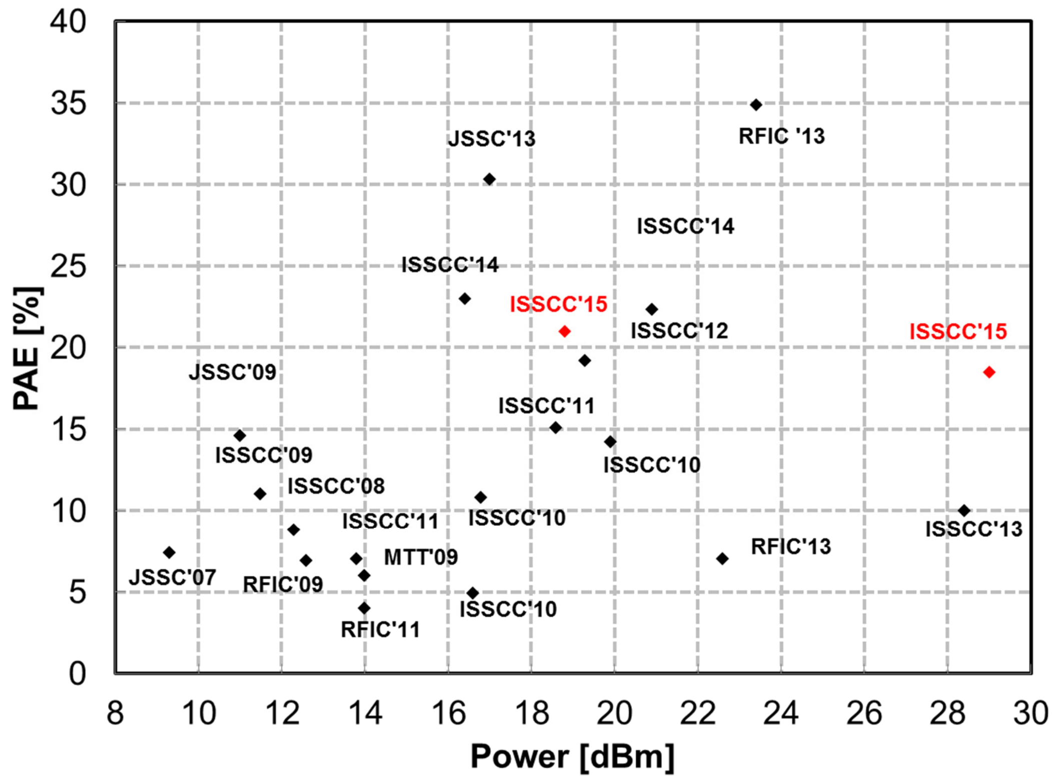

Figure 1: PAE (%) vs. output power for recent submicron mm-Wave CMOS PAs

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Figure 2: Oscillator phase-noise FOM at 20MHz offset frequency versus oscillation frequency

Figure 3: Output power versus frequency for mm-Wave and sub-mm-Wave sources

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Wireless – 2015 Trends

Subcommittee Chair: *Aarno Pärssinen, Broadcom, Finland*

The vision for Wireless Sensor Networks (WSN) and the Internet of Things (IoT) continues towards more mature integration strategy. The commercial landscape is focusing these technologies towards Bluetooth Low Energy (BLE), while still maintaining flexibility by having the ability to function as multimode radios. This conference features some of the first published comprehensively integrated wireless sensor nodes, including MCU, power management, digital baseband modem and wireless transceivers. The key aspect and challenge of these wireless radios continues to be the ability to function at the lowest power possible, while being robust to the presence of other wireless signals. A prominent use case of most of the Wireless Sensor Network nodes is the transmit operation. Therefore, transmit power efficiency is a key metric that determines the evolution of these sensor nodes in terms of power consumption. A development trend in wireless sensor nodes for transmit power efficiency is shown in Figure 1. Similarly, Figure 2 shows that the receiver sensitivity as a function of power consumption in complete SoC's has almost reached the levels of a stand-alone wireless transceiver.

While exponential increase in data rate of cellular devices is still ongoing, a different vector that is also important is the level of integration in these SoC's. The trend in these integration strategies is shown in Figure 3, where the progress has been to transition from BiCMOS to CMOS to baseband modem integration and finally this year to 3G power amplifier integration on the same die. PA integration as well as elimination of the front-end SAW filter, as is shown in another paper in this year's conference significantly advance the trend of BOM reduction and simplification of the overall system complexity.

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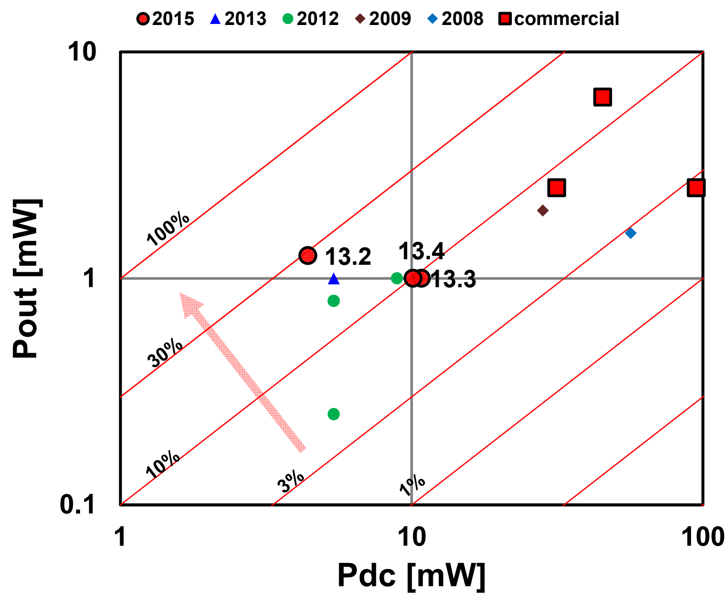

Figure 1: Ultra-Low Power 2.4GHz Wireless Transmit Efficiency Trends Arrow shows desired trends. All symbols except red squares represent ISSCC papers. The ISSCC 2015 paper numbers are indicated next to the red circles.

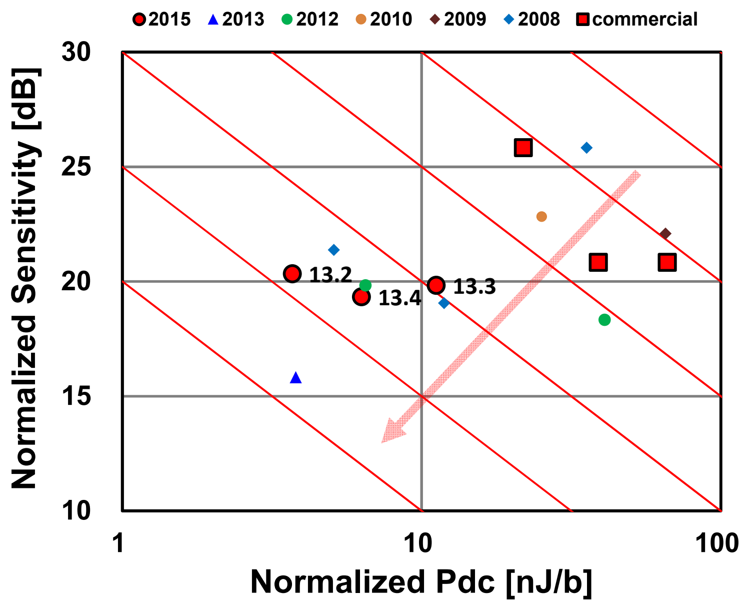

Figure 2: Ultra-Low-Power 2.4GHz Wireless Receiver Sensitivity Trends. Sensitivity is normalized to bandwidth at 2.4GHz carrier. Lines represent constant performance. The triangle is transceiver only and red dots and squares represent full SOCs.

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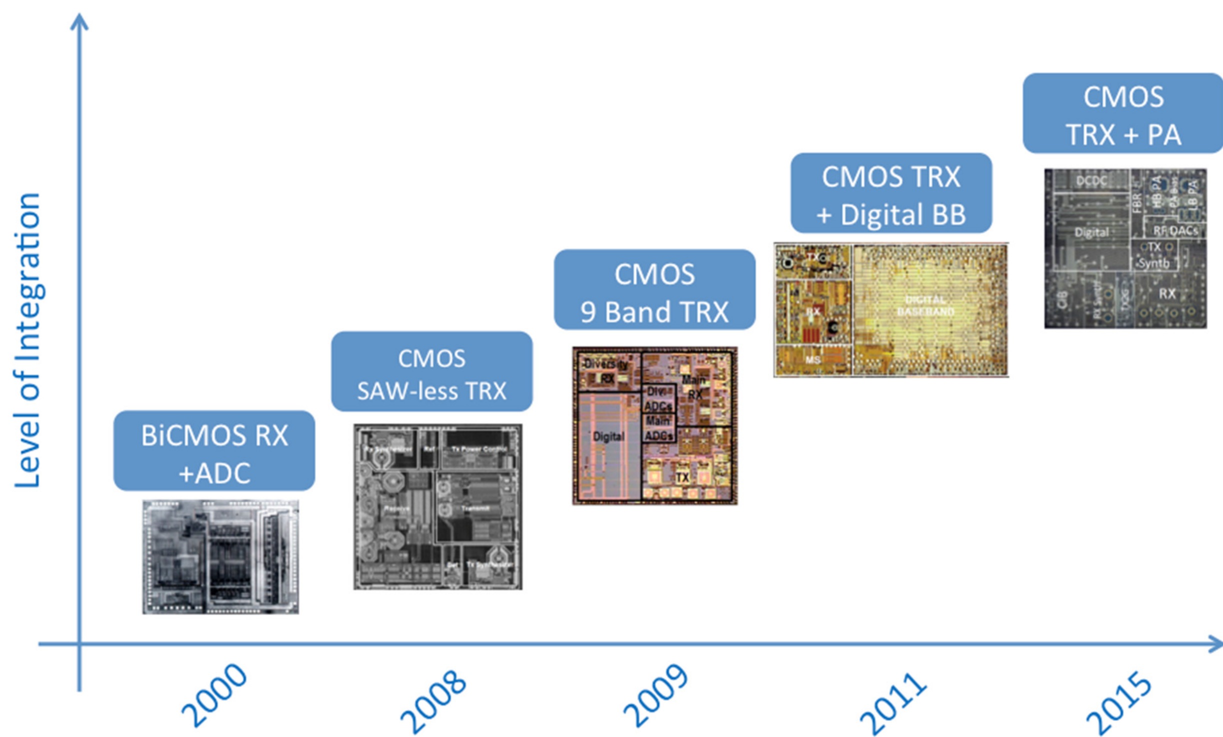

Figure 3: Integration Trends in Cellular Wireless

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Subcommittee Wireline – 2015 Trends

Subcommittee Chair: *Daniel Friedman, IBM T. J. Watson Research, Yorktown Heights, NY*

Over the past decade, wireline I/O has been instrumental in enabling the incredible scaling of computer systems, ranging from handheld electronics to supercomputers. During this time, aggregate I/O bandwidth requirements have increased at a rate of approximately 2 to 3× every 2 years. Demand for bandwidth is driven by applications including memory, graphics, chip-to-chip fabric, backplane, rack-to-rack, and LAN. In part, this increase in bandwidth is enabled by expanding the number of I/O pins per component. As a result, I/O circuitry consumes an increasing amount of area and power on today's chips. Increasing bandwidth has also been enabled by rapidly accelerating the per-pin data rate. Figure 1 shows that per-pin data rate has approximately doubled every four years across a variety of diverse I/O standards ranging from DDR to graphics to high-speed Ethernet. Figure 2 shows that the data rates for published transceivers have kept pace with these standards, enabled in part by process technology scaling. However, continuing along this rather amazing trend for I/O scaling will require more than just transistor scaling. Significant advances in both energy efficiency and signal integrity must be made to enable the next generation of low-power and high-performance computing systems.

Energy Efficiency and Interconnect Density:
Power consumption for I/O circuits is a first-order design constraint for systems ranging from cell phones to servers. As the pin count and per-pin data rate for I/Os has increased on a die, so has the percentage of total power that they consume. Technology scaling enables increased clock and data rates and offers some energy efficiency improvement, especially for digital components. Many recent advances have reduced power for high-speed link components through circuit innovation, including low-power RX equalization (DFE, CTLE), CMOS and resonant clocking, low-swing voltage-mode transmitters and links with low-latency power-saving states. Papers at ISSCC this year include the lowest reported long-range 25Gb/s transceiver achieving 11pJ/b [3.1], and a scaled-supply link that consumes only 0.29pJ/b by operating at 0.45V [3.8].

Simply increasing per-pin baseband data rates with existing circuit architectures and channels is not always a viable path given fixed system power limits. Figure 3 plots the energy efficiency (expressed in mW/Gb/s, which is equivalent to pJ/b) as a function of channel loss for recently reported transceivers. Looking at the most aggressive designs, the data indicates that the scaling factor between link power and signaling loss slightly less than unity—in particular, that 30dB in channel loss corresponds to a roughly 10× increase in pJ/b. In this year's ISSCC, a fast 20ns on/off link is demonstrated that save power by dynamically gating the transceiver [3.7]. A multi-tone transceiver is also demonstrated that consumes only 1pJ/b by shaping the data spectrum to match the channel discontinuities [10.3].

Electrical Interconnect:
Some types of channels, especially those related to medium-distance electrical I/O like server backplanes, must support high data rates over high loss channels. For these links, the key to scaling has been improvements in equalization and clock/data recovery. Recent high-speed transceivers use a combination of fully adaptive equalization methods, including TX FIR, RX CTLE, DFE, as well as RX FIR and/or IIR FFEs. As a result, recent transceivers achieve data-rates above 20Gb/s with channels that have 30dB or more loss. This year's ISSCC includes a paper that describes three 25-to-33Gb/s transceivers operating over up to 40dB loss channel [3.1, 3.2, 3.3], and two transmitters that support both NRZ and PAM4 signaling up to 40Gb/s [3.4, 3.5].

Optical Interconnect:
As the bandwidth demand has accelerated for traditionally electrical wireline interconnects, optics has become an increasingly attractive alternative for interconnects within computing systems. Optical communications have clear benefits for high-speed and long-distance interconnects. Relative to electrical interconnects optics provides lower channel loss. Circuit design and packaging techniques that have traditionally been used for electrical wireline are being adapted to enable integrated optical with extremely low power. This has resulted in rapid progress in optical ICs for Ethernet, backplane and chip-to-chip optical communication. At ISSCC this year, several 20-to-25Gb/s optical transceivers and components will be presented with a focus on power efficiency and optics integration. One paper demonstrates a full transceiver that uses WDM to send multiple 20Gb/s data streams on the same optical fiber [22.5].

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Concluding Remarks:

Continuing to aggressively scale I/O bandwidth is both essential for the industry and extremely challenging. Innovations that provide higher performance and lower power will continue to be made in order to sustain this trend. Advances in circuit architecture, interconnect topologies, and transistor scaling are together changing how I/O will be done over the next decade. The most exciting and most promising of these emerging technologies for wireline I/O will be highlighted at ISSCC 2015.

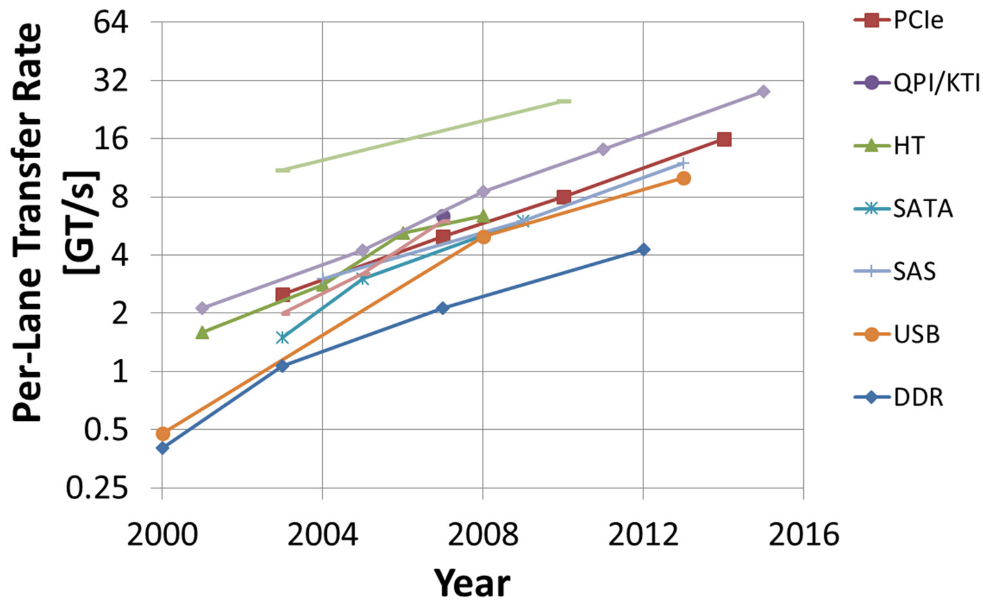

Figure 1: Per-pin data rate vs. Year for a variety of common I/O standards.

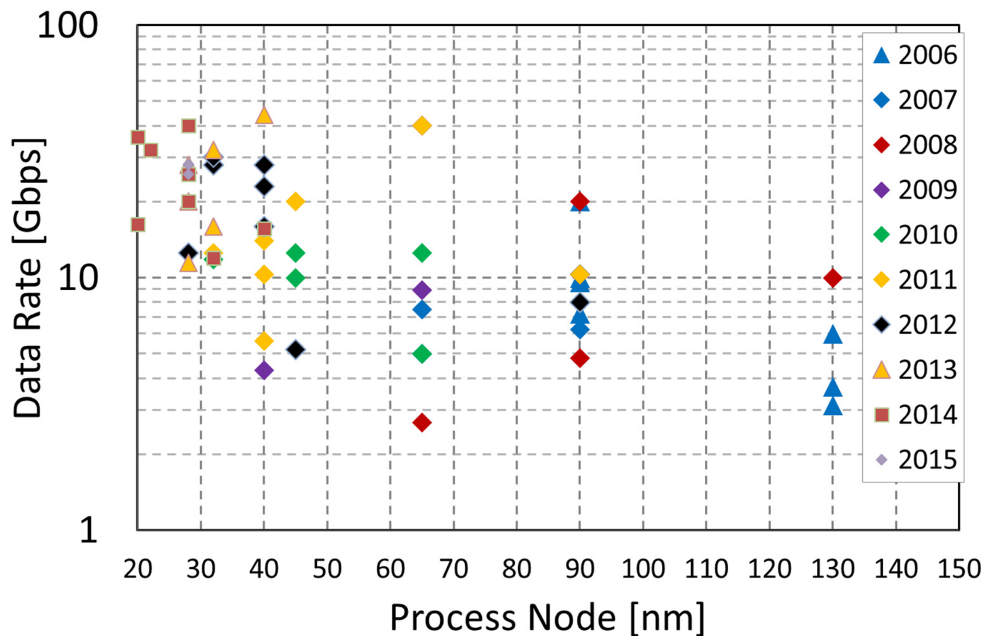

Figure 2: Data-rate vs. process node and year.

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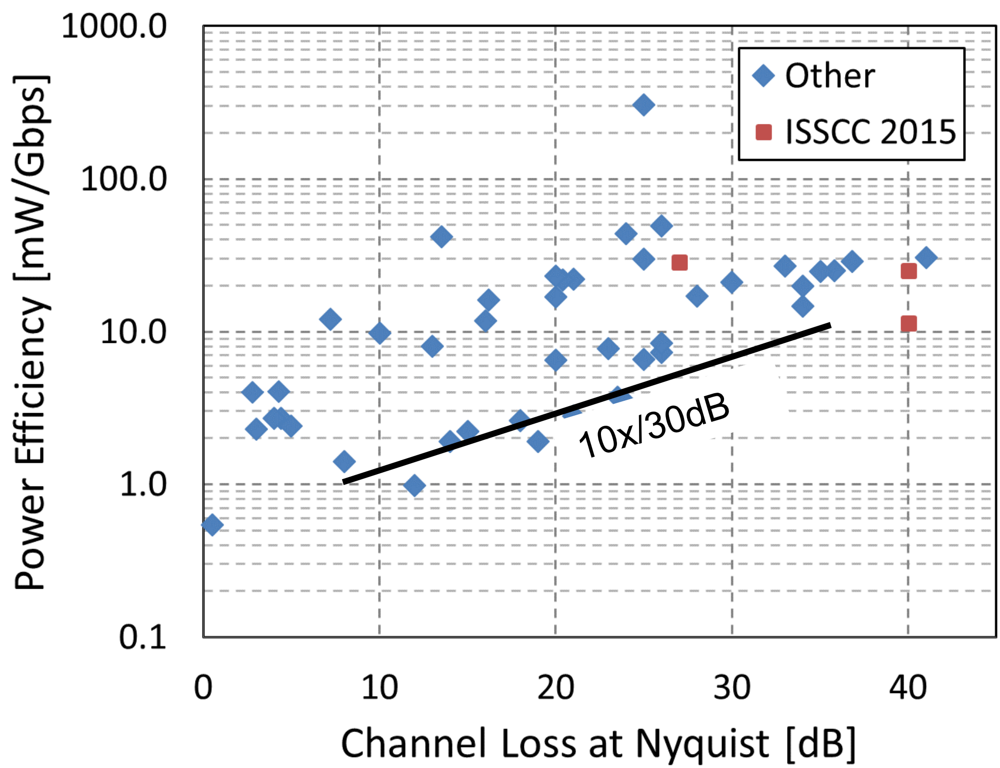

Figure 3: Transceiver power efficiency vs. channel loss.

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INDICATORS – HISTORICAL TRENDS IN TECHNICAL THEMES

DIGITAL SYSTEMS

ENERGY-EFFICIENT DIGITAL SUBCOMMITTEE
HIGH-PERFORMANCE DIGITAL SUBCOMMITTEE
MEMORY SUBCOMMITTEE

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Energy Efficient Digital – 2015 Trends

Subcommittee Chair: *Stephen Kosonocky, AMD, Fort Collins, CO*

Demand for ubiquitous mobile functionality to achieve enhanced productivity, a better social-networking experience, and improved multimedia quality, continues to drive innovation in systems-on-chip (SoC), which are also constrained by a need to improve battery life and reduce cost. While the performance of embedded application processors has increased to meet the rising demands of general-purpose computing, dedicated multimedia accelerators are necessary to provide dramatic improvements in performance and energy efficiency of emerging applications. At the other side of the spectrum, sensor nodes for the Internet-of-Things (IoT) require low energy wireless and sufficient computational capabilities.

Technology scaling continues to be exploited to deliver designs capable of operating at lower voltages, resulting in reduced energy per operation, as well as lowering the area required to implement specific functions. Processors unveiled at ISSCC 2015 are built in a variety of technology nodes, with best-in-class results accomplished with higher integration, and improved performance-per-watt. These are demonstrated in various process nodes ranging from 130nm to 14nm FinFET, as well as low power FD-SOI CMOS technologies.

Energy-efficiency techniques for microcontrollers

Semiconductor chips used for the Internet-of-things (IoT) and other embedded application areas demand energy-efficient active operation, while also requiring ultra-low power state retention to enable event-driven operation with fast wake-up. Typically an energy-efficient microcontroller unit (MCU) is used as the main processing element for local processing and system control these applications. Over time, the microcontroller energy efficiency, shown in Figure 1, has continuously improved through a combination of technology and design techniques, as illustrated in Figure 2.

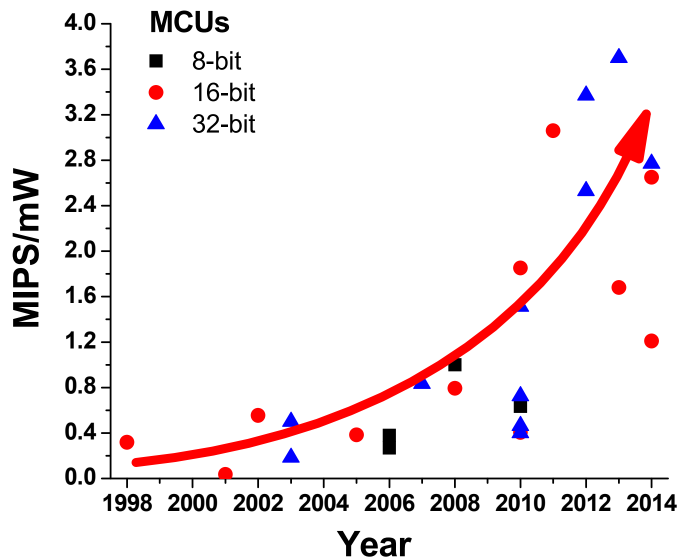

Fig. 1 Energy-efficiency evolution in commercial microcontrollers.

Low-power silicon technology with embedded non-volatile memory enables more power-effective full state retention, while reduced supply and feature sizes cut active energy consumption. At the circuit level, the chase for energy efficiency drives innovation on adaptive and near-threshold operation, enabling further supply voltage reduction. A complete Cortex M0+ ARM core now can scale down to 850nW active power at 250mV, yet can also operate at 66MHz at 0.9V supply. Retention power is tackled by improved leakage reduction techniques, shadow latches in logic, and optimized SRAM design.

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At the architecture level, smaller and smaller microcontrollers are enhanced with advanced integrated power management and variation mitigation. Dedicated accelerators are selectively powered up to improve the efficiency of important compute kernels, such as AES cryptography. The latest state-of-the-art focuses on dynamic scalability and efficient always-on peripherals, such as real time clocks and wake-up sensors, enabling nano-Watt operation from integrated energy harvesters.

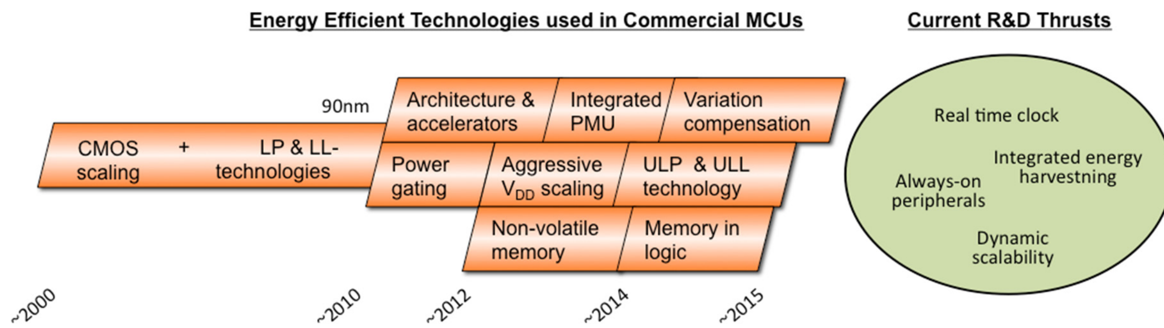

Fig. 2 Energy-efficiency techniques exploited in microcontroller design.

Rising complexity and functionality for application processors

Figure 3 illustrates the major trends of smart phones and tablets relevant to energy-efficient digital circuits. In the late 1990s, a GSM phone contained a simple RISC processor running at 26MHz, supporting a primitive user interface. After a steady increase in clock frequency to roughly 300MHz in the early 2000s, there was a sudden spurt towards 1 GHz and beyond. Moreover, following trends in laptops and desktops, processor architectures have become much more advanced, and smart phones incorporate four and even eight-core 64b processors, now running up to 2.5GHz. Heterogeneity was recently adopted to further improve power efficiency. Overall, energy efficiency has become the main challenge in designing application processors, graphics processors, media processors (video, image, audio), and modems (cellular, WLAN, GPS, Bluetooth) for mobile platforms. For video and image processing, the trend has been towards dedicated, optimized hardware solutions. Some examples of new areas where dedicated processors are particularly needed include gesture-based user interfaces, recognition processors, augmented reality and computational imaging. For all digital circuits, the limited power budget leads to more fine-grained power management, various forms of adaptive voltage-frequency scaling, variable device threshold and biasing schemes, and elaborate thermal management strategies.

Figure 4 shows the evolution of bitrates for wired and wireless links over time. Interestingly, cellular links, wireless LAN, as well as short links show a consistent 10× increase in data rate every five years, with no sign of abating. With essentially constant power and thermal budgets, energy efficiency has become a central theme when designing digital circuits for mobile baseband processing. With benefits from pure CMOS scaling flattening, alternative approaches to improve energy efficiency and system throughputs are pursued, such as new standards, smarter algorithms, more efficient digital signal processors, highly-optimized accelerators, optimized hardware-software partitioning, power management techniques, as well as inter-system aggregation and heterogeneous networks.

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Graphics	2D, 3D	OpenGL (ES1.1)	OpenGL/VG/MAX (ES2.0)	AR (Augmented Reality)			
Display	16b QVGA	VGA	WVGA @ 60fps	SXGA @ 60fps	WQXGA/WQXGA+ @ 60fps		
Camera	1-2M	3M	5~8M	10M	16M	20M	Dual camera	HD camera
Image/Video	JPEG, MPEG-4	H.264/AVC (VGA)	H.264/AVC (D1)	H.264/AVC (Full HD)	H.264/MVC H.264/SVC	H.265	
Audio	MP3	AAC	AAC Plus	WMA Dolby 5.1	Dolby TrueHD/Digital+		
Accelerator	DSP	FPU	SIMD Multi core (2-4)	Multi core (4-8)	Heterogeneous Multi-Processing		
downlink [Mb/s]	EGPRS 0.4	UMTS 0.4- 2	HSPA 1.8 - 7	HSPA+ 7 - 42	LTE 100	LTE-A 150-750	
CPU [MIPS]	-300	300 500	500 800	800 2400	2400 6000	6K 12K	12K 100K

2004 | 2005 | 2006 | 2007 | 2008 | 2009 | 2010 | 2011 | 2012 | 2013 | 2014 | 2015

Fig. 3 Application processor trends in smart phones.

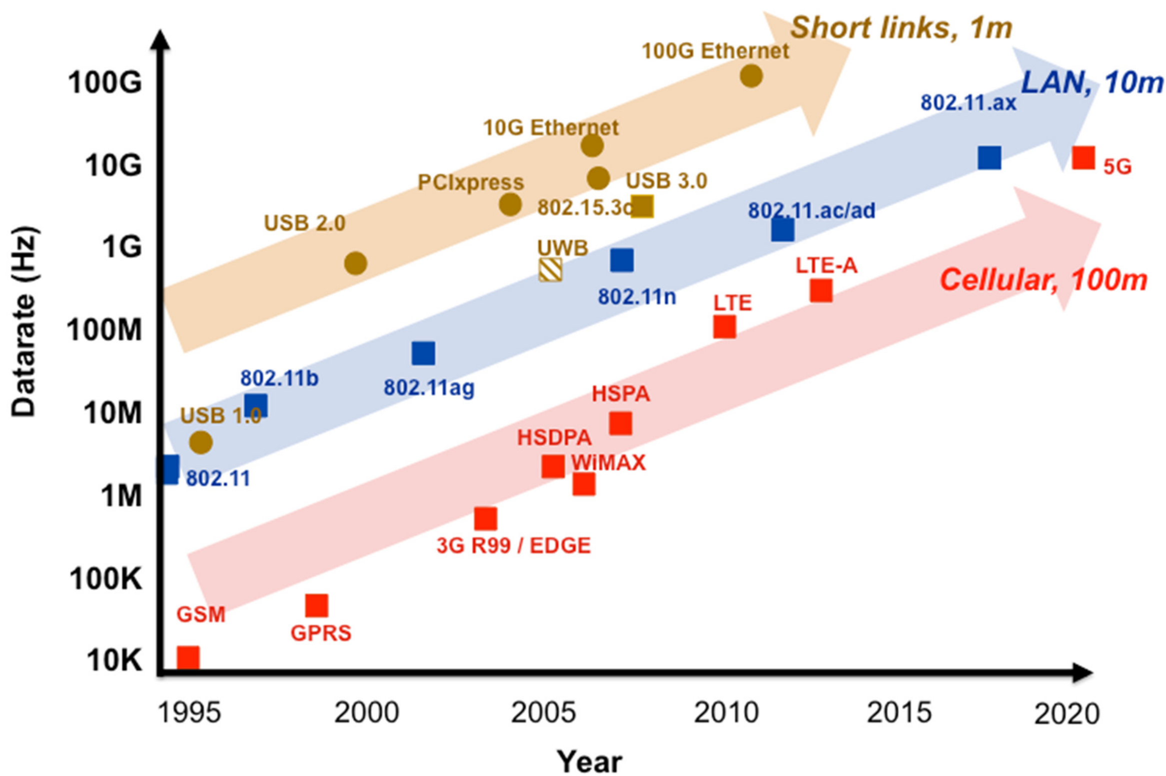

Fig. 4 Wireless and wired datarates over time.

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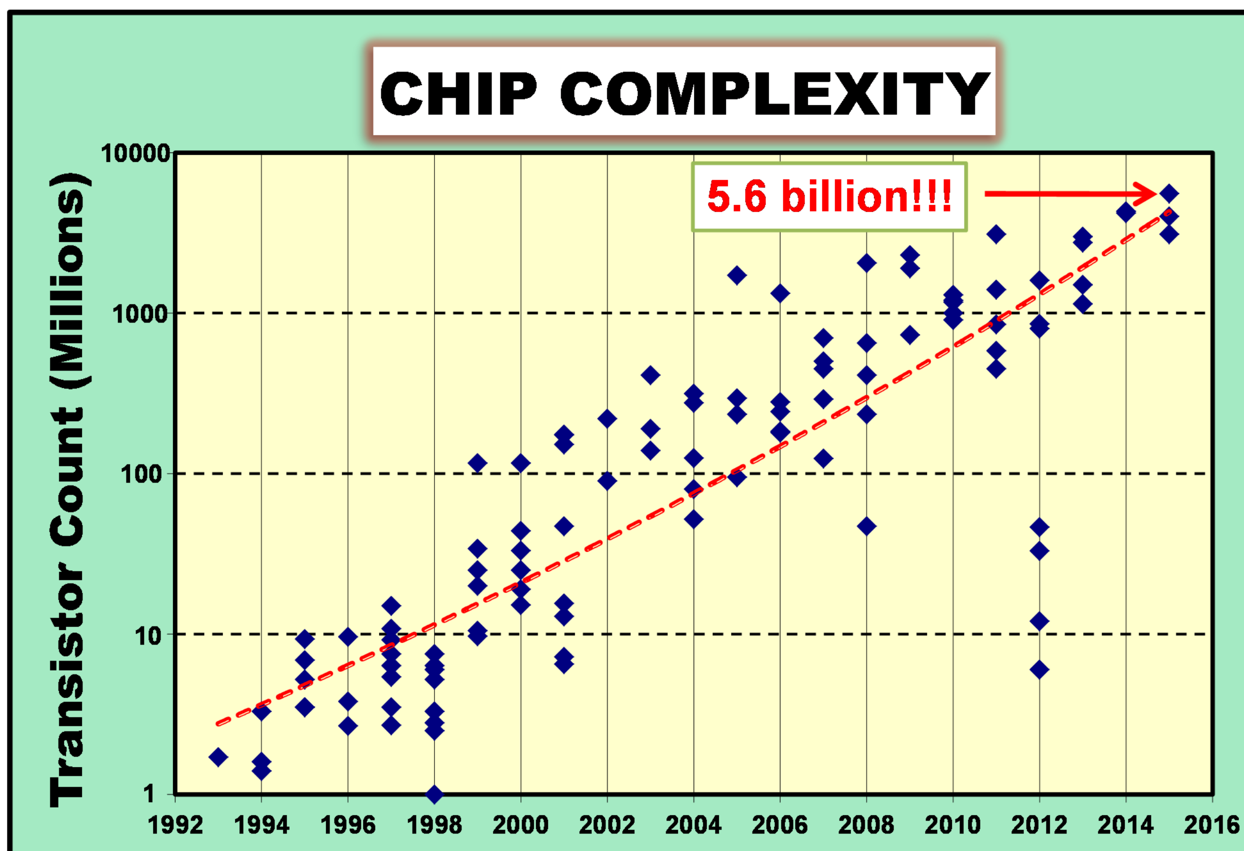
High-Performance Digital – 2015 Trends

Subcommittee Chair: *Stefan Rusu, Intel, Santa Clara, CA*

The relentless march of process technology brings more integration and energy-efficient performance to mainframes, enterprise and cloud servers. ISSCC 2015 features IBM's high-frequency 8-core, 16-thread System z mainframe processor in 22nm SOI with 64MB of eDRAM L3 cache and 4MB/core eDRAM L2 cache. The SPARC M7 processor from Oracle implements 32 S4 cores, a 1.6TB/s bandwidth 64MB L3 Cache and a 0.5TB/s data bandwidth on-chip network (OCN) to deliver more than 3.0x throughput compared to its predecessor. 280 SerDes lanes support up to 18Gb/s line rate and 1TB/s total bandwidth. Intel's next generation Xeon processor supports 18 dual-threaded 64b Haswell cores, 45MB L3 cache, 4 DDR4-2133MHz memory channels, 40 8GT/s PCIe lanes, and 60 9.6GT/s QPI lanes. It has 5.56B transistors in Intel's 22nm tri-gate HKMG CMOS and achieves a 33% performance boost over previous generations.

The chip complexity chart below shows the trend in transistor integration on a single chip over the past two decades. While the 1 billion transistor integration threshold was achieved some years ago, we now commonly see processors incorporating more than 5B transistors on a die.



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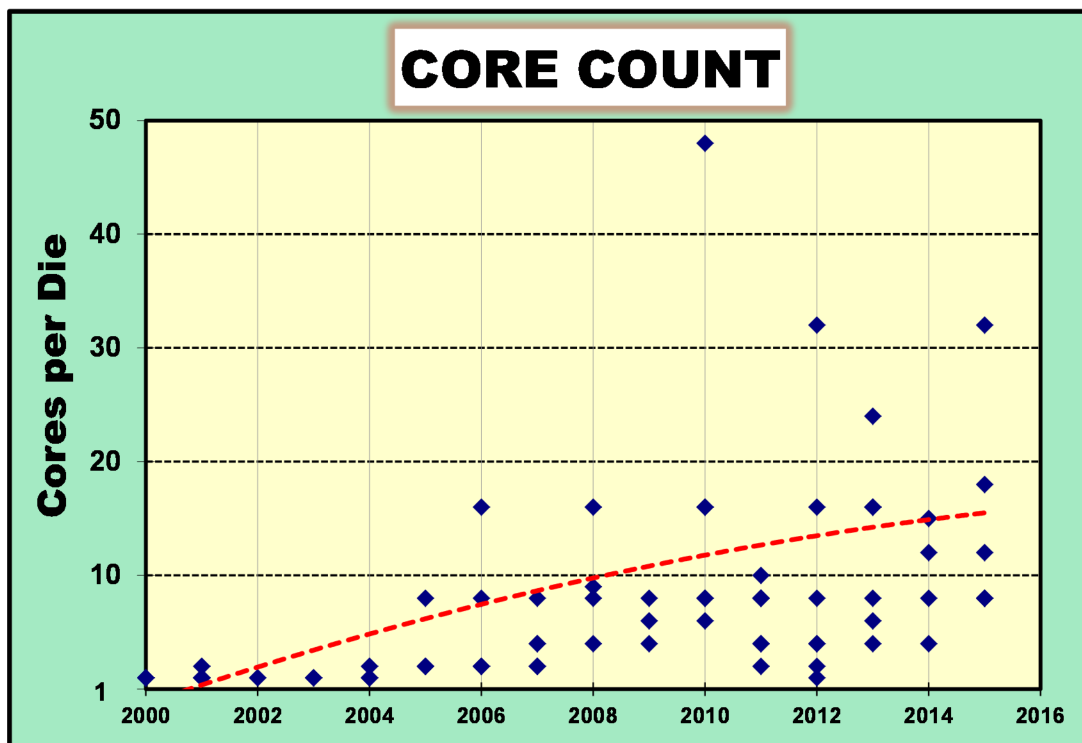

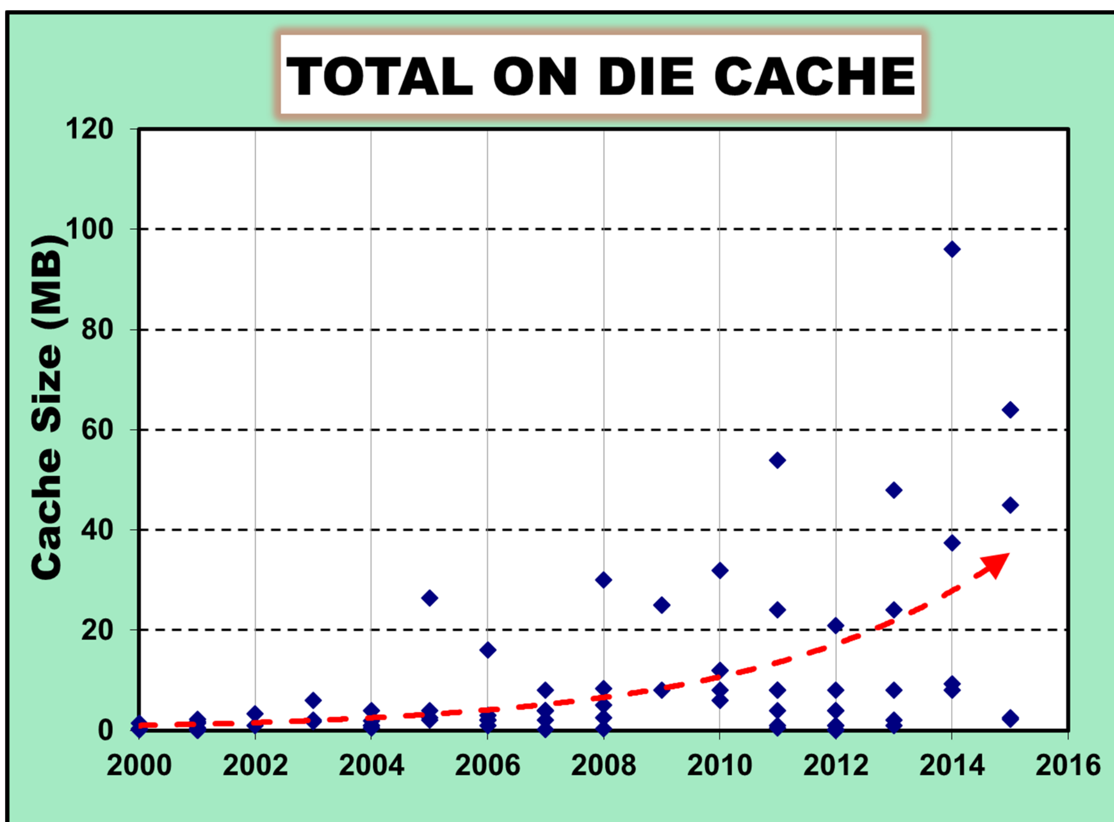

The maximum core clock frequency seems to have saturated in the range of 5-6GHz, primarily limited by thermal considerations. The nominal operating frequency of the power-limited processors this year is around 3.5GHz. Core counts per die are typically above 10, with increases appearing to slow in recent years. Cache size growth continues, with modern chips incorporating tens of MB on-die..

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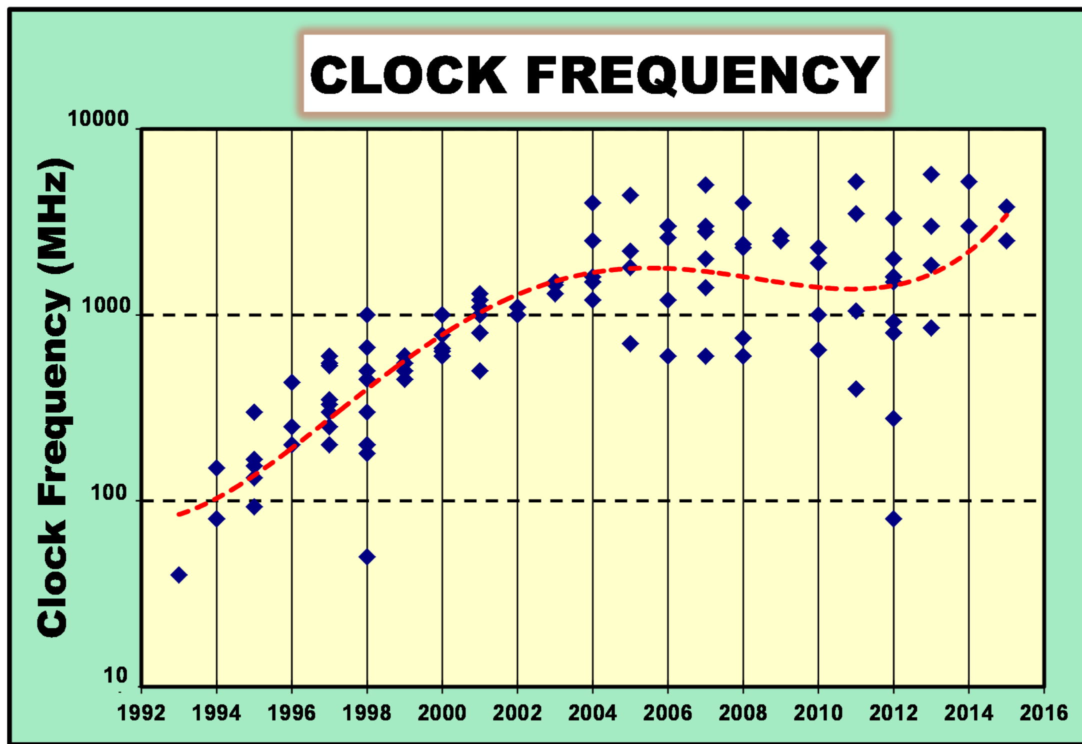

The trend towards digital phase-locked loops (PLL) and delay locked loops (DLL) to better exploit nanometer feature size scaling, and reduce power and area continues. Through use of highly innovative architectural and circuit design techniques, the features of these digital PLLs and DLLs have improved significantly over the recent past. Another new trend evident this year is towards fully digital PLLs being synthesizable and operated with non-LC oscillators. The diagram below shows the jitter performance vs. energy cost for PLLs and multiplying DLLs (MDLL).

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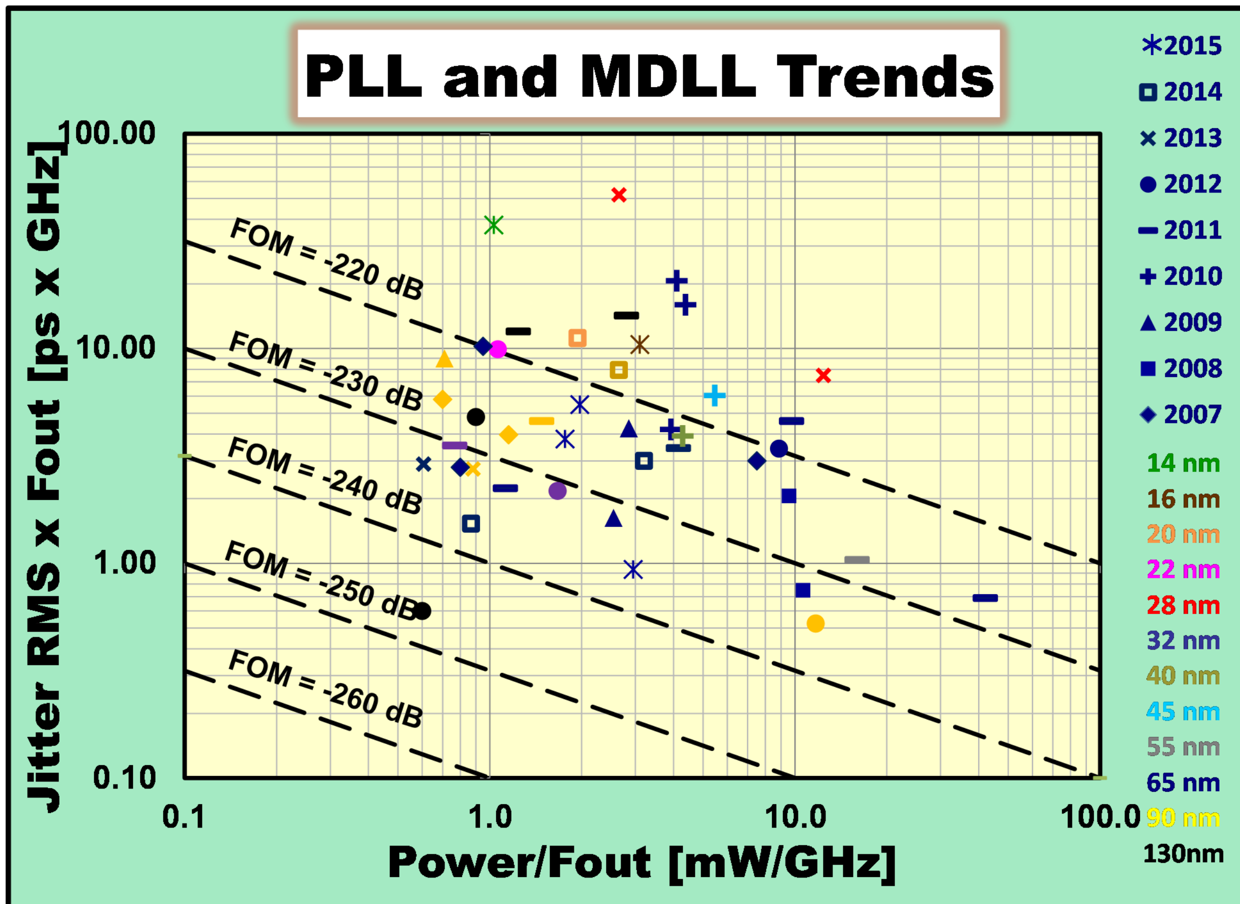

Overall, digital processors continue to grow in complexity, core count and cache integration (see figures above). We observe that traditionally analog building blocks are being implemented using digital techniques to cope with variability and ease scaling to finer geometries.

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MEMORY – 2015 Trends

Subcommittee Chair: *Joo Sun Choi, Samsung Electronics, Hwasung, Korea*

Mobile products are everyone's companion and need to store and process ever increasing amounts of data. Progress is only possible by constant improvements in area, power and performance of volatile and non-volatile memories. FinFET technology is now mainstream for embedded SRAM and DRAM, and has facilitated continued scaling. Improvements in DRAM data rates support the increasing demands of greater data volumes. NAND Flash memories have moved from 2b/cell to 3b/cell and 3D multi-layer designs are now typical. Embedded Flash, which is essential to IoT and wearable applications, has moved to 28nm. STT-MRAM is the most mature of the emerging memories, although ReRAM is quickly catching up.

Some current state-of-the-art papers from ISSCC 2015 include:

- Two 14nm SRAM bitcells; 0.0500 m^2 (HDC) and 0.0588 m^2 (LVC) capable of achieving 1.5GHz operation at 0.6V
- A 14nm FinFET SOI eDRAM with a cell size of 0.01747μm^2 and 1ns access time
- 128Gb 3 b/cell 32 stacked WL layer 3D NAND Flash running at 1Gb/s I/O rate
- A low power 64Gb 2b/cell NAND flash manufactured in 15nm technology
- A 1.1V 10Gb/s/pin transceiver for DRAM interface suitable for use beyond LPDDR4
- A high-speed 1Mb STT-MRAM using 2T2MTJ cells achieves 3.3ns access time and a sub-20nm technology node STT-MRAM uses a high density 1T1MTJ memory cell.
- A 28nm embedded SG_MONOS FLASH developed for automotive applications.

SRAM

Consumer and computing products in 2015, from smart watches to the cloud, depend on low-power and high-performance embedded SRAM. Challenges for SRAM include V_{MIN}, leakage and dynamic power reduction. Last year saw the first introduction of 14nm/16nm technology. This year a 14nm SRAM using 2nd generation FinFET technology discloses the smallest SRAM bitcell ever reported at just 0.050μm^2. As the transistor feature size advances further below 20nm, device variation has made it very difficult to shrink the bit cell size at the desired 50% rate while maintaining or lowering V_{MIN} between generations. Introduction of high-k metal-gate (45nm) and FinFET or fully-depleted SOI transistors (22nm) reduces the V_{TH} mismatch and have enabled further device scaling. Design solutions such as read/write assist circuitry and variation-tolerant sensing schemes have been used to improve SRAM V_{MIN} performance starting at 32nm and are now ubiquitous in high-density SRAM designs at 14/16nm. Dual-rail SRAM design emerges as an effective solution to enable dynamic voltage-frequency scaling (DVFS) by decoupling logic supply rails from SRAM arrays and thus allowing much wider operating window. The use of assist circuit techniques, FinFET transistors and dual-rail architectures is expected to extend the viability of using the high-density 6T SRAM bitcell beyond 14nm. It is important for SRAM to reduce both leakage and dynamic power, keeping products within the same power envelope at the next technology node. Last year we heard about the first FinFET based eDRAM at 22nm. This year a 14nm FinFET based eDRAM is discussed. eDRAM continues to show itself as a desirable way to provide memory scaling in high-performance CPU designs. Figure 1 shows the bit cell and V_{DD} scaling trend of SRAM from major semiconductor manufacturers.

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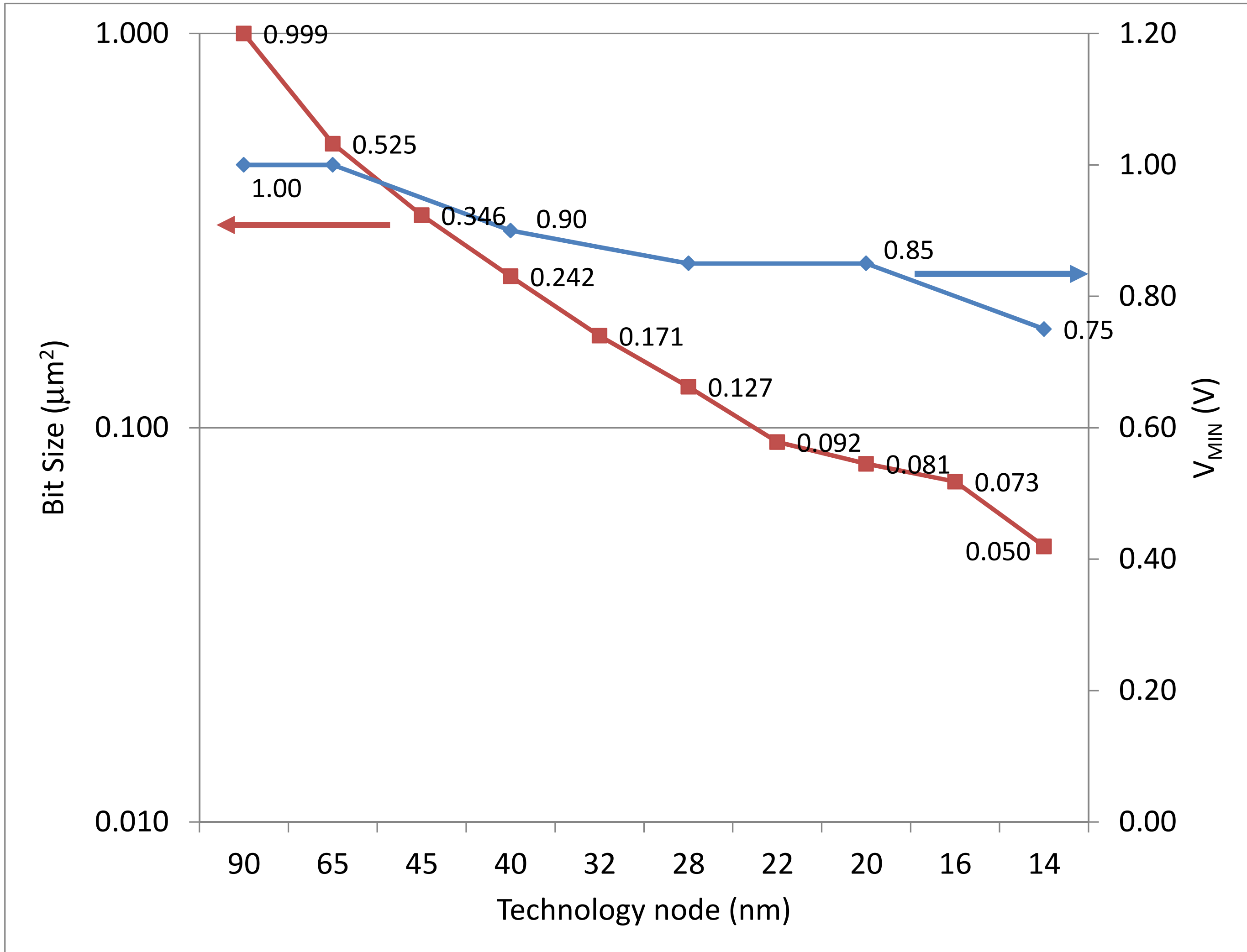

Figure 1 – Bit Cell and V_{DD} scaling trend of SRAM

HIGH-BANDWIDTH DRAM

In order to reduce the bandwidth gap between main memory and processor performance, DRAM data-rates continue to increase at the memory interface with schemes such as DDR(x), LPDDR(x) and GDDR(x), as shown in

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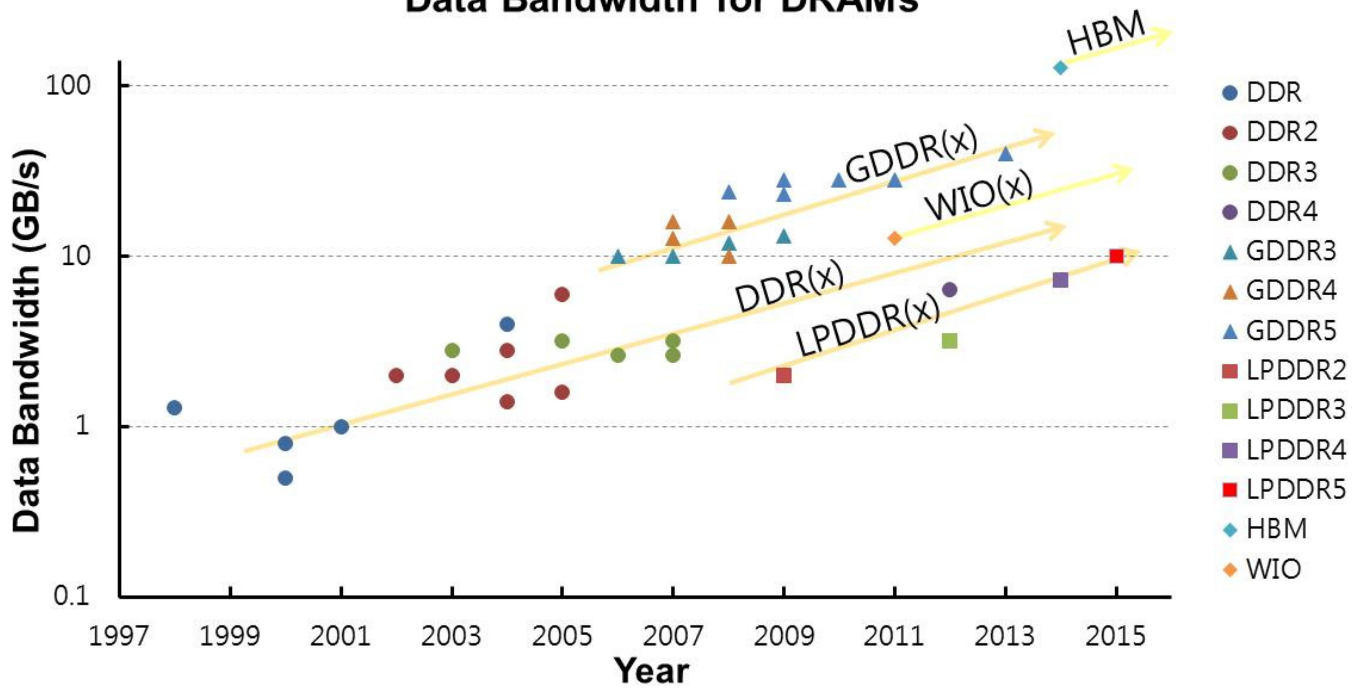

Figure 2. Currently, DDR4 and GDDR5 memory I/Os operate around 3Gb/s/pin and 7Gb/s/pin, respectively, which represent aggregate rates of 6GB/s and 28GB/s, respectively. A digital DLL with hybrid DCC using a 2-step duty-error extraction and 180° phase aligner for 2.67Gb/s/pin 16Gb DDR4 SDRAM with TSV's is covered. Last year LPDDR4 SDRAM was introduced at 3.2G/ps/pin at 1.0V. This year, an interface suitable for use beyond LPDDR4 operating at 10Gb/s is demonstrated.

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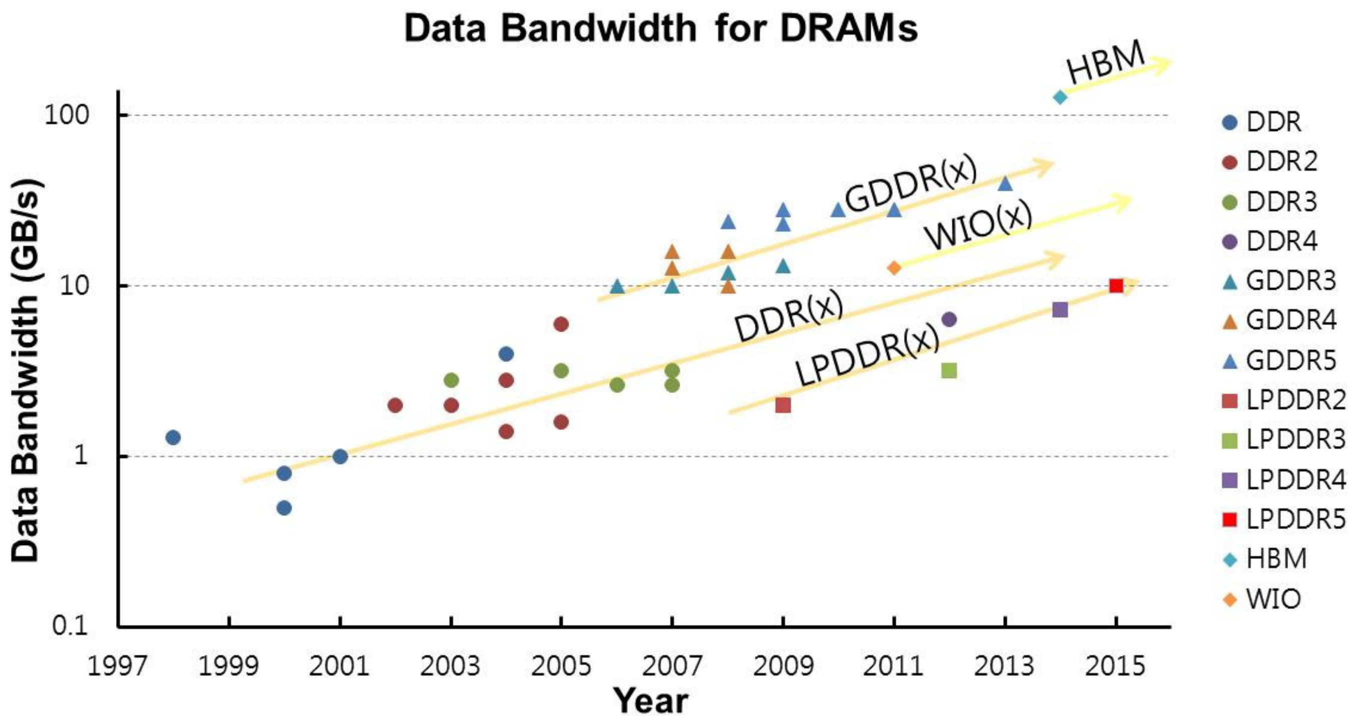

Figure 2 - DRAM Data Bandwidth Trends

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NON-VOLATILE MEMORIES

In the past decade significant investment has been put into the emerging memories field to find an alternative to floating-gate based non-volatile memory. The emerging NVMs, such as phase-change memory (PRAM), ferroelectric RAM (FeRAM), magnetic spin-torque-transfer (STT-MRAM), and resistive memory (ReRAM), are showing potential to achieve high cycling capability and lower power per bit in read/write operations. Figure 3 highlights how 3b/cell (TLC) NAND Flash write throughput continues to improve and even though Figure 4 shows no increase in NAND Flash density over last year, these devices are built with finer dimensions or more sophisticated 3-dimensional vertical bit cells.

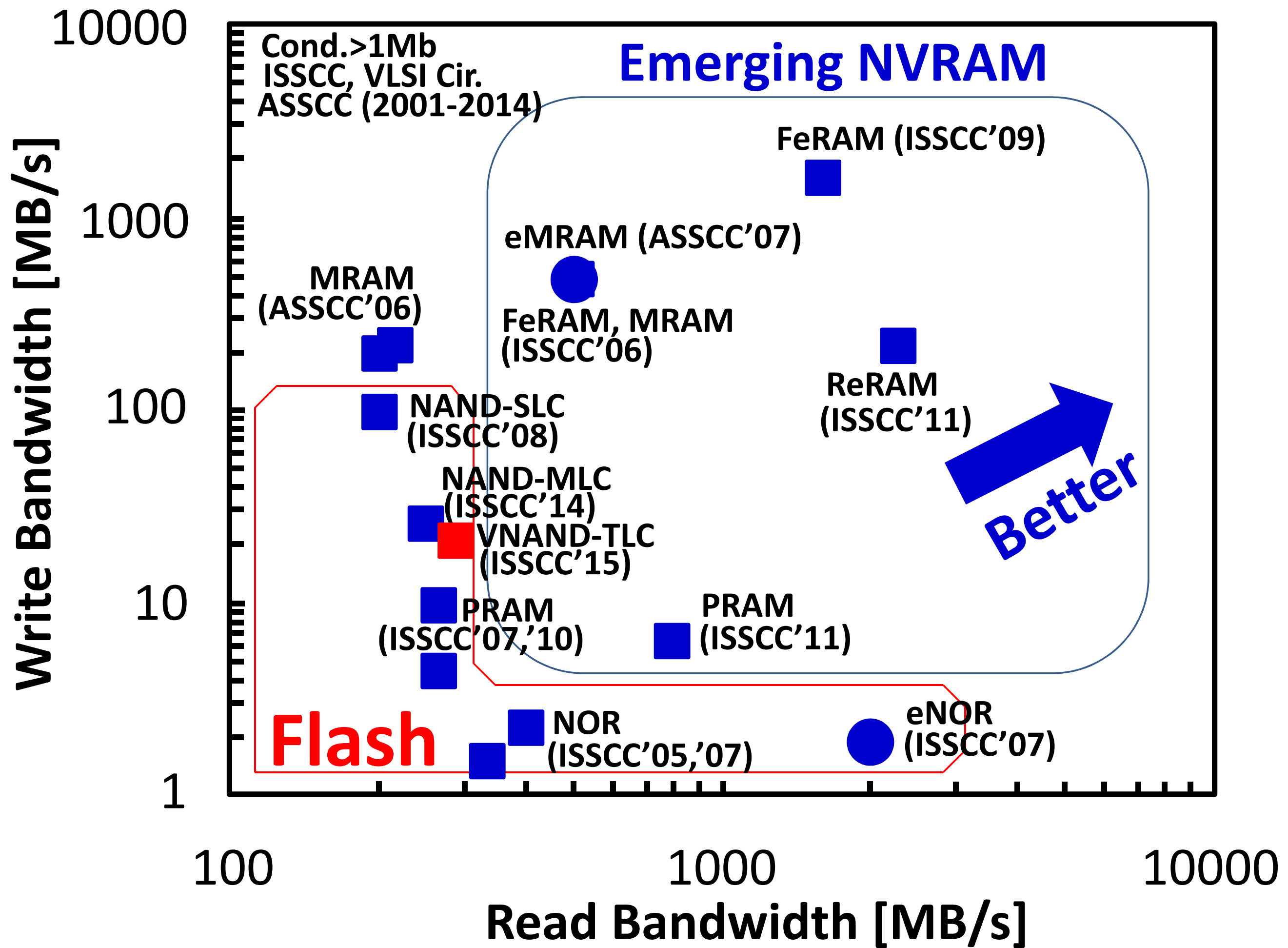

Figure 3 - Read/Write Bandwidth Comparison of Nonvolatile Memories

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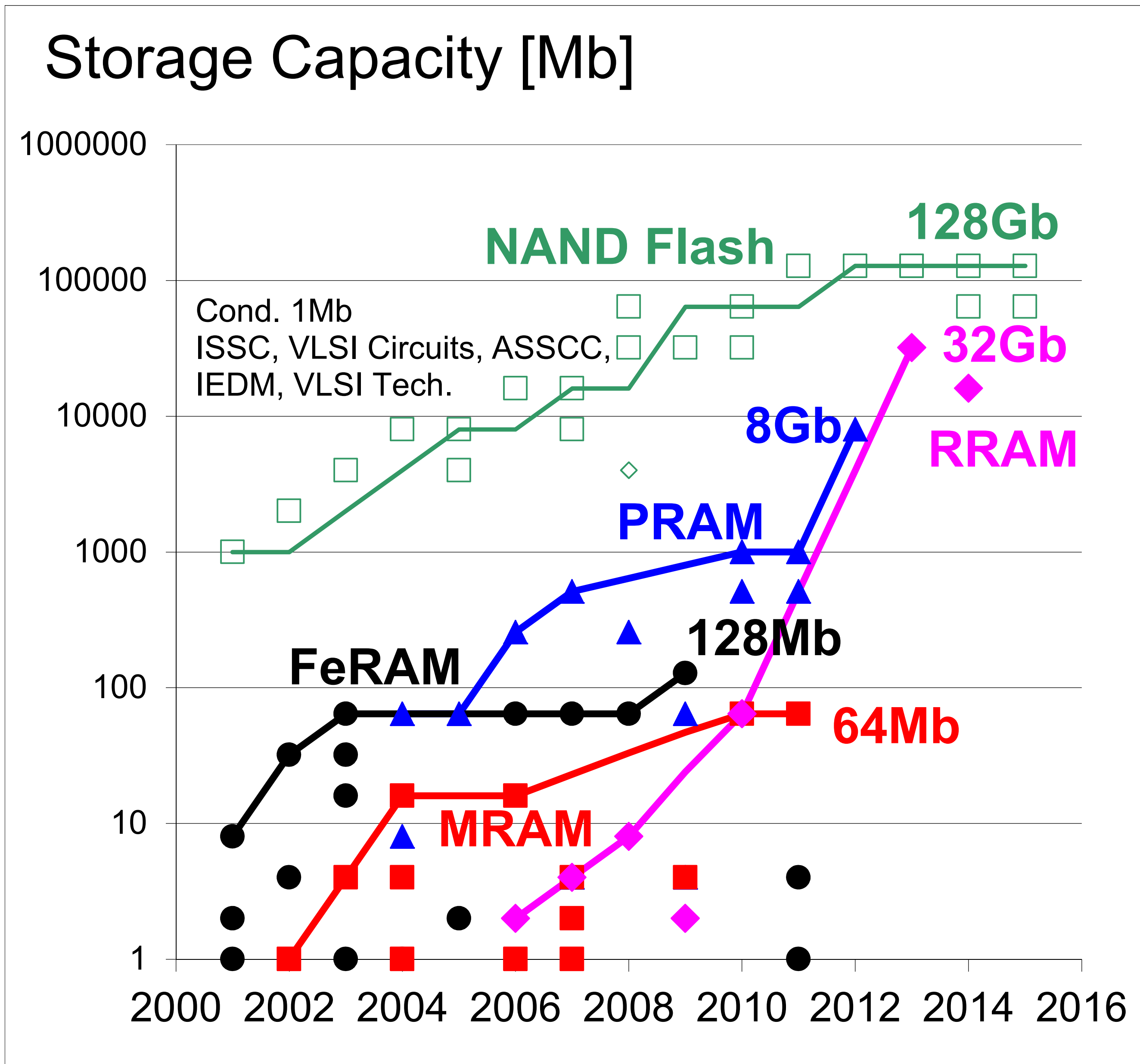

Figure 4 - Memory Capacity Trend of Emerging Nonvolatile Memories

NAND FLASH MEMORY

NAND Flash memory continues to advance towards higher density and lower power, resulting in low-cost storage solutions that are replacing traditional hard-disk storage with solid-state disks (SSDs). SSDs with typical storage density of 240GB have become the mainstream. Despite the growing difficulties to further scale down planar cell technology, the latest 2D NAND Flash technology is scaled down to 15nm, achieving a low power 1.8V 64Gb device occupying only 75mm^2. It will be very interesting to see how far planar NANDs go down the scaling path. This year, 3D NAND is extended to 3b/cell and 32 stacked wordline (WL) layers, to satisfy the ever-growing demand for increased density requirements and lower manufacturing cost. As IoT becomes more of a reality, embedded Flash becomes a critical technology. This year a 28nm SG-MONOS embedded Flash for an automotive application is discussed. Figure 5 shows the observed trend in NAND Flash capacities presented at ISSCC over the past 20 years.

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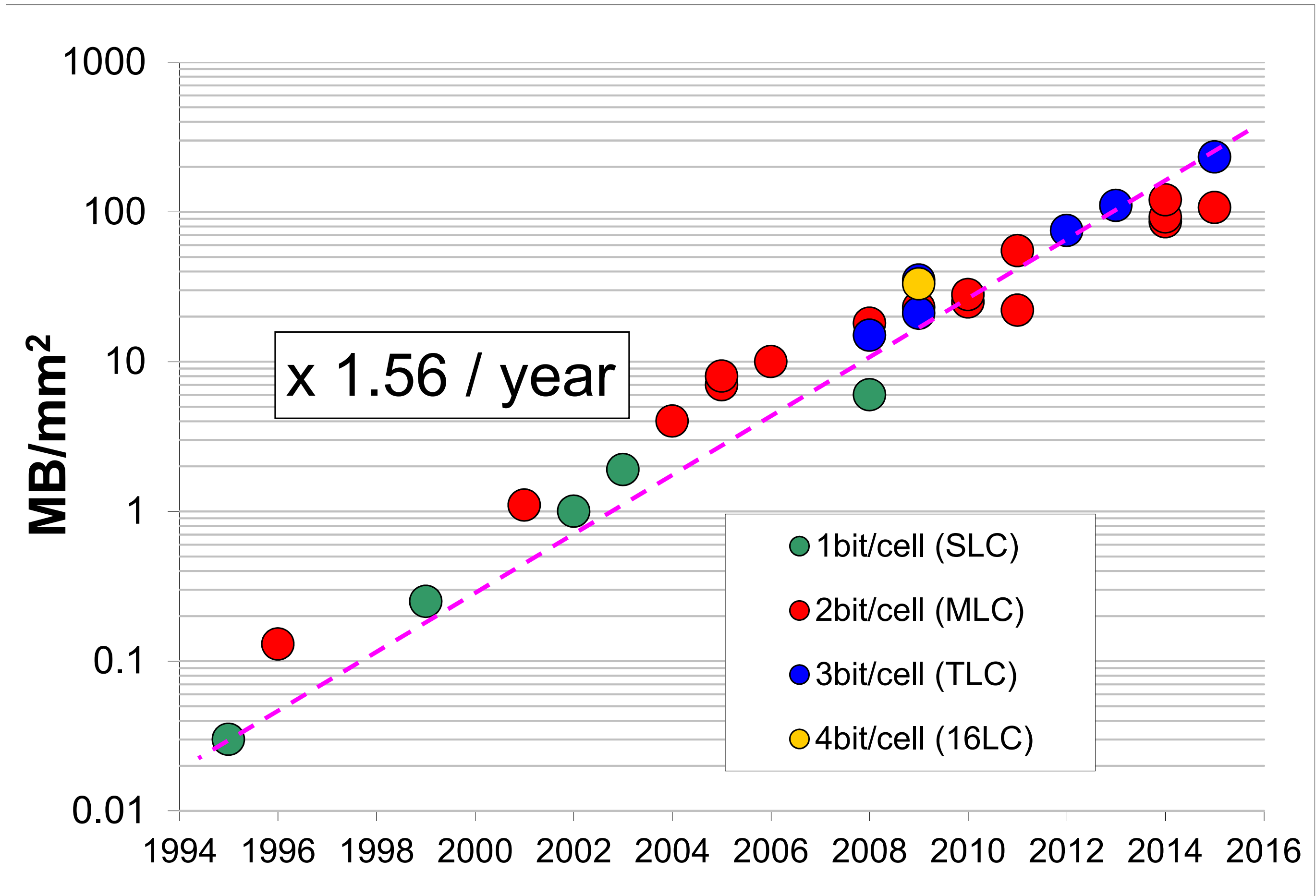

Figure 5 - NAND Flash Memory Trends

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IMAGERS, MEMS, MEDICAL DEVICES & DISPLAYS SUBCOMMITTEE
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IMMD – 2015 Trends (Imagers)

Subcommittee Chair: Makoto Ikeda, University of Tokyo, Tokyo, Japan

The CMOS-image-sensor business is one of the fastest-growing segments of the semiconductor industry. Key applications include cellphone cameras, digital still cameras, camcorders, security cameras, automotive cameras, digital-video cameras, wearable devices, and gaming.

The resolution and miniaturization races are ongoing but slowing down, and while the performance requirements stay constant, pixel size continues to scale down (see Figure 1). Images of over 40M pixels are commercially available, and sensors for large TV format (8K) have been reported. A column-parallel approach based on pipelined and multiple-sampling implementations has become standard for low-power, high-speed, low-noise camera and video applications. Backside illumination is now a mainstream technology for mobile imaging. Wafer stacking of the image array on a CMOS image signal processor is becoming more common.

The importance of digital signal processing technology in cameras continues to grow in order to mitigate sensor imperfections and noise, and to compensate for optical limitations. The level of sensor computation is increasing to thousands of operations-per-pixel, requiring high-performance and low-power digital signal processing solutions.

High Dynamic Range (HDR) is now well established in low-cost consumer imaging. While HDR combines multiple distinct images, new work is progressing with specialized architectures to extend the dynamic range in single exposures, and thus avoid movement artifacts.

As well, global shutters are being introduced to avoid movement artifacts. For precision scientific, medical applications, and consumer products, we now employ single-photon avalanche diode (SPAD) imager arrays. Deep-submicron CMOS SPADs will meet the requirements for high resolution, high accuracy time-to-digital converters (TDCs), and small-pitch imagers with better fill factor. Wafer stacking of the SPAD array on a CMOS image signal processor is an emerging trend.

The market share of CCD imagers continues to shrink and they are now relegated to minor applications. Top-end broadcast and top-end digital cameras have moved from CCD to CMOS sensors (see Figure 1).

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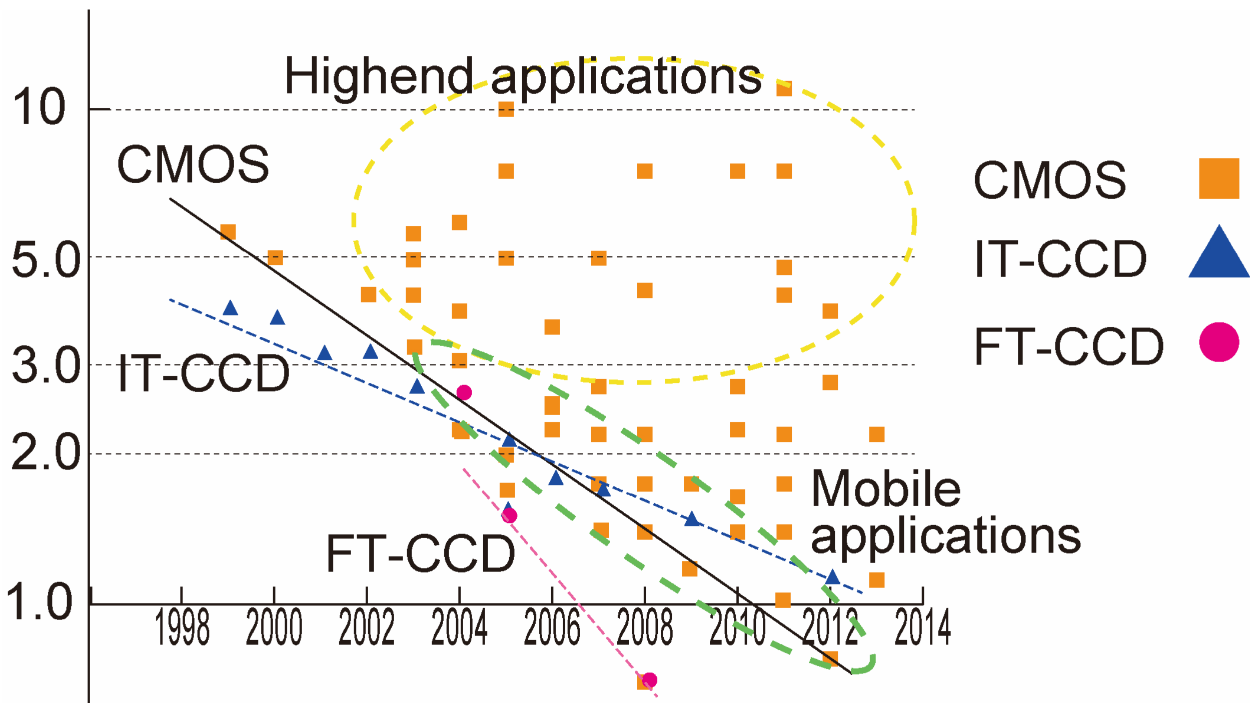

Figure 1: Pixel size trends

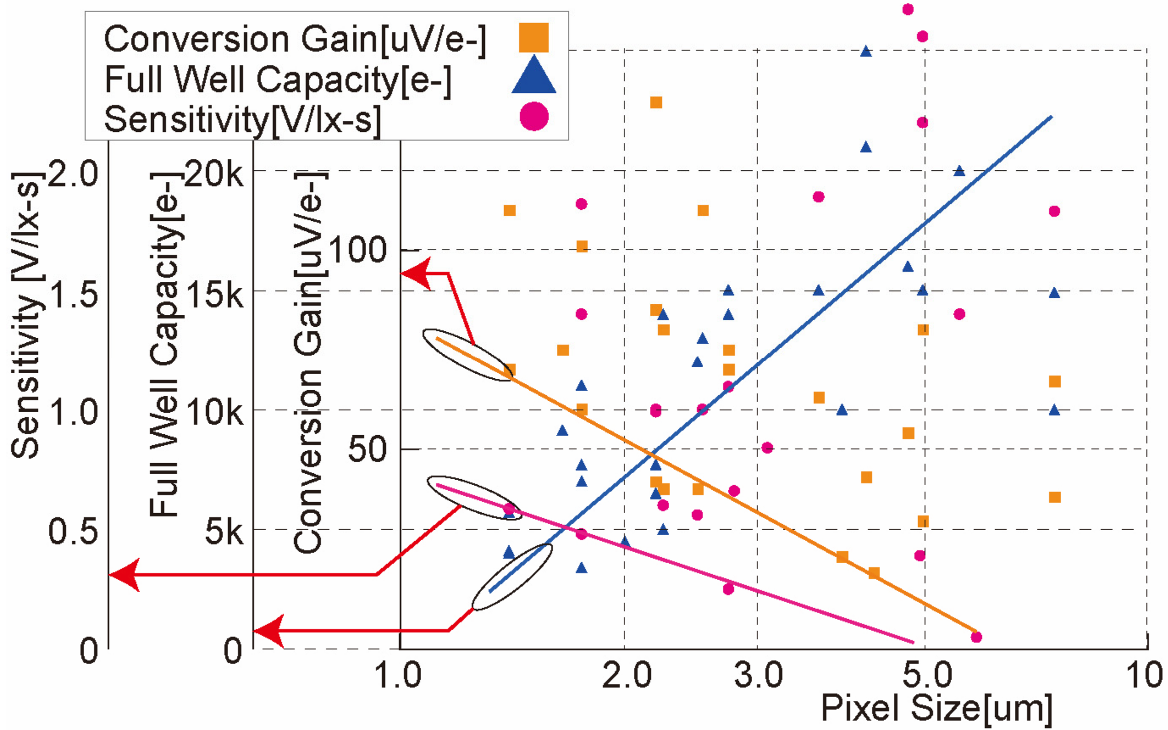

Figure 2: Image sensor performance trends: sensitivity, full-well capacity and conversion gain vs. pixel size.

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IMMD – 2015 Trends (Sensors & MEMS)

Subcommittee Chair: *Makoto Ikeda, University of Tokyo, Tokyo, Japan*

MEMS inertial sensors (accelerometer and gyroscopes) are key components used in a large variety of consumer products, where ultra-low power consumption is a key requirement. For automotive applications, reduced vibration sensitivity and high precision are additional requirements.

CMOS temperature sensors continue to improve, with new circuit techniques increasing accuracy and supporting wider applications. Strides in low-power architectures continue to eclipse previous results with record-setting efficiency that support battery-operated and mobile applications. Pure digital implementations are often used in thermal monitoring for large SoCs, which is an important application where small sensor area is a key feature.

Current sensors are becoming more integrated and precise. These devices detect the magnetic field around a wire or trace carrying a current, and they are used for instance in electrical motor drives, solar power, and battery charge applications.

Capacitive-to-digital converters are essential sensor interface components, where new circuit technologies result in increased accuracy, smaller die size, and reduced power consumption. Digital-centric implementations enable these improvements to be maintained in more advanced processes.

MEMS pressure sensors are getting smaller, and fully integrated systems have been reported.

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IMMD – 2015 Trends (Medical)

Subcommittee Chair: Makoto Ikeda, University of Tokyo, Tokyo, Japan

There is an ever-increasing demand for higher-throughput life-science tools, e.g., cellular and molecular assays, coming from the field of precision and personalized medicine. Electronic platforms for genomics, proteomics, and cellular assays bring improved accuracy and throughput. For example, increased sensitivity has been successfully exploited for detection of chemical reactions through physical means, e.g., pH, charge, or impedance changes, in DNA sequencing.

For improved capability and quality, medical ultrasound is moving toward 3D imaging with large arrays. As these arrays increase in size, the number of connections to the front-end processing circuitry, and the amount of required signal processing are becoming bottlenecks. To resolve this congestion, MEMS transducers and CMOS technology increasingly allow transducer arrays and their signal processors to be mounted together.

Smart wearable sensors for medical applications will support continuous remote monitoring with data transmission to centralized analysis systems. These sensors will adapt their algorithms to match a specific user's vital signs. Potentially, closed-loop control will allow therapy to be applied directly, for instance to suppress seizures or arrhythmias.

Medical imaging is an important field with a growing number of applications. One such example is positron emission tomography (PET), where solid-state implementations allow PET scanning to be carried out simultaneously with magnetic resonance imaging (MRI), which opens up new and improved cancer diagnostic methods. Another example is wide-field microscopy imaging, where higher resolution and shorter time gating are enabled by smaller pixel pitch, and faster detectors, respectively.

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IMMD – 2015 Trends (Displays)

Subcommittee Chair: *Makoto Ikeda, University of Tokyo, Tokyo, Japan*

Touch- and gesture-sensing systems for large displays are in development. These will require extensions of capacitive-sensing technology beyond the present state of the art. Applications will require sensing hand gestures at a distance (30cm), and high-resolution touch for writing recognition. Hovering touch systems, and active as well as passive pen input systems (styluses) are emerging trends. Touch sensors simultaneously detecting position and pressure have been reported.

LCD panels with integrated touch sensing are being driven toward thinner and lower-cost single-chip solutions. Robust circuit technology that is immune to display-driver noise is a key design factor.

Higher-resolution and higher-definition displays are being developed for mobile applications. Displays with more than 500 pixels-per-inch (ppi) are now in production, for 6-inch and smaller displays. While low-temperature polysilicon (LTPS) technology seems to be superior to amorphous-silicon (a-Si), traditional a-Si TFT and oxide TFT technologies supported by compensating driver systems are being prepared to compete.

Plastic organic light-emitting diodes (OLEDs) are entering into commercial production for curved smartphones. These will give improved user experiences, being very thin, light, and unbreakable. They are also expected to find applications in wearable displays.

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Technology Directions – 2015 Trends
"Innovative Systems"

Subcommittee Chair: *Eugenio Cantatore, Eindhoven University of Technology, Eindhoven, The Netherlands*

This year at ISSCC 2015 the theme is "SILICON SYSTEMS — SMALL CHIPS for BIG DATA". System considerations are extremely important for circuit engineers. The system designer defines the performance parameters such as power, bandwidth, SNR or QoS, etc. that hardware has to comply to. The system designer also helps to jointly optimize all the building blocks of the entire system. The next level of innovation will come from the mutual understanding of how all parts of the system work together so that the design team can optimize across multiple layers. For this reason, ISSCC's Technology Directions subcommittee is highlighting system aspects by providing two sessions that focus on innovative systems. These sessions will present papers from two types of systems that will continue to drive future innovations: Session 21 is on "Innovative Personalized Biomedical Systems" and Session 24 showcases "Secure, Efficient Circuits for IoT".

Innovative Biomedical Systems

A breakthrough concept in biomedical electronics has been the development of "anytime and anywhere" human monitoring systems using wearable/implantable devices. It will enable improvements of the quality of life, such as self-health checks, remote medical examination, and constant monitoring for acute diseases.

Key technologies for such systems include:

(1) Small footprint devices and flexible electronics to enhance the comfort of wearable devices,
(2) High accuracy and low-power monitoring devices,
(3) Low-power communication systems for wireless operation.

To develop devices with a small footprint, highly integrated biomedical SoCs capable of sensor detection, diagnosis and wireless communication have been developed. Progress in the development of 3D-integrated electrodes and sensors with MEMS has also contributed to reduce the footprint. To monitor weak vital signs, such as electrocardiogram (ECG) and electroencephalogram (EEG), with a high degree of accuracy, there is clear progress in variation correction methodologies and techniques to compensate for artifacts due to the subject's movements. Furthermore, state-of-the-art biomedical SOCs are capable of multimodal tele-monitoring of various bio-signals. To improve the device longevity, SOCs have evolved to contain a power-efficient dedicated processor and algorithms for diagnosis, ultra-low-power circuit blocks, low-power wireless circuits and energy-harvesting technologies. Furthermore, different communication standards are being developed to satisfy the low-power requirements of portable medical systems.

Another trend in technology directions is a move towards Lab-on-a-Chip or semiconductor systems for diagnosis and disease screening. Silicon solutions are being designed for portable systems to quickly and inexpensively diagnose illness from simple blood tests to imaging to spectroscopy. The trend of using emerging technologies such as MEMS or CMOS-CNT (carbon nanotube) arrays to solve medical problems will make it possible to bring traditionally expensive diagnosis tools to rural and remote areas where medical expertise is typically scarce.

In line with these trends, ISSCC 2015 Session 21 features 9 papers representing the latest technological innovations in bio-medical systems.

Ultra-Low-Power and Secure Systems for IoT Applications

In the past few decades, many new applications such as mobile devices and the Internet have driven the growth of high-performance computing systems. The next big applications will focus on the Internet of Things (IoT) that require secure systems with ultra-low power including autonomous sensors and big-data analysis platforms. Important trends and challenges of the future that need system innovation include:

(1) Counter measures for post-quantum cryptography,
(2) Efficient extraction of relevant context from autonomous sensors,
(3) Processors for big-data analysis.

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To protect privacy and properties in the Internet-of-Things era, various technologies for post-quantum cryptography are being introduced as a counter measure for quantum computers, which will be available in the near future. With quantum computers, mathematically hard problems used to protect encryption keys turn into easy problems. Therefore, new algorithms such as lattice-based ring learning with errors (RLWE) is necessary. For extensive deployment of autonomous smart sensors, low-power architectures for context-aware sensors are being developed. For example, a hierarchical sensing architecture will turn on the minimum amount of sensor circuitry when it is waiting for data to come in, but will later turn on the full sensor after detecting the incoming data. In-sensor feature extraction is another trend to reduce power and performance requirements of host processors. To efficiently analyze massive data collected from various sensors, innovative computing architectures such as spin computing and machine-learning co-processors are also emerging.

New circuit technology is also needed to reach the power and performance requirements of autonomous sensors. One example is an ultra-low power ADC operating near sub-threshold voltage. A second example involves circuits for harvesting energy from thermal and light sources. Sub-threshold operation greatly improves energy efficiency of overall circuits at the expense of maximum operating speed, which is usually not a concern for IoT sensors. At ISSCC 2015, Session 24 includes three papers presenting innovative techniques on counter measures for post-quantum cryptography, ultra-low-power hierarchical sensing, and computing architectures for big data analysis.

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Wide Bandgap Power Devices: GaN and SiC

Power electronics blocks are becoming ubiquitous and can be found in almost every electrical and electronic system from inverters that connect solar panels and wind turbines to the electric grid, to electric vehicles, industrial motors and laptop power adapters. For nearly 50 years, silicon chips have been the basis of power electronic circuits. However, as clean energy technologies and the electronics industry have advanced, silicon chips are reaching their limits in power conversion — resulting in too much wasted heat as well as higher energy consumption. The wide bandgap (WBG) semiconductors such as Gallium Nitride (GaN) and Silicon Carbide (SiC) have the potential to change this. As compared to silicon, WBG semiconductors operate at higher temperatures, frequencies and voltages — helping to eliminate a large portion of the power losses in electricity conversion.

Currently, GaN and SiC technologies, particularly for power devices, are becoming mature. For instance, high-voltage SiC power diodes are expanding their market by leaps and bounds due to their lower loss and higher speed. Furthermore, GaN power switches are being introduced in compact DC/DC converters and inverters for low-power applications due to their high-speed operation, which in turn, is leveraged to meet the demand for smaller system sizes.

As GaN power devices are expanding their application domain, supporting circuit blocks such as specialized integrated gate drivers, high-speed signal and power isolators, and high-frequency passive components that can fully exploit the speed performance of GaN power devices are becoming increasingly important.

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4. INDEX

A paper number mentioned in this section follows the convention S.P, where S is the session number and P is the paper number. For example 23.2 will be second paper in the twenty-third session. You can refer back to the TECHNICAL SESSION OVERVIEWS in this Press Kit for additional details on any given paper. Some of the papers will also be available in the not-so-technical SESSION HIGHLIGHTS part of this Press Kit. All sessions and papers are in ascending order in both the Session Overview and the Session Highlight parts of this Press Kit.

4.1 Technical Topics mapped to Papers

Technical Topic	All papers in the following Sessions
Communication Systems includes Wireless, RF, and Wireline subcommittees	**2, 3, 9, 10, 13, 19, 22, 25**
Analog Systems includes Analog and Data Converters subcommittees	**5, 12, 15, 20, 26**
Digital Systems includes Memory, Energy-Efficient Digital and High-Performance Digital subcommittees	**4, 7, 8, 14, 17, 18, 23**
Innovative Topics includes Imagers/MEMS/Medical Devices and Technology Direction subcommittees	**6, 11, 16, 21, 24, 27**

4.2 Selected Presenting Companies/Institution mapped to Papers

Affiliation	Paper Numbers
*Now at Qualcomm	13.6
Aix-Marseille University	8.4
AMD	4.8
Analog Devices	5.1, 25.1
Apix Analytics	16.5
ARM	8.1, 14.6
Asygn	16.5
Avago Technologies	25.9, 27.4
AVL	9.2
Bosch Sensortec	27.3
Broadcom	2.1, 3.1, 3.4, 9.1, 25.3, 26.3, 26.6
California Institute of Technology	22.3

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Case Western Reserve University	21.4
CEA-LETI-MINATEC	2.10
Chang Gung University	21.6
Chonnam National University	16.6
Chuo University	7.7
Columbia University	14.7, 19.1, 19.4
Coriant Advanced Technology Group	22.6
Cornell University	25.5, 25.8
Daegu Gyeongbuk Institute of Science and Technology	5.10
Dartmouth College	20.2
Delectronics	15.3
Delft University of Technology	5.2, 11.4, 14.5, 25.4, 27.5, 27.7, 27.8
Dialog Semiconductor	13.3
DMCE	9.2
EASii-IC	8.4
Eindhoven University of Technology	9.6, 13.2, 15.4, 21.2, 26.2
EPFL	10.3
ETH Zürich	20.3
Festo	16.1
Fondazione Bruno Kessler (FBK)	11.3
Forza Silicon	6.2
Freescale Semiconductor	4.4
Fudan University	22.4, 22.6
Fujitsu Laboratories	22.2, 22.7, 22.8
Fujitsu Laboratories of America	22.2
Fujitsu Limited	22.2
Fukuoka Institute of Technology	17.3
Georgia Institute of Technology	2.8, 5.6, 11.7, 12.7, 12.9
Hewlett-Packard	22.6
Hewlett-Packard Labs	22.4
HiSilicon	2.2
Hitachi	3.2, 24.3

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Holst Centre / imec	13.2, 20.8, 26.2
Holst Centre / TNO	16.3
Hong Kong University of Science and Technology	12.8, 20.4, 20.5, 25.6
HSG-IMIT	20.6
Hynix Semiconductor	17.6
IBM	17.4
IBM Research	4.1, 4.4, 10.9, 20.3
IBM Systems and Technology	4.1
IBM T.J. Watson	22.1
IBM Zurich	10.6
imec	2.2, 9.3, 16.3, 19.7, 20.8, 22.5
imec - Ghent University	22.5
IMS CHIPS	16.1
Infineon Technologies	5.8
Institute of Microelectronics	5.10
Instituto Superior Tecnico	2.4, 20.4, 26.5
Integrated Device Technology	9.6
Intel	3.5, 3.7, 4.5, 4.7, 8.6, 8.7, 9.2, 10.5, 17.1
InterDigital Communications	19.4
ITRI	17.5
Japan Aerospace Exploration Agency	24.4
JST/ERATO	16.4
KAIST	4.6, 5.10, 6.8, 11.1, 12.1, 12.5, 13.1, 14.4, 18.1, 18.3, 21.1, 21.9, 26.4, 26.7
Kandou Bus	10.3
Keio University	10.1, 24.4
Korea University	17.6
KU Leuven	10.2, 16.3, 20.1, 20.8, 22.5, 24.1, 24.2
Kyung Hee University	16.6
Marvell	9.4
Masdar Institute of Science and Technology	21.8
Massachusetts Institute of Technology	13.7, 15.1, 15.6, 16.8, 25.5

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Maxim Integrated Products	5.2
MAYA Technologies	8.4
MediaTek	9.7, 10.8, 15.1, 15.2, 18.6, 23.3
Murata	2.2
Nanjing University of Science and Technology	27.2
Nanyang Technological University	2.3, 2.5
National Cheng Kung University	20.9
National Chiao Tung University	12.6, 17.5, 20.10
National Taiwan University	5.3, 21.5, 21.6, 23.2
National Taiwan University Hospital	21.6
National Tsing Hua University	17.3, 17.5, 23.2
National University of Singapore	11.6, 14.3, 27.2
NHK Science & Technology Research Laboratories	6.2
NXP Semiconductors	15.7, 20.1
Oculox Technology	21.7
OMRON	20.8
Oracle	4.2, 4.3
Oregon State University	22.4, 22.6
Osaka University	16.4
Panasonic	19.7
Pennsylvania State University	12.7
Photonics Electronics Technology Research Association	22.2
Pohang University of Science and Technology	5.7, 9.5
Princeton University	16.2, 18.4
PsiKick	5.4
Putra University	11.2
Qualcomm	8.5, 12.2, 26.3
Realtek Semiconductor	12.6
Renesas Electronics	7.3, 13.2, 13.4
Renesas System Design	13.4
Robert Bosch	27.1, 27.3
RWTH Aachen University	2.6, 12.4

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Samsung Advanced Institute of Technology	6.3, 13.1
Samsung Electronics	2.7, 5.7, 6.8, 7.2, 7.4, 7.6, 9.5, 10.4, 12.1, 12.9, 14.4, 14.8, 15.5, 17.7, 23.1, 26.1, 26.4, 26.7
Sandisk	7.1
Semiconductor Energy Laboratory	6.5, 16.9
Seoul National University	16.6
Sharif University of Technology	25.8
SHARP	6.6
Shizuoka University	6.4, 11.2
Singapore University of Technology and Design	2.3, 2.5
Sony	6.1
Sony LSI Design	6.1
Sony Semiconductor	6.1
Stanford University	15.7
STMicroelectronics	2.10, 5.5, 8.4, 11.5, 13.5, 22.9, 25.5
Sungkyunkwan University	7.4, 10.4
Synopsys	20.4, 26.5
Teledyne DALSA Semiconductors	15.3
Texas A&M University	3.6, 20.7, 22.4, 22.6
Texas Instruments	5.9, 8.3, 15.8, 16.7, 27.9
The Graduate School for the Creation of New Photonics Industries	6.4
Tokyo Institute of Technology	13.8, 14.1, 19.5, 25.2
Toshiba	2.8, 7.5, 18.2
Toshiba Semiconductor and Storage Products	7.1
Tsinghua University	25.6
TSMC	14.5, 14.9, 17.2
Tyndall National Institute	22.5
U-blox	12.9
Universite Catholique de Louvain	8.4
University of Applied Sciences of Southern Switzerland	21.7
University of Bologna	3.8
University of Bordeaux	2.10

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University of California	2.1, 6.7, 11.8, 13.5, 14.9, 18.5, 25.1, 25.7
University of Delaware	22.6
University of Edinburgh	11.5
University of Freiburg - IMTEK	20.6
University of Illinois	3.7, 3.8, 10.7, 12.2
University of Lille	13.5
University of Macau	2.4, 20.4, 20.5, 26.5
University of Michigan	8.2, 8.4, 12.3, 14.2, 18.7, 21.3, 26.1, 27.6
University of Pavia	22.9
University of Southern California	2.9, 19.3
University of Stuttgart	16.1
University of Texas	16.7
University of Tokyo	6.5, 16.4, 16.9
University of Toronto	13.6
University of Twente	5.5, 15.3, 19.2
University of Virginia	21.3
University of Washington	25.9, 27.4
Vrije Universiteit Brussel	9.3, 19.7
Xilinx	3.3
Yonsei University	19.6

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