IEEE SOLID-STATE CIRCUITS SOCIETY

ADVANCE PROGRAM

2013 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE

FEBRUARY 17, 18, 19, 20, 21

CONFERENCE THEME:

60 YEARS OF (EM)POWERING THE FUTURE

SAN FRANCISCO
MARRIOTT MARQUIS HOTEL

NEW THIS YEAR:
60TH ANNIVERSARY DISTINGUISHED EVENING PANEL

5-DAY PROGRAM

SUNDAY ALL-DAY
2 FORUMS ON Advanced RF Transceiver Design, VLSI Power-Management Techniques
10 TUTORIALS ON 60GHz CMOS LNA Design, High-Bandwidth Memory Interfaces, Energy Harvesting & Processing, FinFET Circuits, Data-Converter-Design Simulation, On-Chip Voltage & Timing Diagnostics, Robust SoC Design, Wireless Transceiver System Design, Voltage-Reference Design, Data & Power Implant Telemetry
2 EVENING EVENTS ON Graduate Student Research in Progress, Batteries Not Included

THURSDAY ALL-DAY
4 FORUMS ON Emerging Technology for Wireline, Scientific Imaging, Frequency Generation & Clock Distribution, Mixed-Signal/RF Design in Future CMOS
A SHORT-COURSE ON RF Blocks for Wireless Tx/Rx

ISSCC VISION STATEMENT

The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and application to maintain technical currency, and to network with leading experts.

CONFERENCE TECHNICAL HIGHLIGHTS

On **Sunday, February 17th**, the day before the official opening of the Conference, ISSCC 2013 offers:

- A choice of up to 4 of a total of 10 Tutorials
- A choice of 1 of 2 Advanced-Circuit-Design Forums

The 90-minute tutorials offer background information and a review of the basics in specific circuit-design topics. In the all-day Advanced-Circuit-Design Forums, leading experts present state-of-the-art design strategies in a workshop-like format. The Forums are targeted at designers experienced in the technical field.

On Sunday evening, there are two events: A Special-Topic Session entitled, **"Batteries Not Included - How Little is Enough for Real Energy Autonomy?"** will be offered starting at 8:00pm. In addition, the **Student Research Preview**, featuring short presentations followed by a poster session from selected graduate-student researchers from around the world will begin at 7:30 pm. Introductory remarks at the Preview will be provided by Nicky Lu, a distinguished innovator, entrepreneur, chief executive, researcher, and design architect.

On **Monday, February 18th**, ISSCC 2013 offers four plenary papers on the theme: **"60 Years of (Em)Powering the Future"**. On Monday at 12:15 pm, there will be a Women's Networking Event, a luncheon. On Monday afternoon, there will be five parallel technical sessions, followed by a Social Hour open to all ISSCC attendees. The Social Hour, held in conjunction with the Book Display, will also include a Demonstration Session (DS1), featuring posters and live demonstrations for selected papers from industry and academia. Monday evening will feature 6 distinguished researchers in a 60th Anniversary Panel entitled **"Antiques from the Innovations Attic"**.

On **Tuesday, February 19th**, there are five parallel technical sessions, both morning and afternoon. A Social Hour open to all ISSCC attendees will follow. The Social Hour, held in conjunction with the Book Display, will include the second Demonstration Session (DS2), featuring posters and live demonstrations for selected papers from industry and academia. Tuesday evening sessions include two evening panels on **"You're Hired - The Top 25 Interview Questions for Circuit Designers"**, and **"SoCs Empowering 2020 Killer Applications"**, as well as one Special-Topic Session on **"High-Speed Communications on 4 Wheels - What's in Your Next Car?"**.

On Wednesday, February 20th, there will be five parallel technical sessions, both morning and afternoon.

On **Thursday, February 21st**, ISSCC offers a choice of five events:

- A Short Course on **"RF Blocks for Wireless Transceivers"**
- Four Advanced-Circuit-Design Forums on
  wireline communications; scientific imaging;
  frequency generation and distribution;
  and mixed-signal/RF design/modeling in evolving CMOS.

Registration for educational events will be filled on a first-come, first-served basis. Use of the ISSCC Web-Registration Site (http://www.isscc.org) is strongly encouraged. Registrants will be provided with immediate confirmation on registration for the Conference, Tutorials, Advanced-Circuit-Design Forums, and the Short Course.

Need Additional Information?
Go to: www.isscc.org

TABLE OF CONTENTS

T1: Basics of 60GHz LNA and PA Design in CMOS

This tutorial will focus on 60GHz CMOS front-end building blocks (low-noise amplifiers and power amplifiers). System specifications will be derived from high-data-rate wireless communication links, and the design of these blocks will be explained step-by-step. Fundamental metrics for noise, linearity, and impedance matching will be addressed. As mm-wave operating frequencies are relatively close to the cutoff frequency of the active devices, little design freedom is left. This inevitably limits the complexity of mm-wave circuits. Further, layout issues of these circuits are discussed, as at mm-wave frequencies the sensitivity to layout parasitics is higher compared to radio front-end circuits in the low-GHz frequency region. This requires very careful electromagnetic modeling, as several interconnects need to be modeled as on-chip integrated transmission lines.

Instructor: Piet Wambacq

Piet Wambacq received the M.Sc. and the Ph.D. degree in Electrical Engineering from the Catholic University of Leuven, Belgium, in 1986 and 1996, respectively. Since 1996, he has been with imec, Belgium, where he is a Principle Scientist in analog, RF and mm-wave IC design using advanced CMOS technologies. Currently his focus is on mm-wave transceiver design. He is also Professor at the Vrije Universiteit Brussel. He has published two books and more than 200 peer-reviewed journal and conference papers.

T2: High-Bandwidth Memory Interface Design

Memory bandwidth has been increased significantly. There are many technical issues to enhance the memory interface such as TSV interface, high-speed serial interface including equalization, ODT, pre-emphasis, wide I/O interface including crosstalk, skew cancellation, and clock generation and distribution. This tutorial provides overviews of recent advances in memory interface design both in architecture and circuit levels. Subtopics will include signal integrity and testing. The future trends for further bandwidth enhancement will be covered as well.

Instructor: Chulwoo Kim

Chulwoo Kim received the B.S. and M.S. degrees in electronics engineering from the Korea University in 1994 and 1996, respectively, and the Ph.D. degree in electrical and computer engineering from the University of Illinois at Urbana-Champaign in 2001. In May 2001, he joined IBM Microelectronics Division, Austin, TX, where he was involved in Cell processor design. Since September 2002, he has been with the Department of Electrical Engineering, Korea University, where he is currently a Professor. In 2008-2009, he was a Visiting Scholar at the University of California, Los Angeles. His current research interests are in the areas of wireline transceiver, memory, power management and data converters. He is currently on the editorial board of the IEEE Transactions on VLSI Systems.

T3: Energy Harvesters and Energy Processing Circuits

The area of energy harvesting has seen significant interest in academic circles over the past decade. With the recent introduction of commercial ICs geared for energy harvesting applications by multiple semiconductor companies, this area is poised to take the next step to commercial adoption. However, challenges remain in the widespread adoption of energy harvesting solutions primarily owing to the limitations in average power output. A sound understanding of the energy flow within the harvesting system (from energy extraction to energy delivery) is crucial in overcoming these challenges.

In this tutorial, we will talk about the basics of commonly used energy harvesters and how their characteristics differ from conventional energy sources. Specialized circuits used to optimize energy extraction from different harvesters will be reviewed. The second part of the tutorial will talk about energy processing circuits like chargers, DC-DC converters and protection circuits for energy storage elements. Theoretical considerations in designing these circuits will be discussed and examples of practical implementations from commercial ICs will be presented.

Instructor: Yogesh Ramadass

Yogesh Ramadass received his B.Tech. degree from the Indian Institute of Technology, Kharagpur in 2004 and the S.M. and Ph.D. degrees in Electrical Engineering from MIT in 2006 and 2009. He is currently working as a lead design engineer at Texas Instruments where he is focused on architecting and designing power converters and mixed-signal circuits for energy harvesting, wireline

and wireless charging applications. Dr. Ramadass was awarded the President of India Gold Medal in 2004. He was a co-recipient of the Jack Kilby best student paper award at ISSCC 2009 and the Beatrice Winner award for editorial excellence at ISSCC 2007. He serves on the Technical Program Committee for ISSCC and ISLPED. He served as the chair of the 'Analog, MEMS, Mixed Signal and Imaging Electronics' committee at ISLPED 2012.

T4: Circuit Design using FinFETs

After HKMG, FinFETs are a powerful yet disruptive technology to enable continuous scaling following Moore's law. The disruptive nature arises from both the 3D structure and the quantization on width choice. FinFETs require new design skills to trade-off among PPA (power-performance-area) and to conduct circuit-process co-optimization. Salient advantages of FinFETs include: increased driving capability per footprint area, better control on short-channel effect, subthreshold slope, and less requirement on channel doping. Thus, threshold voltage can be reduced, which enables a reduction in supply voltage and thus power consumption or increase of performance speed.

The tutorial will focus on critical issues of FinFET design: It starts with a crisp comparison of planar vs. 3D FinFET devices and the associated SPICE modeling. Next, logic design is presented, including effects on standard cells, I/O circuitry, and ESD. Then, the subjects of SRAM and analog/mixed-signal design are treated in detail. Digital chip-level design that requires methodology enhancement and new CAD tool features are carefully discussed. The tutorial will enable CMOS designers to systematically comprehend circuit design using FinFETs.

Instructor: Bing Sheu

Bing Sheu obtained a BSEE from National Taiwan University, and Ph.D. degree from UC Berkeley. He taught at USC during 1985 – 1998, and was promoted to Full Professor in 1997. He moved to industry in 1999 and joined TSMC in 2006 as Director at R&D Design and Technology Platform. He was the original Creator of the BSIM (Berkeley Short-channel IGFET Model). He served as Editor-in-Chief of IEEE Transactions on VLSI Systems (1997 & 98), Founding Editor-in-Chief of IEEE Transactions on Multimedia (1998 & 99), and President of IEEE Circuits and Systems Society (2000). He is an IEEE Fellow, a recipient of IEEE Guillemin-Cauer Award in 1997, and IEEE CAS Society Meritorious Service Award in 2004. He currently serves on the Program Committees of ISSCC and VLSI Circuits Symposium.

T5: Simulation Techniques for Data Converter Design

ADC and DAC designers spend much time running long simulations that verify functionality and performance of their designs. Some converter designs contain many nominally identical cells (e.g. flash ADCs and current steering DACs). In some others the ratio of the sampling and signal frequencies is very high (oversampling ADCs). This tutorial, targeted at non-experts, will showcase some simulation techniques that are used in ADC/DAC designs. A brief overview of various architectures and examples involving behavioural and SPICE-like simulators will be given.

Instructor: Shanthi Pavan

Shanthi Pavan obtained the B.Tech. degree in Electronics and Communication Engineering from the Indian Institute of Technology, Madras in 1995 and the D.Sc. from Columbia University, New York in 1999. He is now a Professor of Electrical Engineering at the Indian Institute of Technology, Madras. His research interests are in the areas of high-speed analog circuit design and signal processing.

Dr. Pavan is the recipient of the IEEE Circuits and Systems Society Darlington Best Paper Award (2009), the Swarnajayanthi Fellowship (2010, from the Government of India), the Young Faculty Recognition Award from IIT Madras (2009, for excellence in teaching), the Technomentor Award from the India Semiconductor Association (2010) and the Young Engineer Award from the Indian National Academy of Engineering (2006). He is the Deputy Editor-in-Chief of the IEEE Transactions on Circuits and Systems: Part I - Regular Papers, and serves on the Data Converter Committee of the ISSCC.

T6: On-Chip Voltage and Timing Diagnostic Circuits

This tutorial introduces a set of practical and powerful techniques and circuits to observe and characterize on-die circuitry. Measuring voltage and timing information on the chip itself alleviates the bandwidth and noise limitations associated with bringing signals off-chip to be measured. Specific applications of these techniques include measurement and characterization of power supply noise, power delivery impedance, clock skew, phase interpolator linearity, I/O eye margins, waveform capture, RX voltage noise and hysteresis, and RX clock-data jitter. Because the measurements are fully integrated, the rest of the system can be automatically adapted based on these metrics in a stand-alone manner. Best of all, many of these techniques leverage existing circuitry and are highly digital.

Instructor: Frank O'Mahony

Frank O'Mahony leads the I/O Circuit Technology group within Advanced Design at Intel in Hillsboro, Oregon. He develops the first wireline I/O circuits for each new CMOS process technology. From 2003 until 2011 he was a member of the Signaling Research group in Intel's Circuit Research Lab. His research interests at Intel include high-speed and low-power data links, clock generation and distribution, and on-die measurement techniques. Frank received the B.S., M.S., and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 1997, 2000, and 2004, respectively. He received the 2003 Jack Kilby Award for Outstanding Student Paper at ISSCC for his work on standing-wave oscillators. Frank is a member of the ISSCC Wireline Subcommittee and an Associate Editor for TCAS-I.

T7: SoC Design Methodology for Improved Robustness

A holistic approach to power and performance attainment for semi-custom SoC designs is required to properly optimize future generation devices. We will cover novel techniques which tie SoC development together from micro-architecture to design signoff using examples from production SoCs. We discuss SoC clocking structures, local vs. distributed dividers, real-world implementation of clock-gating and data-driven clock power reduction. This is tied to design signoff, specifically, margin and signoff corner requirements including use of statistical STA. We will discuss how to select process corners and the type of outlier circuits which must be comprehended. Other novel areas of SoC optimization are considered including repeater insertion and repeater circuits for low power, auto-extraction and use of regularity in place and route, and SRAM power optimization.

Instructor: Anthony M. Hill

Anthony Hill is a Distinguished Member of Technical Staff for Texas Instruments, Dallas, TX. He leads the technology, physical implementation, and signoff team for TI's Multi-Core Systems Business Unit. He has been involved in the execution of 6 generations of complex SOCs and cores from 180nm to 28nm focused on communications infrastructure and high-performance embedded computing centered around TI's C6X DSP family. He joined TI in 1996 after taking his BSEE from Oklahoma State University in 1992, and MSEE and PhD from the University of Illinois Urbana-Champaign in 1993 and 1996. He is currently serving on the ISSCC High-Performance Digital subcommittee.

T8: Wireless Transceiver System Design for Modern Communication Standards

Defining the architecture and deriving specifications for modern wireless communication radio transceivers is a cross-domain task that requires understanding of digital communications, signal processing, radio architectures, analog/RF circuit design, discrete PCB system design, IC process and real-world product experience. This tutorial introduces the basic terminology used, such as NF, IIP2, IIP3, and provides an overview of the architecture selection and specification derivation procedure using state-of-the-art examples such as 3G/LTE cellular, 802.11ad and others. Starting from regulatory and communication standard document requirements such as sensitivity, blocking, spectral mask, EVM, etc., and taking into account different transceiver topologies, detailed transceiver specifications such as gain NF, IIP2, IIP3, cross-modulation, phase noise, filtering profile, I/Q mismatch, ADC resolution are derived and mapped onto circuit blocks. This is done by using both analytical calculations and simulation results, while the various transceiver performance degradation mechanisms are explained.

Instructor: Iason Vassiliou

Iason Vassiliou received his Diploma in Electrical Engineering from the National Technical University of Athens in 1991 and his M.Sc. and Ph.D. in Electrical Engineering from the University of California

at Berkeley in 1995 and 1999, respectively. Currently he is an Associate Technical Director at Broadcom, Greece. His main responsibility is radio system design and has worked on transceivers for WLAN, 60GHz, digital TV and LTE. Mr. Vassiliou holds 10 issued US patents and has authored several conference and journal papers, contributed 2 book chapters on wireless transceivers and analog CAD and has taught as a guest lecturer at professional seminars.

T9: Design of Voltage References

Voltage references are indispensable components in IC design. Their applications range from simple biasing to providing adequate accuracy for ADCs, DACs, VFCs, and other building blocks. In this tutorial, bandgap reference (BGR) fundamentals and the design of CMOS BGRs will be covered. Topics include classic BGRs, op-amp based and non-op-amp based BGRs; BGRs with and without output buffers; stability issues arose from negative and positive feedback; loop-gain function and power-supply rejection; startup issues, trimming and design of resistor strings. Advanced topics include curvature compensation, sub-1V references, micropower references, and alternatives to bandgap references such as fully CMOS references and resistor-less references.

Instructor: Wing-Hung Ki

Wing-Hung Ki received his B.Sc. from UCSD (1984), M.Sc. from Caltech (1985), and Ph.D. from UCLA (1995), all in electrical engineering. From 1992 to 1995, he worked for Micro Linear, San Jose, on the design of power converter controllers. He joined the Hong Kong University of Science and Technology (HKUST) in 1995, and is currently a professor of the Department of Electronic and Computer Engineering. His research interests are IC techniques for power management circuits, power transponders for RFID and energy harvesting applications, and fundamental research in switching converters and charge pumps.

T10: Data and Power Telemetry for Implants

Power and data telemetry are mandatory components for all implantable systems. Especially multichannel recorders and stimulators require both large power and high data rates. Nonetheless, in many systems the telemetry is just implemented with a holistic approach, but not analyzed in large detail. Based on the fact that most implantable devices dissipate the largest amount of power in the telemetry subsystem, a careful design or even active adaptability of the link are thought necessary in order to provide high energy-efficiency as well as to meet with regulatory compliance. Still today, most systems use RF data telemetry and suffer from large power consumption. Power delivery is mostly done without feedback control, or batteries are employed. On the emerging side, power efficient data transfer using UWB or non-RF telemetry, such as optical or ultrasonic approaches have shown to be excellent alternatives. Feedback controlled power telemetry or energy harvesting systems have shown high efficiency. This tutorial will give an overview and design guidelines for high-efficiency data and power telemetry for implantable systems. It first reviews the common RF based approaches, and secondly highlights new approaches such as energy harvesting and non-RF communication.

Instructor: Maurits Ortmanns

Maurits Ortmanns received the Dipl.-Ing. in Electrical Engineering from Saarland University, Germany and the Dr.-Ing. from IMTEK, University of Freiburg, Germany in 1999, and 2004, respectively. From 2004-2005 he was with sciworx GmbH, Hannover, Germany as a project leader in mixed-signal electronics. From 2006-2007 he was Assistant Professor for Integrated Interface Circuits at the University of Freiburg, Germany, and since 2008 he is full Professor and Director of the Institute of Microelectronics at the University of Ulm, Ulm, Germany. His research interests include mixed-signal integrated circuit design, self-correcting and reconfigurable analog circuits, with special emphasis on data converters and biomedical applications. He served as program committee member of ESSCIRC, DATE, ECCTD, ICECS, as Associate Editor of IEEE TCAS I, and is currently a program committee member of ISSCC. He holds several patents, is coauthor of the book “Continuous-Time Sigma-Delta A/D Conversion”, and published more than 120 IEEE journal and conference papers.

F1: Advanced RF Transceiver Design Techniques

Organizer: **Albert Jerng,** Mediatek, *Hsinchu, Taiwan*
Co-Organizer: **Yorgos Palaskas,** *Intel, Hillsboro, OR*

Committee: **Eric Klumperink,** *University of Twente, Enschede, Netherlands*
Didier Belot, *STMicroelectronics, Crolles, France*
Songcheol Hong, *KAIST, Daejeon, Korea*
Brian Floyd, *North Carolina State University, Raleigh, NC*

Radio-frequency performance is limited by fundamental constraints in dynamic range, as CMOS scaling continues to push supply voltages lower. The receiver needs to reject large in-band and out-of-band blockers while detecting small desired signals. The transmitter needs to maintain high efficiency and low distortion, while processing signals with wider bandwidths and higher peak-to-average ratios to support high data rates. Recent developments in RF transceiver design utilize techniques that cancel noise and distortion in receiver and transmitter signal paths. Digital circuits and calibration are increasingly being used to aid radio performance and allow area reduction. This Forum will present advanced circuit design techniques that demonstrate the current state-of-the-art. System specifications will be discussed to provide context for the required circuit enhancements. The first three talks will focus on noise and distortion cancellation techniques used in receivers. The next three talks will focus on transmitter design including both digital and analog linearization techniques. Finally, the last talk will introduce in-device co-existence issues and solutions for wireless systems that require multiple radios operating concurrently. This Forum is aimed at circuit designers and engineers active in radio-transceiver and wireless-system design.

Agenda

Time	Topic
08:00	Breakfast
08:20	**Introduction** **Albert Jerng,** *Mediatek, Hsinchu,Taiwan*
08:30	**Flexible and Linear RX Architectures** **Tajinder Manku,** *Consultant, Waterloo, Canada*
09:20	**Noise- and Distortion Cancellation for RX Front-Ends** **Asad Abidi,** *University of California, Los Angeles, CA*
10:10	Break
10:30	**Interference Cancellation Using Frequency Translated Filtering** **Ahmad Mirzaei,** *Broadcom, Irvine, CA*
11:20	**Transmitter Linearization Using Digital Pre-Distortion** **Peter Asbeck,** *University of California, San Diego, CA*
12:15	Lunch
13:30	**Digital Transmitters for Wireless Applications** **Chih-Ming Hung,** *MStar, Hsinchu, Taiwan*
14:20	**PA Linearization and Efficiency Enhancement** **Patrick Reynaert,** *KU Leuven, Leuven, Belgium*
15:10	Break
15:40	**In-Device Multi-Standard Co-Existence** **Leif Willhelmsson,** *Ericsson, Lund, Sweden*
16:30	Closing Remarks

F2: VLSI Power-Management Techniques: Principles and Applications

Organizer/Chair: **Leland Chang,** *IBM, Yorktown Heights, NY*
Co-Chair: **Shannon Morton,** *NVIDIA, Bristol, United Kingdom*

Committee:
Ken Chang, *Xilinx, San Jose, CA*
Leland Chang, *IBM, Yorktown Heights, NY*
Jin-Man Han, *Samsung, Hwasung, Korea*
Piero Malcovati, *University of Pavia, Pavia, Italy*
Shannon Morton, *NVIDIA, Bristol, United Kingdom*
Vladimir Stojanovic, *MIT, Cambridge, MA*

Across the spectrum of microelectronics applications, power management is critical to enabling of power-efficient products. This Forum will provide practicing circuit designers with a summary of power-management techniques, including perspectives from a wide range of product applications, and an outlook for the future in the context of coming challenges. The first four speakers in this Forum will present the general principles in development today, including power-gating and state-retention modes, PLL/DLL techniques for dynamic frequency scaling, integrated voltage regulators for dynamic voltage scaling, and low-power signaling. In the second half, four speakers representing different industry perspectives, including microprocessors, consumer electronics, microcontrollers and mobile, and DRAM, will utilize practical case studies to detail current usage of power-management techniques and speculate on future trends.

Agenda

Time	Topic
08:00	Breakfast
08:20	**Introduction** **Leland Chang,** *IBM, Yorktown Heights, NY*
08:30	**Advanced Power-Gating and State-Retention Approaches to Leakage-Power Reduction** **David Flynn,** *ARM, Cambridge, United Kingdom*
09:20	**Clocking Techniques for Dynamic Frequency Scaling** **Jaeha Kim,** *Seoul National University, Seoul, Korea*
10:10	Break
10:35	**Dynamic Voltage Scaling Using On-Chip Voltage Regulation** **Gu-Yeon Wei,** *Harvard University, Cambridge, MA*
11:25	**Power Management in High-Performance I/O** **Jared Zerbe,** *Rambus, Sunnyvale, CA*
12:15	Lunch
13:20	**Fine-Grain Power Management in Microprocessors** **Vivek De,** *Intel, Hillsboro, OR*
14:10	**A Key to Power Management for Digital Consumer Applications** **Yukihiro Urakawa,** *Toshiba, Kawasaki, Japan*
15:00	Break
15:20	**Embedded Power-Management Solutions for Ultra-Low-Power SoCs: Implementation Examples of Radio-Connected Microcontrollers and Mobile-Application Microprocessors** **Frédéric Hasbani,** *ST Microelectronics, Crolles, France*
16:10	**Power-Management Techniques in DRAM Design** **Sangho Shin,** *Samsung, Hwasung, Korea*
17:00	Closing remarks

ES1: STUDENT RESEARCH PREVIEW (SRP)

The Student Research Preview (SRP) will highlight selected student research projects in progress. The SRP consists of 23 one-minute presentations followed by a Poster Session, by graduate students from around the world, which have been selected on the basis of a short submission concerning their on-going research. Selection is based on the technical quality and innovation of the work. This year, the SRP will be presented in three sessions: Data Converters and Analog Circuit Techniques; Circuits and Systems for Bio-medical Applications; Memory, Digital, MEMS, and PLL IPs.

The Student Research Preview will begin with a brief talk by the distinguished circuit designer and entrepreneur, Dr. Nicky Lu, Etron Technologies. His talk on "Research with Innovation is Power for Promising Career Growth" is scheduled for Sunday, February 17th, starting at 7:30pm, and is open to all ISSCC registrants.

Chair:	**Jan Van der Spiegel**	University of Pennsylvania, USA
Co-Chair:	**SeongHwan Cho**	KAIST, Korea
Co-Chair:	**Eugenio Cantatore**	Eindhoven University of Technology, The Netherlands
Secretary:	**Tsung-Hsien Lin**	National Taiwan University, Taiwan
Advisor:	**Kenneth C. Smith**	University of Toronto, Canada
Media/Publications:	**Laura Fujino**	University of Toronto, Canada
A/V:	**John Trnka**	Rochester, MN

Committee Members

Bryan Ackland	Stevens Institute of Technology, USA
Bharadwaj Amrutur	India Institute of Science, India
Andrea Baschirotto	University of Milan-Bicocca, Italy
Bevan Baas	University of California, Davis, USA
Jean-Baptiste Begueret	IMS Labs, France
William Bowhill	Intel, USA
Eugenio Cantatore	Eindhoven University of Technology, The Netherlands
Brian Lum Shue Chan	Texas Instruments, USA
SeongHwan Cho	KAIST, Korea
Denis Daly	Cambridge Analog Technologies, USA
Andreas Demosthenous	University College London, UK
Vasantha Erraguntla	Intel, India
Vincent Gaudet	University of Waterloo, Canada
Makoto Ikeda	University of Tokyo, Japan
Takayuki Kawahara	Hitachi, Japan
Jaeha Kim	Seoul National University, Korea
Tsung-Hsien Lin	National Taiwan University, Taiwan
Shen-Iuan Liu	National Taiwan University, Taiwan
Dejan Markovic'	University of California, Los Angeles, USA
Akira Matsuzawa	Tokyo Institute of Technology, Japan
Shahriar Mirabbasi	University of British Columbia, Canada
Sameer Sonkusale	Tufts University, USA
Jan Van der Spiegel	University of Pennsylvania, USA
Marian Verhelst	Kath. University of Leuven, Belgium
Zhihua Wang	Tsinghua University, P.R. China
Jeff Weldon	Carnegie Mellon University, USA

ES2: "Batteries Not Included." – How Little is Enough for Real Energy Autonomy?

Organizer: **Minkyu Je,** *Institute of Microelectronics, A*STAR, Singapore*
Axel Thomsen, *Silicon Laboratories, Austin, TX*

Chair: **Axel Thomsen,** *Silicon Laboratories, Austin, TX*
Minkyu Je, *Institute of Microelectronics, A*STAR, Singapore*

Much has been said about energy scavenging and much has also been said about low power circuitry**. It's a bit analogous to Woody Allen's movie Annie Hall *. But the goal of energy autonomy depends on both sides of the equation. The aim of this evening session is to present the theoretical and practical issues from both sides, add in some system-level techniques, and then follow up with debate on the issues relating to getting realistic energy autonomy. How much do you have to generate? How much are you allowed to consume? Can anyone agree?

(* For younger and/or more naive readers, the numerical value of 3 times a week was considered either "hardly ever" or "constantly" depending on one's point of view.)
** A wide gap exists between the amount of energy that the current technology can harvest, and the energy needed to operate state-of-the-art low-power circuits

Time	Topic
8:00	**Energy Harvesting: Fundamental Limits and Real-World Implementation** **Sywert Brongersma,** *Holst Centre/imec, Eindhoven, Netherlands*
8:30	**An Energy-Centric Design Approach to Achieve Nanowatt Microsystems** **Dennis Sylvester,** *University of Michigan, Ann Arbor, MI*
9:00	**Ultra-Low-Power Analog Design: Towards True Energy Autonomy** **Jerald Yoo,** *Masdar Institute of Science and Technology, Abu Dhabi, UAE*
9:30	**Duty Cycling of Analog and Mixed-Signal Circuits: A Straightforward Solution for Significant Power Consumption Reduction?** **Christian Enz,** *CSEM and EPFL, Neuchâtel, Switzerland*

Plenary Session — Invited Papers

Chair: **Anantha Chandrakasan,** *Massachusetts Institute of Technology, Cambridge, MA*
ISSCC Conference Chair

Associate Chair:
Bram Nauta, *University of Twente, Enschede, The Netherlands*
ISSCC Program Committee Chair

FORMAL OPENING OF THE CONFERENCE **8:30AM**

1.1 "Architecting the Future through Heterogeneous Computing" 8:45AM

Lisa Su, *Senior Vice President and General Manager, Global Business Units, AMD, Austin, TX, USA*

Heterogeneous computing is changing the way system designers, software developers, and end users, are creating and experiencing the future of technology. The most-compelling emerging algorithms are parallel in nature rather than serial CPU-centric. Virtually every computing device – whether smartphone, tablet, or PC – is transitioning to a new world: with smaller, lighter, and cooler form factors; with more media and less text; with higher DPI screens and high-definition video; and with a transformation from traditional user interfaces to more-natural ones, involving touch and gesture recognition.

This metamorphosis opens up tremendous opportunity for computing to impact today's norms,.where most parallel code still runs on CPUsthat are optimizedfor scalar workloads. Such mismatches are highly inefficient and wastes a tremendous amount of power. Similarly, video and multimedia content is best handled by parallel processing, and GPUs are much more efficient at running those workloads. In general, the key to efficient affordable optimized computing is running the right workload on the right processor at the right time. This talk addresses the industry's efforts to accelerate the adoption of heterogeneous computing, and expands upon the benefits that the end users can expect from these advances in our every day lives.

1.2 "Smart Life Solutions" from Home to City 9:20AM

Yoshiyuki Miyabe, *Managing Director and CTO, Panasonic, Osaka, Japan*

It has been predicted that the global demand for electricity will be twice the current level by 2035. In this event, even efficient use of resources can ensure only a limited energy supply. This energy bottleneck is one of the serious social issues in our future. Meanwhile, other inter-related developments proceed: electronic products are becoming increasingly sophisticated; users are aging; and, as a result, the demand for user-friendly interfaces is growing. To resolve these social issues, we are working to provide "Smart Life Solutions", which support both the eco-solution concept of intelligent energy saving, and the smart-solution concept of providing products and services optimized for individual lifestyles, by means of information and communication technology.

In the history of consumer electronics, evolving component technology has driven functional evolution: Television is a good example of this. We entered this arena in 1952, with a 17-inch black-and-white TV that contained 22 vacuum tubes. Subsequently, advances in components (transistors, ICs, microprocessors, and system LSIs), directly enabled the progress of TV sets to color, satellite, analog high definition, digital high definition, 3D, and Smart. The latest 3D and Smart TVs include system LSIs in 40-nm CMOS that contain 700 million transistors operating at 1 GHz. It is not an exaggeration to say that all growth in digital products has been driven by the progress in semiconductor technology.

In this talk, I will introduce examples of "Smart Life Solutions": Smart Homes to provide safe and comfortable living environments while saving energy; Smart Surveillance to provide safe and intelligent retail environments; Smart Mobility to provide more convenient transportation - automobiles with lower environmental impact; and Smart Cities to provide lifestyle values through comprehensive town planning .

To achieve these solutions, key developments include advanced sensing technology, communications technology (which has drastically reduced costs), and power-device technology (which contributes to energy saving). These developments are all supported by innovative semiconductor technology.

This talk will also introduce initiatives for applying semiconductor technology to new fields, with examples from our research and development activities such as artificial photosynthesis. As well, it will describe expectations for the evolution of semiconductor technology.

ISSCC, SSCS, IEEE AWARD PRESENTATIONS **9:55AM**

BREAK **10:25AM**

1.3 Continuing to Shrink: Next-Generation Lithography - Progress and Prospects **10:40AM**

Martin van den Brink, *Executive Vice President and Chief Product & Technology Officer, ASML, Veldhoven, The Netherlands*

Optical lithography has been the key manufacturing technology for integrated-circuit production, enabling a million-fold reduction in average transistor length over 50 years. The development of projection scanners, step and repeat tools, and now, step and scan systems at higher numerical apertures and shorter wavelengths have led to today's main lithographic production tool: the 193nm immersion scanner. With 20nm half-pitch fabrication, at half the effective resolution limit, it is necessary to use multiple patterning, either through pattern splitting and multiple exposures, or through a self-aligned spacer process. This leads to one of two consequences: on the one hand, to a significant increase in the number of mask levels, process cost, and manufacturing complexity; and, on the other hand, to significant layout restrictions which require closer collaboration between semiconductor design and manufacturing for optimal imaging results and high yield. Even so, for lithography systems to achieve these small resolutions, there are other requirements: a sharp increase in process overlay to achieve nanometer-specific positioning of the projected image on the silicon wafer); and Critical Dimension Uniformity (CDU) (to specify the nanometer consistency of the projected image). Computational lithography and high-speed diffraction-based metrology are needed to meet these challenges. To relax the complexity of the double-patterning process and layout restrictions, EUV lithography has been developed to support 1x-nm logic and memory fabrication, and has been demonstrated to meet imaging and overlay requirements. The major challenge remaining is productivity!

1.4 The Evolution of Technology **11:15AM**

Carver Mead, *Professor Emeritus, Caltech, Pasadena, CA, USA*

Faraday's Law of induction gave us generators, motors, telegraph, telephone, etc. The vacuum tube gave us long-distance telephone, radio, hi-fi audio, television, and early computers. Microcircuits have given us personal computers, cell phones, the Internet, and GPS positioning.

Now, What?

PRESENTATION TO PLENARY SPEAKERS **11:50AM**

CONCLUSION **11:55AM**

Ultra-High-Speed Transceivers and Equalizers

Session Chair: ***Ken Chang,*** *Xilinx, San Jose, CA*
Associate Chair: ***Hisakatsu Yamaguchi,*** *Fujitsu Laboratories, Kawasaki, Japan*

2.1 A 32Gb/s Wireline Receiver with a Low-Frequency Equalizer, CTLE and 2-Tap DFE in 28nm CMOS **1:30 PM**

S. Parikh[1], T. Kao[1], Y. Hidaka[1], J. Jiang[1], A. Toda[1], S. Mcleod[1], W. Walker[1], Y. Koyanagi[2], T. Shibuya[2], J. Yamada[3]
[1]Fujitsu Laboratories of America, Sunnyvale, CA; [2]Fujitsu Laboratories, Kawasaki, Japan
[3]Fujitsu, Kawasaki, Japan

2.2 A 66Gb/s 46mW 3-Tap Decision-Feedback Equalizer in 65nm CMOS **2:00 PM**

Y. Lu, E. Alon, University of California, Berkeley, CA

2.3 A Sub-2W 39.8-to-44.6Gb/s Transmitter and Receiver Chipset with SFI-5.2 Interface in 40nm CMOS **2:30 PM**

B. Raghavan, D. Cui, U. Singh, H. Maarefi, D. Pi, A. Vasani, Z. Huang, A. Momtaz, J. Cao
Broadcom, Irvine, CA

Break **3:00 PM**

2.4 A 195mW / 55mW Dual-Path Receiver AFE for Multistandard 8.5-to-11.5 Gb/s Serial Links in 40nm CMOS **3:15 PM**

B. Zhang, A. Nazemi, A. Garg, N. Kocaman, M. R. Ahmadi, M. Khanpour, H. Zhang, J. Cao, A. Momtaz
Broadcom, Irvine, CA

2.5 32Gb/s Data-Interpolator Receiver with 2-Tap DFE in 28nm CMOS **3:45 PM**

Y. Doi[1], T. Shibasaki[1], T. Danjo[1], W. Chaivipas[1], T. Hashida[1], H. Miyaoka[2], M. Hoshino[3], Y. Koyanagi[1], T. Yamamoto[4], S. Tsukamoto[1], H. Tamura[1]
[1]Fujitsu Laboratories, Kawasaki, Japan; [2]Fujitsu Semiconductor, Yokohama, Japan
[3]Fujitsu Microelectronics Solutions, Yokohama, Japan
[4]Fujitsu Laboratories of America, Sunnyvale, CA

2.6 A 32-to-48Gb/s Serializing Transmitter Using Multiphase Sampling in 65nm CMOS **4:15 PM**

A. A. Hafez, M-S. Chen, C-K. Yang, University of California, Los Angeles, CA

2.7 32Gb/s 28nm CMOS Time-Interleaved Transmitter Compatible with NRZ Receiver with DFE **4:45 PM**

Y. Ogata[1], Y. Hidaka[2], Y. Koyanagi[1], S. Akiya[3], Y. Terao[3], K. Suzuki[1], K. Kashiwa[4], M. Suzuki[4], H. Tamura[1]
[1]Fujitsu Laboratories, Kawasaki, Japan; [2]Fujitsu Laboratories of America, Sunnyvale, CA
[3]Fujitsu, Kawasaki, Japan; [4]Fujitsu Microelectronics Solutions, Akiruno, Japan

2.8 A 0.94mW/Gb/s 22Gb/s 2-Tap Partial-Response DFE Receiver in 40nm LP CMOS **5:00 PM**

K. Jung[1], A. Amirkhany[2], K. Kaviani[2]
[1]University of California, Berkeley, CA
[2]Rambus, Sunnyvale, CA

Conclusion **5:15 PM**

Processors

Session Chair: ***Se-Hyun Yang,*** *Samsung, Yongin, Korea*
Associate Chair: ***Eric Fluhr,*** *IBM, Round Rock, TX*

3.1 5.5GHz System z Microprocessor and Multichip Module — 1:30 PM

J. Warnock[1], Y. H. Chan[2], H. Harrer[3], D. Rude[2], R. Puri[4], S. Carey[2], G. Salem[5], G. Mayer[3], Y-H. Chan[2], M. Mayo[2], A. Jatkowski[2], G. Strevig[6], L. Sigal[4], A. Datta[7], A. Gattiker[8], A. Bansal[4], D. Malone[2], T. Strach[3], H. Wen[6], P-K. Mak[2], C-L. Shum[2], D. Plass[2], C. Webb[2]
[1]IBM Systems and Technology Group, Yorktown Heights, NY
[2]IBM Systems and Technology Group, Poughkeepsie, NY
[3]IBM Systems and Technology Group, Boeblingen, Germany
[4]IBM Research, Yorktown Heights, NY; [5]IBM Systems and Technology Group, Williston, VT
[6]IBM Systems and Technology Group, Austin, TX
[7]IBM Systems and Technology Group, Bangalore, India; [8]IBM Research, Austin, TX

DS1

3.2 A 3.6GHz 16-Core SPARC SoC Processor in 28nm — 2:00 PM

J. Hart, S. Butler, H. Cho, Y. Ge, G. Gruber, D. Huang, C. Hwang, D. Jian, T. Johnson, L. Kwong, R. Masleid, U. Nawathe, A. Ramachandran, Y. Sheng, J. Shin, S. Turullois, Z. Qin, K. Yen, Oracle, Santa Clara, CA

3.3 A 3.40ms/GF(p_{521}) and 2.77ms/GF(2^{521}) DF-ECC Processor with Side-Channel Attack Resistance — 2:30 PM

J-W. Lee, S-C. Chung, H-C. Chang, C-Y. Lee,
National Chiao Tung University, Hsinchu, Taiwan

Break — 3:00 PM

3.4 Jaguar: A Next-Generation Low-Power x86-64 Core — 3:15 PM

T. Singh, J. Bell, S. Southard, AMD, Austin, TX

3.5 Godson-3B1500: A 32nm 1.35GHz 40W 172.8GFLOPS 8-Core Processor — 3:45 PM

W. Hu[1,2], Y. Zhang[1,2], L. Yang[2], B. Fan[2], Y. Chen[1,2], S. Zhong[2], H. Wang[2], Z. Qi[1,2], P. Wang[1,2], X. Gao[2], X. Yang[2], B. Xiao[1,2], H. Wang[2], Z. Yang[1,2], L. Yang[1,2], S. Chen[1,2]
[1]Chinese Academy of Sciences, Beijing, China; [2]Loongson Technology, Beijing, China

3.6 A 65nm 39GOPS/W 24-Core Processor with 11Tb/s/W Packet-Controlled Circuit-Switched Double-Layer Network-on-Chip and Heterogeneous Execution Array — 4:15 PM

P. Ou, J. Zhang, H. Quan, Y. Li, M. He, Z. Yu, X. Yu, S. Cui, J. Feng, S. Zhu, J. Lin, M. Jing, X. Zeng, Z. Yu, Fudan University, Shanghai, China

3.7 Bandwidth and Power Management of Glueless 8-Socket SPARC T5 System — 4:30 PM

V. Krishnaswamy[1], D. Huang[2], S. Turullols[1], J. Shin[1]
[1]Oracle, Santa Clara, CA; [2]Oracle, San Diego, CA

3.8 A 10th Generation 16-Core SPARC64 Processor for Mission-Critical UNIX Server — 4:45 PM

R. Kan[1], T. Tanaka[1], G. Sugizaki[1], R. Nishiyama[1], S. Sakabayashi[1], Y. Koyanagi[2], R. Iwatsuki[1], K. Hayasaka[1], T. Uemura[3], G. Ito[1], Y. Ozeki[1], H. Adachi[1], K. Furuya[1], T. Motokurumada[1]
[1]Fujitsu, Kawasaki, Japan; [2]Fujitsu Laboratories, Kawasaki, Japan
[3]Fujitsu Semiconductor, Yokohama, Japan

Conclusion — 5:15 PM

Harvesting and Wireless Power

Session Chair: ***Jae-Youl Lee,*** *Samsung, Yongin, Korea*
Associate Chair: ***Saska Lindfors,*** *Texas Instruments, Helsinki, Finland*

4.1 A Resonant Regulating Rectifier (3R) Operating at 6.78 MHz for A 6W Wireless Charger with 86% Efficiency — **1:30 PM**

J-H. Choi[1], S-K. Yeo[2], C-B. Park[1], S. Park[2], J-S. Lee[2], G-H. Cho[1]
[1]KAIST, Daejeon, Korea; [2]Samsung Electronics, Suwon, Korea

4.2 A 13.56MHz Fully Integrated 1X/2X Active Rectifier with Compensated Bias Current for Inductively Powered Devices — **2:00 PM**

Y. Lu, X. Li, W-H. Ki, C-Y. Tsui, C. P. Yue,
HKUST, Hong Kong, China

4.3 A 400nW Single-Inductor Dual-Input-Tri-Output DC-DC Buck-Boost Converter with Maximum Power Point Tracking for Indoor Photovoltaic Energy Harvesting — **2:15 PM**

K. Chew, Z. Sun, H. Tang, L. Siek,
Nanyang Technological University, Singapore, Singapore

4.4 An Adaptive Load-Line Tuning IC for Photovoltaic Module Integrated Mobile Device with 470µs Transient Time, Over 99% Steady-State Accuracy and 94% Power Conversion Efficiency — **2:30 PM**

W-C. Liu, Y-H. Wang, T-H. Kuo,
National Cheng Kung University, Tainan, Taiwan

Break — **3:00 PM**

4.5 A 3.4mW Photovoltaic Energy-Harvesting Charger with Integrated Maximum Power Point Tracking and Battery Management — **3:15 PM**

T-H. Tsai, K. Chen,
National Chung Cheng University, Chia-Yi, Taiwan

4.6 A Self-Biased 5-to-60V Input Voltage and 25-to-1600µW Integrated DC-DC Buck Converter with Fully Analog MPPT Algorithm Reaching up to 88% End-to-End Efficiency — **3:45 PM**

S. Stanzione[1], C. van Liempd[1], R. van Schaijk[1], Y. Naito[2], R. F. Yazicioglu[3], C. van Hoof[1,4]
[1]imec - Holst Centre, Eindhoven, The Netherlands; [2]Panasonic, Osaka, Japan
[3]imec, Leuven, Belgium; [4]KU Leuven, Leuven, Belgium

4.7 A 1µW-to-1mW Energy-Aware Interface IC for Piezoelectric Harvesting with 40nA Quiescent Current and Zero-Bias Active Rectifiers — **4:15 PM**

C. van Liempd[1], S. Stanzione[1], Y. Allasasmeh[1], C. van Hoof[2,3]
[1]imec - Holst Centre, Eindhoven, The Netherlands
[2]imec, Heverlee, Belgium; [3]KU Leuven, Leuven, Belgium

4.8 A Single-Inductor 0.35µm CMOS Energy-Investing Piezoelectric Harvester — **4:45 PM**

D. Kwon, G. A. Rincon-Mora
Georgia Institute of Technology, Atlanta, GA

Conclusion — **5:15 PM**

RF Techniques

Session Chair: ***Mike Keaveney,*** *Analog Devices, Limerick, Ireland*
Associate Chair: ***Joseph Golat,*** *Motorola, Schaumburg, IL*

5.1 SAW-Less Analog Front-End Receivers for TDD and FDD **1:30 PM**

I. Fabiano[1], M. Sosio[1], A. Liscidini[1,2], R. Castello[1]
[1]University of Pavia, Pavia, Italy
[2]*Now at the University of Toronto, Toronto, ON, Canada

5.2 Simultaneous Spatial and Frequency-Domain Filtering at the Antenna Inputs Achieving up to +10dBm Out-of-Band/Beam P_{1dB} **2:00 PM**

A. Ghaffari, E. E. Klumperink, F. van Vliet, B. Nauta
University of Twente, Enschede, The Netherlands

5.3 A Phase-Noise and Spur Filtering Technique Using Reciprocal-Mixing Cancellation **2:30 PM**

M. Mikhemar, D. Murphy, A. Mirzaei, H. Darabi
Broadcom, Irvine, CA

Break **3:00 PM**

5.4 A 30.3dBm 1.9GHz-Bandwidth 2×4-Array Stacked 5.3GHz CMOS Power Amplifier **3:15 PM**

M. Fathi, D. K. Su, B. A. Wooley
Stanford University, Stanford, CA

5.5 A 1.8GHz Linear CMOS Power Amplifier with Supply-Path Switching Scheme for WCDMA/LTE Applications **3:45 PM**

K. Onizuka, S. Saigusa, S. Otaka
Toshiba, Kawasaki, Japan

5.6 A New TX Leakage-Suppression Technique for an RFID Receiver Using a Dead-Zone Amplifier **4:15 PM**

S-S. Lee[1], J. Lee[2], I-Y. Lee[1], S-G. Lee[1], J. Ko[2]
[1]KAIST, Daejeon, Korea
[2]PHYCHIPS, Daejeon, Korea

5.7 A 200mW 100MHz-to-4GHz 11th-Order Complex Analog Memory Polynomial Predistorter for Wireless Infrastructure RF Amplifiers **4:45 PM**

F. Roger
Scintera, Sunnyvale, CA

Conclusion **5:15 PM**

Emerging Medical and Sensor Technologies

Session Chair: ***David Ruffieux,*** *CSEM, Neuchatel, Switzerland*
Associate Chair: ***Yogesh Ramadass,*** *Texas Instruments, Dallas, TX*

6.1 An 87mA·min Iontophoresis Controller IC with Dual-Mode Impedance Sensor for Patch-Type Transdermal Drug Delivery System **1:30 PM**

K. Song, U. Ha, J. Lee, K. Bong, H-J. Yoo
KAIST, Daejeon, Korea

DS1

6.2 A 1.83µJ/Classification Nonlinear Support-Vector-Machine-Based Patient-Specific Seizure Classification SoC **2:00 PM**

M. Altaf, J. Tillak, Y. Kifle, J. Yoo
Masdar Institute of Science and Technology, Abu Dhabi, United Arab Emirates

6.3 Through-Silicon-Via-Based Double-Side Integrated Microsystem for Neural Sensing Applications **2:30 PM**

C-W. Chang[1], P-T. Huang[1], L-C. Chou[1], S-L. Wu[1], S-W. Lee[1], C-T. Chuang[1], K-N. Chen[1], J-C. Chiou[1,2], W. Hwang[1,3], Y-C. Lee[3], C-H. Wu[3], K-H. Chen[3], C-T. Chiu[3], H-M. Tong[3]
[1]National Chiao Tung University, Hsinchu, Taiwan
[2]China Medical University, Taichung, Taiwan
[3]Advanced Semiconductor Engineering Group, Kaohsiung, Taiwan

Break **3:00 PM**

6.4 1µm-Thickness 64-Channel Surface Electromyogram Measurement Sheet with 2V Organic Transistors for Prosthetic Hand Control **3:15 PM**

H. Fuketa[1,2], K. Yoshioka[1,2], Y. Shinozuka[1,2], K. Ishida[1,2], T. Yokota[1,2], N. Matsuhisa[1,2], Y. Inoue[1,2], M. Sekino[1,2], T. Sekitani[1,2], M. Takamiya[1,2], T. Someya[1,2], T. Sakurai[1,2]
[1]University of Tokyo, Tokyo, Japan; [2]JST/ERATO, Tokyo, Japan

6.5 A 4b ADC Manufactured in a Fully-Printed Organic Complementary Technology Including Resistors **3:45 PM**

S. Abdinia[1], M. Benwadih[2], R. Coppard[2], S. Jacob[2], G. Maiellaro[3], G. Palmisano[3], M. Rizzo[4], A. Scuderi[4], F. Tramontana[4], A. van Roermund[1], E. Cantatore[1]
[1]Eindhoven University of Technology, Eindhoven, The Netherlands
[2]CEA-LITEN, Grenoble, France; [3]University of Catania, Catania, Italy
[4]STMicroelectronics, Catania, Italy

6.6 An Organic VCO-Based ADC for Quasi-Static Signals Achieving 1LSB INL at 6b Resolution **4:00 PM**

D. Raiteri[1], P. van Lieshout[2], A. van Roermund[1], E. Cantatore[1]
[1]Eindhoven University of Technology, Eindhoven, The Netherlands
[2]Polymer Vision, Eindhoven, The Netherlands

6.7 A 1024×8 700ps Time-Gated SPAD Line Sensor for Laser Raman Spectroscopy and LIBS in Space and Rover-Based Planetary Exploration **4:15 PM**

Y. Maruyama[1], J. Blacksberg[2], E. Charbon[1]
[1]Delft University of Technology, Delft, The Netherlands
[2]Jet Propulsion Laboratory, Pasadena, CA

6.8 Experimental Demonstration of a Fully Digital Capacitive Sensor Interface Built Entirely Using Carbon-Nanotube FETs **4:45 PM**

M. Shulaker[1], J. van Rethy[2], G. Hills[1], H-Y. Chen[1], G. Gielen[2], H-S. Wong[1], S. Mitra[1]
[1]Stanford University, Stanford, CA; [2]KU Leuven, Heverlee, Belgium

DS1

Conclusion **5:15 PM**

DEMONSTRATION SESSION 1 (DS1)*MONDAY, FEBRUARY 18TH 4:00-7:00 PM

This year, the Demonstration Sessions of techniques presented in selected regular papers, both Academic and Industrial, will take place on two evenings: Monday, February 18 and Tuesday, February 19, from 4 pm until 7 pm in the Golden Gate Hall. These demonstrations will feature real-life applications made possible by new ICs presented at ISSCC 2013, as noted by the symbol, **DS1** in the Advance Program. Scheduling details will be provided at www.isscc.org shortly before the Conference. Meanwhile, a list of the selected papers is as follows:

Monday, February 18th

3.1	5.5GHz System z Microprocessor and Multichip Module	1:30 PM
6.1	An 87mA·min Iontophoresis Controller IC with Dual-Mode Impedance Sensor for Patch-Type Transdermal Drug Delivery System	1:30 PM
6.8	Experimental Demonstration of a Fully Digital Capacitive Sensor Interface Built Entirely Using Carbon-Nanotube FETs	4:45 PM

Tuesday, February 19th

7.6	A 1.23pJ/b 2.5Gb/s Monolithically Integrated Optical Carrier-Injection Ring Modulator and All-Digital Driver Circuit in Commercial 45nm SO	11:15 AM
8.7	A Low-Cost Miniature 120GHz SiP FMCW/CW Radar Sensor with Software Linearization	11:15 AM
9.3	A 0.48V 0.57nJ/Pixel Video-Recording SoC in 65nm CMOS	9:30 AM
9.5	A 249Mpixel/s HEVC Video-Decoder Chip for Quad Full HD Applications	10:15 AM
9.6	Reconfigurable Processor for Energy-Scalable Computational Photography	10:45 AM
9.8	A 646GOPS/W Multi-Classifier Many-Core Processor With Cortex-Like Architecture for Super-Resolution Recognition	11:45 AM
10.5	A 4Ω 2.3W Class-D Audio Amplifier with Embedded DC-DC Boost Converter, Current-Sensing ADC and DSP for Adaptive Speaker Protection	10:15 AM
11.3	A Versatile Timing Microsystem Based on Wafer-Level Packaged XTAL/BAW Resonators with Sub-µW RTC Mode and Programmable HF Clocks	9:30 AM
11.5	A 0.15mm-Thick Non-Contact Connector for MIPI Using Vertical Directional Coupler	10:45 AM
11.6	1.2Gb/s 3.9pJ/b Mono-Phase Pulse-Modulation Inductive-Coupling Transceiver for mm-Range Board-to-Board Communication	11:15 AM

**DS1 may include additional demonstrations of work reported at the Student Research Preview.*

EP1: Antiques from the Innovations Attic

Organizer: **Trudy Stetzler**, *Texas Instruments, Stafford,TX*

Moderators: **Anantha Chandrakasan**, *Massachusetts Institute of Technology, Cambridge, MA*
Bram Nauta, *University of Twente, Enschede, The Netherlands*

When you clean up your attic you may find things that you have totally forgotten about: old toys you used to play with, old books with lost stories. And then you think back to those past days and view them in the context of today's busy life. This panel does a similar thing; we have asked 6 experts from academia and industry to dig into their memories and find lost treasures in circuit design. This panel features surprises from the past sixty years (or more) and the panelists explain why the concept is significant today and should be pulled from the innovation attic.

Panelists:

Robert Brodersen, *University of California, Berkeley, CA*
Rinaldo Castello, *University of Pavia, Pavia, Italy*
Yoshiaki Daimon Hagihara, *Sojo University, Kumamoto, Japan*
Thomas Lee, *Microsystems Technology Office, DARPA, Arlington, VA*
Nicky Lu, *Etron Technology, Hsinchu, Taiwan*
Eric Vittoz, *Independent Consultant, Cernier, Switzerland*

Optical Transceivers and Silicon Photonics

Session Chair: ***Ichiro Fujimori,*** *Broadcom, Irvine, CA*
Associate Chair: ***Masafumi Nogawa,*** *NTT Microsystem Integration Laboratories, Atsugi, Japan*

7.1 A Quad 25Gb/s 270mW TIA in 0.13µm BiCMOS with <0.15dB Crosstalk Penalty — **8:30 AM**

G. Kalogerakis, T. Moran, T. Nguyen, G. Denoyer, Finisar, Sunnyvale, CA

7.2 A 4× 25-to-28Gb/s 4.9mW/Gb/s -9.7dBm High-Sensitivity Optical Receiver Based on 65nm CMOS for Board-to-Board Interconnects — **9:00 AM**

T. Takemoto[1], H. Yamashita[1], T. Yazaki[2], N. Chujo[2], Y. Lee[1], Y. Matsuoka[1]
[1]Hitachi, Tokyo, Japan; [2]Hitachi, Kanagawa, Japan

7.3 100Gb/s Ethernet Chipsets in 65nm CMOS Technology — **9:30 AM**

J-Y. Jiang[1], P-C. Chiang[1], H-W. Hung[1], C-L. Lin[1], T. Yoon[2], J. Lee[1]
[1]National Taiwan University, Taipei, Taiwan; [2]Basas Microelectronics, Beijing, China

Break — **10:00 AM**

7.4 A Blind Baud-Rate ADC-Based CDR — **10:15 AM**

C. Ting[1], J. Liang[1], A. Sheikholeslami[1], M. Kibune[2], H. Tamura[2]
[1]University of Toronto, Toronto, Canada; [2]Fujitsu Laboratories, Kawasaki, Japan

7.5 A Ring-Resonator-Based Silicon Photonics Transceiver with Bias-Based Wavelength Stabilization and Adaptive-Power-Sensitivity Receiver — **10:45 AM**

C. Li[1], R. Bai[2], A. Shafik[1], E. Zhian Tabasy[1], G. Tang[1], C. Ma[2], C-H. Chen[3], Z. Peng[3], M. Fiorentino[3], P. Chiang[2,4], S. Palermo[1]
[1]Texas A&M University, College Station, TX; [2]Oregon State University, Corvallis, OR
[3]Hewlett Packard, Palo Alto, CA; [4]Fudan University, Shanghai, China

7.6 A 1.23pJ/b 2.5Gb/s Monolithically Integrated Optical Carrier-Injection Ring Modulator and All-Digital Driver Circuit in Commercial 45nm SOI — **11:15 AM** **DS1**

B. R. Moss[1], C. Sun[1], M. Georgas[1], J. Shainline[2], J. S. Orcutt[1], J. C. Leu[1], M. Wade[2], Y-H. Chen[1], K. Nammari[2], X. Wang[1], H. Li[1], R. Ram[1], M. A. Popovic[2], V. Stojanovic[1]
[1]Massachusetts Institute of Technology, Cambridge, MA
[2]University of Colorado, Boulder, CO

7.7 A 20Gb/s NRZ/PAM-4 1V Transmitter in 40nm CMOS Driving a Si-Photonic Modulator in 0.13µm CMOS — **11:30 AM**

X. Wu[1], B. Dama[2], P. Gothoskar[2], P. Metz[2], K. Shastri[2], S. Sunder[2], J. van der Spiegel[1], Y. Wang[2], M. Webster[2], W. Wilson[2]
[1]University of Pennsylvania, Philadelphia, PA; [2]Cisco Systems, Allentown, PA

7.8 Optical Receivers Using DFE-IIR Equalization — **11:45 AM**

J. Proesel, A. Rylyakov, C. Schow, IBM Research, Yorktown Heights, NY

7.9 A 10Gb/s 6V_{pp} Differential Modulator Driver in 0.18µm SiGe-BiCMOS — **12:00 PM**

Y. Zhao[1], L. Vera[1], J. R. Long[1], D. L. Harame[2]
[1]Delft University of Technology, Delft, The Netherlands; [2]IBM, Essex Junction, VT

Conclusion — **12:15 PM**

Millimeter-Wave Techniques

Session Chair: ***Ullrich Pfeiffer,*** *University of Wuppertal, Wuppertal, Germany*
Associate Chair: ***Gabriel Rebeiz,*** *University of California, San Diego, La Jolla, CA*

8.1 A 210GHz Fully Integrated Differential Transceiver with Fundamental-Frequency VCO in 32nm SOI CMOS — **8:30 AM**

Z. Wang[1], P-Y. Chiang[1], P. Nazari[1], C-C. Wang[2], Z. Chen[3], P. Heydari[1]
[1]University of California, Irvine, CA
[2]Peregrine Semiconductor, San Diego, CA
[3]Beijing Institute of Technology, Beijing, China

8.2 A 260GHz Broadband Source with 1.1mW Continuous-Wave Radiated Power and EIRP of 15.7dBm in 65nm CMOS — **9:00 AM**

R. Han, E. Afshari, Cornell University, Ithaca, NY

8.3 A 260GHz Amplifier with 9.2dB Gain and -3.9dBm Saturated Power in 65nm CMOS — **9:30 AM**

O. Momeni, University of California, Davis, CA

8.4 A 0.7W Fully Integrated 42GHz Power Amplifier with 10% PAE in 0.13µm SiGe BiCMOS — **9:45 AM**

W. Tai[1], L. Carley[1], D. S. Ricketts[2]
[1]Carnegie Mellon University, Pittsburgh, PA
[2]North Carolina State University, Raleigh, NC

Break — **10:00 AM**

8.5 A 93-to-113GHz BiCMOS 9-Element Imaging Array Receiver Utilizing Spatial-Overlapping Pixels with Wideband Phase and Amplitude Control — **10:15 AM**

F. Caster II, L. Gilreath, S. Pan, Z. Wang, F. Capolino, P. Heydari
University of California, Irvine, CA

8.6 A 94GHz 3D-Image Radar Engine with 4TX/4RX Beamforming Scan Technique in 65nm CMOS — **10:45 AM**

P-N. Chen, P-J. Peng, C. Kao, Y-L. Chen, J. Lee
National Taiwan University, Taipei, Taiwan

8.7 A Low-Cost Miniature 120GHz SiP FMCW/CW Radar Sensor with Software Linearization — **11:15 AM**

Y. Sun[1], M. Marinkovic[1], G. Fischer[1], W. Winkler[2], W. Debski[2], S. Beer[3], T. Zwick[3], M. G. Girma[4], J. Hasch[4], C. J. Scheytt[5]
[1]IHP, Frankfurt Oder, Germany
[2]Silicon Radar, Frankfurt Oder, Germany
[3]Karlsruhe Institute of Technology, Karlsruhe, Germany
[4]Robert Bosch, Stuttgart, Germany
[5]University of Paderborn, Paderborn, Germany

DS1

8.8 A 10mW 37.8GHz Current-Redistribution BiCMOS VCO with an Average FOM_T of -193.5dBc/Hz — **11:45 AM**

Q. Wu[1], T. Quach[2], A. Mattamana[2], S. Elabd[1], S. R. Dooley[2], J. J. McCue[1], P. L. Orlando[2]G. L. Creech[2], W. Khalil[1]
[1]Ohio State University, Columbus, OH
[2]Air Force Research Laboratory, Wright-Patterson AFB, Dayton, OH

Conclusion — **12:15 PM**

Mobile Application Processors and Media Accelerators

Session Chair: ***Michael Polley,*** *Texas Instruments, Dallas, TX*
Associate Chair: ***Yongha Park,*** *Samsung, Yongin, Korea*

9.1 28nm High-κ Metal-Gate Heterogeneous Quad-Core CPUs for High-Performance and Energy-Efficient Mobile Application Processor — 8:30 AM

Y. Shin[1], K. Shin[1], P. Kenkare[2], R. Kashyap[2], H-J. Lee[1], D. Seo[1], B. Millar[2], Y. Kwon[1], R. Iyengar[2], M-S. Kim[1], A. Chowdhury[2], S-I. Bae[1], I. Hon[1], W. Jeong[2], A. Lindner[2], U. Cho[1], K. Hawkins[2], J. Son[1], S. Hwang[1]
[1]Samsung Electronics, Yongin, Korea; [2]Samsung Electronics, Austin, TX

9.2 A 28nm High-κ Metal-Gate Single-Chip Communications Processor with 1.5GHz Dual-Core Application Processor and LTE/HSPA+-Capable Baseband Processor — 9:00 AM

M. Fujigaya[1], N. Sakamoto[1], T. Koike[1], T. Irita[1], K. Wakahara[1], T. Matsuyama[1], K. Hasegawa[1], T. Saito[1], A. Fukuda[1], K. Teranishi[1], K. Fukuoka[2], N. Maeda[2], K. Nii[2], T. Kataoka[1], T. Hattori[1]
[1]Renesas Mobile, Tokyo, Japan; [2]Renesas Electronics, Tokyo, Japan

9.3 A 0.48V 0.57nJ/Pixel Video-Recording SoC in 65nm CMOS — 9:30 AM

T-J. Lin[1], C-A. Chien[1], P-Y. Chang[1], C-W. Chen[2], P-H. Wang[3], T-Y. Shyu[1], C-Y. Chou[2],S-C. Luo[2], J-I. Guo[3], T-F. Chen[3], G. Chuang[2], Y-H. Chu[2], L-C. Cheng[2], H-M. Su[4], C. Jou[5], M. Ieong[5], C-W. Wu[2], J-S. Wang[1]
[1]National Chung Cheng University, Chiayi, Taiwan
[2]Industrial Technology Research Institute, Hsinchu, Taiwan
[3]National Chiao Tung University, Hsinchu, Taiwan
[4]Andes Technology, Hsinchu, Taiwan; [5]TSMC, Hsinchu, Taiwan
DS1

9.4 72.5GFLOPS 240Mpixel/s 1080p 60fps Multi-Format Video Codec Application Processor Enabled with GPGPU for Fused Multimedia Application — 9:45 AM

Y. Park, C. Yu, K. Lee, H. Kim, Y. Park, C. Kim, Y. Choi, J. Oh, C. Oh, G. Moon, S. Kim, H. Jang, J-A. Lee, C. Kim, S. Park
Samsung Electronics, Yongin, Korea

Break — 10:00 AM

9.5 A 249Mpixel/s HEVC Video-Decoder Chip for Quad Full HD Applications — 10:15 AM

C-T. Huang[1], M. Tikekar[1], C. Juvekar[1], V. Sze[2], A. Chandrakasan[1]
[1]Massachusetts Institute of Technology, Cambridge, MA; [2]Texas Instruments, Dallas, TX
DS1

9.6 Reconfigurable Processor for Energy-Scalable Computational Photography — 10:45 AM

R. Rithe[1], P. Raina[1], N. Ickes[1], S. V. Tenneti[2], A. P. Chandrakasan[1]
[1]Massachusetts Institute of Technology, Cambridge, MA
[2]California Institute of Technology, Pasadena, CA
DS1

9.7 A 470mV 2.7mW Feature Extraction-Accelerator for Micro-Autonomous Vehicle Navigation in 28nm CMOS — 11:15 AM

D. Jeon, Y. Kim, I. Lee, Z. Zhang, D. Blaauw, D. Sylvester
University of Michigan, Ann Arbor, MI

9.8 A 646GOPS/W Multi-Classifier Many-Core Processor With Cortex-Like Architecture for Super-Resolution Recognition — 11:45 AM

J. Park, I. Hong, G. Kim, Y. Kim, K. Lee, S. Park, K. Bong, H-J. Yoo
KAIST, Daejeon, Korea
DS1

Conclusion — 12:15 PM

Analog Techniques

Session Chair: ***Jafar Savoj,*** *Xilinx, San Jose, CA*
Associate Chair: ***Chris Mangelsdorf,*** *Analog Devices, Tokyo, Japan*

10.1 A 0.1-to-1.2GHz Tunable 6th-Order N-Path Channel-Select Filter with 0.6dB Passband Ripple and +7dBm Blocker Tolerance **8:30 AM**

M. Darvishi, R. van der Zee, B. Nauta, University of Twente, Enschede, The Netherlands

10.2 A 2mW 800MS/s 7th-Order Discrete-Time IIR Filter with 400kHz-to-30MHz BW and 100dB Stop-Band Rejection in 65nm CMOS **9:00 AM**

M. Tohidian, I. Madadi, R. B. Staszewski
Delft University of Technology, Delft, The Netherlands

10.3 A Multi-Path Chopper-Stabilized Capacitively Coupled Operational Amplifier with 20V-Input-Common-Mode Range and 3μV Offset **9:30 AM**

Q. Fan, J. Huijsing, K. A. A. Makinwa, Delft University of Technology, Delft, The Netherlands

10.4 A 0.06mm² 14nV/√Hz Chopper Instrumentation Amplifier with Automatic Differential-Pair Matching **9:45 AM**

I. Akita[1], M. Ishida[1,2]
[1]Toyohashi University of Technology, Toyohashi, Japan
[2]Electronics-Inspired Interdisciplinary Research Institute (EIIRIS), Toyohashi, Japan

Break **10:00 AM**

10.5 A 4Ω 2.3W Class-D Audio Amplifier with Embedded DC-DC Boost Converter, Current-Sensing ADC and DSP for Adaptive Speaker Protection **10:15 AM**

DS1

M. Berkhout, L. Dooper, B. Krabbenborg, J. Somberg
NXP Semiconductors, Nijmegen, The Netherlands

10.6 A 62mW Stereo Class-G Headphone Driver with 108dB Dynamic Range and 600μA/Channel Quiescent Current **10:45 AM**

J. Chen[1], S. Arunachalam[1], T. L. Brooks[1], I. Mehr[1], F. Cheung[1], H. Venkatram[2]
[1]Broadcom, Irvine, CA; [2]Oregon State University, Corvallis, OR

10.7 A 120nW 18.5kHz RC Oscillator with Comparator Offset Cancellation for ±0.25% Temperature Stability **11:00 AM**

A. Paidimarri[1], D. Griffith[2], A. Wang[3], A. P. Chandrakasan[1], G. Burra[2]
[1]Massachusetts Institute of Technology, Cambridge, MA
[2]Texas Instruments, Dallas, TX; [3]MediaTek, Austin, TX

10.8 A 63,000 Q-Factor Relaxation Oscillator with Switched-Capacitor Integrated Error Feedback **11:15 AM**

Y. Cao[1,2], P. Leroux[1], W. De Cock[2], M. Steyaert[1]
[1]KU Leuven, Heverlee, Belgium; [2]SCK-CEN, Mol, Belgium

10.9 A 0.45V 423nW 3.2MHz Multiplying DLL with Leakage-Based Oscillator for Ultra-Low-Power Sensor Platforms **11:45 AM**

D-W. Jee[1], D. Sylvester[2], D. Blaauw[2], J-Y. Sim[1]
[1]Pohang University of Science and Technology, Pohang, Korea
[2]University of Michigan, Ann Arbor, MI

Conclusion **12:15 PM**

Emerging Memory and Wireless Technology

Session Chair: ***Fu-Lung Hsueh,*** *TSMC, Hsinchu, Taiwan*
Associate Chair: ***Shinichiro Mutoh,*** *NTT, Atsugi, Japan*

11.1 A 3.4pJ FeRAM-Enabled D Flip-Flop in 0.13µm CMOS for Nonvolatile Processing in Digital Systems — **8:30 AM**

M. Qazi[1], A. Amerasekera[2], A. P. Chandrakasan[1]
[1]Massachusetts Institute of Technology, Cambridge, MA; [2]Texas Instruments, Dallas, TX

11.2 Nonvolatile Logic-in-Memory Array Processor in 90nm MTJ/MOS Achieving 75% Leakage Reduction Using Cycle-Based Power Gating — **9:00 AM**

M. Natsui[1], D. Suzuki[1], N. Sakimura[2], R. Nebashi[2], Y. Tsuji[2], A. Morioka[2], T. Sugibayashi[2], S. Miura[2], H. Honjo[2], K. Kinoshita[1], S. Ikeda[1], T. Endoh[1], H. Ohno[1], T. Hanyu[1]
[1]Tohoku University, Sendai, Japan; [2]NEC, Tsukuba, Japan

11.3 A Versatile Timing Microsystem Based on Wafer-Level Packaged XTAL/BAW Resonators with Sub-µW RTC Mode and Programmable HF Clocks — **9:30 AM** **DS1**

D. Ruffieux[1], N. Scolari[1], F. Giroud[1], T. C. Le[1], S. Dalla Piazza[2], F. Staub[2], K. Zoschke[3], C. A. Manier[3], H. Oppermann[3], J. Dekker[4], T. Suni[4], G. Allegato[5]
[1]CSEM, Neuchatel, Switzerland; [2]Micro Crystal, Grenchen, Switzerland
[3]Fraunhofer IZM, Berlin, Germany; [4]VTT, Espoo, Finland
[5]STMicroelectronics, Agrate Brianza, Italy

Break — **10:00 AM**

11.4 Microwave Amplification with Nanomechanical Resonators — **10:15 AM**

F. Massel[1], T. T. Heikkilä[1], J-M. Pirkkalainen[1], S-U. Cho[1], H. Saloniemi[2], P. J. Hakonen[1], M. A. Sillanpää[1]
[1]Aalto University, Espoo, Finland; [2]VTT, Espoo, Finland

11.5 A 0.15mm-Thick Non-Contact Connector for MIPI Using Vertical Directional Coupler — **10:45 AM** **DS1**

W. Mizuhara, T. Shidei, A. Kosuge, T. Takeya, N. Miura, M. Taguchi, H. Ishikuro, T. Kuroda
Keio University, Yokohama, Japan

11.6 1.2Gb/s 3.9pJ/b Mono-Phase Pulse-Modulation Inductive-Coupling Transceiver for mm-Range Board-to-Board Communication — **11:15 AM** **DS1**

H. Cho[1], U. Ha[1], T. Roh[1], D. Kim[2], J. Lee[2], Y. Oh[2], H-J. Yoo[1]
[1]KAIST, Daejeon, Korea; [2]Samsung Electronics, Suwon, Korea

11.7 Retrodirective Transponder Array with Universal On-Sheet Reference for Wireless Mobile Sensor Networks Without Battery or Oscillator — **11:45 AM**

H. Fukuda, T. Terada, T. Kuroda, Keio University, Yokohama, Japan

11.8 A Scalable 2.9mW 1Mb/s eTextiles Body Area Network Transceiver with Remotely Powered Sensors and Bi-Directional Data Communication — **12:00 PM**

N. V. Desai[1], J. Yoo[2], A. P. Chandrakasan[1]
[1]Massachusetts Institute of Technology, Cambridge, MA
[2]Masdar Institute of Science and Technology, Abu Dhabi, United Arab Emirates

Conclusion — **12:15 PM**

Nonvolatile Memory Solutions

Session Chair: ***Jin-Man Han,*** *Samsung Electronics, Hwasung, Korea*
Associate Chair: ***Daniele Vimercati,*** *Micron Technology, Agrate Brianza, Italy*

12.1 A 130.7mm² 2-Layer 32Gb ReRAM Memory Device in 24nm Technology — 1:30 PM

T-Y. Liu[1], T. Yan[1], R. Scheuerlein[1], Y. Chen[1], J. Lee[1], G. Balakrishnan[1], G. Yee[1], H. Zhang[1], A. Yap[1], J. Ouyang[1], T. Sasaki[2], S. Addepalli[1], A. Al-Shamma[1], C-Y. Chen[1], M. Gupta[1], G. Hilton[1], S. Joshi[1], A. Kathuria[1], V. Lai[1], D. Masiwal[1], M. Matsumoto[1], A. Nigam[1], A. Pai[1], J. Pakhale[1], C. Siau[1], X. Wu[1], R. Yin[1], L. Peng[1], J. Kang[1], S. Huynh[1], H. Wang[1], N. Nagel[3], Y. Tanaka[3], M. Higashitani[1], T. Minvielle[1], C. Gorla[1], T. Tsukamoto[4], T. Yamaguchi[4], M. Okajima[4], T. Okamura[4], S. Takase[2], T. Hara[2], H. Inoue[4], L. Fasoli[1], M. Mofidi[1], R. Shrivastava[1], K. Quader[1]

[1]Sandisk, Milpitas, CA; [2]Toshiba, Yokohama, Japan; [3]Sandisk, Yokkaichi, Japan; [4]Toshiba, Yokkaichi, Japan

12.2 40nm Embedded SG-MONOS Flash Macros for Automotive with 160MHz Random Access for Code and Endurance Over 10M Cycles for Data — 2:00 PM

T. Kono[1], T. Ito[1], T. Tsuruda[1], T. Nishiyama[1], T. Nagasawa[1], T. Ogawa[1], Y. Kawashima[2], H. Hidaka[1], T. Yamauchi[1]

[1]Renesas Electronics, Itami, Japan; [2]Renesas Electronics, Hitachinaka, Japan

12.3 A 6nW Inductive-Coupling Wake-Up Transceiver for Reducing Standby Power of Non-Contact Memory Card by 500× — 2:30 PM

N. Miura, M. Saito, M. Taguchi, T. Kuroda, Keio University, Yokohama, Japan

12.4 Time-Differential Sense Amplifier for Sub-80mV Bitline Voltage Embedded STT-MRAM in 40nm CMOS — 2:45 PM

M. Jefremow[1,2], T. Kern[1], W. Allers[1], C. Peters[1], J. Otterstedt[1], O. Bahlous[1], K. Hofmann[1], R. Allinger[1], S. Kassenetter[1], D. Schmitt-Landsiedel[2]

[1]Infineon Technologies, Neubiberg, Germany; [2]Technical University Munich, Munich, Germany

Break — 3:00 PM

12.5 A 128Gb 3b/cell NAND Flash Design Using 20nm Planar-Cell Technology — 3:15 PM

G. Naso[1], L. Botticchio[1], M. Castelli[1], C. Cerafogli[1], M. Cichocki[1], P. Conenna[1], A. D'Alessandro[1], L. De Santis[1], D. Di Cicco[1], W. Di Francesco[1], M. Gallese[1], G. Gallo[2], M. Incarnati[1], C. Lattaro[1], A. Macerola[1], G. Marotta[1], V. Moschiano[1], D. Orlandi[1], F. Paolini[1], S. Perugini[1], L. Pilolli[1], P. Pistilli[2], G. Rizzo[2], F. Rori[1], M. Rossini[1], G. Santin[1], E. Sirizotti[1], A. Smaniotto[2], U. Siciliani[2], M. Tiburzi[1], R. Meyer[3], A. Goda[3], B. Filipiak[3], T. Vali[1], M. Helm[4], R. Ghodsi[4]

[1]Micron, Avezzano, Italy; [2]Micron, Padua, Italy; [3]Micron, Boise, ID; [4]Micron, San Jose, CA

12.6 Filament Scaling Forming Technique and Level-Verify-Write Scheme with Endurance Over 10^7 Cycles in ReRAM — 3:45 PM

A. Kawahara[1], K. Kawai[1], Y. Ikeda[1], Y. Katoh[1], R. Azuma[1], Y. Yoshimoto[1], K. Tanabe[2], Z. Wei[1], T. Ninomiya[1], K. Katayama[1], R. Yasuhara[1], S. Muraoka[1], A. Himeno[1], N. Yoshikawa[1], H. Murase[1], K. Shimakawa[1], T. Takagi[1], T. Mikawa[1], K. Aono[1]

[1]Panasonic, Kyoto, Japan, [2]Panasonic, Nagaokakyo, Japan

12.7 A 45nm 6b/cell Charge-Trapping Flash Memory Using LDPC-Based ECC and Drift-Immune Soft-Sensing Engine — 4:15 PM

K-C. Ho[1,2], P-C. Fang[1], H-P. Li[1], C-Y. M. Wang[1], H-C. Chang[2]

[1]Macronix, Hsinchu, Taiwan; [2]National Chiao Tung University, Hsinchu, Taiwan

12.8 Cycling Endurance Optimization Scheme for 1Mb STT-MRAM in 40nm Technology — 4:30 PM

H-C. Yu, K-C. Lin, K-F. Lin, C-Y. Huang, Y-D. Chih, T-C. Ong, J. Chang, S. Natarajan, L. Tran

TSMC, Hsinchu, Taiwan

12.9 Unified Solid-State-Storage Architecture with NAND Flash Memory and ReRAM that Tolerates 32× Higher BER for Big-Data Applications — 4:45 PM

DS2

S. Tanakamaru[1,2], M. Doi[1], K. Takeuchi[1], [1]Chuo University, Tokyo, Japan; [2]University of Tokyo, Tokyo, Japan

Conclusion — 5:15 PM

High-Performance Wireless

Session Chair: ***Brian Floyd,*** *North Carolina State University, Raleigh, NC*
Associate Chair: ***Kenichi Okada,*** *Tokyo Institute of Technology, Tokyo, Japan*

13.1 A Fully Integrated 60GHz CMOS Transceiver Chipset Based on WiGig/IEEE802.11ad with Built-In Self Calibration for Mobile Applications **1:30 PM**

DS2

T. Tsukizawa, N. Shirakata, T. Morita, K. Tanaka, J. Sato, Y. Morishita, M. Kanemaru, R. Kitamura, T. Shima, T. Nakatani, K. Miyanaga, T. Urushihara, H. Yoshikawa, T. Sakamoto, H. Motozuka, Y. Shirakawa, N. Yosoku, A. Yamamoto, R. Shiozaki, N. Saito
Panasonic, Yokohama, Japan

13.2 A Digitally Modulated mm-Wave Cartesian Beamforming Transmitter with Quadrature Spatial Combining **2:00 PM**

J. Chen[1], L. Ye[1], D. Titz[2], F. Gianesello[3], R. Pilard[3], A. Cathelin[3], F. Ferrero[2], C. Luxey[2], A. M. Niknejad[1]
[1]University of California, Berkeley, CA; [2]University of Nice, Nice, France
[3]STMicroelectronics, Crolles, France

13.3 A 50mW-TX 65mW-RX 60GHz 4-Element Phased-Array Transceiver with Integrated Antennas in 65nm CMOS **2:30 PM**

L. Kong, D. Seo, E. Alon, University of California, Berkeley, CA

13.4 A Low-Power Radio Chipset in 40nm LP CMOS with Beamforming for 60GHz High-Data-Rate Wireless Communication **2:45 PM**

V. Vidojkovic[1], V. Szortyka[1,2], K. Khalaf[1,2], G. Mangraviti[1,2], S. Brebels[1], W. van Thillo[1], K. Vaesen[1], B. Parvais[1], V. Issakov[1], M. Libois[1], M. Matsuo[3], J. Long[4], C. Soens[1], P. Wambacq[1,2]
[1]imec, Leuven, Belgium; [2]Vrije Universiteit, Brussels, Belgium
[3]Panasonic, Yokohama, Japan; [4]Delft University of Technology, Delft, The Netherlands

Break **3:00 PM**

13.5 A Mixed-Signal 32-Coefficient RX-FFE 100-Coefficient DFE for an 8Gb/s 60GHz Receiver in 65nm LP CMOS **3:15 PM**

C. Thakkar[1,2], N. Narevsky[1], C. D. Hull[2], E. Alon[1]
[1]University of California, Berkeley, CA; [2]Intel, Hillsboro, OR

13.6 A 2-to-16GHz 204mW 3mm-Resolution Stepped-Frequency Radar for Breast-Cancer Diagnostic Imaging in 65nm CMOS **3:45 PM**

M. Caruso, M. Bassi, A. Bevilacqua, A. Neviani, University of Padova, Padova, Italy

13.7 A Scalable Direct-Sampling Broadband Radar Receiver Supporting Simultaneous Digital Multibeam Array in 65nm CMOS **4:15 PM**

C-M. Lai, J-M. Wu, P-C. Huang, T-S. Chu, National Tsing Hua University, Hsinchu, Taiwan

13.8 A Digital Single-Wire Multiswitch (DSWM) Channel-Stacking IC in 45nm CMOS for Satellite Outdoor Units **4:45 PM**

W. Gao[1], B. Huff[1], K. Hess[1], D. Coulibaly[2], C. Pala[1], J. Cao[1], J. Bhatia[1], M. Waltari[1], L. Levin[1], C. Cathelin[2], T. Nouvet[2], N. Nidhi[1], R. Kodkani[1], R. Maeda[1], D. Costa[1], J. McFee[1], R. Moazzam[1], H. Vincent[2], P. Durieux[2]
[1]NXP Semiconductors, San Diego, CA; [2]NXP Semiconductors, Caen, France

Conclusion **5:15 PM**

Digital PLLs and Building Blocks

Session Chair: ***Anthony Hill,*** *Texas Instruments, Dallas, TX*
Associate Chair: ***Atsuki Inoue,*** *Fujitsu, Kawasaki, Japan*

14.1 A 0.022mm² 970µW Dual-Loop Injection-Locked PLL with -243dB FOM Using Synthesizable All-Digital PVT Calibration Circuits — **1:30 PM**

W. Deng, A. Musa, T. Siriburanon, M. Miyahara, K. Okada, A. Matsuzawa
Tokyo Institute of Technology, Tokyo, Japan

14.2 A 0.032mm² 3.1mW Synthesized Pixel Clock Generator with 30ps$_{rms}$ Integrated Jitter and 10-to-630MHz DCO Tuning Range — **2:00 PM**

W. Kim[1], J. Park[2], J. Kim[2], T. Kim[2], H. Park[2], D. Jeong[1]
[1]Seoul National University, Seoul, Korea; [2]Samsung Electronics, Yongin, Korea

14.3 An All-Digital PLL Using Random Modulation for SSC Generation in 65nm CMOS — **2:30 PM**

N. Da Dalt, P. Pridnig, W. Grollitsch, Infineon Technologies, Villach, Austria

14.4 A 0.026mm² 5.3mW 32-to-2000MHz Digital Fractional-N Phase Locked-Loop Using a Phase-Interpolating Phase-to-Digital Converter — **2:45 PM**

T-K. Jang, X. Nan, F. Liu, J. Shin, H. Ryu, J. Kim, T. Kim, J. Park, H. Park
Samsung Electronics, Yongin, Korea

Break — **3:00 PM**

14.5 A 2.5GHz 2.2mW/25µW On/Off-State Power 2ps$_{rms}$-Long-Term-Jitter Digital Clock Multiplier with 3-Reference-Cycles Power-On Time — **3:15 PM**

T. Anand, M. Talegaonkar, A. Elshazly, B. Young, P. Hanumolu
Oregon State University, Corvallis, OR

14.6 3D Clock Distribution Using Vertically/Horizontally-Coupled Resonators — **3:45 PM**

Y. Take, N. Miura, H. Ishikuro, T. Kuroda, Keio University, Yokohama, Japan

14.7 All-Digital Hybrid Temperature Sensor Network for Dense Thermal Monitoring — **4:00 PM**

S. Paek, W. Shin, J. Lee, H-E. Kim, J-S. Park, L-S. Kim, KAIST, Daejeon, Korea

14.8 A 95fJ/b Current-Mode Transceiver for 10mm On-Chip Interconnect — **4:15 PM**

S-K. Lee[1,2], S-H. Lee[1], D. Sylvester[3], D. Blaauw[3], J-Y. Sim[1]
[1]Pohang University of Science and Technology, Pohang, Korea
[2]Samsung Electronics, Hwasung, Korea
[3]University of Michigan, Ann Arbor, MI

14.9 Razor-Lite: A Side-Channel Error-Detection Register for Timing-Margin Recovery in 45nm SOI CMOS — **4:45 PM**

S. Kim, I. Kwon, D. Fick, M. Kim, Y-P. Chen, D. Sylvester
University of Michigan, Ann Arbor, MI

Conclusion — **5:15 PM**

Data Converter Techniques

Session Chair: ***Michael Perrott,*** *Masdar Institute of Science and Technology, Abu Dhabi, United Arab Emirates*
Associate Chair: ***Geert van der Plas,*** *imec, Leuven-Heverlee, Belgium*

15.1 A 28fJ/conv-step CT ΔΣ Modulator with 78dB DR and 18MHz BW in 28nm CMOS Using a Highly Digital Multibit Quantizer — **1:30 PM**

Y-S. Shu, J-Y. Tsai, P. Chen, T-Y. Lo, P-C. Chiu
MediaTek, Hsinchu, Taiwan

15.2 A 2.2/2.7fJ/conversion-step 10/12b 40kS/s SAR ADC with Data-Driven Noise Reduction — **2:00 PM**

P. Harpe, E. Cantatore, A. van Roermund
Eindhoven University of Technology, Eindhoven, The Netherlands

15.3 A 71dB-SNDR 50MS/s 4.2mW CMOS SAR ADC by SNR Enhancement Techniques Utilizing Noise — **2:30 PM**

T. Morie, T. Miki, K. Matsukawa, Y. Bando, T. Okumoto, K. Obata, S. Sakiyama, S. Dosho
Panasonic, Moriguchi, Japan

Break — **3:00 PM**

15.4 A 1V 14b Self-Timed Zero-Crossing-Based Incremental ΔΣ ADC — **3:15 PM**

C. Chen, Z. Tan, M. A. Pertijs
Delft University of Technology, Delft, The Netherlands

15.5 A 6.3μW 20b Incremental Zoom-ADC with 6ppm INL and 1μV Offset — **3:45 PM**

Y. Chae[1], K. Souri[2], K. A. A. Makinwa[2]
[1]Yonsei University, Seoul, Korea
[2]Delft University of Technology, Delft, The Netherlands

15.6 A 20b Clockless DAC with Sub-ppm-Linearity 7.5nV/√Hz-Noise and 0.05ppm/°C-Stability — **4:15 PM**

R. C. McLachlan[1], A. Gillespie[1], M. C. Coln[2], D. Chisholm[1], D. T. Lee[1]
[1]Analog Devices, Edinburgh, United Kingdom
[2]Analog Devices, Wilmington, MA

15.7 A 2.4-to-5.2fJ/conversion-step 10b 0.5-to-4MS/s SAR ADC with Charge-Average Switching DAC in 90nm CMOS — **4:45 PM**

C-Y. Liou, C-C. Hsieh
National Tsing Hua University, Hsinchu, Taiwan

15.8 Adaptive Cancellation of Gain and Nonlinearity Errors in Pipelined ADCs — **5:00 PM**

Y. Miyahara[1], M. Sano[1], K. Koyama[1], T. Suzuki[1], K. Hamashita[1], B-S. Song[2]
[1]Asahi Kasei Microdevices, Atsugi, Japan
[2]University of California, San Diego, La Jolla, CA

Conclusion — **5:15 PM**

Biomedical Circuits & Systems

Session Chair: ***Refet Firat Yazicioglu,*** *imec, Leuven, Belgium*
Associate Chair: ***TaeChan Kim,*** *Samsung Semiconductor, Yongin, Korea*

16.1 A Fully Integrated 8-Channel Closed-Loop Neural-Prosthetic SoC for Real-Time Epileptic Seizure Control **1:30 PM**

W-M. Chen[1], H. Chiueh[1], T-J. Chen[1], C-L. Ho[1], C. Jeng[1], S-T. Chang[1], M-D. Ker[1], C-Y. Lin[1], Y-C. Huang[1], C-W. Chou[1], T-Y. Fan[1], M-S. Cheng[1], S-F. Liang[2], T-C. Chien[2], S-Y. Wu[2], Y-L. Wang[2], F-Z. Shaw[2], Y-H. Huang[2], C-H. Yang[1], J-C. Chiou[1], C-W. Chang[1], L-C. Chou[1], C-Y. Wu[1]

[1]National Chiao Tung University, Hsinchu, Taiwan
[2]National Cheng Kung University, Tainan, Taiwan

DS2

16.2 An Implantable 455-Active-Electrode 52-Channel CMOS Neural Probe **2:00 PM**

C. Mora Lopez[1], A. Andrei[1], S. Mitra[1], M. Welkenhuysen[1], W. Eberle[1], C. Bartic[2], R. Puers[2], R. F. Yazicioglu[1], G. Gielen[2]

[1]imec, Heverlee, Belgium; [2]KU Leuven, Heverlee, Belgium

16.3 A 0.45V 100-Channel Neural-Recording IC with Sub-μW/Channel Consumption in 0.18μm CMOS **2:30 PM**

D. Han[1,2], Y. Zheng[1], R. Rajkumar[3], G. Dawe[3], M. Je[2,3]

[1]Nanyang Technological University, Singapore, Singapore
[2]Institute of Microelectronics, Singapore, Singapore
[3]National University of Singapore, Singapore, Singapore

16.4 24-Channel Dual-Band Wireless Neural Recorder with Activity-Dependent Power Consumption **2:45 PM**

S. Mitra[1], J. Putzeys[1], F. Battaglia[2], C. M. Lopez[1], M. Welkenhuysen[1], C. Pennartz[2], C. van Hoof[1], R. F. Yazicioglu[1]

[1]imec, Leuven, Belgium; [2]University of Amsterdam, Amsterdam, The Netherlands

Break **3:00 PM**

16.5 A 37.6mm² 1024-Channel High-Compliance-Voltage SoC for Epiretinal Prostheses **3:15 PM**

K. Chen, Y-K. Lo, W. Liu, University of California, Los Angeles, CA

16.6 A Fully Intraocular 0.0169mm²/pixel 512-Channel Self-Calibrating Epiretinal Prosthesis in 65nm CMOS **3:45 PM**

M. Monge[1], M. Raj[1], M. Honarvar-Nazari[1], H-C. Chang[1], Y. Zhao[1], J. Weiland[2,3], M. Humayun[2,3], Y-C. Tai[1], A. Emami-Neyestanak[1]

[1]California Institute of Technology, Pasadena, CA; [2]Doheny Eye Institute, Los Angeles, CA
[3]University of Southern California, Los Angeles, CA

16.7 A Near-Field-Communication (NFC) Enabled Wireless Fluorimeter for Fully Implantable Biosensing Applications **4:15 PM**

A. D. Dehennis[1], M. Mailand[2], D. Grice[2], S. Getzlaff[2], A. E. Colvin[1]

[1]Senseonics, Germantown, MD; [2]Zentrum Mikroelektronik Dresden, Dresden, Germany

DS2

16.8 An Integrated Magnetic Spectrometer for Multiplexed Biosensing **4:45 PM**

C. Sideris, A. Hajimiri, California Institute of Technology, Pasadena, CA

16.9 A 20μW Intra-Cardiac Signal-Processing IC with 82dB Bio-Impedance Measurement Dynamic Range and Analog Feature Extraction for Ventricular Fibrillation Detection **5:00 PM**

S. Kim[1], L. Yan[1], S. Mitra[1], M. Osawa[2], Y. Harada[2], K. Tamiya[2], C. van Hoof[1,3], R. Yazicioglu[1]

[1]imec, Leuven, Belgium; [2]Olympus, Tokyo, Japan; [3]KU Leuven, Leuven, Belgium

Conclusion **5:15 PM**

DEMONSTRATION SESSION 2 (DS2)* TUESDAY, FEBRUARY 19TH 4:00-7:00 PM

This year, the Demonstration Sessions of techniques presented in selected regular papers, both Academic and Industrial, will take place on two evenings: Monday, February 18 and Tuesday, February 19, from 4 pm until 7 pm in the Golden Gate Hall. These demonstrations will feature real-life applications made possible by new ICs presented at ISSCC 2013, as noted by the symbol, DS2 in the Advance Program. Scheduling details will be provided at www.isscc.org shortly before the Conference. Meanwhile, a list of the selected papers is as follows:

Tuesday, February 19th

12.9	**Unified Solid-State-Storage Architecture with NAND Flash Memory and ReRAM that Tolerates 32× Higher BER for Big-Data Applications**	**4:45 PM**
13.1	**A Fully Integrated 60GHz CMOS Transceiver Chipset Based on WiGig/IEEE802.11ad with Built-In Self Calibration for Mobile Applications**	**1:30 PM**
16.1	**A Fully Integrated 8-Channel Closed-Loop Neural-Prosthetic SoC for Real-Time Epileptic Seizure Control**	**1:30 PM**
16.7	**A Near-Field-Communication (NFC) Enabled Wireless Fluorimeter for Fully Implantable Biosensing Applications**	**4:15 PM**

Wednesday, February 20th

17.1	**A 6.4Gb/s Near-Ground Single-Ended Transceiver for Dual-Rank DIMM Memory Interface Systems**	**8:30 AM**
23.4	**A 5.5Gb/s 5mm Contactless Interface Containing a 50Mb/s Bidirectional Sub-Channel Employing Common-Mode OOK Signaling**	**3:15 PM**
24.6	**Reliable and Energy-Efficient 1MHz 0.4V Dynamically Reconfigurable SoC for ExG Applications in 40nm LP CMOS**	**3:45 PM**
24.7	**An 8MHz 75µA/MHz Zero-Leakage Non-Volatile Logic-Based Cortex-M0 MCU SoC Exhibiting 100% Digital State Retention at V_{DD}=0V with <400ns Wakeup and Sleep Transitions**	**4:15 PM**
24.8	**A 100GB/s Wide I/O with 4096b TSVs Through an Active Silicon Interposer with In-Place Waveform Capturing**	**4:45 PM**
25.4	**A 1.9nJ/b 2.4GHz Multistandard (Bluetooth Low Energy/Zigbee/IEEE802.15.6) Transceiver for Personal/Body-Area Networks**	**2:45 PM**
25.7	**A 5.5mW IEEE-802.15.6 Wireless Body-Area-Network Standard Transceiver for Multichannel Electro-Acupuncture Application**	**3:45 PM**
26.1	**A 10.3GS/s 6b Flash ADC for 10G Ethernet Applications**	**1:30 PM**
27.7	**3D Camera Based on Linear-Mode Gain-Modulated Avalanche Photodiodes**	**4:15 PM**

**DS2 may include additional demonstrations of work reported at the Student Research Preview.*

TIMETABLE OF ISSCC 2013 SESSIONS

Sunday, February 17th	ISSCC 2013 TUTORIALS					
8:30AM	**T1:** Basics of 60 GHz LNA and PA Design in CMOS		**T2:** High-Bandwidth Memory Interface Design		**T3:** Energy Harvesters and Energy Processing Circuits	
10:30AM	**T4:** Circuit Deisgn using FinFETs		**T5:** Simulation Techniques for Data Converter Design		**T6**: On-Chip Voltage and Timing Diagnostic Circuits	
1:30PM	**T7:** SoC Design Methodology for Improved Robustness		**T8:** Wireless Transceiver System Design for Modern Communication Standards			
3:30PM	**T9**: Design of Voltage References		**T10:** Data and Power Telemetry for Implants			
	ISSCC 2013 FORUMS					
8:00AM	**F1:** Advanced RF Transceiver Design Techniques			**F2:** VLSI Power Management Techniques: Principles and Applications		

Events below in Bold Box included in Conference registration

	ISSCC 2013 EVENING SESSIONS					
	7:30 PM ES1: Student Research Review: Poster Session with Short Presentations		**8:00 PM ES2:** "Batteries Not Included" - How Little is Enough for Real Energy Autonomy?			
Monday, February 18th	ISSCC 2013 PAPER SESSIONS					
8:30AM	**Session 1:** Plenary Session					
1:30PM	**Session 2:** Ultra High-Speed Trans-ceivers & Equalizers	**Session 3:** Processors	**Session 4:** Harvesting and Wireless Power	**Session 5:** RF Techniques	**Session 6:** Emerging Medical & Sensor Technologies	
5:15PM	Demonstration Session (4:00-7:00 PM), Author Interviews, Social Hour					
	ISSCC 2013 SESSIONS					
8:00PM	**EP1: 60th Anniversary Distinguished Evening Panel : "Antiques from the Innovations Attic"**					
Tuesday, February 19th	ISSCC 2013 PAPER SESSIONS					
8:30AM	**Session 7:** Optical Transceivers & Silicon Photonics	**Session 8:** Millimeter-Wave Techniques	**Session 9:** Mobile Application Processors & Media Accelerators	**Session 10:** Analog Techniques	**Session 11:** Emerging Memory & Wireless Technology	
1:30PM	**Session 12:** Non-Volatile Memory Solutions	**Session 13:** High-Performance Wireless	**Session 14:** Digital PLLs & Building Blocks	**Session 15:** Data Converter Techniques	**Session 16:** Biomedical Circuits & Systems	
5:15PM	Demonstration Session (4:00-7:00 PM), Author Interviews, Social Hour					
	ISSCC 2013 EVENING SESSIONS					
8:00PM	**ES3:** High-speed Communications on 4 Wheels - What's in your Next Car?		**EP2:** You're Hired - The Top 25 Interview Questions for Circuit Designers		**EP3:** Empowering the Killer SoC Applications of 2020	
Wednesday, February 20th	ISSCC 2013 PAPER SESSIONS					
8:30AM	**Session 17:** High-Performance DRAM Interfaces **Session 18:** Advanced Embedded SRAM		**Session 19:** Wireless Transceivers for Smart Devices	**Session 20:** Frequency Generation	**Session 21:** Power Converters	**Session 22:** Sensors & Displays
1:30PM	**Session 23:** Short Reach Links, XCVR Techniques, & PLLs		**Session 24:** Energy Aware Digital Design	**Session 25:** Energy-Efficient Wireless	**Session 26:** High-Speed Data Converters	**Session 27:** Image Sensors
5:15 PM	Author Interviews					

Thursday, February 21st	ISSCC 2013 SHORT COURSE			
8:00 AM	**SC1:** RF Blocks for Wireless Transceivers			
	ISSCC 2013 FORUMS			
8:00AM	**F3:** Emerging Technologies for Wireline Communications	**F4:** Scientific Imaging	**F5:** Frequency Generation and Clock Distribution	**F6:** Mixed-Signal/RF Design and Modeling in Next-Generation CMOS

ES3: High-Speed Communications on 4 Wheels: What's in your Next Car?

Organizer: **Nicola Da Dalt,** *Infineon Technologies, Villach, Austria*

Chair: **Ajith Amerasekera,** *Texas Instruments, Dallas, TX*

Communications inside vehicles is experiencing a growing demand due to applications like infotainment, driver assistance, safety systems and diagnostics, requiring data-rates beyond what is offered by current solutions.
Considering that cabling is the third highest cost factor and the third heaviest component in the car, there is a clear need to go beyond the current low data-rate solutions and converge to a high data-rate backbone network. Solutions, both electrical and optical, are being proposed by car-makers and silicon manufacturers. The evening session will give an overview on the status and outlook on an emerging market that is already shipping 650 million communication ports per year.

Time	Topic
8:00	**The Car: Transformation from Mechanical to Electronic Device** **Kirsten Matheus and Stefan Sturm,** *BMW, Munich, Germany*
8:25	**Wireless Communications In and Around the Car: Status and Outlook** **Norikazu Jack Endo,** *Toyota Info Techn. Center, Tokyo, Japan*
8:50	**From CAN to BroadR-Reach: the Development of Wireline Technologies for Automotive Communications** **Mehmet Tazebay,** *Broadcom, Irvine, CA*
9:15	**Gigabit Ethernet on Reduced Twisted Pair: Leveraging IEEE 802.3 Ethernet Technologies for Next-Generation Vehicle Communications** **Steven B. Carlson,** *High Speed Design, Portland, OR*
9:40	**Optical Fiber: The Backbone of Automotive Communication, Now and Into the Future** **Evan Marchman,** *Microchip Technology, Austin, TX*

EP2: You're Hired - The Top 25 Interview Questions for Circuit Designers

Organizer: **Michael P. Flynn,** *University of Michigan, Ann Arbor, MI*
Co-Organizer: **John Khoury**, *Silicon Labs, Austin, TX*

Moderators: **Michael P. Flynn,** *University of Michigan, Ann Arbor, MI*
John Khoury, *Silicon Labs, Austin, TX*

Circuit designers have to survive one or many technical interviews before being hired for their dream job. Many students and practicing engineers feel confident that they have a strong and intuitive understanding of circuits. However, even the best circuit designers can be stumped by exotic circuits or through a misunderstanding of fundamental concepts. This panel of industry and academic circuit designers will entertain and challenge the audience and each other with questions that often arise during job interviews. The audience can judge which interview questions are fair game in the pursuit of the highly coveted mixed-signal integrated circuit job.

Panelists:

Eric Swanson, *Cirrus Logic, Austin, TX*
Sanroku Tsukamoto, *Fujitsu Laboratories, Kawasaki, Japan*
Marcel Pelgrom, *Consultant, Helmond, The Netherlands*
Beomsup Kim, *Qualcomm, Santa Clara, CA*
Ali Hajimiri, *California Institute of Technology, Pasadena, CA*
Behzad Razavi, *University of California, Los Angeles, CA*

EP3: Empowering the Killer SoC Applications of 2020

Organizers: **Shekhar Borkar,** *Intel, Hillsboro, OR*
Uming Ko, *MediaTek, Austin, TX*
Ali Keshavarzi, *Cypress, San Jose, CA*

Moderators: **Ali Keshavarzi,** *Cypress, San Jose, CA*
Eugenio Cantatore, *Eindhoven University, Eindhoven, The Netherlands*

A distinguished panel from global industry and academia will debate the nature of systems driving the killer applications of 2020. Can we forecast the future killer applications? We have had the computing revolution, then communications, and now the sensor era. Are sensors driving the next killer applications? Are there any other revolutions in sight? What circuits and system innovations can ISSCC bring forward for the next killer applications? What technology elements, device structures and memory architectures are required? Should we continue with silicon technology and find breakthroughs through system architecture, algorithms, SoC integration and packaging? Or should we prepare for "beyond silicon" technologies? Are any beyond-silicon technologies realistic for the future?

Panelists:

Atsushi Murase, *NTT, Tokyo, Japan*
Babak Parviz, *Google, Mountain View, CA*
J. Augusto de Oliveira, *Cypress, San Jose, CA*
Simon Segars, *ARM, Cambridge, United Kingdom*
Raj Yavatkar, *Intel, Hillsboro, OR*
Jong-Shik Yoon, *Samsung, Suwon, South Korea*

High-Performance DRAM Interfaces

Session Chair: ***Yasuhiro Takai,*** *Elpida Memory, Sagamihara, Japan*
Associate Chair: ***James Sung,*** *Etron Technology, Hsinchu, Taiwan*

17.1 A 6.4Gb/s Near-Ground Single-Ended Transceiver for Dual-Rank DIMM Memory Interface Systems — 8:30 AM

K. Kaviani[1], M. Bucher[2], B. Su[2], B. Daly[2], B. Stonecypher[2], W. Dettloff[2], T. Stone[2], K. Prabhu[3], P. Kumar Venkatesan[3], F. Heaton[2], R. Kollipara[1], Y. Lu[1], C. J. Madden[1], J. Eble[2], L. Luo[2], N. Nguyen[1]
[1]Rambus, Sunnyvale, CA
[2]Rambus, Chapel Hill, NC
[3]Rambus, Bangalore, India

DS2

17.2 A 27% Reduction in Transceiver Power for Single-Ended Point-to-Point DRAM Interface with the Termination Resistance of 4×Z_0 at both TX and RX — 9:00 AM

S-M. Lee[1], J-H. Kim[1], J. Kim[2], Y. Kim[2], H. Lee[2], J-Y. Sim[1], H-J. Park[1]
[1]Pohang University of Science and Technology, Pohang, Korea
[2]Hynix Semiconductor, Icheon, Korea

17.3 A 5.7mW/Gb/s 24-to-240Ω 1.6Gb/s Thin-Oxide DDR Transmitter with 1.9-to-7.6V/ns Clock-Feathering Slew-Rate Control in 22nm CMOS — 9:30 AM

M. A. Kossel, C. Menolfi, T. Toifl, P. A. Francese, M. Brändli, P. Buchmann, L. Kull, T. Meyer Andersen, T. Morf
IBM, Rüschlikon, Switzerland

17.4 An Adaptive-Bandwidth PLL for Avoiding Noise Interference and DFE-Less Fast Precharge Sampling for over 10Gb/s/pin Graphics DRAM Interface — 9:45 AM

J. Song[1], H-W. Lee[2], S-B. Lim[1], S. Hwang[1], Y. Kim[2], Y-J. Choi[2], B-T. Chung[2], C. Kim[1]
[1]Korea University, Seoul, Korea
[2]Hynix Semiconductor, Icheon, Korea

Break 10:00 AM

Advanced Embedded SRAM

Session Chair: ***Michael Clinton,*** *Texas Instruments, Dallas, TX*
Associate Chair: ***Atsushi Kawasumi,*** *Toshiba, Kawasaki, Japan*

18.1 A 20nm 112Mb SRAM in High-κ Metal-Gate with Assist Circuitry for Low-Leakage and Low-V_{MIN} Applications **10:15 AM**

J. Chang, Y-H. Chen, H. Cheng, W-M. Chan, H-J. Liao, Q. Li, S. Chang, S. Natarajan, R. Lee, P-W. Wang, S-S. Lin, C-C. Wu, K-L. Cheng, M. Cao, G. Chang
TSMC, Hsinchu, Taiwan

18.2 An SRAM Using Output Prediction to Reduce BL-Switching Activity and Statistically-Gated SA for up to 1.9× Reduction in Energy/Access **10:45 AM**

M. E. Sinangil[1], A. P. Chandrakasan[2]
[1]Nvidia, Bedford, MA
[2]Massachusetts Institute of Technology, Cambridge, MA

18.3 A 27% Active and 85% Standby Power Reduction in Dual-Power-Supply SRAM Using BL Power Calculator and Digitally Controllable Retention Circuit **11:15 AM**

F. Tachibana, O. Hirabayashi, Y. Takeyama, M. Shizuno, A. Kawasumi, K. Kushida, A. Suzuki, Y. Niki, S. Sasaki, T. Yabe, Y. Unekawa
Toshiba, Kawasaki, Japan

18.4 A 64Mb SRAM in 22nm SOI Technology Featuring Fine-Granularity Power Gating and Low-Energy Power-Supply Partition Techniques for 37% Leakage Reduction **11:45 AM**

H. Pilo[1], C. A. Adams[2], R. M. Houle[1], S. M. Lamphier[1], M. M. Lee[1], F. M. Pavlik[1], S. N. Sambatur[3], A. Seferagic[1], R. Wu[1], M. I. Younus[4]
[1]IBM, Essex Junction, VT
[2]IBM, Rochester, MN
[3]IBM, Bangalore, India
[4]IBM, Hopewell Junction, NY

18.5 7GHz L1 Cache SRAMs for the 32nm zEnterprise™ EC12 Processor **12:00 PM**

J. D. Davis[1], P. A. Bunce[1], D. M. Henderson[1], Y. H. Chan[1], U. Srinivasan[1], D. Rodko[1], P. Patel[1], T. J. Knips[1], T. Werner[2]
[1]IBM, Poughkeepsie, NY
[2]IBM, Boeblingen, Germany

Conclusion **12:15 PM**

Wireless Transceivers for Smart Devices

Session Chair: ***Sven Mattisson,*** *Ericsson, Lund, Sweden*
Associate Chair: ***Koji Takinami,*** *Panasonic, Yokohama, Japan*

19.1 A Fully Integrated 2×2 b/g and 1×2 a-Band MIMO WLAN SoC in 45nm CMOS for Multi-Radio IC **8:30 AM**

R. Kumar[1], T. Krishnaswamy[1], G. Rajendran[1], D. Sahu[1], A. Sivadas[1], M. Nandigam[1], S. Ganeshan[1], S. Datla[1], A. Kudari[1], H. Bhasin[1], M. Agrawal[1], S. Narayan[1], Y. Dharwekar[1], R. Garg[1], V. Edayath[1], T. Suseela[1], V. Jayaram[1], S. Ram[1], V. Murugan[1], A. Kumar[1], S. Mukherjee[1], N. Dixit[1], E. Nussbaum[2], J. Dror[2], N. Ginzburg[2], A. EvenChen[2], A. Maruani[2], S. Sankaran[3]
[1]Texas Instruments, Bangalore, India; [2]Texas Instruments, Ra'anana, Israel
[3]Texas Instruments, Dallas, TX

19.2 A Digitally Modulated 2.4GHz WLAN Transmitter with Integrated Phase Path and Dynamic Load Modulation in 65nm CMOS **9:00 AM**

L. Ye[1], J. Chen[1], L. Kong[1], P. Cathelin[2], E. Alon[1], A. Niknejad[1]
[1]University of California, Berkeley, CA; [2]ST-Ericsson, Grenoble, France

19.3 A 24.7dBm All-Digital RF Transmitter for Multimode Broadband Applications in 40nm CMOS **9:30 AM**

C. Lu[1], H. Wang[1], C. Peng[2], A. Goel[3], S. Son[1], P. Liang[2], A. Niknejad[4], H. Hwang[2], G. Chien[1]
[1]MediaTek, San Jose, CA; [2]MediaTek, Hsinchu, Taiwan
[3]University of Southern California, Los Angeles, CA; [4]University of California, Berkeley, CA

Break **10:00 AM**

19.4 A Universal GNSS (GPS/Galileo/Glonass/Beidou) SoC with a 0.25mm² Radio in 40nm CMOS **10:15 AM**

C. Tan[1], F. Song[1], T. Choke[1], M. Kong[1], D-C. Song[1], C-H. Yong[1], W. Shu[1], Z. You[2], Y-H. Lin[2], O. Shanaa[1]
[1]MediaTek, Singapore, Singapore; [2]MediaTek, Hsinchu, Taiwan

19.5 A Receiver for LTE Rel-11 and Beyond Supporting Non-Contiguous Carrier Aggregation **10:45 AM**

L. Sundström, M. Anderson, R. Strandberg, S. Ek, J. Svensson, F. Mu, T. Olsson, I. ud Din, L. Wilhelmsson, D. Eckerbert, S. Mattisson
Ericsson, Lund, Sweden

19.6 A Multiband 40nm CMOS LTE SAW-Less Modulator with -60dBc C-IM3 **11:15 AM**

M. Ingels[1], Y. Furuta[2], X. Zhang[1], S. Cha[3], J. Craninckx[1]
[1]imec, Leuven, Belgium; [2]Renesas Electronics, Itami, Japan
[3]Renesas Electronics, Takasaki, Japan

19.7 An LTE Transmitter Using a Class-A/B Power Mixer **11:30 AM**

P. Rossi[1], N. Codega[2], D. Gerna[1], A. Liscidini[2,3], D. Ottini[1], Y. He[4], A. Pirola[1], E. Sacchi[1], G. Uehara[5], C. Yang[5,6], R. Castello[2]
[1]Marvell, Pavia, Italy; [2]University of Pavia, Pavia, Italy
[3]*Now at the University of Toronto, Toronto, ON, Canada; [4]Marvell, Aliso Viejo, CA
[5]Marvell, Austin, TX; [6]*Now at Silicon Laboratories, Austin, TX

19.8 A 0.27mm² 13.5dBm 2.4GHz All-Digital Polar Transmitter Using 34%-Efficiency Class-D DPA in 40nm CMOS **11:45 AM**

J-W. Lai[1], C-H. Wang[1], K. Kao[1], A. Lin[1], Y-H. Cho[1], L. Cho[1], M-H. Hung[1], X-Y. Shih[1], C-M. Lin[1], S-H. Yan[1], Y-H. Chung[1], P. Liang[1], G-K. Dehng[1], H-S. Li[1], G. Chien[2], R. B. Staszewski[3]
[1]MediaTek, Hsinchu, Taiwan; [2]MediaTek, San Jose, CA
[3]Delft University of Technology, Delft, The Netherlands

Conclusion **12:00 PM**

Frequency Generation

Session Chair: ***Marc Tiebout,*** *Infineon Technologies, Villach, Austria*
Associate Chair: ***Jing-Hong Conan Zhan,*** *MediaTek, HsinChu, Taiwan*

20.1 A 2.5-to-3.3GHz CMOS Class-D VCO **8:30 AM**

L. Fanori, P. Andreani
Lund University, Lund, Sweden

20.2 Third-Harmonic Injection Technique Applied to a 5.87-to-7.56GHz 65nm CMOS Class-F Oscillator with 192dBc/Hz FOM **9:00 AM**

M. Babaie[1,2], R. B. Staszewski[1]
[1]Delft University of Technology, Delft, The Netherlands
[2]Aktieve Rangschikkings Monolitische Microgolf Onderdelen B.V., Delft, The Netherlands

20.3 A 33.6-to-46.2GHz 32nm CMOS VCO with 177.5dBc/Hz Minimum Noise FOM Using Inductor Splitting for Tuning Extension **9:30 AM**

E. Mammei[1], E. Monaco[2], A. Mazzanti[1], F. Svelto[1]
[1]University of Pavia, Pavia, Italy
[2]STMicroelectronics, Pavia, Italy

Break **10:00 AM**

20.4 A 56.4-to-63.4GHz Spurious-Free All-Digital Fractional-N PLL in 65nm CMOS **10:15 AM**

W. Wu[1], X. Bai[1,2], R. B. Staszewski[1], J. R. Long[1]
[1]Delft University of Technology, Delft, The Netherlands
[2]University of Science and Technology of China, Hefei, China

20.5 A 57.9-to-68.3GHz 24.6mW Frequency Synthesizer with In-Phase Injection-Coupled QVCO in 65nm CMOS **10:45 AM**

X. Yi, C. Boon, H. Liu, J. Lin, J. Ong, W. Lim
Nanyang Technological University, Singapore, Singapore

20.6 A 2.4ps$_{rms\text{-}jitter}$ Digital PLL with Multi-Output Bang-Bang Phase Detector and Phase-Interpolator-Based Fractional-N Divider **11:15 AM**

R. Nonis, W. Grollitsch, T. Santa, D. Cherniak, N. Da Dalt
Infineon Technologies, Villach, Austria

20.7 A 50-to-930MHz Quadrature-Output Fractional-N Frequency Synthesizer with 770-to-1860MHz Single-Inductor LC-VCO and Without Noise Folding Effect for Multistandard DTV Tuners **11:45 AM**

Z. Tang[1], X. Wan[1,2], M. Wang[1,2], J. Liu[1]
[1]Fudan University, Shanghai, China
[2]Ratio Microelectronics, Shanghai, China

Conclusion **12:15 PM**

Power Converters

Session Chair: ***Wing-Hung Ki,*** *HKUST, Hong Kong, Hong Kong*
Associate Chair: ***Marco Berkhout,*** *NXP Semiconductors, Nijmegen, The Netherlands*

21.1 An 82.4% Efficiency Package-Bondwire-Based Four-Phase Fully Integrated Buck Converter with Flying Capacitor for Area Reduction — **8:30 AM**

C. Huang, P. K. T. Mok, HKUST, Hong Kong, China

21.2 An AC-Coupled Hybrid Envelope Modulator for HSUPA Transmitters with 80% Modulator Efficiency — **9:00 AM**

P. Riehl[1], P. Fowers[2], H-P. Hong[3], M. Ashburn[1]
[1]MediaTek, Woburn, MA
[2]MediaTek, West Malling, United Kingdom
[3]MediaTek, Hsinchu, Taiwan

21.3 A CMOS Dual-Switching Power-Supply Modulator with 8% Efficiency Improvement for 20MHz LTE Envelope Tracking RF Power Amplifiers — **9:30 AM**

M. Hassan[1], P. M. Asbeck[1], L. E. Larson[2]
[1]University of California, San Diego, La Jolla, CA
[2]Brown University, Providence, RI

Break — **10:00 AM**

21.4 90.6% Efficient 11MHz 22W LED Driver Using GaN FETs and Burst-Mode Controller with 0.96 Power Factor — **10:15 AM**

S. Bandyopadhyay[1], B. Neidorff[2], D. Freeman[3], A. P. Chandrakasan[1]
[1]Massachusetts Institute of Technology, Cambridge, MA
[2]Texas Instruments, Manchester, NH
[3]Texas Instruments, Dallas, TX

21.5 A Fully Integrated Successive-Approximation Switched-Capacitor DC-DC Converter with 31mV Output Voltage Resolution — **10:45 AM**

S. Bang, A. Wang, B. Giridhar, D. Blaauw, D. Sylvester
University of Michigan, Ann Arbor, MI

21.6 A Sub-ns Response Fully Integrated Battery-Connected Switched-Capacitor Voltage Regulator Delivering 0.19W/mm^2 at 73% Efficiency — **11:15 AM**

H-P. Le, J. Crossley, S. R. Sanders, E. Alon
University of California, Berkeley, CA

21.7 A 93% Efficiency Reconfigurable Switched-Capacitor DC-DC Converter Using On-Chip Ferroelectric Capacitors — **11:45 AM**

D. El-Damak, S. Bandyopadhyay, A. Chandrakasan
Massachusetts Institute of Technology, Cambridge, MA

21.8 A Soft Self-Commutating Method Using Minimum Control Circuitry for Multiple-String LED Drivers — **12:00 PM**

J. Kim, J. Lee, S. Park
Dankook University, Yongin, Korea

Conclusion — **12:15 PM**

Sensors & Displays

Session Chair: ***Aaron Partridge,*** *SiTime, Sunnyvale, CA*
Associate Chair: ***Young-Sun Na,*** *LG Electronics, Seoul, Korea*

22.1 A Fully Differential Charge-Balanced Accelerometer for Electronic Stability Control — **8:30 AM**
V. P. Petkov[1], G. K. Balachandran[1], J. Beintner[2]
[1]Robert Bosch, Palo Alto, CA; [2]Robert Bosch, Reutlingen, Germany

22.2 A 0.25mm² AC-Biased MEMS Microphone Interface with 58dBA SNR — **9:00 AM**
S. Ersoy[1], R. H. van Veldhoven[1], F. Sebastiano[1], K. Reimann[1], K. A. A. Makinwa[2]
[1]NXP Semiconductors, Eindhoven, The Netherlands
[2]Delft University of Technology, Delft, The Netherlands

22.3 A 0.5V <4µW CMOS Photoplethysmographic Heart-Rate Sensor IC Based on a Non-Uniform Quantizer — **9:15 AM**
M. Alhawari[1,2], N. Albelooshi[1], M. H. Perrott[1]
[1]Masdar Institute of Science and Technology, Abu Dhabi, United Arab Emirates
[2*]Now at Khalifa University, Abu Dhabi, United Arab Emirates

22.4 A Micropower Battery Current Sensor with ±0.03% (3σ) Inaccuracy from -40 to +85°C — **9:30 AM**
S. Heidary Shalmany[1], D. Draxelmayr[2], K. A. A. Makinwa[1]
[1]Delft University of Technology, Delft, The Netherlands
[2]Infineon Technologies, Villach, Austria

Break — **10:00 AM**

22.5 A 55dB SNR with 240Hz Frame Scan Rate Mutual Capacitor 30×24 Touch-Screen Panel Read-Out IC Using Code-Division Multiple Sensing Technique — **10:15 AM**
H. Shin[1], S. Ko[1], H. Jang[1], I. Yun[2], K. Lee[1]
[1]KAIST, Daejeon, Korea; [2]Zinitix, Daejeon, Korea

22.6 A Highly Noise-Immune Touch Controller Using Filtered-Delta-Integration and a Charge-Interpolation Technique for 10.1-inch Capacitive Touch-Screen Panels — **10:45 AM**
J-H. Yang[1], S-H. Park[1], J-M. Choi[2], H-S. Kim[1], C-B. Park[1], S-T. Ryu[1], G-H. Cho[1]
[1]KAIST, Daejeon, Korea; [2]Siliconworks, Daejeon, Korea

22.7 A 5.6mV Inter-Channel DVO 10b Column-Driver IC with Mismatch-Free Switched-Capacitor Interpolation for Mobile Active-Matrix LCDs — **11:15 AM**
H-S. Kim, J-H. Yang, S-H. Park, S-T. Ryu, G-H. Cho, KAIST, Daejeon, Korea

22.8 A [10°C ; 70°C] 640×480 17µm Pixel Pitch TEC-Less IR Bolometer Imager with Below 50mK and Below 4V Power Supply — **11:30 AM**
B. Dupont, A. Dupret, S. Becker, A. Hamelin, F. Guellec, P. Imperinetti, W. Rabaud
CEA-LETI-MINATEC, Grenoble, France

22.9 3D Volumetric Ultrasound Imaging with a 32×32 CMUT Array Integrated with Front-End ICs Using Flip-Chip Bonding Technology — **11:45 AM**
A. Bhuyan[1], J. Choe[1], B. Lee[1], I. Wygant[2], A. Nikoozadeh[1], O. Oralkan[3], B. T. Khuri-Yakub[1]
[1]Stanford University, Stanford, CA; [2]Texas Instruments, Santa Clara, CA
[3]North Carolina State University, Raleigh, NC

Conclusion — **12:15 PM**

Short Reach Links, XCVR Techniques, & PLLs

Session Chair: ***Gerrit den Besten,*** *NXP Semiconductors, Eindhoven, The Netherlands*
Associate Chair: ***Koichi Yamaguchi,*** *Renesas Electronics, Kawasaki, Japan*

23.1 A 0.1pJ/b 5-to-10Gb/s Charge-Recycling Stacked Low-Power I/O for On-Chip Signaling in 45nm CMOS SOI **1:30 PM**

Y. Liu[1], P-H. Hsieh[2], S. Kim[1], J-S. Seo[1], R. Montoye[1], L. Chang[1], J. Tierno[3], D. Friedman[1]
[1]IBM T. J. Watson, Yorktown Heights, NY; [2]National Tsing Hua University, Hsinchu, Taiwan
[3]Apple, Cupertino, CA

23.2 A Scalable 0.128-to-1Tb/s 0.8-to-2.6pJ/b 64-Lane Parallel I/O in 32nm CMOS **2:00 PM**

M. Mansuri[1], J. E. Jaussi[1], J. T. Kennedy[1], T-C. Hsueh[1], S. Shekhar[1], G. Balamurugan[1], F. O'Mahony[1], C. Roberts[1], R. Mooney[2], B. Casper[1]
[1]Intel, Hillsboro, OR; [2]Intel, Mapleton, UT

23.3 A 0.54pJ/b 20Gb/s Ground-Referenced Single-Ended Short-Haul Serial Link in 28nm CMOS for Advanced Packaging Applications **2:30 PM**

J. W. Poulton[1], W. J. Dally[2], X. Chen[2], J. G. Eyles[1], T. H. Greer III[1], S. G. Tell[1], C. T. Gray[1]
Nvidia, Durham, NC; [2]Nvidia, Santa Clara, CA

Break **3:00 PM**

23.4 A 5.5Gb/s 5mm Contactless Interface Containing a 50Mb/s Bidirectional Sub-Channel Employing Common-Mode OOK Signaling **3:15 PM** **DS2**

K. Hijioka, M. Matsudaira, K. Yamaguchi, M. Mizuno,
Renesas Electronics, Kawasaki, Japan

23.5 An 8Gb/s 1.5mW/Gb/s 8-Tap 6b NRZ/PAM-4 Tomlinson-Harashima Precoding Transmitter for Future Memory-Link Applications in 22nm CMOS **3:45 PM**

M. A. Kossel, T. Toifl, P. A. Francese, M. Brändli, C. Menolfi, P. Buchmann, L. Kull, T. Meyer Andersen, T. Morf
IBM, Rüschlikon, Switzerland

23.6 An 8Gb/s 0.65mW/Gb/s Forwarded-Clock Receiver Using an ILO with Dual Feedback Loop and Quadrature Injection Scheme **4:15 PM**

J-H. Seol[1], Y-J. Kim[1], S-H. Chung[1], K-S. Ha[2], S-J. Bae[2], J-B. Lee[2], J. Choi[2], L-S. Kim[1]
[1]KAIST, Daejeon, Korea; [2]Samsung Electronics, Hwasung, Korea

23.7 A 3.1mW Phase-Tunable Quadrature-Generation Method for CEI 28G Short-Reach CDR in 28nm CMOS **4:30 PM**

K. Bhardwaj[1], S. Narayan[2], S. Shumarayev[3], T. Lee[1]
[1]Stanford University, Stanford, CA; [2]Inphi, Santa Clara, CA; [3]Altera, San Jose, CA

23.8 A Divider-Less Sub-Harmonically Injection-Locked PLL with Self-Adjusted Injection Timing **4:45 PM**

I-T. Lee[1], Y-J. Chen[2], S-I. Liu[1], C-P. Jou[2], F-L. Hsueh[2], H-H. Hsieh[2]
[1]National Taiwan University, Taipei, Taiwan; [2]TSMC, Hsinchu, Taiwan

23.9 A Wideband Fractional-N Ring PLL with Fractional-Spur Suppression Using Spectrally Shaped Segmentation **5:00 PM**

T-K. Kao[1], C-F. Liang[1], H-H. Chiu[1], M. Ashburn[2]
[1]MediaTek, Hsinchu, Taiwan; [2]MediaTek, Woburn, MA

Conclusion **5:15 PM**

Energy-Aware Digital Design

Session Chair: ***Wim Dehaene,*** *KU Leuven, Leuven, Belgium*
Associate Chair: ***Masaya Sumita,*** *Panasonic, Nagaokakyo, Japan*

24.1 A 10.4pJ/b (32, 8) LDPC Decoder with Time-Domain Analog and Digital Mixed-Signal Processing **1:30 PM**
D. Miyashita[1], R. Yamaki[2], K. Hashiyoshi[3], H. Kobayashi[1], S. Kousai[1], Y. Oowaki[1], Y. Unekawa[1]
[1]Toshiba, Kawasaki, Japan,[2]Toshiba, Yokohama, Japan
[3]Toshiba Microelectoronics, Kawasaki, Japan

24.2 A 1.15Gb/s Fully Parallel Nonbinary LDPC Decoder with Fine-Grained Dynamic Clock Gating **2:00 PM**
Y. Park, Y. Tao, Z. Zhang, University of Michigan, Ann Arbor, MI

24.3 Ultra-Wide Body-Bias Range LDPC Decoder in 28nm UTBB FDSOI Technology **2:30 PM**
P. Flatresse[1], B. Giraud[2], J-P. Noel[1], B. Pelloux-Prayer[1], F. Giner[1], D-K. Arora[3], F. Arnaud[1], N. Planes[1], J. Le Coz[1], O. Thomas[2], S. Engels[1], G. Cesana[1], R. Wilson[1], P. Urard[1]
[1]STMicroelectronics, Crolles, France, [2]CEA-LETI-MINATEC, Grenoble, France
[3]STMicroelectronics, Greater Noida, India

24.4 Self-Super-Cutoff Power Gating with State Retention on a 0.3V 0.29fJ/Cycle/Gate 32b RISC Core in 0.13µm CMOS **2:45 PM**
J-S. Chen, C. Yeh, J-S. Wang, National Chung Cheng University, Chaiyi, Taiwan

Break **3:00 PM**

24.5 A Low-Power 1GHz Razor FIR Accelerator with Time-Borrow Tracking Pipeline and Approximate Error Correction in 65nm CMOS **3:15 PM**
P. N. Whatmough, S. Das, D. M. Bull, ARM, Cambridge, United Kingdom

24.6 Reliable and Energy-Efficient 1MHz 0.4V Dynamically Reconfigurable SoC for ExG Applications in 40nm LP CMOS **3:45 PM**
M. Konijnenburg[1], Y. Cho[2], M. Ashouei[1], T. Gemmeke[1], C. Kim[2], J. Hulzink[1], J. Stuyt[1], M. Jung[2], J. Huisken[1], S. Ryu[2], J. Kim[2], H. de Groot[1]
[1]imec - Holst Centre, Eindhoven, The Netherlands
[2]Samsung Advanced Institute of Technology, Seoul, Korea
DS2

24.7 An 8MHz 75µA/MHz Zero-Leakage Non-Volatile Logic-Based Cortex-M0 MCU SoC Exhibiting 100% Digital State Retention at V_{DD}=0V with <400ns Wakeup and Sleep Transitions **4:15 PM**
DS2
S. C. Bartling, S. Khanna, M. P. Clinton, S. R. Summerfelt, J. A. Rodriguez, H. P. McAdams
Texas Instruments, Dallas, TX

24.8 A 100GB/s Wide I/O with 4096b TSVs Through an Active Silicon Interposer with In-Place Waveform Capturing **4:45 PM**
S. Takaya[1], M. Nagata[1], A. Sakai[2], T. Kariya[2], S. Uchiyama[2], H. Kobayashi[2], H. Ikeda[2]
[1]Kobe University, Kobe, Japan
[2]Association of Super-Advanced Electronics Technologies, Tokyo, Japan
DS2

24.9 Intermittent Resonant Clocking Enabling Power Reduction at any Clock Frequency for 0.37V 980kHz Near-Threshold Logic Circuits **5:00 PM**
H. Fuketa[1], M. Nomura[2], M. Takamiya[1], T. Sakurai[1]
[1]University of Tokyo, Tokyo, Japan
[2]Semiconductor Technology Academic Research Center, Yokohama, Japan

Conclusion **5:15 PM**

Energy-Efficient Wireless

Session Chair: ***Shouhei Kousai,*** *Toshiba, Kawasaki, Japan*
Associate Chair: ***Gangadhar Burra,*** *Texas Instruments, Plano, TX*

25.1 A 45nm CMOS Near-Field Communication Radio with 0.15A/m RX Sensitivity and 4mA Current Consumption in Card Emulation Mode — 1:30 PM

Y. Darwhekar[1], E. Braginskiy[2], K. Levy[2], A. Agrawal[1], V. Singh[1], R. Issac[2], O. Blonskey[2], O. Adler[2], Y. Benkuzari[2], M. Ben-Shachar[2], S. Manian[1], A. Sivadas[1], S. Mukherjee[1], G. Burra[3], N. Tal[2], Y. Shlivinski[2], G. Bitton[2]
[1]Texas Instruments, Bangalore, India; [2]Texas Instruments, Ra'anana, Israel
[3]Texas Instruments, Dallas, TX

25.2 An Ultra-Low-Power 9.8GHz Crystal-Less UWB Transceiver with Digital Baseband Integrated in 0.18µm BiCMOS — 2:00 PM

J. K. Brown[1], K-K. Huang[2], E. Ansari[2], R. R. Rogel[2], Y. Lee[2], D. D. Wentzloff[2]
[1]Cavium, Marlborough, MA; [2]University of Michigan, Ann Arbor, MI

25.3 A Self-Duty-Cycled and Synchronized UWB Receiver SoC Consuming 375pJ/b for -76.5dBm Sensitivity at 2Mb/s — 2:30 PM

B. Vigraham, P. Kinget, Columbia University, New York, NY

25.4 A 1.9nJ/b 2.4GHz Multistandard (Bluetooth Low Energy/Zigbee/IEEE802.15.6) Transceiver for Personal/Body-Area Networks — 2:45 PM — DS2

Y-H. Liu[1], X. Huang[1], M. Vidojkovic[1], A. Ba[1], P. Harpe[2], G. Dolmans[1], H. de Groot[1]
[1]imec - Holst Centre, Eindhoven, The Netherlands
[2]Eindhoven University of Technology, Eindhoven, The Netherlands

Break 3:00 PM

25.5 A 1.7mW 0.22mm² 2.4GHz ZigBee RX Exploiting a Current-Reuse Blixer + Hybrid Filter Topology in 65nm CMOS — 3:15 PM

Z. Lin[1], P-I. Mak[1], R. Martins[1,2]
[1]University of Macau, Macau, China; [2]Instituto Superior Tecnico, Lisbon, Portugal

25.6 A 110pJ/b Multichannel FSK/GMSK/QPSK/π/4-DQPSK Transmitter with Phase-Interpolated Dual-Injection DLL-Based Synthesizer Employing Hybrid FIR — 3:30 PM

S-J. Cheng[1], Y. Gao[1], W-D. Toh[1], Y. Zheng[2], M. Je[1,3], C-H. Heng[3]
[1]Institute of Microelectronics, Singapore, Singapore
[2]Nanyang Technological University, Singapore, Singapore
[3]National University of Singapore, Singapore, Singapore

25.7 A 5.5mW IEEE-802.15.6 Wireless Body-Area-Network Standard Transceiver for Multichannel Electro-Acupuncture Application — 3:45 PM — DS2

H. Lee, K. Lee, S. Hong, K. Song, T. Roh, J. Bae, H-J. Yoo, KAIST, Daejeon, Korea

25.8 Wideband UHF ISM-Band Transceiver Supporting Multichannel Reception and DSSS Modulation — 4:15 PM

J. van Sinderen[1], G. W. de Jong[1], F. Leong[1], X. He[1], M. Apostolidou[1], H. Kundur Subramaniyan[1], R. Rutten[1], J. Niehof[1], J. Verlinden[1], H. Wang[1], A. Hoogstraate[1], K. Kwok[1], R. Verlinden[1], R. Hoogendoorn[1], D. Jeurissen[2], A. Salfelner[2], E. Bergler[2], J. M. Velandia Torres[2], C. J. Haji-Michael[2], T. Unterweger[2], E. Tarvainen[2], M. Posch[2], R. Schmidt[2], M. Stattmann[2], J. Tyminski[2], P. Jean[3], S. Darfeuille[3], O. Aymard[3], A. le Grontec[3], C. Boucey[3], C. Kelma[3], G. Monnerie[3]
[1]NXP Semiconductors, Eindhoven, The Netherlands; [2]NXP Semiconductors, Gratkorn, Austria
[3]NXP Semiconductors, Caen, France

25.9 A 1.6mW 300mV-Supply 2.4GHz Receiver with -94dBm Sensitivity for Energy-Harvesting Applications — 4:45 PM

F. Zhang[1], K. Wang[1], J. Koo[1], Y. Miyahara[2], B. Otis[1]
[1]University of Washington, Seattle, WA; [2]Panasonic, Yokohama, Japan

25.10 A Super-Regenerative Radio on Plastic Based on Thin-Film Transistors and Antennas on Large Flexible Sheets for Distributed Communication Links — 5:15 PM

L. Huang, W. Rieutort-Louis, Y. Hu, J. Sanz-Robinson, S. Wagner, J. C. Sturm, N. Verma
Princeton University, Princeton, NJ

Conclusion 5:30 PM

High-Speed Data Converters

Session Chair: ***Boris Murmann,*** *Stanford University, Stanford, CA*
Associate Chair: ***Tetsuya Iizuka,*** *University of Tokyo, Tokyo, Japan*

26.1 A 10.3GS/s 6b Flash ADC for 10G Ethernet Applications — 1:30 PM

S. Verma, A. Kasapi, L-M. Lee, D. Liu, D. Loizos, S-H. Paik, A. Varzaghani, S. Zogopoulos, S. Sidiropoulos
Broadcom, Santa Clara, CA

DS2

26.2 An 11b 3.6GS/s Time-Interleaved SAR ADC in 65nm CMOS — 2:00 PM

E. Janssen[1], K. Doris[1], A. Zanikopoulos[1], A. Murroni[1], G. van der Weide[1], Y. Lin[1], L. Alvado[2], F. Darthenay[2], Y. Fregeais[2]
[1]NXP Semiconductors, Eindhoven, The Netherlands
[2]NXP Semiconductors, Caen, France

26.3 A 14b 2.5GS/s 8-Way-Interleaved Pipelined ADC with Background Calibration and Digital Dynamic Linearity Correction — 2:30 PM

B. Setterberg[1], K. Poulton[1], S. Ray[1], D. J. Huber[1], V. Abramzon[1], G. Steinbach[1], J. P. Keane[1], B. Wuppermann[1], M. Clayson[1], M. Martin[2], R. Pasha[2], E. Peeters[3], A. Jacobs[3], F. Demarsin[3], A. Al-Adnani[3], P. Brandt[3]
[1]Agilent Technologies, Santa Clara, CA
[2]Agilent Technologies, Colorado Springs, CO
[3]Agilent Technologies, Rotselaar, Belgium

Break — 3:00 PM

26.4 A 3.1mW 8b 1.2GS/s Single-Channel Asynchronous SAR ADC with Alternate Comparators for Enhanced Speed in 32nm Digital SOI CMOS — 3:15 PM

L. Kull[1,2], T. Toifl[1], M. Schmatz[1], P. A. Francese[1], C. Menolfi[1], M. Braendli[1], M. Kossel[1], T. Morf[1], T. Meyer Andersen[1], Y. Leblebici[2]
[1]IBM Research, Rüschlikon, Switzerland
[2]EPFL, Lausanne, Switzerland

26.5 An 8.6 ENOB 900MS/s Time-Interleaved 2b/cycle SAR ADC with a 1b/cycle Reconfiguration for Resolution Enhancement — 3:45 PM

H-K. Hong[1], H-W. Kang[1], B. Sung[1], C-H. Lee[2], M. Choi[2], H-J. Park[2], S-T. Ryu[1]
[1]KAIST, Daejeon, Korea
[2]Samsung Electronics, Yongin, Korea

26.6 A 14b 80MS/s SAR ADC with 73.6dB SNDR in 65nm CMOS — 4:15 PM

R. Kapusta[1], J. Shen[1], S. Decker[1], H. Li[2], E. Ibaragi[2]
[1]Analog Devices, Wilmington, MA
[2]Analog Devices, Tokyo, Japan

26.7 A 12b 1.6GS/s 40mW DAC in 40nm CMOS with >70dB SFDR over Entire Nyquist Bandwidth — 4:45 PM

W-T. Lin, T-H. Kuo
National Cheng Kung University, Tainan, Taiwan

Conclusion — 5:15 PM

Image Sensors

Session Chair: ***Robert Johansson,*** *OmniVision Technologies, Oslo, Norway*
Associate Chair: ***Shoji Kawahito,*** *Shizuoka University, Hamamatsu, Japan*

27.1 A 3.4μW CMOS Image Sensor with Embedded Feature-Extraction Algorithm for Motion-Triggered Object-of-Interest Imaging — 1:30 PM

J. Choi, S. Park, J. Cho, E. Yoon, University of Michigan, Ann Arbor, MI

27.2 A 467nW CMOS Visual Motion Sensor with Temporal Averaging and Pixel Aggregation — 2:00 PM

G. Kim, M. Barangi, Z. Foo, N. Pinckney, S. Bang, D. Blaauw, D. Sylvester
University of Michigan, Ann Arbor, MI

27.3 A Rolling-Shutter Distortion-Free 3D Stacked Image Sensor with -160dB Parasitic Light Sensitivity In-Pixel Storage Node — 2:30 PM

J. Aoki, Y. Takemoto, K. Kobayashi, N. Sakaguchi, M. Tsukimura, N. Takazawa, H. Kato, T. Kondo, H. Saito, Y. Gomi, Y. Tadaki
Olympus, Hachioji, Japan

27.4 A 1/4-inch 8Mpixel Back-Illuminated Stacked CMOS Image Sensor — 2:45 PM

S. Sukegawa[1], T. Umebayashi[1], T. Nakajima[1], H. Kawanobe[1], K. Koseki[2], I. Hirota[1], T. Haruta[1], M. Kasai[1], K. Fukumoto[1], T. Wakano[1], K. Inoue[3], H. Takahashi[1], T. Nagano[1], Y. Nitta[1], T. Hirayama[1], N. Fukushima[1]
[1]Sony, Atsugi, Japan; [2]Sony LSI Design, Atsugi, Japan
[3]Sony Semiconductor, Kumamoto, Japan

Break — 3:00 PM

27.5 An 8×16-pixel 92kSPAD Time-Resolved Sensor with On-Pixel 64ps 12b TDC and 100MS/s Real-Time Energy Histogramming in 0.13μm CIS Technology for PET/MRI Applications — 3:15 PM

L. H. Braga[1], L. Gasparini[1], L. Grant[2], R. K. Henderson[3], N. Massari[1], M. Perenzoni[1], D. Stoppa[1], R. Walker[3]
[1]Fondazione Bruno Kessler, Trento, Italy
[2]STMicroelectronics, Edinburgh, United Kingdom
[3]University of Edinburgh, Edinburgh, United Kingdom

27.6 A 0.18μm CMOS SoC for a 100m-Range 10fps 200×96-Pixel Time-of-Flight Depth Sensor — 3:45 PM

C. Niclass, M. Soga, H. Matsubara, M. Ogawa, M. Kagami
Toyota Central R&D Labs, Nagakute, Japan

27.7 3D Camera Based on Linear-Mode Gain-Modulated Avalanche Photodiodes DS2 — 4:15 PM

O. Shcherbakova[1,2], L. Pancheri[1], G-F. Dalla Betta[1], N. Massari[2], D. Stoppa[2]
[1]University of Trento, Trento, Italy. [2]Fondazione Bruno Kessler, Trento, Italy

27.8 A 3D Vision 2.1Mpixel Image Sensor for Single-Lens Camera Systems — 4:45 PM

S. Koyama, K. Onozawa, K. Tanaka, Y. Kato, Panasonic, Nagaokakyo, Japan

27.9 A 187.5μV_{rms}-Read-Noise 51mW 1.4Mpixel CMOS Image Sensor with PMOSCAP Column CDS and 10b Self-Differential Offset-Cancelled Pipeline SAR-ADC — 5:00 PM

J. Deguchi[1], F. Tachibana[1], M. Morimoto[1], M. Chiba[1], T. Miyaba[2], H. Tanaka[1], K. Takenaka[2], S. Funayama[1], K. Amano[1], K. Sugiura[1], R. Okamoto[1], S. Kousai[1]
[1]Toshiba, Kawasaki, Japan; [2]Toshiba Microelectronics, Kawasaki, Japan

Conclusion — 5:15 PM

RF Blocks for Wireless Transceivers

Organizer: **Willy Sansen,** *K.U. Leuven, Leuven, Belgium*

Instructors: **Hooman Darabi,** *Broadcom, Irvine, CA*
John Long, *Delft University of Technbologies, The Netherlands*
Ali Hajimiri, *Caltech, CA*
Ali Niknejad, *UC Berkeley, CA*

IC's for Communications

Hooman Darabi, *Broadcom, Irvine, CA*

In this presentation we offer architectural considerations of both receivers and transmitters for advanced mobile and wireless applications. An overview of RF standards, along with system level analysis of various architectures, is presented. The key radio requirements are derived and translated to circuit specifications, followed by a detailed discussion of different schemes and their pros and cons. General system level concerns for integrated transceivers, particularly in CMOS, such as linearity, frequency planning, blockers and spurious mixing are introduced and appropriate architecture level solutions are presented and discussed in detail.

Speaker Biography: Hooman Darabi received the BS and MS degrees both in Electrical Engineering from Sharif University of Technology, Tehran in 1994, and 1996 respectively. He received the Ph.D. degree in electrical engineering from the University of California, Los Angeles, in 1999. He is currently a Senior Technical Director , and a Fellow, with Broadcom Corporation, Irvine, CA, within the RF group in the Mobile and Wireless Business Unit. He is also an adjunct professor with the UCI EECS department. His interests include analog and RF IC design for wireless communications. Hooman holds over 200 issued or pending patents with Broadcom, and has published over 50 peer reviewed or conference papers. He is an IEEE distinguished lecturer.

Design of Building Blocks for the RF Transceiver Front-End

John Long, *Delft University of Technologies, Delft, The Netherlands*

The design of an RF front-end from specification to transistor-level circuit is outlined in this lecture. Circuits include: low-noise amplifiers (LNAs), up- and down-conversion mixers, voltage-controlled and digitally controlled oscillators (VCOs and DCOs), LO and power amplifier buffers. Integration of these sub-blocks into I/Q up- and down-converters using submicron CMOS technology (e.g., 65nm) is assumed. Packaging effects, supply isolation, and circuit layout for optimum RF performance and reliability are also considered.

Speaker Biography: John R. Long received the B.Sc.-E.E. from the University of Calgary in 1984, and the M. Eng. and Ph.D. degrees in Electronics Engineering from Carleton University in 1992 and 1996, respectively, all with distinction. He was employed for 10 years by Bell-Northern Research Ltd., Ottawa, Canada designing GaAs ASICs for Gb/s fibre-optic transmission systems. Professor Long is currently chair of the Electronics Research Laboratory at the Delft University of Technology in the Netherlands. His current research interests include: low-power transceiver circuitry for highly-integrated radio applications, and electronics design for high-speed data communications systems

High-Frequency CMOS Power Generation and Phased-Array Transmitters

Ali Hajimiri, *Caltech, CA*

Over the last decade, silicon integrated circuits have come a long way in power generation despite their diminishing voltage-handling capability. This is primarily due to innovations in circuit topologies and architectures. In this lecture, we will discuss some of the underlying principles enabling power generation at high frequencies in silicon, such as parallelism, stacking, active -EM integration, periodic structures, and self healing. These concepts will be demonstrated and explored in phased-array transmitters and high-frequency power amplifiers with an emphasis on innovative architectures for beam control, signal generation, and efficient radiation through several practical and illustrative examples.

Speaker Biography: Ali Hajimiri received his Ph.D. degrees in Electrical Engineering from Stanford University. He is Thomas G. Myers Professor of Electrical Engineering and director of the Microelectronics Laboratory at the California Institute of Technology. Prior to joining Caltech he worked for Philips Semiconductors, Sun Microsystems, and Lucent Technologies (Bell Labs). He holds more than 50 patents and was selected to the TR35 top innovator's list. He has graduated more than twenty Ph.D. students, many of whom hold top leadership positions in academia and industry. He and his students have won several best paper and other awards. He co-founded Axiom Microdevices Inc. that produced and shipped the first commercially viable fully-integrated CMOS PA for cellular handsets.

mm-Wave Phased-Array Receivers

Ali Niknejad, *UC Berkeley, Berkeley, CA*

Abstract: A phased-array receiver offers many advantages, such as a lower effective noise factor, beam steering, beam nulling, and better immunity to interference and multi-path due to spatial gain. However, the design of a phased-array at mm-wave frequencies presents a unique set of challenges related to the phase shifters. Basic architectures for the phased array will be compared (RF, LO, IF) in terms of noise, linearity and power consumption. Circuit realizations of active and passive phase shifters will be presented, followed by some design examples from CMOS and SiGe prototypes.

Speaker Biography: Ali M. Niknejad is a professor in the EECS department at UC Berkeley and co-director of the Berkeley Wireless Research Center and the BSIM Research Group. His research interests lie within the area of wireless and broadband communications and biomedical imaging (RF, mm-wave, and sub-THz), including the implementation of integrated communication systems in silicon using CMOS, SiGe, and BiCMOS processes. The focus areas of his research include analog, RF, mixed-signal, mm-wave circuits, device physics and compact modeling, and numerical techniques in electromagnetics.

F3: Emerging Technologies for Wireline Communication

Organizer: **Elad Alon,** *University of California, Berkeley, Berkeley, CA*
Chair: **Azita Emami,** *California Institute of Technology, Pasadena, CA*

Committee: **Gerritt den Besten,** *NXP Semiconductors, City, The Netherlands*
Ichiro Fujimori, *Broadcom, Irvine, CA*
Tadahiro Kuroda, *Keio University, Yokohama, Japan*
Masafumi Nogawa, *NTT, Atsugi,* Japan
Hisakatsu Yamaguchi, *Fujitsu, Kawasaki, Japan*

Future systems will be shaped by advanced interconnects enabled by emerging wireline communications technologies. Thus, the objective of this Forum is to present an overview of the opportunities, challenges, and solutions associated with emerging optical as well as electrical communication technologies. The Forum begins with a talk describing design considerations for integrated Power Over Ethernet. The next three presentations focus on emerging optical-link technologies, beginning with a talk describing the key enablers for next-generation optical access systems. The next talk highlights the design and impact on future networks of coherent-optical transceivers, followed by a presentation describing the integration of silicon-photonic devices into state-of-the-art CMOS technologies with minimal process changes. The next two talks focus on advanced electrical links, including an exploration of power-efficient equalization, as well as examination of multiple modulation formats (NRZ and PAM4) for new 100Gb/s backplane standards. The final two talks of the Forum highlight the bandwidth-density opportunities offered by 2.5/3D integration technologies, describing how wireline circuit techniques enable substantial performance improvements in both inductivecoupling, as well as TSV-based through- and across-chip interfaces.

Agenda

Time	Topic
08:00	Breakfast
08:20	**Introduction** **Azita Emami,** *California Institute of Technology, Pasadena, CA*
08:30	**Integrated Power Over Ethernet ICs – Challenges and Solutions** **Stefan Van Roeyen,** *Broadcom, Eke, Belgium*
09:20	**Recent Progress in Next-Generation Optical-Access Systems and Optical-Transceiver Technologies** **Junichi Nakagawa,** *Mitsubishi Electric, Amagasaki, Japan*
10:10	Break
10:35	**Coherent Optical Transceivers: Design and Impact on Future Optical Networks** **Oscar Agazzi,** *ClariPhy Communications, Irvine, CA*
11:25	**Monolithic Electronic-Photonic Integration for Chip-to-Chip Interconnect** **Jason Orcutt,** *Massachusetts Institute of Technology, Cambridge, MA*
12:15	Lunch
13:20	**Power-Reduction Techniques and Tradeoffs for Advanced Equalization** **Chih-Kong Ken Yang,** *University of California, Los Angeles, CA*
14:10	**Signaling at 100Gb/s: Evolution of the 100Gb Backplane Standard** **Vasudevan Parthasarathy,** *Broadcom, Irvine, CA*
15:00	Break
15:20	**ThruChip Interface for 3D ICs** **Noriyuki Miura,** *Keio University, Yokohama, Japan*
16:10	**Compact Low-Power 2.5D and 3D I/O Technologies** **Yong Liu**, *IBM, Yorktown Heights, NY*
17:00	Closing Remarks (Chair)

F4: Scientific Imaging

Organizer/Chair: **Makoto Ikeda,** *University of Tokyo, Tokyo, Japan*

Committee: **Ehsan Afshari,** *Cornell University, Ithaca, NY*
Yusuke Oike, *Sony, Atsugi, Japan*
David Ruffieux, *CSEM, Neuchatel, Switzerland*
Johannes Solhusvik, *Omnivision, Oslo, Norway*
Albert Theuwissen, *Harvest Imaging, Bree, Belgium, Delft University of Technology, Delft, The Netherlands*

Imaging techniques open new vistas for various scientific fields: These include observation of: ultra-high-speed events, very dark signals under a couple of photons, signals with a frequency range outside that of visible light (such as X-ray, Infrared, and THz). The objective of this Forum is to present applications and circuit details of system and sensor device techniques which underpin or realize these scientific imaging techniques. This will start with an overview of scientific imaging over a broad wavelength range, followed by a discussion of associated CMOS-based sensor devices and circuits for multi-spectral imaging. The next two talks will cover ultra-high-speed imaging up to 20Mfps, and ultra-high-sensitivity imaging by SPAD. There follow two talks covering IR-imaging and readout circuittry, one uncooled , and the other under ultra-low temperature conditions for astronomy. The final three talks will highlight THz imaging, including an overview, system aspects, and CMOS realization.

Agenda

Time	Topic
08:00	Breakfast
08:30	**Introduction** **Makoto Ikeda,** *University of Tokyo, Tokyo, Japan*
08:35	**Overview of Scientific Imaging in the Frequency Range from X-Rays to Terahertz** **Valérie Nguyen,** *CEA Leti MINATEC, Grenoble, France*
09:20	**Multispectral Imaging: When CMOS Does the Trick!** **Matteo Perenzoni,** *Fondazione Bruno Kessler, Torento, Italy*
10:05	Break
10:30	**Ultra-High-Speed Imaging** **Shigetoshi Sugawa,** *Tohoku University, Sendai, Japan*
11:15	**Single-Photon Imaging with SPADs** **Robert Henderson,** *University of Edinburgh, Edinburgh, United Kingdom*
12:00	Lunch
13:00	**State-of-the-Art in Uncooled IR Sensors and Readout Circuitry** **Patrick Robert,** *ULIS, Veurey-Voroize, France*
13:45	**High-Sensitivity Astronomical-Imaging Arrays with Cryogenic Electronics for Terahertz Waves** **Hiroshi Matsuo,** *National Observatory of Japan, Tokyo, Japan*
14:30	Break
14:50	**THz Imaging: What You See and What You Don't!** **Peter H. Siegel,** *Caltech/JPL, Pasedena, CA*
15:35	**Advanced Microwave Imaging Based on Modern Semiconductor Technologies** **Sherif-Sayed Ahmed,** *Rohde & Schwarz, Munich, Germany*
16:20	**THz CMOS Image Sensors Using Schottky Barrier Diodes for Lensless Portable Applications** **Kenneth O,** *University of Texas at Dallas, Dallas, TX*
17:05	Closing Remarks (Chair)

F5: Frequency Generation and Clock Distribution

Organizer: **Antonio Liscidini,** *University of Toronto, Toronto, Canada*

Committee: **SeongHwan Cho,** *KAIST, Daejeon, Korea*
Tony Chan Carusone, *University of Toronto, Toronto, Canada*
Tanay Karnik, *Intel, Hillsboro, OR*
Mike Keaveney, *Analog Devices, Limerick, Ireland*
Brian Otis, *University of Washington, Seattle, WA*
Aaron Partridge, *SiTime, Sunnyvale, CA*
Christoph Sandner, *Infineon Technologies, Villach, Austria*

This Forum explores the primary challenges in the generation and distribution of frequency-reference signals in modern integrated circuits (analog and digital). Based on a bottom-up approach, the Forum begins with an overview of the building blocks used for frequency generation and distribution. It continues by discussing particular challenges presented by the design of frequency synthesizers and their interaction with the rest of the system. The first three talks provide insights into the design of frequency generators: harmonic oscillators, ring oscillators, and MEMS topologies. The fourth presentation deals with various single- and dual-modulus divider topologies necessary for wireless or wireline applications. Then, frequency synthesizers for millimeter-wave wireless communications and PLLs for wireline applications are presented. The last two talks give an overview of the main challenges in clock distribution for both microprocessors and RF analog transceivers. The Forum concludes with a brief panel discussion, providing an opportunity for participants to give feedback and ask questions.

Agenda

Time	Topic
08:00	Breakfast
08:20	**Introduction** **Antonio Liscidini,** *University of Toronto, Toronto, Canada*
08:30	**Integrated Harmonic Voltage-Controlled Oscillators** **Pietro Andreani,** *University of Lund, Lund, Sweden*
09:20	**Fully-Integrated Frequency References in CMOS** **Fabio Sebastiano,** *NXP, Eindhoven, The Netherlands*
10:10	Break
10:35	**High-Frequency Piezoelectric MEMS Oscillators** **Gianluca Piazza,** *Carnegie Mellon University, Pittsburgh, PA*
11:25	**High-Performance Frequency Dividers** **Behzad Razavi,** *University of California, Los Angeles, CA*
12:15	Lunch
13:20	**Insights into Frequency Synthesizers for millimeter-Wave Wireless Communications** **Enrico Temporiti,** *ST Microelectronics, Pavia, Italy*
14:10	**Design and Implementation of Low-Power and Small-Size PLLs for SoC Applications including Wirelines** **Jaejin Park,** *Samsung, Giheung, South Korea*
15:00	Break
15:20	**Microprocessor Clocking Architectures** **Kurd Nasser,** *Intel, Hillsboro, OR*
16:10	**LO Distribution Techniques to Prevent LO Pulling and RX Sensitivity Degradation in Highly-Integrated Wireless Transceivers** ***Jinho Park,*** *Marvell Semiconductors, Santa Clara, CA*
17:00	Panel Discussion
17:20	Closing Remarks (Chair)

F6: Mixed-Signal/RF Design and Modeling in Next-Generation CMOS

Organizer/Chair: **Boris Murmann,** *Stanford University, Stanford, CA*

Committee: **Jafar Savoj,** *Xilinx, San Jose, CA*
Piet Wambacq, imec*, Heverlee, Belgium*
Jieh-Tsorng Wu, *National Chiao-Tung University, Hsinchu, Taiwan*

Technology awareness and modeling is important in all areas of mixed-signal and RF design. This Forum intends to provide, for next-generation CMOS, a holistic overview and discussion spanning a variety of important aspects of device modeling, reliability, and simulation. It begins with an analog/RF-centric comparison between FinFET and ultra-thin-body SOI technology. The next two talks then venture into bias stress and Electrostatic Discharge Protection (ESD), which are two issues of ever-increasing importance for future scaling. The fourth presentation discusses the latest developments surrounding the popular BSIM transistor model, and explains how this new model can be efficiently coupled to the analog/RF design process. Motivated by their increasing significance in integrated RF transceivers, the next talk outlines a future roadmap for passive components in scaled technologies. Then, we expand upon modeling challenges that arise when components are stacked in three dimensions. Finally, this series of modeling talks is rounded up by two comprehensive presentations that summarize key challenges from the foundry and EDA-tool-vendor perspectives.

Agenda

Time	Topic
08:00	Breakfast
08:20	**Introduction** **Boris Murmann,** *Stanford University, Stanford, CA*
08:30	**FinFET versus UTBB SOI for RF/Analog Applications** **Tsu-Jae King Liu,** *University of California, Berkeley, CA*
09:20	**Reliability Modeling for nm-Scale Components** **Praveen Raghavan,** *imec, Heverlee, Belgium*
10:10	Break
10:35	**ESD-Protection Design in Nanometer CMOS** **Ming-Dou Ker,** *National Chiao-Tung University, Hsinchu, Taiwan*
11:25	**The BSIM6 MOSFET Compact Model and Its Use for Analog and RF Design** **Christian Enz,** *CSEM, Neuchâtel, Switzerland*
12:15	Lunch
13:20	**Development of Passives in Advanced CMOS: A Key Enabler for RF Applications up to mm-Wave** **Frédéric Gianesello,** *STMicroelectronics, Crolles, France*
14:10	**3D Stacking, the Best of Both Worlds: Modeling Issues in an Optimized Heterogeneous (Analog/Digital) Stacked Design** **Liam Madden,** *Xilinx, San Jose, CA*
15:00	Break
15:20	**Foundry Perspectives on Analog/RF Challenges in Next-Generation CMOS** **Sally Liu,** *TSMC, Hsinchu, Taiwan*
16:10	**Next-Generation Analog/RF EDA Tools** **Li-Da Huang,** *Synopsys, Austin, TX*
17:00	Closing Remarks (Chair)

COMMITTEES

EXECUTIVE COMMITTEE

CONFERENCE CHAIR
Anantha Chandrakasan, *Massachusetts Institute of Technology, Cambridge, MA*

SECRETARY, FORUMS AND DATA TEAM
Siva Narendra, *Tyfone, Portland, OR*

DIRECTOR OF FINANCE AND BOOK DISPLAY COORDINATOR
Bryant Griffin, *Penfield, NY*

PROGRAM CHAIR
Bram Nauta, *University of Twente, Enschede, The Netherlands*

PROGRAM VICE CHAIR
Trudy Stetzler, *Texas Instruments, Stafford, TX*

STUDENT RESEARCH CHAIR AND UNIVERSITY RECEPTIONS
Jan van der Spiegel, *University of Pennsylvania, Philadelphia, PA*

DEMONSTRATION SESSION CHAIR
Bill Bowhill, *Intel, Hudson, MA*

DEMONSTRATION SESSION CO-CHAIR
Chris van Hoof, *imec, Leuven, Belgium*

ITPC FAR EAST REGIONAL CHAIR
Makoto Ikeda, *University of Tokyo, Tokyo, Japan*

ITPC FAR EAST REGIONAL VICE CHAIR
Kazutami Arimoto, *Renesas Electronics, Itami, Japan*

ITPC FAR EAST REGIONAL SECRETARY
Jae-Youl Lee, *Samsung, Yongin, Korea*

ITPC EUROPEAN REGIONAL CHAIR
Aarno Pärssinen, *Renesas Mobile, Helsinki, Finland*

ITPC EUROPEAN REGIONAL VICE CHAIR
Eugenio Cantatore, *Eindhoven University of Technology, Eindhoven, The Netherlands*

ITPC EUROPEAN REGIONAL SECRETARY
Alison Burdett, *Toumaz Technology, Abingdon, United Kingdom*

TUTORIALS CHAIR
Ali Sheikholeslami, *University of Toronto, Toronto, Canada*

ADCOM REPRESENTATIVE
Bryan Ackland, *Stevens Institute of Technology, Old Bridge, NJ*

DIRECTOR OF PUBLICATIONS AND PRESENTATIONS
Laura Fujino, *University of Toronto, Toronto, Canada*

DIRECTOR OF AUDIOVISUAL SERVICES
John Trnka, *Rochester, MN*

PRESS LIAISON AND AWARDS & RECOGNITION COMMITTEE (ARC) CHAIR
Kenneth C. Smith, *University of Toronto, Toronto, Canada*

PRESS COORDINATOR
Alice Wang, *MediaTek USA, Austin, TX*

DIRECTOR OF OPERATIONS
Melissa Widerkehr, *Widerkehr and Associates, Montgomery Village, MD*

TECHNICAL EDITORS

Jason H. Anderson, *University of Toronto, Toronto, Canada*
Vincent Gaudet, *University of Waterloo, Waterloo, Canada*
Glenn Gulak *(Editor-at-Large)*, *University of Toronto, Toronto, Canada*
James W. Haslett, *University of Calgary, Calgary, Canada*
Shahriar Mirabbasi, *(Editor-at-Large)* *University of British Columbia, Vancouver, Canada*
Kostas Pagiamtzis, *Semtech, Gennum Products Group, Burlington, Canada*
Kenneth C. Smith *(Editor-at-Large),* *University of Toronto, Toronto, Canada*

MULTI-MEDIA COORDINATORS

Dave Halupka, *Kapik Integration, Toronto, Canada*
Aleksey Tyshchenko, *Intel, Toronto, Canada*

COMMITTEES

INTERNATIONAL TECHNICAL PROGRAM COMMITTEE

PROGRAM CHAIR:
Bram Nauta, *University of Twente, Enschede, The Netherlands*

PROGRAM VICE CHAIR:
Trudy Stetzler, *Texas Instruments, Stafford, TX*

ANALOG SUBCOMMITTEE

Chair: Bill Redman-White, Southampton University, Southampton, United Kingdom
Marco Berkhout, NXP Semiconductors, Nijmegen, The Netherlands
Tony Chan Carusone, University of Toronto, Toronto, Canada
Baher Haroun, Texas Instruments, Dallas, TX
Minkyu Je, Institute of Microelectronics, A*STAR, Singapore,
Jerry (Xicheng) Jiang, Broadcom, Irvine, CA
Wing Hung Ki, HKUST, Hong Kong, China
Kimmo Koli, ST-Ericsson, Turku, Finland
Jae-Youl Lee, Samsung, Yongin, Korea
Tsung-Hsien Lin, National Taiwan University, Taipei, Taiwan
Saska Lindfors, Texas Instruments, Helsinki, Finland
Piero Malcovati, University of Pavia, Pavia, Italy
Chris Mangelsdorf, Analog Devices K.K, Tokyo, Japan
Christoph Sandner, Infineon Technologies Austria, Villach, Austria
Jafar Savoj, Xilinx, San Jose, CA
Michiel Steyaert, KULeuven, Hevrelee, Belgium
Axel Thomsen, Silicon Laboratories, Austin, TX
Ed (Adrianus JM) van Tuijl, University of Twente, Enschede, The Netherlands

DATA CONVERTERS SUBCOMMITTEE

Chair: Boris Murmann, Stanford University, Stanford, CA
Brian Brandt, Maxim Integrated Products, North Chelmsford, MA
Lucien Breems, NXP Semiconductors, Eindhoven, The Netherlands
Marco Corsi, Texas Instruments, Dallas, TX
Michael Flynn, University of Michigan, Ann Arbor, MI
Tetsuya Iizuka, University of Tokyo, Tokyo, Japan
John Khoury, Silicon Laboratories, Austin, TX
Hae-Seung Lee, Massachusetts Institute of Technology, Cambridge, MA
Takahiro Miki, Renesas Electronics, Hyogo, Japan
Gerhard Mitterregger, Intel Mobile Communications Austria, St. Magdalen, Austria
Un-Ku Moon, Oregon State University, Corvallis, OR
Jan Mulder, Broadcom, Bunnik, The Netherlands
Katsu Nakamura, Analog Devices, Wilmington, MA
Ken Nishimura, Agilent, Santa Clara, CA
Shanthi Pavan, Indian Institute Of Technology, Chennai, India
Michael Perrott, Masdar Institute of Science and Technology, Abu Dhabi, United Arab Emirates
Geert Van der Plas, imec, Leuven, Belgium
Jieh-Tsorng Wu, National Chiao-Tung University, Hsin-Chu, Taiwan

ENERGY-EFFICIENT DIGITAL SUBCOMMITTEE

Chair: Stephen Kosonocky, Advanced Micro Devices, Fort Collins, CO
Kazutami Arimoto, Okayama Prefectural University, Okayama, Japan
Wim Dehaene, KU Leuven, Leuven, Belgium
Vasantha Erraguntla, Intel Technology India, Bangalore, India
Shannon Morton, Nvidia, Bristol, United Kingdom
Byeong-Gyu Nam, Chungnam National University, Daejeon, Korea
Yongha Park, Samsung, Yongin, Korea
Michael Polley, Texas Instruments, Dallas, TX
Bing Sheu, TSMC, Hsinchu, Taiwan
Masaya Sumita, Panasonic, Moriguchi, Japan
Kees van Berkel, ST-Ericsson, Eindhoven, The Netherlands
Victor Zyuban, IBM T.J. Watson Research Center, Yorktown Heights, NY

HIGH-PERFORMANCE DIGITAL SUBCOMMITTEE

Chair: Stefan Rusu, Intel, Santa Clara, CA
Lew Chua-Eoan, Qualcomm, San Diego, CA
Tim Fischer, AMD, Fort Collins, CO
Eric Fluhr, IBM, Austin, TX
Hiroo Hayashi, Toshiba Corporation, Kawasaki, Japan
Anthony Hill, Texas Instruments, Dallas, TX
Atsuki Inoue, Fujitsu, Kawasaki, Japan
Tanay Karnik, Intel, Hillsboro, OR
Tobias Noll, RWTH Aachen University, Aachen, Germany
Luke (Jinuk) Shin, Oracle, Santa Clara, CA
Vladimir Stojanovic, Massachusetts Institute of Technology, Cambridge, MA
Se-Hyun Yang, Samsung, Yongin, Korea

IMAGERS, MEMS, MEDICAL AND DISPLAYS SUBCOMMITTEE

Chair: Roland Thewes, TU Berlin, Berlin, Germany
Ralf Brederlow, Texas Instruments, Freising, Germany
Maysam Ghovanloo, Georgia Institute of Technology, Atlanta, GA
Makoto Ikeda, University of Tokyo, Tokyo, Japan
Robert Johansson, OmniVision, Oslo, Norway
Sam Kavusi, Bosch Research and Technology Center, Palo Alto, CA
Shoji Kawahito, Shizuoka University, Hamamatsu, Japan
Tae-Chan Kim, Samsung, Yongin, Kprea
Hideaki Kurata, Hitachi, Tokyo, Japan
Wentai Liu, UCLA, Los Angeles, CA
Young-Sun Na, LG Electronics, Seoul, Korea
Yoshiharu Nakajima, Japan Display, Kanagawa, Japan
Yusuke Oike, Sony, Kanagawa, Japan
Maurits Ortmanns, University of Ulm, Ulm, Germany
Aaron Partridge, SiTime, Sunnyvale, CA
Michiel Pertijs, TU Delft, Delft, The Netherlands
David Stoppa, Fondazione Bruno Kessler, Trento, Italy
Refet Firat Yazicioglu, IMEC, Leuven, Belgium

MEMORY SUBCOMMITTEE

Chair: Kevin Zhang, Intel, Hillsboro, OR
Colin Bill, Global Foundries, Sunnyvale, CA
Jonathan Chang, TSMC, Hsinchu, Taiwan
Leland Chang, IBM T. J. Watson Research Center Yorktown Heights, NY
Sungdae Choi, SK hynix, Icheon-si, Korea
Michael Clinton, Texas Instruments, Dallas, TX
Jin-Man Han, Samsung Electronics, Hwasung, Korea
Satoru Hanzawa, Hitachi, Tokyo, Japan
Uksong Kang, Samsung Electronics, Hwasung-si, Korea
Atsushi Kawasumi, Toshiba, Kawasaki, Japan
Chulwoo Kim, Korea University, Seoul, Korea
James Sung, Etron Technology, Hsinchu, Taiwan
Yasuhiro Takai, Elpida Memory, Kanagawa, Japan
Daniele Vimercati, Micron Technology, Agrate, Italy
Tadaaki Yamauchi, Renesas Electronics, Itami, Japan

RF SUBCOMMITTEE

Chair: Andreia Cathelin, STMicroelectronics, Crolles, France
Ehsan Afshari, Cornell University, Ithaca, NY
Hooman Darabi, Broadcom, Irvine, CA
Brian Floyd, North Carolina State University, Raleigh, NC
Joseph Golat, Motorola, Algonquin, IL
Songcheol Hong, KAIST, Daejeon, Korea
Mike Keaveney, Analog Devices, Limerick, Ireland
Antonio Liscidini, University of Toronto, Toronto, Canada
Brian Otis, University of Washington, Seattle, WA
Ullrich Pfeiffer, University of Wuppertal, Wuppertal, Germany
Gabriel Rebeiz, UCSD, La Jolla, CA
Jussi Ryynanen, Aalto University, Espoo, Finland
Carlo Samori, Politecnico di Milano, Milano, Italy
Marc Tiebout, Infineon Technologies Austria, Villach, Austria
Piet Wambacq, imec, Heverlee, Belgium
Taizo Yamawaki, Renesas Mobile, Takasaki, Japan
Masoud Zargari, Qualcomm-Atheros, Irvine, CA
Jing-Hong Zhan, MediaTek, HsinChu, Taiwan

TECHNICAL DIRECTIONS SUBCOMMITTEE

Chair: Hoi-Jun Yoo, KAIST, Daejeon, Korea
Shekhar Borkar, Intel, Hillsboro, OR
Alison Burdett, Toumaz Technology, Abingdon, United Kingdom
Eugenio Cantatore, Eindhoven University of Technology, Eindhoven, The Netherlands
Eric Colinet, CEA-LETI, Grenoble, France
Paul Heremans, imec, Leuven, Belgium
Fu-Lung Hsueh, TSMC, Hsinchu, Taiwan
Ali Keshavarzi, Cypress, San Jose, CA
Uming Ko, MediaTek, Austin, TX
Tadahiro Kuroda, Keio University, Yokohama, Japan
Shinichiro Mutoh, NTT, Atsugi, Japan
Masaitsu Nakajima, Panasonic, Osaka, Japan
Chris Nicol, Wave Semiconductor, Sunnyvale, CA
Pirooz Pavarandeh, Maxim Integrated Products, San Jose, CA
Yogesh K. Ramadass, Texas Instruments, Dallas, TX
David Ruffieux, CSEM, Neuchated, Switzerland

WIRELESS SUBCOMMITTEE

Chair: David Su, Qualcomm Atheros, San Jose, CA
Didier Belot, STMicroelectronics, Crolles, France
Gangadhar Burra, Texas Instruments, Dallas, TX
Jan Crols, AnSem, Heverlee, Belgium
Hossein Hashemi, University of Southern California, Los Angeles, CA
Myung-Woon Hwang, FCI, Sungnam, Korea
Albert Jerng, Mediatek, Hsinchu, Taiwan
Eric Klumperink, University of Twente, Enschede, The Netherlands
Shouhei Kousai, Toshiba, Kawasaki, Japan
Sven Mattisson, Ericsson, Lund, Sweden
Alyosha Molnar, Cornell University, Ithaca, NY
Kenichi Okada, Tokyo Institute of Technology, Tokyo, Japan
Yorgos Palaskas, Intel, Hillsboro, OR
Aarno Pärssinen, Renesas Mobile, Helsinki, Finland
Woogeun Rhee, Tsinghua University, Beijing, China
Koji Takinami, Panasonic, Yokohama, Japan
Jan Van Sinderen, NXP, Eindhoven, The Netherlands
Iason Vassiliou, Broadcom, Alimos, Greece

WIRELINE SUBCOMMITTEE

Chair: Daniel Friedman, IBM Thomas J. Watson Research Center, Yorktown Heights, NY
Elad Alon University of California, Berkeley, Berkeley,CA
Ajith Amerasekera, Texas Instruments, Dallas, TX
Ken Chang, Xilinx, San Jose, CA
SeongHwan Cho, KAIST, Daejon, Korea
Nicola Da Dalt, Infineon, Villach, Austria
Gerrit den Besten, NXP Semiconductors, Eindhoven, The Netherlands
Azita Emami-Neyestanak, California Institute of Technology, Pasadena, CA
Ichiro Fujimori, Broadcom Corporation, Irvine, CA
Chewnpu Jou, TSMC, Hsinchu, Taiwan
Jack Kenney, Analog Devices, Somerset, NJ
Masafumi Nogawa, NTT Microsystem Integration Laboratories, Atsugi, Japan
Frank O'Mahony, Intel, Hillsboro, OR
Ali Sheikholeslami, University of Toronto, Toronto, Canada
Koichi Yamaguchi, Renesas Electronics, Kawasaki, Japan
Hisakatsu Yamaguchi, Fujitsu Laboratories, Kawasaki, Japan

EUROPEAN REGIONAL COMMITTEE

ITPC EUROPEAN REGIONAL CHAIR
Aarno Pärssinen, Renesas Mobile, Helsinki, Finland

ITPC EUROPEAN REGIONAL VICE CHAIR
Eugenio Cantatore, Eindhoven University of Technology, Eindhoven, The Netherlands

ITPC EUROPEAN REGIONAL SECRETARY
Alison Burdett, Toumaz Technology, Abingdon, United Kingdom

Didier Belot, STMicroelectronics, Crolles, France
Marco Berkhout, NXP Semiconductors, Nijmegen, The Netherlands
Ralf Brederlow, Texas Instruments, Freising, Germany
Lucien Breems, NXP Semiconductors, Eindhoven, The Netherlands
Andreia Cathelin, STMicroelectronics, Crolles, France
Eric Colinet, CEA-LETI, Grenoble, France
Jan Crols, AnSem, Heverlee, Belgium
Nicola Da Dalt, Infineon, Villach, Austria
Wim Dehaene, KU Leuven, Leuven, Belgium
Gerrit den Besten, NXP Semiconductors, Eindhoven, The Netherlands
Paul Heremans, imec, Leuven, Belgium
Robert Johansson, OmniVision, Oslo, Norway
Mike Keaveney, Analog Devices, Limerick, Ireland
Eric Klumperink, University of Twente, Enschede, The Netherlands
Kimmo Koli, ST-Ericsson, Turku, Finland
Saska Lindfors, Texas Instruments, Helsinki, Finland
Antonio Liscidini, University of Toronto, Toronto, Canada
Piero Malcovati, University of Pavia, Pavia, Italy
Sven Mattisson, Ericsson, Lund, Sweden
Gerhard Mitterregger, Intel Mobile Communications Austria, St. Magdalen, Austria
Shannon Morton, Nvidia, Bristol, United Kingdom
Jan Mulder, Broadcom, Bunnik, The Netherlands
Tobias Noll, RWTH Aachen University, Aachen, Germany
Maurits Ortmanns, University of Ulm, Ulm, Germany
Michael Perrott Masdar Institute of Science and Technology, Abu Dhabi, United Arab Emirates
Michiel Pertijs, TU Delft, Delft, The Netherlands
Ullrich Pfeiffer, University of Wuppertal, Wuppertal, Germany
Bill Redman-White, Southampton University, Southampton, United Kingdom
David Ruffieux, CSEM, Neuchated, Switzerland

European Members (continued):

Jussi Ryynanen, Aalto University, Espoo, Finland
Carlo Samori, Politecnico di Milano, Milano, Italy
Christoph Sandner, Infineon Technologies Austria, Villach, Austria
Michiel Steyaert, KU Leuven, Hevrelee, Belgium
David Stoppa, Fondazione Bruno Kessler, Trento, Italy
Roland Thewes, TU Berlin, Berlin, Germany
Marc Tiebout, Infineon Technologies, Villach, Austria
Kees van Berkel, ST-Ericsson, Eindhoven, The Netherlands
Geert Van der Plas, imec, Leuven, Belgium
Jan Van Sinderen, NXP, Eindhoven, The Netherlands
Ed van Tuijl, University of Twente, Enschede, The Netherlands
Iason Vassiliou, Broadcom, Alimos, Greece
Daniele Vimercati, Micron Technology, Agrate, Italy
Piet Wambacq, imec, Heverlee, Belgium
Refet Firat Yazicioglu, imec, Leuven, Belgium

FAR EAST REGIONAL COMMITTEE

ITPC FAR EAST REGIONAL CHAIR
Makoto Ikeda, University of Tokyo, Tokyo, Japan

ITPC FAR EAST REGIONAL VICE-CHAIR
Kazutami Arimoto, Okayama Prefectural University, Soja, Japan

ITPC FAR EAST REGIONAL SECRETARY
Jae-Youl Lee, Samsung, Yongin, Korea

Jonathan Chang, TSMC, Hsinchu, Taiwan
SeongHwan Cho, KAIST, Daejon, Korea
Sungdae Choi, SK hynix, Icheon-si, Korea
Vasantha Erraguntla, Intel Technology India, Bangalore, India
Jin-Man Han, Samsung Electronics, Hwasung, Korea
Satoru Hanzawa, Hitachi, Tokyo, Japan
Hiroo Hayashi, Toshiba, Kawasaki, Japan
Fu-Lung Hsueh, TSMC, Hsinchu, Taiwan
Myung-Woon Hwang, FCI, Sungnam, Korea
Tetsuya Iizuka, University of Tokyo, Tokyo, Japan
Atsuki Inoue, Fujitsu, Kawasaki, Japan
Minkyu Je, Institute of Microelectronics, A*STAR, Singapore
Albert Jerng, Mediatek, Hsinchu, Taiwan
Chewnpu Jou, TSMC, Hsinchu, Taiwan
Uksong Kang, Samsung Electronics, Hwasung, Korea
Shoji Kawahito, Shizuoka University, Hamamatsu, Japan
Atsushi Kawasumi, Toshiba, Kawasaki, Japan
Wing Hung Ki, HKUST, Hong Kong, China
Chulwoo Kim, Korea University, Seoul, Korea
Tae-Chan Kim, Samsung, Yongin, Korea
Shouhei Kousai, Toshiba, Kawasaki, Japan
Hideaki Kurata, Hitachi, Tokyo, Japan
Tadahiro Kuroda, Keio University, Yokohama, Japan
Tsung-Hsien Lin, National Taiwan University, Taipei, Taiwan
Chris Mangelsdorf, Analog Devices K.K, Tokyo, Japan
Takahiro Miki, Renesas Electronics, Itami, Japan
Shinichiro Mutoh, NTT, Atsugi, Japan
Young-Sun Na, LG Electronics, Seoul, Korea
Masaitsu Nakajima, Panasonic, Osaka, Japan
Yoshiharu Nakajima, Japan Display, Kanagawa, Japan
Byeong-Gyu Nam, Chungnam National University, Daejeon, Korea
Masafumi Nogawa, NTT Microsystem, Atsugi, Japan
Yusuke Oike, Sony, Atsugi, Japan
Kenichi Okada, Tokyo Institute of Technology, Tokyo, Japan
Yongha Park, Samsung, Yongin, Korea
Shanthi Pavan, Indian Institute of Technology Madras, Chennai, India
Woogeun Rhee, Tsinghua University, Beijing, China
Bing Sheu, TSMC, Hsinchu, Taiwan
Masaya Sumita, Panasonic Corporation, Moriguchi, Japan
James Sung, Etron Technology, Hsinchu, Taiwan
Yasuhiro Takai, Elpida Memory, Sagamihara, Japan
Koji Takinami, Panasonic, Yokohama, Japan
Jieh-Tsorng Wu, National Chiao-Tung University, Hsinchu, Taiwan
Koichi Yamaguchi, Renesas Electronics, Kawasaki, Japan
Hisakatsu Yamaguchi, Fujitsu Laboratories, Kawasaki, Japan
Tadaaki Yamauchi, Renesas Electronics, Itami, Japan
Taizo Yamawaki, Renesas Mobile, Takasaki-shi, Japan
Se-Hyun Yang, Samsung, Yongin-Si, Korea
Hoi-Jun Yoo, KAIST, Daejeon, Korea
Jing-Hong Zhan, MediaTek, Hsinchu, Taiwan

HOW TO REGISTER FOR ISSCC

Online: This is the fastest, most convenient way to register and will give you immediate email confirmation of your events. To register online (which requires a credit card), go to the ISSCC website at www.isscc.org and select the link to the registration website.

FAX, mail or email: Use the "2013 IEEE ISSCC Registration Form" which can be downloaded from the registration website. All payments must be made in U.S. Dollars, by credit card or check. Checks must be made payable to "ISSCC 2013". It will take several days before you receive email confirmation when you register using the form. **Registration forms received without full payment will not be processed until payment is received at YesEvents.** Please read the descriptions and instructions on the back of the form carefully.

On site: The On-site Registration and Advance Registration Pickup Desks at ISSCC 2013 will be located in the Yerba Buena Ballroom Foyer at the San Francisco Marriott Marquis. All participants, except as noted below, should register or pick up their registration materials at these desks as soon as possible. **Pre-registered Presenting Authors and pre-registered members of the ISSCC Program and Executive Committees must go to the Nob Hill Room, Ballroom level, to collect their conference materials.**

REGISTRATION DESK HOURS:

Saturday, February 16	4:00 pm to 7:00 pm
Sunday, February 17	6:30 am to 8:30 pm
Monday, February 18	6:30 am to 3:00 pm
Tuesday, February 19	8:00 am to 3:00 pm
Wednesday, February 20	8:00 am to 3:00 pm
Thursday, February 21	7:00 am to 2:00 pm

Students must present their Student ID at the Registration Desk to receive the student rates. Those registering at the IEEE Member rate must provide their IEEE Membership number.

Deadlines: The deadline for registering at the Early Registration rates is 11:59 pm Pacific Time **Friday January 11, 2013.** After January 11th, and on or before 11:59 pm Pacific Time Monday January 28, 2013, registrations will be processed **at the Late Registration rates. After January 28th, you must register on site at the On-site rates.** You are urged to register early to obtain the lowest rates and ensure your participation in all aspects of ISSCC 2013.

Cancellations/Adjustments/Substitutions: Prior to 11:59 pm Pacific Time **Monday January 28, 2013,** conference registration can be cancelled. Fees paid will be refunded (less a processing fee of $75). Registration category or credit card used can also be changed (for a processing fee of $35). Send an email to the registration contractor at ISSCCinfo@yesevents.com to cancel or make other adjustments. **No refunds will be made after 11:59 pm Pacific Time January 28, 2013.** Paid registrants who do not attend the conference will be sent all relevant conference materials. Transfer of registration to someone else is allowed with **WRITTEN** permission from the original registrant.

IEEE Membership Saves on ISSCC Registration

Take advantage of reduced ISSCC registration fees by using your IEEE membership number. If you're an IEEE member and have forgotten your member number, simply phone IEEE at 1(800) 678-4333 and ask. IEEE membership staff will take about two minutes to look up your number for you. If you come to register on site without your membership card, you can phone IEEE then, too. Or you can request a membership number look-up by email. Use the online form at: www.ieee.org/about/help/member_support.html. If you're not an IEEE member, consider joining before you register to save on your fees. Join online at www.ieee.org/join at any time and you'll receive your member number by email. If you join IEEE at the conference, you can also select a free Society membership. This offer is not available to existing IEEE members.

SSCS Membership – a Valuable Professional Resource for your Career Growth

Membership in the Solid-State Circuit Society offers you the chance to explore solutions within a global community of colleagues in our field. Membership extends to you the opportunity to grow and share your knowledge, hone your expertise, expand or specialize your network of colleagues, advance your career, and give back to the profession and your local community.

We invite you to join or renew today to participate in exclusive educational events, access to leading research and best practice literature, and start your own career legacy by mentoring students and young professionals entering our field. It all starts with becoming a member of the Solid-State Circuit Society where you can:
-Connect with your Peers – valuable networking opportunities through our world-class conferences, publication offerings, social media extensions, and interactive educational opportunities.
-Keep up with the latest trends and cutting-edge developments in our industry – through our electronic newsletters, member magazine "Solid-State Circuits Magazine", and our award winning "Journal of Solid-State Circuits".
-Valuable career and educational tools - saving you both time and money with 24/7 access to our website and member-only professional development and educational material; Distinguished Lecturer Tours, Tutorials, and webinars by subject matter experts.
-Exclusive access to SSCS Conference Digests for ISSCC, CICC, A-SSCC, ESSCIRC, and Symposium on VLSI Circuits.
-Publications and EBooks – discounted access to vast online document libraries of journals, standards, and conference papers offer you one-third of the world's technical research to keep your knowledge current. New in 2012-13, two new virtual journals – the RFIC-VJ and the soon to be available, ESS-CDC.

SSCS Membership Saves Even More on ISSCC Registration

This year, SSCS members will receive an exclusive benefit of a $40 discount on the registration fee for ISSCC in addition to the IEEE discount. Also, the SSCS will again reward our members with a $10 Starbucks gift card when they attend the Conference as an SSCS member in good standing.

Join or renew your membership with IEEE's Solid-State Circuit Society today at sscs.ieee.org – you will not want to miss out on the opportunity and benefits your membership will provide now and throughout your career.

ITEMS INCLUDED IN REGISTRATION

Technical Sessions: Registration includes admission to all technical and evening sessions starting Sunday evening and continuing throughout Monday, Tuesday and Wednesday. ISSCC does not offer partial conference registrations.
Technical Book Display: Several technical publishers will have collections of professional books and textbooks for sale during the Conference. The Book Display will be open on Monday from Noon to 7:00 pm; on Tuesday from 10:00 am to 7:00 pm; and on Wednesday from 10:00 am to 3:00 pm.
Demonstration Sessions: Hardware demonstrations will support selected papers during the Social Hours on Monday and Tuesday.
Author Interviews: Author Interviews will be held Monday, Tuesday and Wednesday evenings. Authors from each day's papers will be available to discuss their work.
Social Hour: Social Hour refreshments will be available starting at 5:15 pm on Monday and Tuesday in both the Book Display and Author Interview areas.
University Events: Several universities are planning social events during the Conference. Check the University Events display at the conference for the list of universities, locations and times of these events.
ISSCC travel mug: A convenient travel mug will be given to all Conference registrants.
Publications: Conference registration includes:
-The **Digest of Technical Papers** in hard copy, on a DVD, and by download. Hard copy/DVD are available on site during registration hours beginning on Sunday at 10:00 am.
-**Download of all paper visuals:** The Conference DVD has been replaced by a download of the Digest and presentation visuals. Instructions and an ID/password will be provided.

OPTIONAL EVENTS

Educational Events: Many educational events are available at ISSCC 2013 for an additional fee. There are ten 90-minute Tutorials and two all-day Forums on Sunday. There are four additional all-day Forums on Thursday as well as an all-day Short Course. All events include a course handout in color. The all-day events also include breakfast, lunch and break refreshments. See the schedule for details of the topics and times.

Women's Networking Event: ISSCC will be offering a networking event for women in solid-state circuits on **Monday at 12:15 pm**. This luncheon is an opportunity to hear from an accomplished speaker, get to know other women in the profession and discuss a range of topics including leadership, work-life balance, and professional development. This event is open to women only at a discounted fee.

OPTIONAL PUBLICATIONS

ISSCC 2013 Publications: The following ISSCC 2013 publications can be purchased in advance or on site:
Additional copies of the **Digest of Technical Papers** in book or DVD format.
2013 Tutorials DVD: All of the 90 minute Tutorials **(mailed in May).**
2013 Short Course DVD: "RF Blocks for Wireless Transceivers" **(mailed in May)**.
Short Course and Tutorial DVDs contain audio and written English transcripts synchronized with the presentation visuals. In addition, the Short Course DVD contains a pdf file of the presentations suitable for printing, and pdf files of key reference material.
Earlier ISSCC Publications: Selected publications from earlier conferences can be purchased. There are several ways to purchase this material:
-Items listed on the registration form can be purchased with registration and picked up at the conference or mailed to you when available.
-Visit the ISSCC Publications Desk. This desk is located in the registration area and has the same hours as conference registration. With payment by cash, check or credit card, you can pick up (or order for future delivery) materials at this desk. Tutorial and Short Course DVDs from prior conferences are available. See the order form for titles and prices.
-Visit the ISSCC website at www.isscc.org and click on the link "SHOP ISSCC" where you can order online or download an order form to mail, email or fax. For a small shipping fee, this material will be sent to you immediately (or when available) and you will not have to wait until you attend the conference to get it.

HOW TO MAKE HOTEL RESERVATIONS

TO ALL ATTENDEES WHO NEED A HOTEL ROOM: We are offering this year a $100 Marriott rebate coupon! If you register for ISSCC 2013 and spend at least three nights at the San Francisco Marriott Marquis, a credit of $100 will be applied to your hotel bill. Enjoy the convenience of staying at the Conference hotel AND save money too! See the hotel reservations website for details.

Online: ISSCC participants are urged to make their hotel reservations at the San Francisco Marriott Marquis online. Go to the conference website and click on the Hotel Reservation link. **Conference room rates are $229 for a single/double, $249 for a triple and $269 for a quad** (per night plus tax). In addition, ISSCC attendees booked in the ISSCC group receive **in-room Internet access for free**. All online reservations require the use of a credit card. Online reservations are confirmed immediately. You should print the page containing your confirmation number and reservation details and bring it with you when you travel to ISSCC.
Telephone: Call 877-622-3056 (US) or 415-896-1600 and ask for "Reservations." When making your reservation, identify the group as ISSCC 2013 to get the group rate.
Hotel Deadline: Reservations must be received at the San Francisco Marriott Marquis no later than January 28, 2013 to obtain the special ISSCC rates. A limited number of rooms are available at these rates. **Once this limit is reached or after January 28th, the group rates may no longer be available and reservations will be filled at the best available rate.**
Changes: Before the hotel deadline, your reservation can be changed by calling the telephone numbers above. After the deadline, call the Marriott Marquis at 415-896-1600 (ask for "Reservations"). Have your hotel confirmation number ready.

IEEE NON-DISCRIMINATION POLICY

IEEE is committed to the principle that all persons shall have equal access to programs, facilities, services, and employment without regard to personal characteristics not related to ability, performance, or qualifications as determined by IEEE policy and/or applicable laws.

EVENT PHOTOGRAPHY

Attendance at, or participation in, this conference constitutes consent to the use and distribution by IEEE of the attendee's image or voice for informational, publicity, promotional and/or reporting purposes in print or electronic communications media. Video recording by participants and other attendees during any portion of the conference is not allowed without special prior written permission of IEEE.

REFERENCE INFORMATION

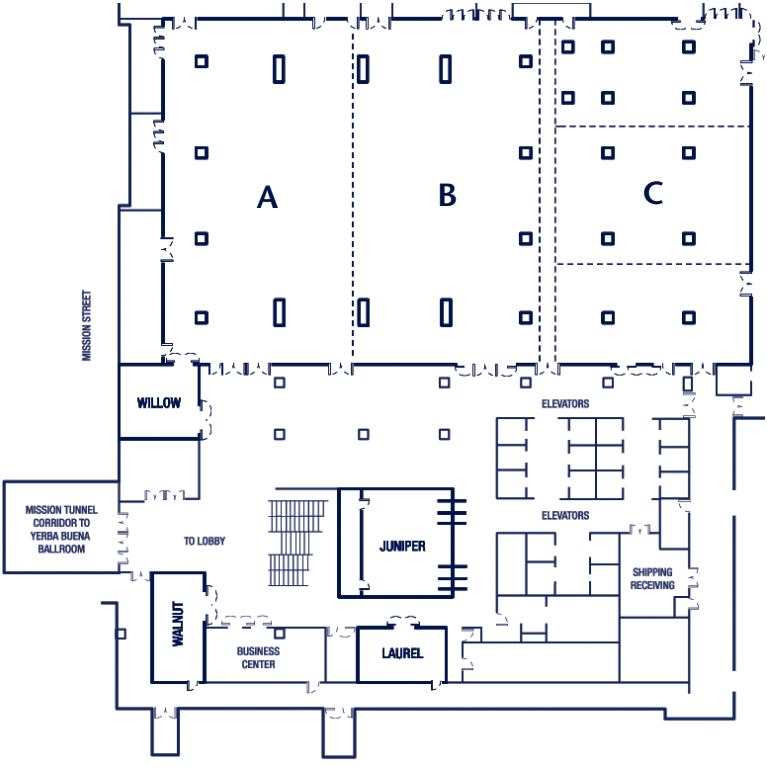
TAKING PICTURES, VIDEOS OR AUDIO RECORDINGS DURING ANY OF THE SESSIONS IS NOT PERMITTED

Conference Website:	www.isscc.org
ISSCC Email:	ISSCC@ieee.org
Registration questions:	ISSCCinfo@yesevents.com
Hotel Information:	San Francisco Marriott Marquis Phone: 415-896-1600 55 Fourth Street San Francisco, CA 94103
Press Information:	Kenneth C. Smith Phone: 416-418-3034 University of Toronto Email: lcfujino@aol.com
Registration:	YesEvents Phone: 410-559-2200 or 800-937-8728 P.O. Box 32862 Baltimore, MD 21282 Fax: 410-559-2217 Email: issccinfo@yesevents.com

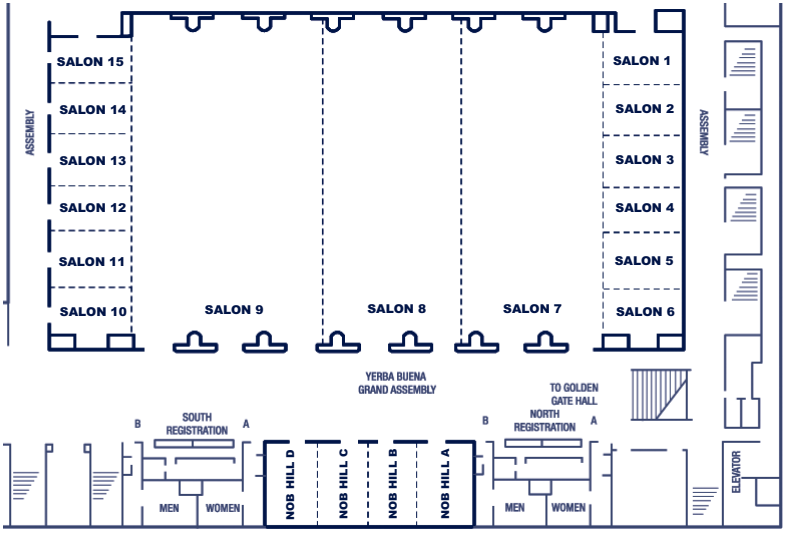
Hotel Transportation: Visit the ISSCC website "Attendees" page for helpful travel links and to download a document with directions and pictures of how to get from the San Francisco Airport (SFO) to the Marriott Marquis. You can get a map and driving directions from the hotel website at www.marriott.com/hotels/travel/sfodt-san-francisco-marriott-marquis/

Next ISSCC Dates and Location: ISSCC 2014 will be held on February 9-13, 2014 at the San Francisco Marriott Marquis Hotel.

Golden Gate Ballroom



Yerba Buena Ballroom



IEEE

445 Hoes Lane
P.O. Box 1331
Piscataway, NJ 08855-1331
USA

ISSCC.org

sscs.ieee.org

ISSCC 2013 ADVANCE PROGRAM