ADVANCE PROGRAM

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS

ISSCC®

UNIVERSITY OF PENNSYLVANIA

2010 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE

FEBRUARY 7, 8, 9, 10, 11

CONFERENCE THEME:

SENSING THE FUTURE

SAN FRANCISCO MARRIOTT MARQUIS HOTEL

MARRIOTT MARQUIS REBATE AND FREE INTERNET SEE INSIDE!

IEEE SOLID-STATE CIRCUITS SOCIETY

THURSDAY ALL-DAY: 4 FORUMS: Optical Communications; High-Speed Image Capture; Portable Medical Electronics; Signal and Power Integrity for SOCs

SHORT-COURSE: CMOS Phase-Locked Loops for Frequency Synthesis

SUNDAY ALL-DAY: 2 FORUMS: 3D Integration Technology; Reconfigurable RF and Data Converters

9 TUTORIALS: Battery Management; RF Front-end Passives; Specifying and Testing ADCs; RF CMOS Power Amplifiers; Energy-efficient On-chip Networks; Design of Smart Sensors; High-speed Memory Interfaces; Power Gating; PLL Design in nm CMOS

SPECIAL-TOPIC SESSION: Beyond CMOS: Emerging Technologies — **STUDENT RESEARCH PREVIEW**

5-DAY PROGRAM

ISSCC VISION STATEMENT

The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and application to maintain technical currency, and to network with leading experts.

CONFERENCE TECHNICAL HIGHLIGHTS

On **Sunday, February 7th**, the day before the official opening of the Conference, ISSCC 2010 offers:

- A choice of up to 4 of a total of 9 Tutorials
- A choice of 1 of 2 Advanced-Circuit-Design Forums

The 90-minute tutorials offer background information and a review of the basics in specific circuit design topics. In the all-day Advanced-Circuit-Design Forums, leading experts present state-of-the-art design strategies in a workshop-like format. The Forums are targeted at designers experienced in the technical field.

On Sunday evening, a Special-Topic Evening Session entitled: "Beyond CMOS: Emerging Technologies", will be offered starting at 8:00pm. In addition the Student Research Preview Session starting a 7:45pm, featuring short presentations by selected graduate student researchers from around the world, will also be offered.

On **Monday, February 8th**, ISSCC 2010 offers four plenary papers followed by five parallel technical sessions. A Social Hour open to all ISSCC attendees will follow the afternoon sessions on Monday. The Social Hour will feature posters from the winners of the joint ISSCC/DAC Student-Design Contest. Monday evening features a panel discussion on "Analog Circuits: Stump the Panel", as well as two Special-Topic Sessions on "Energy-Efficient High-Speed Interfaces" and "Fusion of MEMS and Circuits".

On **Tuesday, February 9th**, ISSCC 2010 offers five parallel morning and afternoon technical sessions. A Social Hour open to all ISSCC attendees will follow the afternoon sessions on Tuesday. The Social Hour will feature posters from the winners of the joint ISSCC/DAC Student-Design Contest. Tuesday evening sessions include an evening panel on "The Semiconductor Industry in 2025", as well as two Special-Topic Sessions on "Can RF SoCs (Self) Test Their Own RF?" and "Can We Rebuild Them? Bionics Beyond 2010".

Wednesday, February 10th, features five parallel sessions morning and afternoon.

On **Thursday, February 11th**, ISSCC 2010 offers a choice of five events:

- A Short Course on "CMOS Phase-Locked Loops for Frequency Synthesis"
- Four Advanced-Circuit-Design Forums

Registration for educational events will be filled on a first-come, first-served basis. Use of the ISSCC Web-Registration Site (http://www.isscc.org) is strongly encouraged. Registrants will be provided with immediate confirmation on registration for Tutorials, Advanced-Circuit-Design Forums and the Short Course.

Need Additional Information?
Go to: www.isscc.org

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TUTORIALS

T1: Battery Management for Portable Devices

With the increasing demand for portable devices, batteries have become an essential component of everyday life. In recent years Li-ion batteries stepped up as the main choice to power almost every electronic gadget in the world due to their high capacity-per-volume and long lifetime. However, proper battery management techniques are needed to ensure long-lasting battery and safety-of-operation.

This tutorial covers the basics of battery chemicals with a brief overview of the different battery types. It then concentrates on Li-ion battery packs and reviews the various charging algorithms, including trickle charging, pre-charging, constant-current/constant voltage and pulse charging. The tutorial then shows some practical examples of battery charging circuits (both linear and switched-mode chargers) and covers the techniques needed to ensure safety and preserve capacity.

Instructor: Francesco Rezzi is Design Engineer Director at Marvell Semiconductor in Pavia, Italy. He is currently involved in the design and definition of power-management circuits for portable application as well as baseband, audio and video analog signal processing. In the past he also worked for Maxim Integrated Products as Principal Engineer for the Non Portable Power Management group and at STMicroelectronics as design engineer for the HD read-channel group. He holds several US patents and publications.

T2: SoC Integration of RF Front-End Passives

RF front-end passives, such as SAW filters and duplexers, have proven resistant to integration as part of a low-cost CMOS SoC. Traditional RF designs are unsuitable because of the modest quality factor for on-chip spiral inductors as well as manufacturing variation of on-chip capacitors which limit performance. Important repercussions from continuing to use off-chip front-end passives are: higher cost, larger physical space, and higher complexity in PCB and package design, particularly for multimode, and multiband applications such as cellular or software-defined radios. In this tutorial, we first study the system-level requirements for front-end passives and discuss the SoC implementation challenges from the circuit point of view. We then introduce several architectural and circuit-level techniques that can address these problems, followed by case studies for both 2G and 3G transceivers.

Instructor: Hooman Darabi was born in Tehran, Iran in 1972. He received the BS and MS degrees both in Electrical Engineering from Sharif University of Technology, Tehran in 1994, and 1996, respectively. He received the Ph.D. degree in electrical engineering from the University of California, Los Angeles, in 1999. He is currently a director, Engineering with Broadcom, Irvine, CA, where he is in charge of all the cellular RF IC developments. His interests include analog and RF IC design for wireless communications. Dr. Darabi holds over 120 issued or pending patents with Broadcom, and has published over 30 peer reviewed or conference papers.

T3: Specifying and Testing ADCs

The importance of key ADC performance criteria, such as noise, linearity, spurious response and metastability is reviewed in the context of applications for broadband and narrowband communication, instrumentation and radar. Basic ADC testing techniques are presented. Because the output of an ADC is digital, the entire field of digital signal processing is at our disposal to perform signal analysis and parameter estimation on the output data. A few examples of these advanced testing techniques are described as special cases of using the full power of DSP to characterize converter circuits. Finally, the tutorial presents the material in a unified way such that specifying and testing ADCs should not be seen as two separate subjects, but merely two aspects of the same thing.

Instructor: Aaron Buchwald is currently CEO and co-founder of Mobius Semiconductor, a privately held start-up in Irvine, CA. He has 27 years experience in the field of analog integrated circuit design. Dr. Buchwald joined Broadcom in 1994 as the first member of the analog group, where he designed several generations of ADCs and front-end circuitry for products in the cable, satellite and networking markets. He was later responsible for development of multi-gigabit serial transceivers for XAUI, CX4 and Fiber Channel. Dr. Buchwald was formerly an Assistant Professor at the Hong Kong University of Science and Technology (HKUST). Prior to that he worked at Siemens in Munich, Germany and Hughes Aircraft in El Segundo, CA. Dr. Buchwald has a BSEE from the University of Iowa, and an MS and PhD from the University of California, Los Angeles. He is Co-author of the book *Integrated Fiber-Optic Receivers*, Kluwer, 1995 and was the co-recipient of the ISSCC outstanding paper award in 1997 for the design of a 10-bit video-rate data converter.

T4: RF CMOS Power Amplifiers and Linearization Techniques

The tutorial starts with a general overview of the basics of RF power amplifier (PA) design, defining the problem, the important specifications, and the generic topologies. Then we discuss three classes of CMOS PAs. The first class covers output powers around 0dBm. The second class is for WLAN/WPAN applications with output powers around 20 to 24dBm. Approaches to boosting the performance such as current summing and/or voltage summing are covered. The third class consists of PAs with output powers around 30dBm (1W) needed for cellular applications. The final section of the tutorial addresses PA linearization techniques as many modern communication standards require linear PA operation. The tutorial will cover the principles behind polar, Cartesian, Doherty and out-phasing techniques.

Instructor: Domine M. W. Leenaerts received the Ph.D. degree in electrical engineering from Eindhoven University of Technology, Eindhoven, the Netherlands, in 1992. He worked for Philips Research and since 2006 he has worked at NXP Semiconductors, Research as Senior Principal Scientist. Dr. Leenaerts is an Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS, elected member on the IEEE Solid-State Circuits Society Administrative Committee and Fellow IEEE.

T5: Design of Energy-Efficient On-Chip Networks

This tutorial addresses the challenges in designing efficient core-to-core and core-to-memory communication fabrics in emerging processor chips with dozens to hundreds of cores. In this power- and area-constrained environment, network design must be tightly integrated with underlying hardware–interconnect channel and router designs. The tutorial covers a broad spectrum of network topologies and design tradeoffs, from large-diameter, low-radix networks like mesh, to small-diameter, high-radix networks like crossbars. Network-design-space exploration are described based on underlying physical models of the router and wire channels, including traditional repeated interconnects as well as alternatives like equalized electrical and silicon-photonic interconnects.

Instructor: Vladimir Stojanović is an Associate Professor of Electrical Engineering and Computer Science at MIT. His research interests include design, modeling and optimization of integrated systems, from CMOS and emerging devices to VLSI microarchitectures and processor networks. He is also interested in design and implementation of digital communication techniques in high-speed electrical and optical interconnects and high-speed mixed-signal IC design. He received the M.S. and Ph.D. degrees in electrical engineering from Stanford University, in 2000 and 2005, respectively, and the Dipl. Ing. degree from the University of Belgrade, Serbia, in 1998. He was also with Rambus, Los Altos, CA, from 2001 to 2004.

T6: Design of Smart Sensors

Sensors are everywhere! Temperature sensors throttle SoCs, accelerometers activate airbags, and magnetic-field sensors form the basis of electronic compasses. These are all examples of smart sensors, i.e., sensors that are co-integrated with their readout electronics and so provide digital output. However, processing the weak analog output of typical sensors is quite challenging, especially when it must be done in standard CMOS, whose precision is limited by $1/f$ noise, component tolerances and mismatch. In this tutorial, a system approach to the design of smart sensors is presented. The use of dynamic techniques, such as chopping, auto-zeroing, dynamic element matching and $\Delta\Sigma$ modulation, to trade speed for precision is discussed. The proposed methodology is illustrated by case studies describing the design of state-of-the-art CMOS sensors for the measurement of wind velocity, magnetic field and temperature.

Instructor: Kofi A.A. Makinwa is a Professor at Delft University of Technology, The Netherlands, where he leads a group that designs precision analog circuits, $\Delta\Sigma$ modulators, and smart sensors. He holds B.Sc. (1st Class Hons.) and M.Sc. degrees from Obafemi Awolowo University, Nigeria, an M.E.E. (*cum laude*) degree from the Philips International Institute, The Netherlands and a Ph.D. degree from Delft University of Technology. From 1989 to 1999 he was a research scientist at Philips Research Laboratories, after which he joined Delft University of Technology. He holds 14 patents, has (co)-authored over 100 technical papers, and has given tutorials at several conferences, including ISSCC. Dr. Makinwa is a recipient of the Dutch Technology Foundation's Simon Stevin Gezel award, and a (co)-recipient of several best paper awards, including one from the JSSC and three from the ISSCC. He is an IEEE distinguished lecturer and a member of the Young Academy of the Royal Netherlands Academy of Arts and Sciences.

TUTORIALS

T7: High-Speed Memory Interfaces

High-speed memory interfaces are well established in the DDRx and GDDRx line-ups for DRAMs. With high bitrates up to 10Gb/s using less advanced MOS capability, DRAM-specific DLL/PLL circuit techniques and many signal integrity solutions are abundant in many application areas of memory. The prospect of 3D chip-stacks is also a focus of interest for higher-bandwidth and lower-power interface solutions. This tutorial provides a good perspective in current state-of-the-art and insights into future directions, instructive to memory designers and memory users as well as circuit engineers who are interested in portable, low-power, high-performance interfaces.

Instructor: Yasuhiro Takai received the B.S. and M.S. degrees in electronic engineering from Tohoku University, Sendai, Japan, in 1986 and 1988, respectively. He joined NEC, Kanagawa in 1988. He was engaged in developing the first SDRAM and the first DDR-SDRAM, presented papers in 1993 and 1999, respectively. He was transferred to Elpida Memory, Kanagawa in 2000, where he was engaged in developing the first DDR2-SDRAM in Elpida in 2002. During his career, he has been engaged in more than 15 DRAM-product development or projects from 4Mb fast-page DRAM to 1Gb DDR3-SDRAM. He works on designing high-speed, high-accuracy circuits.

T8: Power Gating

Integrated power gating has emerged as a primary knob for balancing the needs for high performance and low standby power during periods of circuit inactivity. This tutorial provides a comprehensive overview of various power-gating techniques along with the challenges for integration in design flows for both logic and embedded SRAM. A general overview of power-gating methods is provided, including derivative techniques, trade-offs in power savings and frequency degradation, followed by power gate construction techniques, sizing and floorplan impacts, electrical analysis, IR/EM considerations, in-rush current and supply-noise control. Also discussed are implications for CAD tools for electrical analysis and verification, test, as well as system-level control of power islands.

Instructor: Stephen Kosonocky is a Fellow Design Engineer at Advanced Micro Devices Research and Development Laboratory, working from Fort Collins, CO, since 2007, focusing on low-power microprocessor design. Prior to AMD, he was with IBM T.J. Watson Research Center for 13 years, where he worked on embedded DRAM, SRAM, low-power circuits and microprocessors; Siemens Corporate Research for 6 years; and Samsung Princeton Design Center for 1 year. He received a BS, MS, and Ph.D. from Rutgers University, New Brunswick, in 1986, 1991 and 1994, respectively. He has authored or co-authored 49 publications and is an inventor on 34 issued patents.

T9: PLL Design in Nanometer CMOS

A PLL is perhaps the most widely used mixed-signal circuit block in an SoC. Advancements in process technology offer advantages as well as challenges for the design of PLLs. This tutorial highlights the challenges and present design techniques to overcome them. A brief discussion of PLL basics is presented first. Noise transfer functions from various points in the loop to the output are shown and the importance of having a low oscillator gain is highlighted. Optimization of loop parameters to minimize phase-noise and area is emphasized. Challenges posed by nanometer CMOS technology are then discussed. Circuit techniques to overcome these are discussed for critical building blocks. Process and temperature compensation techniques to minimize VCO gain, capacitance multiplication techniques to minimize loop-filter area, and a rail-to-rail output swing charge-pump with matched up/down currents to minimize spurs are a few of the circuit techniques that are discussed.

Instructor: K. R. (Kumar) Lakshmikumar received the Ph.D., in Electrical Engineering from Carleton University, Ottawa, Canada in 1985. He has been making significant contributions to many aspects of mixed-signal design such as, system design, chip-architecture, circuit design, characterization and testing, and introduction to manufacture. These designs address diverse applications such as, cellular telephony, serial data transceivers, and DSL systems. He has held senior engineering and management positions at Bell Labs, Multilink and Conexant Systems. He is currently with Ikanos Communications, Red Bank, NJ. He has many patents and papers to his credit. His paper on MOS device matching in the December 1986 issue of IEEE Journal of Solid-State Circuits is among the top 20 most referenced papers published by the journal between 1968 and 1992.

Sunday February 7th

F1: Silicon 3D-Integration Technology and Systems

Organizer: **Pascal Urard,** *STMicroelectronics, Crolles, France*

Co-organizer: **Ken Takeuchi,** *University of Tokyo, Tokyo, Japan*

Chair: **Kerry Bernstein,** *Applied Research Associates, South Royalton, VT*

Committee: **Hideto Hidaka,** *Renesas Techonology, Itami, Japan*
                     Michael Phan, *Qualcomm, Raleigh, NC*
                     Joo Sun Choi, *Samsung Electronics, Hwasung, Korea*
                     Bob Payne, *Texas Instruments, Dallas, TX*
                     Vladimir Stojanovic, *MIT, Cambridge, MA*
                     Kees Van Berkel, *ST- Ericsson, Eindhoven, The Netherlands*
                     Takayasu Sakurai*, University of Tokyo, Tokyo, Japan*

This Forum brings together 3D-integration technologies (System-in-Package, Through-Silicon-Via, Contactless-Chip-to-Chip-Communication,...), key components (SDRAM, flash, SoC, sensor,...) and 3D applications (imagers, smart phones, solid-state disk drives,...).

Key issues addressed by the panel experts will include:
    -3D-integration standards
    -3D-integration technologies: SiP, Chip-Scale Packages, Bit-Cost-Scalable 3D cell
        stacking, TSV, contactless interfaces,...
    -Power issues, mechanical issues, temperature distribution
    -Product benefits and yields

And, finally, the panel will provide an answer to the question: When will 3D be ready for show time?

Forum Agenda

Time	Topic
8:00	Breakfast
8:20	**Introduction** **Pascal Urard,** *STMicroelectronics, Crolles, France*
8:30	**3D TSVs - Ready for Design!** **Pol Marchal,** *IMEC, Leuven, Belgium*
9:15	**3D for Wireless Mobile Multimedia Applications -** **Opportunities and Challenges** **Georg Kimmich,** *ST-Ericsson, Grenoble, France*
10:00	Break
10:15	**Chip-Scale Camera Module Using Through-Silicon-Via** **Jean-Luc Jaffard,** *STMicroelectronics, Grenoble, France*
11:00	**2.5D & 3D ICs: Solutions & Challenges** **Ho-Ming Tong,** *ASE Group, Kaoshiung, Taiwan*
11:45	**Contactless Interfaces in 3D-Integration** **Hiroki Ishikuro,** *Keio University, Yokohama, Japan*
12:30	Lunch
1:30	**Advancements in SiP Integration and Interconnect Technology** **Flynn Carson,** *STATS ChipPACK, Singapore*
2:15	**TSV Technology and its Application to DRAM** **Uksung Kang,** *Samsung, Korea*
3.00	Break
3:15	**3D Flash Memory Technology and Circuit Design** **Yoshihisa Iwata,** *Toshiba, Yokohama, Japan*
4:00	**3D Integration Challenges in Computing** **Samuel Naffziger,** *AMD, Fort Collins, CO*
4:10	Panel Discussion
5:10	Conclusion

F2: Reconfigurable RF and Data Converters

Co-Organizers: **Stefan Heinen,** *RWTH Aachen University, Aachen, Germany*
               Domine Leenaerts, *NXP, Eindhoven,The Netherlands*

Committee: **Trudy Stetzler,** *Texas Instruments, Dallas, TX*
               Stefan Heinen, *RWTH Aachen University, Aachen, Germany*
               Domine Leenaerts, *NXP, Eindhoven, The Netherlands*
               Yiannos Manoli, *University of Freiburg, Freiburg, Germany*
               Jan Craninckx, *IMEC, Leuven, Belgium*
               Ali Niknejad, *University of California, Berkeley, CA*
               Didier Belot, *ST Microelectronics, Crolles, France*
               Raf Roovers, *NXP, Eindhoven, The Netherlands*
               K. P. Pun, *Chinese University of Hong Kong, China*
               Jed Hurwitz, *Gigle Semiconductor, Edinburgh, Scotland*

Digital cellular standards have emerged over the past 20 years. Today, 2G systems like GSM/EDGE are providing worldwide coverage for voice and basic data services. The increasing use by 4 billon users has led to high demand for low-cost multistandard multimode and multiband terminals. RF integration using reconfigurable circuits is a key technology for achieving the required technical performance, and more importantly, the needed cost position. Another important commercial aspect of mobile communication systems is the efficient usage of the available spectrum, using cognitive- radio techniques. The key requirement for this view of cognitive radio is a reconfigurable RF frontend, providing the required flexibility. Therefore, this Forum will investigate the current status of, and R&D trends in, reconfigurable systems, focusing on non-4G-based reconfigurable RF and reconfigurable data converters. Target systems include cognitive radio and multimode/multistandard systems, including short-range systems such as Bluetooth and WLAN. The Forum will cover reconfigurable RF frontends, their corresponding reconfigurable A/D converters, as well as performance-on-demand concepts, and adaptive power consumption.

Attendance is limited and pre-registration is required. This all-day Forum encourages open information exchange.

The targeted participants are circuit designers and concept engineers working on wireless systems, who want to learn about the impact of reconfigurability in the circuit and system design of RF transceivers.

Forum Agenda

Time	Topic
8:00	Breakfast
8:20	**Introduction**
	Stefan Heinen, *RWTH Aachen University, Aachen, Germany*
8:30	**Reconfigurable RF CMOS Circuits for Cognitive Radios**
	Kenichi Okada, *Tokyo Institute of Technology, Tokyo, Japan*
9:30	Break
10:00	**Sampled Analog Signal Processor for Cognitive Radio**
	Yann Deval, *University of Bordeaux, Bordeaux, France*
11:00	**Reconfigurable Multimode Frontends with Interference and Noise Rejection**
	Hooman Darabi, *Broadcom, Irvine, CA*
12:00	Lunch
1:00	**Reconfigurable Circuits for Wireless Communications**
	Stephane Boudaud, *CSR, Sophia Antipolis,France*
2:00	**Multi-Standard Radios for 2G and 3G**
	Harald Pretl, *DICE - Infineon, Linz, Austria*
3:00	Break
3:30	**Reconfigurable ADCs for 2G and 3G**
	Robert van Veldhoven, *NXP, Eindhoven, The Netherlands*
4:30	**Reconfigurable Radio Front-Ends in 40nm CMOS**
	Jan Craninckx, *IMEC, Leuven, Belgium*
5:30	Panel Discussion
6:00	Conclusions

ES1: Beyond CMOS - Emerging Technologies

Organizers: **Donhee Ham,** *Harvard University, Cambridge, MA*
                         David Scott, *TSMC, Hsinchu, Taiwan*

Chair: **Donhee Ham,** *Harvard University, Cambridge, MA*

CMOS integrated circuits represent an enormously successful electronics paradigm, which underpins today's personal computers and cellular phones. While the hegemony of CMOS integrated circuits in computation and information processing will undoubtedly last into the foreseeable future, researchers from many areas of science and technology have been seeking alternative or complementary solid-state circuit technologies using new physical devices. These new developments are exciting from research and intellectual points of view, but will they lead to important breakthroughs? This Session will provide the audience with opportunities to learn, ponder, criticize, or accept the new technologies and applications.

Time	Topic
8:00	**The Return of the Empty State: Vacuum Nanoelectronics for TeraHertz Applications** **Thomas H. Lee,** *Stanford University, Stanford, CA*
8:30	**Semiconductor Chips with Brain** **Peter Fromherz,** *Max Planck Institute, Martinsried, Germany*
9:00	**From Electronics to Plasmonics: One-Dimensional Plasmonic Circuits** **Xiaofeng Li,** *Harvard University, Cambridge, MA*
9:30	**Organic Transistors and Circuits** **Takayasu Sakurai,** *University of Tokyo, Tokyo, Japan*

ES2: Student Research Preview

The Student-Research Preview highlights selected student research projects. The Session consists of twenty-four 5-minute presentations by graduate students (Masters and PhD) from around the world, who have been selected on the basis of a short submission detailing their on-going research. Selection is based on the technical quality of their proposed work. Note that the work described is not intended to be complete or final.

This year, the Student-Research Preview (ES2) is scheduled as an evening session on Sunday, February 7, 2010, starting at 7:45pm, which is open to all ISSCC registrants.

Chair:	**Jan Van der Spiegel,** *University of Pennsylvania*
Co-Chair:	**Makoto Ikeda,** *University of Tokyo*
Co-Chair:	**Eugenio Cantatore**, *Tech. University of Eindhoven*
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    National Taiwan University
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SESSION 1

PLENARY SESSION — INVITED PAPERS

Chair: **Anantha Chandrakasan,** *Massachusetts Institute of Technology, Cambridge, MA*
ISSCC Conference Chair

Associate Chair:
Albert Theuwissen, *Harvest Imaging/Delft University of Technology, Bree, Belgium*
ISSCC Program Committee Chair

FORMAL OPENING OF THE CONFERENCE   **8:15AM**

1.1   **MEMS for Automotive and Consumer Applications**   **8:30AM**

Jiri Marek, Senior Vice President, Robert Bosch, Reutlingen, Germany

A car skids, and stabilizes itself without driver intervention; a laptop falls, and protects the hard drive automatically before impact on the floor; an airbag fires when triggered by a crash before the driver impacts the steering wheel, thereby significantly reducing physical injury; – all these systems are based exclusively on MEMS sensors. These crucial components of electronic systems are making system reactions to human needs more intelligent, and much faster than humans can provide.

In order to make these systems possible, sensors had to become smaller and more powerful, as well as more cost-effective, and less power-consuming. Such sensors can be realized by surface micro-machining. Thus, the development of these processes was the breakthrough leading to industrial mass-production for micro-electro-mechanical systems (MEMS). Besides leading-edge micromechanical processes, one needs innovative and robust ASIC designs, thorough simulations of electrical and mechanical behaviour, a deep understanding of the interactions (mainly over temperature and lifetime) of the package and the mechanical structures, and so on... Such understanding was achieved at Bosch over 20 years of intense and successful development activities, during which more than one billion sensors were produced.

The success story for MEMS sensors began with automotive applications. The first sensors fabricated using surface micro-machining were accelerometers for airbag systems, and gyroscopes for vehicle dynamics-control systems (ESP®). Today, it is hard to imagine a car without MEMS sensors! Our continuous development efforts led to miniaturized sensors which opened up new applications in consumer electronics. Thus, for example, an acceleration sensor can switch the cell-phone display from portrait to landscape format, depending on how the cell phone is being held; Or, a sensor installed in a laptop detects if a laptop has been dropped, and protects the hard drive against data loss, even before it hits the ground! In vehicle-navigation applications, a micromechanical pressure sensor can measure altitude with an accuracy of 25 centimetres. Such precise vertical location makes mobile navigation possible in 3-dimensional road networks, such as multilevel highways and parking structures, enabling automatic emergency-call exact-location systems. Other applications of micro-mechanical sensors in consumer electronics include weather stations, altimeters in watches, training monitors in shoes and sportswear, and intuitive user interfaces for cell phones, remote controls, and game consoles, that react to faint touches or changes in position.

This Plenary presenation will provide an overview of current MEMS applications (from sensors through inkjet heads to micromirrors) and of their market share. It will describe the processes needed for surface micro-machining, and emphasize the challenges of MEMS compared to standard IC design and fabrication. Following some examples of the evolution of MEMS designs, a short survey of MEMS activities at Bosch will be presented. Included will be a description of the newest inertial sensor for ESP®-systems. The presentation will conclude with an outlook on arising new MEMS applications such as in energy harvesters and micro-fuel-cells.

1.2   **Harnessing Technology to Advance the Next-Generation**   **9:10AM**
             Mobile User-Experience

Greg Delagi, Senior Vice-President, Texas Instruments, Dallas, TX

The current mobile-handset market is a vital and growing one, being driven by technology advances, including increased bandwidth and processing performance, as well as reduced power consumption and improved screen technologies. The 3G/4G handsets of today are multimedia internet devices with increased screen size, HD video and gaming, interactive touch screens, HD camera and camcorders, as well as incredible social, entertainment, and productivity applications.

While mobile-technology advancements to date have made us more social in many ways, new advancements over the next decade will bring us to the next level allowing mobile users to experience new types of "virtual" social interactions with all the senses. The mobile handsets of the future will be smart autonomous lifestyle devices with a multitude of incorporated sensors, applications and display options, all designed to make your life easier and more productive! With future display media, including 3D imaging, virtual interaction and conferencing will be possible, making every call feel like you are in the same room, providing an experience far beyond today's video conferencing technology. 3D touch screen with integrated image projection technologies will work in conjunction with gesturing to bring a new era of intuitive mobile-device applications, interaction, and information sharing.

Looking to the future, there are many challenges to be faced in delivering a smart mobile companion device that will meet the user demands. One demand will be for the availability of new and compelling services, and features on the "mobile companion". These mobile companions will be more than just Internet devices, and will function as on-the-go workstations, allowing users to function as if they were sitting in front of their computer in the office or at home. The massive amounts of data that will be transmitted through, to and from these mobile companions will require immense improvements in system performance, including specialized circuits, highly parallel architectures, and new packaging design.

Another concern of the smart-mobile-companion user will be that their device is able to deliver an always-on always-aware use in a way that is completely seamless and transparent. These handsets will automatically determine the best and most appropriate modem link from the multiple choices on the device, including WiFi, LTE, 5G, and mmWave, based on which link will optimize performance, battery life, and network charges to deliver the best possible user experience. In this future, adaptive connectivity will require many different solutions, including the standard modem technologies of today, as well as new man-machine interfaces and body-area-networks.

All of the new and exciting applications and features of these mobile- companion devices are going to require additional energy due to added computational requirements. However, a gap in energy efficiency is quickly developing between the energy that can be delivered by today's battery technologies, and the energy needed to deliver all-day operation or two-day always-on standby without a recharge. New innovations ranging from low-voltage digital and analog circuits, non-volatile memory, and adaptive power management, to energy harvesting, will be needed to further improve the battery life of these mobile-companion devices, extending their battery life to a week or more.

Increased bandwidth combined with decreased latency, lower power requirements combined with energy scavenging and harvesting, massive multimedia processing power, and new interface technologies will all work together to revolutionize how we interact with our smart-companion devices of the future. The implementation challenges to be faced in bringing these technologies to market may seem daunting and numerous at first, but with the strong collaboration in research and development from universities, government agencies, and corporations, the smart mobile-companion devices of the future will likely become reality within 10 years!

SESSION 1

BREAK   **10:25AM**

1.3   **Challenges of Image-Sensor Development**   **10:35AM**

Tomoyuki Suzuki, Senior Vice-President, Sony, Atsugi, Kanagawa, Japan

The semiconductor industry has flourished on a strong tide of computerization and digitalization.   Now, the new tide of network technology is rapidly extending the industry even further. Besides digitalization of text and numbers, digitalization of images has played an important role in accelerating this network trend. In this process, the development of image-sensing technologies has been indispensable. Moreover, we believe that image sensors will provide new growth opportunities for semiconductors, creating many innovations for future consumer and industrial markets.

From the viewpoint of the digital camera, the history of the semiconductor industry began in 1969 with the invention of the CCD image sensor at Bell Laboratories (for which the Nobel Prize was granted in 2009), with subsequent development by many companies starting in the 1970s. The first consumer-use of CCDs came in video cameras in the mid-1980s. Thereafter, with increasing CCD pixel density, the market for digital still cameras expanded very rapidly into the 21st century. In 2005, the digital HD video camera was launched, which was able to record a 1080i high definition image using a CMOS image sensor. CMOS image sensors have achieved strong performance through their high image quality and high speed. Accordingly, the market for CMOS-equipped D-SLR and cell phone cameras is expanding.

As a result of technology improvement, camera size has decreased by a factor of 500 in the last 25 years! This results primarily from pixel miniaturization in the image sensor. It is said that the photosensitivity of the image sensor per unit area has increased ten-fold per decade through the development of devices and process technologies for improving image quality. For example, in 1987 an n-type substrate was adopted for the CCD to shrink the pixel size, and to implement the electronic-shutter function. As well, a Tungsten light shield reduced the smear signal to -100dB for a pixel size of 3.9µm. This led to the 2M pixel digital still camera in 1999. In 1998, Sony began CMOS image sensor development targeting high-speed imaging. Read-out speed improvement was realized by raising the degree of parallelism. Recently, a 10M pixel CMOS image sensor with high image quality, providing more than 70dB dynamic range, and high-speed read-out of 576M pixels/s (10M pixels at 50 frames/s) has been developed. This sensor can also be operated in a 6M pixel mode at 60 frames/s with a 16:9 aspect ratio. This imager has been realized using two important technologies: the column ADC, and the back-illuminated structure. In the current consumer camera market, it has successfully created a new camera universe, providing not only the digital still camera but also video camera. From now on, cell phone cameras will adopt this type of CMOS image sensor.

In the future, the performance of the digital camera is expected to improve tremendously with the evolution of the CMOS image sensor. There are many "key milestones" in this evolution, such as "3D", "4K×2K", "global shutter", and so on. We are developing new materials, new structures, and new processes to achieve these new functions. With this evolution of the CMOS image sensor, the excitement and enjoyment of the imaging world will continue to spread even further!

1.4 **Nanoelectronics in Retrospect, Prospect and Principle** **11:15AM**

James Meindl, *Georgia Institute of Technology, Atlanta, GA*

The information revolution has been the paramount economic development of the past five decades. Its principal driver has been silicon microchip technology, which has advanced in productivity by a factor of approximately one billion and in performance by a factor of nearly one million (for microprocessor chips, for example). These concurrent advances have been implemented by a *synergistic fusion* of top-down directed assembly microtechnology (or scaling currently to the 25nm to 50nm range), and bottom-up self assembly nanotechnology producing 300mm diameter single crystal ingots of silicon. IGFET dynamic power-delay product is projected to continue to benefit from scaling. However, static gate-tunneling current and subthreshold channel leakage current, device parameter manufacturing tolerances and interconnect latency, severely aggravated by size effects in copper, progressively degrade from scaling. Consequently, novel *ancillary* technologies have been introduced, including: 1) increased chip input/output (I/O) interconnect density providing improved electrical and optical I/O bandwidth and reduced power distribution network noise; 2) improved heat removal, for example through microchannel fluidic cooling; and 3) 3D chip stacking with through-silicon vias to reduce cell multiprocessor-to-cache memory off-chip interconnect lengths are now projected as critical means of prolonging the exponential rate of the advance of silicon microchip technology. Following anticipated saturation of the advance of silicon technology early in the 2020 decade, a new *genre* of nanoelectronics is a coveted goal and one leading candidate appears to be graphene, particularly due to its ballistic carrier transport, adjustable energy band gap of nanoribbons, susceptibility to fusion of top-down and bottom-up nanotechnology, and potential for 3D monolithic integration. However, we have not yet witnessed in graphene the 21st century equivalents of two Nobel Prize winning inventions, the transistor and the integrated circuit!

CONCLUSION **11:55AM**

SESSION 2

2.1   A True Time-Delay-Based Bandpass Multi-Beam Array at mm-Waves Supporting Instantaneously Wide Bandwidths

1:30 PM

T-S. Chu, H. Hashemi
University of Southern California, Los Angeles, CA

A true time-delay-based bandpass multi-beam matrix at mm-waves is introduced that is suitable for applications with instantaneously wide bandwidth signals and for MIMO systems. A 0.13μm SiGe BiCMOS chip prototype covers the 30-to-40GHz frequency range instantaneously and supports 6 channels while producing 7 simultaneous beams with 18° spatial resolution and ±54° of spatial coverage.

2.2   A Wideband Beamformer for a Phased-Array 60GHz Receiver in 40nm Digital CMOS

2:00 PM

K. Raczkowski[1,2], W. De Raedt[1], B. Nauwelaers[2], P. Wambacq[1,3]
[1]IMEC, Heverlee, Belgium
[2]K.U. Leuven, Leuven, Belgium
[3]Vrije Universiteit Brussel, Brussels, Belgium

A programmable analog baseband beamformer for a 4-antenna 60GHz phased-array receiver is implemented in 40nm digital CMOS. It is based on current amplifiers employing shunt feedback. The phase shifter resolution is better than 20°, with a bandwidth of 1.7GHz, power consumption of 35mW, input-referred noise current of $170nA_{rms}$ and output IP3 of -6dBV.

2.3   A 60GHz-Band 2×2 Phased-Array Transmitter in 65nm CMOS

2:30 PM

W. L. Chan[1], J. R. Long[1], M. Spirito[1], J. J. Pekarik[2]
[1]Delft University of Technology, Delft, Netherlands
[2]IBM, Burlington, VT

A 60GHz-band 2×2 phased-array transmitter with independent tuning of vertical and horizontal polarizations is implemented in 65nm bulk CMOS. Two-dimensional phase tuning via LO phase shifting is implemented in a transmitter that adopts zero-IF upconversion with dynamic DC biasing to minimize LO feedthrough. The $2.9 \times 1.4mm^2$ chip consumes a total of 590mW from a 1V supply when driving all 4 channels at a maximum saturated output of 11dBm with 20dB gain per transmitter.

Break   3:00 PM

2.4   A 5.2-to-13GHz Class-AB CMOS Power Amplifier with a 25.2dBm Peak Output Power at 21.6% PAE

3:15 PM

H. Wang, C. Sideris, A. Hajimiri
California Institute of Technology, Pasadena, CA

A push-pull Class-AB CMOS PA is implemented using a broadband load-pull matching technique. The amplifier achieves a -3dB bandwidth of 5.2 to 13GHz with +25.2 dBm peak P_{sat} and 21.6% peak PAE. The EVM for QPSK (4.5MS/s) and 16-QAM (5MS/s) are below 2.9% and 6.8% at 1dB compression point. The measured BER for a wideband BPSK signal up to 7.5Gb/s is less than 10^{-13}.

2.5　A Passive-Mixer-First Receiver with Baseband-Controlled RF Impedance Matching, < 6dB NF, and > 27dBm Wideband IIP3

3:45 PM

C. Andrews, A. C. Molnar

Cornell University, Ithaca, NY

A passive-mixer-first receiver in 65nm CMOS is presented where baseband feedback resistors provide a tunable impedance match to the RF port using the transparency property of passive mixers. Tuned to an S_{11}<-12dB, the circuit achieves >27dBm wideband IIP3, <6dB NF and >70dB of gain with 60mW power consumption.

2.6　3.3GHz DCO with a Frequency Resolution of 150Hz for All-Digital PLL

4:15 PM

L. Fanori, A. Liscidini, R. Castello

University of Pavia, Pavia, Italy

A 3.3GHz DCO that achieves a minimum frequency quantization step of 150Hz without any dithering is presented. The fine digital tuning is obtained through a capacitive degeneration of a portion of the transistor switching pair used in a classical LC-tank oscillator. The DCO exhibits a phase noise of -127.5dBc/Hz @ 1MHz drawing 16mA from a 1.8V supply, resulting in an FoM of 183dBc/Hz. The active area is 700um×450um.

2.7　Suppression of Flicker Noise Upconversion in a 65nm CMOS VCO in the 3.0-to-3.6GHz Band

4:30 PM

S. Levantino, M. Zanuso, C. Samori, A. Lacaita

Politecnico di Milano, Milan, Italy

This work proposes a method to suppress upconversion of flicker noise of switching FETs in LC VCOs over a wide tuning range, without compromising startup and $1/f^2$ noise and with no trimming. A demonstrator fabricated in 65nm CMOS draws 0.6mA from a 1.2V supply and exhibits phase noise below -44dBc/Hz at 1kHz and -114dBc/Hz at 1MHz over the 3.0-to-3.6GHz tuning range.

2.8　A 9.2μA Gen 2 Compatible UHF RFID Sensing Tag with -12dBm Sensitivity and 1.25μV$_{rms}$ Input-Referred Noise Floor

4:45 PM

D. Yeager, F. Zhang, A. Zarrasvand, B. P. Otis

University of Washington, Seattle, WA

This work presents a 9.2μA fully-passive sensor tag in 0.13μm CMOS for biomedical research and human health monitoring. The sensor tag includes a 260nA temperature-compensated 3MHz reference oscillator. Subthreshold tag logic consumes 6μA from the 0.7V supply. A 1.2μA fully-differential chopper-stabilized amplifier with 1.25μV$_{rms}$ input-referred noise is integrated for sensor interfacing. The system exhibits a range of 3m and was deployed to perform wireless in-flight recording on a moth.

Conclusion　　　**5:15 PM**

SESSION 3

CELLULAR TECHNIQUES

Session Chair: Aarno Pärssinen, *Nokia, Helsinki, Finland*
Associate Chair: George Chien, *MediaTek, San Jose, CA*

3.1   A Quad-Band Class-39 RF CMOS Receiver for Evolved EDGE

1:30 PM

T. Dellsperger[1], D. Tschopp[1], J. Rogin[1], Y. Chen[1], T. Burger[2], Q. Huang[1,2]

[1]Advanced Circuit Pursuit, Zollikon, Switzerland

[2]ETH Zürich, Zürich, Switzerland

A single-chip RF receiver to support EDGE Evolution with downlink dual-carrier (DLDC) receive diversity and EVM <3% in all bands for demodulating 32-QAM signals is described. DLDC multislot class 39 and single-carrier multislot class 44 have been achieved. Both receive paths achieve a NF <2.5dB, an IIP3 >-3.5dBm in the GSM 850/900MHz band, and each draws <57mA from battery.

3.2   A 0.8mm^2 All-Digital SAW-Less Polar Transmitter in 65nm EDGE SoC

2:00 PM

J. Mehta[1], R. Staszewski[1,2], O. Eliezer[1], S. Rezeq[1], K. Waheed[1], M. Entezari[1], G. Feygin[1], S. Vemulapalli[1], V. Zoicas[1], C-M. Hung[1], N. Barton[1], I. Bashir[1], K. Maggio[1], M. Frechette[1] M-C. Lee[1], J. Wallberg[1], P. Cruise[1], N. Yanduru[1]

[1]Texas Instruments, Dallas, TX

[2]Delft University of Technology, Delft, Netherlands

A 0.8mm^2 small-signal polar EDGE TX, part of a 65nm CMOS SoC, incorporates a fully-digital implementation for the amplitude path meeting the strict emission mask without a SAW filter. Various RF impairments in the AM circuitry are digitally compensated, resulting in 2.5% rms EVM (high-band, HB) and over 8dB margin with the close-in mask. The TX consumes 105mA in HB at 1.2V.

3.3   A Tri-Band SAW-Less WCDMA/HSPA RF CMOS Transceiver with On-Chip DC-DC Converter Connectable to Battery

2:30 PM

Q. Huang[1,2], J. Rogin[1], X. Chen[1], D. Tschopp[1], T. Burger[2], T. Christen[1], D. Papadopoulos[1], I. Kouchev[1], C. Martelli[1,2], T. Dellsperger[1]

[1]Advanced Circuit Pursuit, Zollikon, Switzerland

[2]ETH Zürich, Zürich, Switzerland

A SAW-less (in Rx, Tx) tri-band (2 high, 1 low) WCDMA/HSPA transceiver IC is presented. An Rx IIP2 enhancement technique achieves IIP2 of +55dBm without production calibration or special processing steps. Integration of an on-chip DC-DC converter simplifies RF subsystem eBOM and reduces current drain from battery to 40mA/65mA in Rx, Tx mode, respectively.

Break   3:00 PM

3.4   A 45nm WCDMA Transmitter Using Direct Quadrature Voltage Modulator with High Oversampling Digital Front-End

3:15 PM

X. He, J. van Sinderen, R. Rutten

NXP Semiconductors, Eindhoven, Netherlands

A 45nm WCDMA transmitter using a direct quadrature voltage modulator with high oversampling digital front-end is described. The highly digitized transmitter realizes modulation in the voltage domain. Delivering 1dBm WCDMA output power, the transmitter achieves -158dBc/Hz noise and 2% EVM, while consuming 30mW including the digital front-end.

3.5   A 900MHz Direct ΔΣ Receiver in 65nm CMOS

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3:30 PM

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K. Koli[1], J. Jussila[1], P. Sivonen[1], S. Kallioinen[2], A. Pärssinen[2]

[1]Nokia Research Center, currently with ST-Ericsson, Turku, Finland

[2]Nokia Research Center, Otaniemi Lablet, Espoo, Finland

A 900MHz direct-conversion receiver with a ΔΣ feedback loop to RF occupies an active area of $1.2mm^2$ in 65nm CMOS. The concept prototype for low-band cellular operations achieves NF of 2.3 and 6.2 dB in conventional and ΔΣ modes, respectively, and out-of-band IIP3 up to +4 dBm when the ΔΣ loop is active. The chip consumes 80mW from a 1.2V supply.

3.6   A 10MHz Signal Bandwidth Cartesian-Loop Transmitter Capable of Off-Chip PA Linearization

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3:45 PM

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H. Ishihara, M. Hosoya, S. Otaka, O. Watanabe

Toshiba, Kawasaki, Japan

This paper presents a wide signal bandwidth Cartesian loop transmitter (CLT) for off-chip PA linearization. The CLT can linearize a 10MHz bandwidth signal by using a feedforward technique to avoid instability caused by a time delay of an RF path. ACLR is improved from 30.2dB to 38.4dB and EVM is improved from 5.9% to 1.6% when a 10MHz 64-QAM 802.16e signal is applied.

3.7   A 23mW Fully Integrated GPS Receiver with Robust Interferer Rejection in 65nm CMOS

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4:15 PM

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H. Moon, S. Lee, S-C. Heo, H. Yu, J. Yu, J-S. Chang, S-I. Choi, B-H. Park

Samsung Electronics, Yongin, Korea

A $2.5 mm^2$ GPS radio chip with a robust interference rejection performance working in the L1 band at 1575.42MHz is implemented in a 65nm CMOS process. The receiver with internal LNA shows 2.3dB NF, 30dB IRR, and -15dBm blocker IP_{1dB} at 1710MHz. Power consumption of 23mW from a single 1.8V supply is achieved by using a switched-mode power supply (SMPS).

3.8   A Low-Power Low-Noise Direct-Conversion Front-End with Digitally Assisted IIP2 Background Self Calibration

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4:45 PM

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Y. Feng[1], G. Takemura[2], S. Kawaguchi[2], N. Itoh[2], P. Kinget[1]

[1]Columbia University, New York, NY

[2]Toshiba, Kawasaki, Japan

A low-power, low-noise direct-conversion 1.8GHz front-end for WCDMA-type applications features an efficient, robust, digitally assisted self-calibration loop that maintains the IIP2 of the receiver to better than 60dBm. It has a conversion gain of 38.5dB, a DSB NF of 2.6dB, and an IIP3 of -17.6dBm, consumes 15mA from a 1.5V supply, and occupies $1.56mm^2$ in a 0.13μm CMOS process.

<div align="center">

Conclusion   **5:00 PM**

</div>

SESSION 4

ANALOG TECHNIQUES

Session Chair: Doug Smith, *SMSC, Austin, TX*
Associate Chair: Chris Mangelsdorf, *Analog Devices, Tokyo, Japan*

4.1   A Thermal-Diffusivity-Based Frequency Reference in Standard CMOS with an Absolute Inaccuracy of ±0.1% from -55°C to 125°C

1:30 PM

M. Kashmiri, M. Pertijs, K. Makinwa
Delft University of Technology, Delft, Netherlands

An on-chip frequency reference exploiting the well-defined thermal diffusivity of IC-grade silicon has been realized in a standard 0.7μm CMOS process. It has an output frequency of 1.6MHz, and achieves an absolute inaccuracy (device-to-device spread) of ±0.1% from -55°C to 125°C, and a temperature coefficient of ±11.2ppm/°C, while dissipating 7.8mW from a 5V supply.

4.2   A Micropower Chopper-Correlated Double-Sampling Amplifier with 2μV Standard Deviation Offset and 37nV/√Hz Input Noise Density

2:00 PM

M. Belloni[1], E. Bonizzoni[1], A. Fornasari[2], F. Maloberti[1]
[1]University of Pavia, Pavia, Italy   [2]National Semiconductor, Rozzano, Italy

A chopper ripple-free circuit with input noise density of 37nV/√Hz is presented. The CMOS scheme chops the input and demodulates the result after amplification with CDS. Offset temperature dependence is better than 0.03μV/°C. The analog current consumption is 12.8μA with supplies ranging from 1.8V to 5V. The noise efficiency factor is 5.5.

4.3   A Single-Trim CMOS Bandgap Reference with a 3σ Inaccuracy of ±0.15% from -40°C to 125°C

2:30 PM

G. Ge[1], C. Zhang[1], G. Hoogzaad[1], K. Makinwa[2]
[1]NXP Semiconductors, Nijmegen, Netherlands
[2]Delft University of Technology, Delft, Netherlands

A CMOS bandgap reference with a 3σ inaccuracy of ±0.15% from -40°C to 125°C is presented. This level of precision is achieved by a single PTAT trim at room temperature, together with the use of chopping and higher-order curvature correction to remove non-PTAT errors. The bandgap reference draws 55uA from a 1.8V supply, and occupies 0.12mm² in 0.14μm CMOS.

4.4   A 21nV/√Hz Chopper-Stabilized Multipath Current-Feedback Instrumentation Amplifier with 2μV Offset

2:45 PM

Q. Fan, J. H. Huijsing, K. A. Makinwa
Delft University of Technology, Delft, Netherlands

This paper describes a chopper-stabilized current-feedback instrumentation amplifier (CFIA) with a ripple-reduction loop (RRL). A smooth 1st-order response is obtained by embedding the RRL in a multipath structure to bury the notch caused by the RRL. The CFIA achieves 2μV offset, 21nV/√Hz with NEF of 9.6. The CFIA can also be configured as an opamp which achieves 2× reduction in NEF.

Break   3:00 PM

4.5   A 10mW Stereo Audio CODEC in 0.13μm CMOS

3:15 PM

X. Jiang[1], J. Song[1], T. L. Brooks[1], J. Chen[1], V. Chandrasekar[1], F. Cheung[1], S. Galal[1], D. Cheung[1], G. Ahn[2], M. Bonu

[1]Broadcom, Irvine, CA   [2]Sogang University, Seoul, Korea

A 1.5V stereo audio CODEC in 0.13μm CMOS demonstrates circuit techniques that minimize power consumption for microphone and speaker interfaces. The CODEC includes a 0.35mA microphone PGA, a 0.35mA continuous-time ΔΣ ADC and a 1mA Class-AB speaker amplifier. The audio input and output paths achieve 92dB and 98dB SNR, respectively, with 6.5mA total stereo current.

4.6   Class-G Headphone Driver in 65nm CMOS Technology

3:45 PM

A. Lollio[1], G. Bollati[2], R. Castello[1]
[1]University of Pavia, Pavia, Italy
[2]Marvell, Pavia, Italy

A 65nm CMOS Class-G headphone driver operates from ±1.4V, ±0.35V supplies. At low power level it uses the low voltage supply to reduce the dissipation to 1.63mW @ Pout=0.5mW into 32Ω. At higher power level, the smooth transition between the voltage supply rails allows a THD+N better than -80dB for Pout≤16mW into 32Ω. The SNR is 101dB, quiescent power is 0.41mW and active die area is 0.14mm^2.

4.7   45nm CMOS 8Ω Class-D Audio Driver with 79% efficiency and 100dB SNR

4:15 PM

S. Samala, V. Mishra, K. Chakravarthi
Texas Instruments, Bangalore, India

A direct battery connect (2.35V to 5.5V) 100dB SNR Class-D audio driver in 45nm CMOS is presented. At 3.5V supply, 525mW is delivered into an 8Ω load with 79% efficiency.

4.8   A 105dB-Gain 500MHz-Bandwidth 0.1Ω-Output-Impedance Amplifier for an Amplitude Modulator in 65nm CMOS

4:30 PM

C. Kim[1,2], C-S. Chae[1], Y-S. Yuk[1], Y-G. Kim[3], J-K. Kwon[3], G-H. Cho[1]
[1]KAIST, Daejeon, Korea
[2]Hynix Semiconductor, Gyeonggi, Korea
[3]Electronics and Telecommunications Research Institute, Daejeon, Korea

A 500MHz -3dB bandwidth linear amplifier in 65nm CMOS at 1.2V supply is presented for an amplitude modulator in a polar transmitter. The design uses a gain-boosting scheme for 105dB DC gain at an 8Ω load and a buffered switching Class-AB bias scheme. It has 0.1Ω output impedance at 5MHz and can drive 60mA peak current. The chip efficiency is 83.5% and area is 1.35mm^2.

4.9   A 3.4GHz-Sample-Rate 800MHz-Bandwidth Highly Reconfigurable Analog FIR Filter in 45nm CMOS

4:45 PM

E. Rouat[1], E. O'hAnnaidh[2], S. Verhaeren[1], S. Le Tual[1], C. Garnier[1]
[1]STMicroelectronics, Crolles, France   [2]ST-Ericsson, Crolles, France

A 16-tap analog FIR filter with 3.2GHz-clock achieves fully reconfigurable transfer functions over an 800MHz range. Time domain convolution is realized by switching programmable transconductance values and exploiting a current integration technique to merge sampling, summing and anti-aliasing functions. The circuit draws 65mW from a 1.1V supply and occupies 0.15mm^2 in 45nm CMOS.

4.10   A 34dB SNDR Instantaneously-Companding Baseband SC Filter for 802.11a/g WLAN Receivers

5:00 PM

V. Maheshwari[1], W. A. Serdijn[1], J. R. Long[1], J. J. Pekarik[2]
[1]Delft University of Technology, Delft, Netherlands
[2]IBM, Burlington, VT

To handle peak-to-average power ratio in 802.11a/g WLAN RX baseband, a 5th-order, 10.5MHz cut-off frequency, instantaneously companding SC LPF is fabricated in a 0.13μm CMOS process. It occupies 2.2mm^2 active chip area and consumes 53mW with a DR of 79dB over an SNDR of 34dB and EVM$_{rms}$<3.8%, saving 3.3× power and 1.5× chip area as compared to the non-companding case.

Conclusion 5:15 PM

SESSION 5

PROCESSORS

Session Chair: Stefan Rusu, *Intel, Santa Clara, CA*
Associate Chair: Sonia Leon, *Sun Microsystems, Santa Clara, CA*

5.1 Westmere: A Family of 32nm IA Processors

1:30 PM

N. A. Kurd, S. Bhamidipati, C. Mozak, J. L. Miller, T. Wilson, M. Nemani, M. Chowdhury

Intel, Hillsboro, OR

Westmere is a family of next-generation IA processors for mobile, desktop and server segments on a second-generation high-κ metal-gate 32nm process offering increased core count, cache size, and frequency within same power envelope as the previous generation with further improvements in power efficiency, rich set of new features, and support for low-voltage DDR3.

5.2 A 40nm 16-Core 128-Thread CMT SPARC SoC Processor

2:00 PM

J. Shin, K. Tam, D. Huang, B. Petrick, H. Pham, C. Hwang, H. Li, A. Smith, T. Johnson, F. Schumacher, D. Greenhill, A. Leon, A. Strong

Sun Microsystems, Santa Clara, CA

A 16-core SPARC SoC processor enables up to 512 threads in a 4-way glueless system to maximize throughput. The 6MB L2 cache of 461GB/s and the 308-pin SerDes I/O of 2.4Tb/s support the required bandwidth. Six clock and four voltage domains, as well as power management and circuit techniques, optimize performance, power, variability and yield trade-offs across the $377mm^2$ die.

5.3 A 45nm 37.3GOPS/W Heterogeneous Multi-Core SoC

2:30 PM

Y. Yuyama[1], M. Ito[1], Y. Kiyoshige[1], Y. Nitta[1], S. Matsui[1], O. Nishii[1], A. Hasegawa[1], M. Ishikawa[2], T. Yamada[2], J. Miyakoshi[2], K. Terada[2], T. Nojiri[2], M. Satoh[2], H. Mizuno[2], K. Uchiyama[2], Y. Wada[3], K. Kimura[3], H. Kasahara[3], H. Maejima[4]

[1]Renesas Technology, Kodaira, Japan   [2]Hitachi, Kodaira, Japan

[3]Waseda University, Shinjuku, Japan   [4]Tokyo Institute of Technology, Yokohama, Japan

A 648MHz $153.8mm^2$ 45nm CMOS SoC integrates eight general-purpose CPUs, four dynamically reconfigurable processors, two 1024-way matrix-processors, peripherals and interfaces. Using core enhancement, DDR3-I/F improvement and clock buffer deactivation, this SoC achieves 37.3GOPS/W at 1.15V.

Break   3:00 PM

5.4 The Implementation of POWER7™: A Highly Parallel and Scalable Multi-Core High-End Server Processor

3:15 PM

D. Wendel[1], R. Kalla[2], R. Cargoni[2], J. Clables[2], J. Friedrich[2], J. Kahle[2], B. Sinharoy[3], W. Starke[2], S. Taylor[2], S. Weitzel[2], S. G. Chu[2], S. Islam[2], V. Zyuban[4]

[1]IBM, Boeblingen, Germany   [2]IBM, Austin, TX

[3]IBM, Poughkeepsie, NY   [4]IBM T.J. Watson, Yorktown Heights, NY

POWER7™ the next generation processor of the POWER™ family is introduced. The 8-core chip, supporting 32 threads, is implemented in 45nm 11M CMOS SOI. The 32kB L1 caches feature 1 read port banked write for the I-cache and 2 read ports banked write for the D-cache. The on-chip cache hierarchy consists of a 256kB fast, private SRAM L2 and a 32MB shared L3, implemented in embedded DRAM.

5.5   A Wire-Speed Power™ Processor: 2.3GHz 45nm SOI with 16 Cores and 64 Threads

3:45 PM

C. Johnson[1], D. H. Allen[2], J. Brown[2], S. Vanderwiel[2], R. Hoover[2], H. Achilles[3],
C-Y. Cher[4], G. A. May[5], H. Franke[4], J. Xenedis[4], C. Basso[6]
[1]IBM Research, Rochester, MN   [2]IBM Systems and Technology Group, Rochester, MN
[3]IBM Systems and Technology Group, Bedford, NH
[4]IBM Research, Yorktown Heights, NY
[5]IBM Systems and Technology Group, Essex Junction, VT
[6]IBM Systems and Technology Group, Raleigh, NC

A 64-thread simultaneous multi-threaded processor uses architecture
and implementation techniques to achieve high throughput at low power.
Included are static V_{DD} scaling, multi-voltage design,
clock gating, multiple V_T devices, dynamic thermal control,
eDRAM and low-voltage circuit design. Power is reduced by >50% in a
428mm^2 chip. Worst-case power is 65W at 2.0GHz, 0.85V.

5.6   An x86-64 Core Implemented in 32nm SOI CMOS

4:15 PM

R. Jotwani[1],   S. Sundaram[1],   S. Kosonocky[2],   A. Schaefer[1],   V. Andrade[1],   G. Constant[1],   A. Novak[1],
S. Naffziger[2]
[1]AMD, Austin, TX   [2]AMD, Fort Collins, CO

The 32nm implementation of an AMD x86-64 core occupying 9.69mm^2 and containing more than 35 million transistors (excluding L2 cache), operates at frequencies >3GHz. The core incorporates numerous design and power improvements to enable an operating range of 2.5 to 25W and a zero-power gated state that make the core well-suited to a broad range of mobile and desktop products.

5.7   A 48-Core IA-32 Message-Passing Processor with DVFS in 45nm CMOS

4:45 PM

J. Howard[1], S. Dighe[1], Y. Hoskote[1], S. Vangal[1], D. Finan[1], G. Ruhl[1], D. Jenkins[1], H. Wilson[1], N. Borkar[1],
G. Schrom[1], F. Pailet[1], S. Jain[2], T. Jacob[2], S. Yada[2], S. Marella[2], P. Salihundam[2], V. Erraguntla[2],
M. Konow[3], M. Riepen[3], G. Droege[3], J. Lindemann[3], M. Gries[3], T. Apel[3], K. Henriss[3], T. Lund-Larsen[3],
S. Steibl[3], S. Borkar[1], V. De[1], R. Van Der Wijngaart[4], T. Mattson[5]
[1]Intel, Hillsboro, OR   [2]Intel, Bangalore, India   [3]Intel, Braunschweig, Germany
[4]Intel, Santa Clara, CA   [5]Intel, DuPont, WA

A 567mm^2 processor on 45nm CMOS integrates 48 IA-32 cores and 4 DDR3 channels in a 6×4 2D-mesh network. Cores communicate through message passing using 384KB of on-die shared memory. Fine-grain power management takes advantage of 8 voltage and 28 frequency islands to allow independent DVFS of cores and mesh. As performance scales, the processor dissipates between 25W and 125W.

5.8   A 4.1Tb/s Bisection-Bandwidth 560Gb/s/W Streaming Circuit-Switched 8×8 Mesh Network-on-Chip in 45nm CMOS

5:15 PM

M. A. Anders, H. Kaul, S. K. Hsu, A. Agarwal, S. K. Mathew, F. Sheikh, R. K. Krishnamurthy, S. Borkar
Intel, Hillsboro, OR

An on-die multi-core circuit-switched network achieves 2.64Tb/s throughput for an 8×8 2D mesh, consuming 4.73W in 45nm CMOS at 1.1V and 50°C. Pipelined circuit-switched transmission, circuit channel queue circuits and dual supplies enable up to 1.51Tb/s/W energy efficiency, with scalable streaming performance of 6.43Tb/s.

Conclusion   5:30 PM

SESSION 6

Session Chair: Iliana Fujimori-Chen, *Analog Devices, Wilmington, MA*
Associate Chair: Roland Thewes, *TU Berlin, Berlin, Germany*

6.1   A Mobile-Display-Driver IC Embedding a Capacitive-Touch-Screen Controller System

1:30 PM

H-R. Kim, Y-K. Choi, S-H. Byun, S-W. Kim, K-H. Choi, H-Y. Ahn, J-K. Park, D-Y. Lee, Z-Y. Wu, H-D. Kwon, Y-Y. Choi, C-J. Lee, H-H. Cho, J-S. Yu, M. Lee
Samsung Electronics, Yongin, Korea

We present a display-driver IC embedding a capacitive-touch-screen controller. It is designed to operate with conventional overlay-type and on-cell touch display panels. The IC exhibits performance of 40ms latency and 120Hz update rate within ±0.5mm jitter. It has been evaluated on a 16.7M-color wQVGA AMOLED panel with on-cell touch screen.

6.2   A Double-Loop Control LED Backlight Driver IC for Medium-Sized LCDs

2:00 PM

S-I. Hong[1], J-W. Han[1], D-H. Kim[2], O-K. Kwon[1]
[1]Hanyang University, Seoul, Korea   [2]Silicon Mitus, Seoul, Korea

We present an LED backlight driver IC that uses a double loop control method to achieve 50kHz PWM dimming frequency with 8b resolution. The measured output voltage of the boost converter is 26.41V and its maximum ripple voltage is 500mV$_{pp}$. Measured rise and fall times of the LED current are 86ns and 7ns, respectively.

6.3   Stable RGBW AMOLED Display with OLED Degradation Compensation Using Electrical Feedback

2:30 PM

G. Chaji[1], S. Alexander[1], J. Dionne[1], Y. Azizi[1], C. Church[1], J. Hamer[2], J. Spindler[2], A. Nathan[1,3]
[1]Ignis Innovation, Kitchener, Canada   [2]Eastman Kodak, Rochester, NY
University College London, London, United Kingdom

We present an electronic monitoring and feedback scheme for an AMOLED display that substantially reduces the appearance of image degradation and increases useful lifetime. We describe the methodology and show results on a 32-inch 1080p OLED display that establishes the benefits. We further explain how the same technique can be used as a diagnostic tool to identify and discriminate among defects introduced during the manufacturing process.

Break   3:00 PM

6.4   An Inductively Powered Scalable 32-Channel Wireless Neural Recording System-on-a-Chip for Neuroscience Applications

3:15 PM

S. Lee, H-M. Lee, M. Kiani, U-M. Jow, M. Ghovanloo
Georgia Institute of Technology, Atlanta, GA

An inductively powered 32-channel wireless integrated neural recording system, capable of endless recording from small freely behaving animals, is reported. A power scheduling mechanism maintains the power consumption of the LNAs constant regardless of the number of channels. Closed-loop power transmission maintains the received power constant despite animal movements.

6.5   A 20µW Neural Recording Tag with Supply-Current-Modulated AFE in 0.13µm CMOS

3:30 PM

Z. Xiao, C-M. Tang, C. M. Dougherty, R. Bashirullah

University of Florida, Gainesville, FL

A 20µW wirelessly powered implantable neural recording system, with adaptively tuned bandwidth and sample rate, utilizes a duty-cycled amplifier and communication scheme to minimize power. Backscattering and a supply-current-modulated AFE allow for remote powering or battery operation, with amplifier current of 0.8µA. The circuit occupies 1.54mm^2 in 0.13µm CMOS.

6.6   A 30µW Analog Signal Processor ASIC for Biomedical Signal Monitoring

3:45 PM

R. F. Yazicioglu[1], S. Kim[1], T. Torfs[1], P. Merken[2], C. Van Hoof[1,3]

[1]IMEC, Leuven, Belgium

[2]RMA, Brussels, Belgium

[3]K.U. Leuven, Leuven, Belgium

An analog signal processor ASIC for ECG signals is presented. In addition to the power efficient extraction of ECG signals, it proposes an adaptive sampling scheme for data reduction, continuous-time electrode-tissue impedance monitoring for sensing motion artifacts, and band-power extraction for beat detection. The ASIC operates on a 2V supply.

6.7   A 1V 22µW 32-Channel Implantable EEG Recording IC

4:15 PM

X. Zou, W-S. Liew, L. Yao, Y. Lian

National University of Singapore, Singapore, Singapore

An implantable EEG recording IC including 32 analog low noise amplifiers, band-pass filters, adjustable gain stages, and a 10b SAR ADC is presented. The chip, implemented in 0.35µm CMOS process, achieves 1.15µV$_{rms}$ total noise in a 0.5-to-150Hz band and consumes 22µW from a 1V supply, attaining a noise efficiency factor of 2.24.

6.8   A Timing Controlled AC-DC Converter for Biomedical Implants

4:30 PM

E. K. Lee

Alfred Mann Foundation, Santa Clarita, CA

An AC-DC converter is designed for supplying light-load digital circuits in a biomedical implant. When the AC input is just above the DC output (VDCo), a boosted switch is turned on and then turned off according to the load current by controlling the switch timing via a feedback loop. A power efficiency of 93.8% is achieved with a 3.5V peak AC input, VDCo = 2V, and an output power of 10mW.

6.9   A CMOS Electrochemical Impedance Spectroscopy Biosensor Array for Label-Free Biomolecular Detection

4:45 PM

A. Manickam, A. Chevalier, M. McDermott, A. D. Ellington, A. Hassibi

University of Texas, Austin, TX

A fully integrated 10×10 electrochemical impedance spectroscopy array is designed for label-free biomolecular detection applications. Each biosensor pixel includes an on-chip bio-functionalized electrode and a direct-conversion receiver capable of measuring complex admittance levels as low as $10^{-9}\Omega^{-1}$ with a dynamic range larger than 90dB in a 10Hz-to-50MHz frequency range.

Conclusion 5:15 PM

ES3: Energy-Efficient High-Speed Interfaces

Organizers: **Naresh Shanbhag,** *University of Illinois at Urbana-Champaign, Urbana, IL*
                 Koichi Yamaguchi, *NEC, Kanagawa, Japan*
Chair: **Robert Payne,** *Texas Instruments, Dallas, TX*

Power consumption of interface circuits is becoming an important issue as new applications requiring distributed processing emerge, and/or the demand for large-scale data centers grows. Techniques, such as advanced signal processing, optical I/O interconnect, and through-silicon vias (TSV) have emerged as potential solutions for low-power high-data-rate interface circuits. The goal of this Session is to address the following questions: Where is power consumed in a data center? What are the circuit- and system-level challenges in designing energy-efficient interface circuits? What technology options are available for interface power reduction? What are the performance, power, and cost trade-offs in designing high-speed interfaces of the future?

Time	Topic

8:00   **Power Issues in Data Centers: Trends and Technologies**
                 Subodh Bapat, *SUN Microsystems, Menlo Park, CA*

8:25   **Getting PHY Power into Balance**
                 Brian Leibowitz, *Rambus, Los Altos, CA*

8:50   **Optical I/O Opportunities for Energy-Efficient and Small Form-Factor**
          Inter-Chip Communication
                 Ian Young, *Intel, Hillsboro, Oregon*

9:15   **Inductively Coupled Through-Chip Interface**
                 Tadahiro Kuroda, *Keio University, Yokohama, Japan*

9:40   **Panel Discussion**

ES4: Fusion of MEMS and Circuits

Organizer: **Satoshi Shigematsu,** *NTT, Atsugi, Japan*
Organizer: **Kazutami Arimoto,** *Renesas Technology, Hyogo, Japan*
Chair: **Christoph Hagleitner,** *IBM Zurich Research Lab, Switzerland*

The rapidly growing demand for sensor devices which use MEMS (measuring acceleration, gas, pressure, and so on) will drive the fusion of MEMS and circuits. This fusion is key to scaling at a rate that is "More than Moore". Today's devices use MEMS technology for inductors and capacitors. In the future, MEMS and circuits will be combined not only physically but for architecture, verification, modeling, manufacturing, testing, software, and algorithms. This Session will describe the requirements of tightly integrated MEMS and circuits, integrated design techniques, system examples, and the future collaboration of designers and researchers of integrated MEMS and circuits.

Time	Topic

8:00   **State of Arts and Future of the Fusion of MEMS and Circuits**
                 Kazuya Masu, *Tokyo Institute of Technology, Yokohama, Japan*

8:20   **Digital Light Processing (DLP®) Technology - The Fusion of Digital Optical**
          MEMS, CMOS, and Algorithms
                 Jim Hall, *Texas Instruments, Plano, TX*

8:40   **Fusion of MEMS Sensors and Circuits - Inertial Sensor as an Example**
                 Kazusuke Maenaka, *University of Hyogo, Himeji, Japan*

9:00   **The Fusion of Design Environments: An EDA-Compatible MEMS+IC**
          Design Platform
                 Matton Kamon, *Coventor, Cambridge, MA*

9:20   **MEMS Sensors at the Heart of Consumer Electronics and Mobile Handsets**
                 Fabio Pasolini, *STMicroelectronics, Milan, Italy*

EP1: Analog Circuits: Stump the Panel

Organizers: **Jed Hursitz,** *Gigle Semiconductor, Edinburgh, United Kingdom*
                     Chris Mangelsdorf, *Analog Devices, Tokyo, Japan*
                     Bill Redman-White, *NXP/Southampton University,*
                                 Southhampton, United Kingdom

Moderators: **Bill Redman-White**, *NXP/Southampton University,*
                                 Southhampton, United Kingdom
                     Chris Mangelsdorf, *Analog Devices, Tokyo, Japan*

We have assembled a group of "Analog Agony Uncles" to take your questions in a light-hearted game show format - if the experts cannot either (a) deliver an intelligent answer, or (b) make us all laugh, then a prize could be yours! Questions should be submitted in advance so we can load them on the computer ready for the panel session. Send us problems and riddles that will baffle our experts and impress your friends ... recruiters welcome. To submit your (possibly)-prize-winning problem, visit our website: www.analogevents.com/isscc2010.

Panelists:

       Bob Pease, *National Semiconductor, Santa Clara, CA*
       Willy Sansen, *Katholieke Universitat, Leuven, Belgium*
       Bob Blauschild, *Consultant, Los Gatos, CA*
       Barrie Gilbert, *Analog Devices, Beaverton, OR*
       Yannis Tsividis, *Columbia University, New York, NY*
       Akira Matsuzawa, *Tokyo Institute of Technology, Tokyo, Japan*

SESSION 7

DESIGNING IN EMERGING TECHNOLOGIES
Session Chair: Satoshi Shigematsu, *NTT Electronics, Yokohama, Japan*
Associate Chair: Shekhar Borkar, *Intel, Hillsboro, OR*

7.1 A 3V 6b Successive-Approximation ADC Using Complementary Organic Thin-Film Transistors on Glass

8:30 AM

W. Xiong[1], U. Zschieschang[2], H. Klauk[2], B. Murmann[1]

[1]Stanford University, Stanford, CA

[2]Max Planck Institute for Solid-State Research, Stuttgart, Germany

A successive-approximation ADC is implemented in an organic thin-film process. The design uses an auto-zeroed, inverter-based comparator and on-chip calibration to achieve 6b precision in presence of large component variation. The ADC is fabricated on a glass substrate and uses 53 p- and n-type organic transistors and 19 capacitors.

7.2 An Analog Organic First-Order CT $\Delta\Sigma$ ADC on a Flexible Plastic Substrate with 26.5dB Precision

9:00 AM

H. Marien[1], M. Steyaert[1], N. van Aerle[2], P. Heremans[1,3]

[1]K.U. Leuven, Leuven, Belgium   [2]Polymer Vision, Eindhoven, Netherlands   [3]IMEC, Heverlee, Belgium

We present an analog organic first-order CT $\Delta\Sigma$ ADC fabricated with a dual-gate organic electronic technology on plastic foil. This analog circuit achieves a 26.5dB precision and performs at a clock speed up to 500Hz. It consumes 100µA at15V. The circuit is designed following a V_t-insensitive design strategy and applies high-pass filters for offset cancellation. The active area is $13\times20mm^2$.

7.3 User Customizable Logic Paper (UCLP) with Organic Sea-of Transmission-Gates (SOTG) Architecture and Ink-Jet Printed Interconnects

9:30 AM

K. Ishida[1], N. Masunaga[1], R. Takahashi[1], T. Sekitani[1], S. Shino[2], U. Zschieschang[3], H. Klauk[3], M. Takamiya[1], T. Someya[1], T. Sakurai[1]

[1]University of Tokyo, Tokyo, Japan   [2]Mitsubishi Paper Mills, Kyoto, Japan

[3]Max Planck Institute for Solid-State Research, Stuttgart, Germany

User customizable logic paper (UCLP) with a sea-of-transmission-gates (SOTG) of organic CMOS transistors is developed to enable users to fabricate custom integrated circuits by printing 200µm width interconnects with at-home ink-jet printers for educational purposes. Compared with the conventional gate array, the SOTG reduces the area of the circuits by 11 to 85%.

Break   10:00 AM

7.4 Robust Digital Design in Organic Electronics by Dual-Gate Technology

10:15 AM

K. Myny[1,2], M. J. Beenhakkers[3], N. A. van Aerle[3], G. H. Gelinck[4], J. Genoe[1,5], W. Dehaene[1,2], P. Heremans[1,2]

[1]IMEC, Leuven, Belgium   [2]K.U. Leuven, Leuven, Belgium

[3]Polymer Vision, Eindhoven, Netherlands

[4]TNO Science and Industry, Eindhoven, Netherlands

[5]Katholieke Hogeschool Limburg, Diepenbeek, Belgium

A comprehensive study of dual-gate organic thin-film transistors targeting more robust organic circuitry is performed. The difference between zero-V_{gs}-load and diode-load logic is studied and an optimized design for both is presented. This new design is used in 99-stage ring oscillators, to determine stage delays, and in 64b RFID transponder chips yielding data rates of 4.3kb/s.

7.5 An Integrated Organic Circuit Array for Flexible Large-Area Temperature Sensing

10:30 AM

D. He, I. A. Nausieda, K. K. Ryu, A. I. Akinwande, V. Bulovic, C. G. Sodini

Massachusetts Institute of Technology, Cambridge, MA

An integrated organic temperature-sensing circuit array compatible with flexible and large-area substrates is presented. The array outputs an average value of 6.8mV/°C, which is 22× more responsive than the MOSFET implementation while dissipating 90nW/cell. Highly linear outputs enable two-point calibrations that remove the effects of cell-to-cell variation.

7.6   Capacitively Coupled Non-Contact Probing Circuits for Membrane-Based Wafer-Level Simultaneous Testing

10:45 AM

M. Daito[1], Y. Nakata[1], S. Sasaki[1], H. Gomyo[1], H. Kusamitsu[1], Y. Komoto[1], K. Iizuka[1], K. Ikeuchi[2], G. Kim[2], M. Takamiya[2], T. Sakurai[2]

[1]Association of Super-Advanced Electronics Technologies, Yokohama, Japan

[2]University of Tokyo, Tokyo, Japan

A capacitively coupled probing circuit with a de-skewer, a low-pass filter and a weak-feedback receiver realize membrane-based wafer-level simultaneous testing robustly with more than 300Kpin connections. Both the probe chip and 300mm DUT-wafer are fabricated in 90nm and the measured power consumption of RX core is 0.5mW with BER of 10^{-12} at 1Gb/s.

7.7   A Wafer-Level Heterogeneous Technology Integration for Flexible Pseudo-SoC

11:00 AM

H. Yamada, Y. Onozuka, A. Iida, K. Itaya, H. Funaki

Toshiba, Kawasaki, Japan

A flexible pseudo-SoC incorporating electrostatic MEMS grating light valves and 40V high-speed puls-width modulator (PWM) driver CMOS chip is developed to demonstrate wafer-level heterogeneous technology integration. The pseudo-SoC forms a global layer (line/space = 1μm/1μm) on the MEMS and CMOS chips, which are both embedded in epoxy resin, with a total thickness of 100μm.

7.8   Design Issues and Considerations for Low-Cost 3D TSV IC Technology

11:15 AM

G. Van der Plas[1], P. Limaye[1], A. Mercha[1], H. Oprins[1], C. Torregiani[1], S. Thijs[1], D. Linten[1], M. Stucchi[1], K. Guruprasad[1], D. Velenis[1], D. Shinichi[2], V. Cherman[1], B. Vandevelde[1], V. Simons[1], I. De Wolf[1], R. Labie[1], D. Perry[3], S. Bronckers[1], N. Minas[1], M. Cupac[1], W. Ruythooren[1], J. van Olmen[1], A. Phommahaxay[1], M. de Potter de ten Broeck[1], A. Opdebeeck[1], M. Rakowski[1], B. De Wachter[1], M. Dehan[1], M. Nelis[1], R. Agarwal[1], W. Dehaene[4], Y. Travaly[1], P. Marchal[1], E. Beyne[1]

[1]IMEC, Leuven, Belgium   [2]Panasonic, Leuven, Belgium

[3]Qualcomm, Leuven, Belgium   [4]K.U. Leuven, Leuven, Belgium

We investigate key design issues of a low-cost 3D Cu-TSV technology: impact of TSV on MOS devices and interconnect, reliability, thermal hot spots, ESD, signal integrity and impact on circuit performance. We experimentally verify their importance and propose changes in current design practices to enable low-cost systems.

7.9   Demonstration of Integrated Micro-Electro-Mechanical Switch Circuits for VLSI Applications

11:45 AM

F. Chen[1], M. Spencer[2], R. Nathanael[2], C. Wang[3], H. Fariborzi[1], A. Gupta[2], H. Kam[2], V. Pott[2], J. Jeon[2], T-J. K. Liu[2], D. Markovic[3], V. Stojanovic[1], E. Alon[2]

[1]Massachusetts Institute of Technology, Cambridge, MA

[2]University of California, Berkeley, CA   [3]University of California, Los Angeles, CA

A testchip demonstrates monolithic integration of micro-electro-mechanical (MEM) switch circuit building blocks for logic, timing, I/O and memory functions. Experimental results show functionality for an inverter, XOR, carry-generation block, oscillator, DAC, latch, and 10-cell DRAM.

7.10   Fully Depleted Extremely Thin SOI for Mainstream 20nm Low-Power Technology and Beyond

12:00 PM

A. Khakifirooz[1], K. Cheng[1], B. Jagannathan[2], P. Kulkarni[1], J. W. Sleight[3], D. Shahrjerdi[3], J. B. Chang[3], S. Lee[4], J. Li[4], H. Bu[1], R. Gauthier[1], B. Doris[1], G. Shahidi[3]

[1]IBM, Albany, NY   [2]IBM, Hopewell Junction, NY

[3]IBM T. J. Watson, Yorktown Heights, NY   [4]IBM, Essex Junction, VT

We present circuit design aspects of fully depleted extremely thin SOI (ETSOI) enabling 22nm low-power CMOS and beyond, and demonstrate that all devices including analog, I/O, and passive devices can be fabricated in the thin silicon layer. Excellent device matching, g_m/g_{ds} scaling to small gate length, good RF performance, and absence of history effect are the main features of the ETSOI technology.

Conclusion   12:15 PM

SESSION 8

HIGH-SPEED WIRELINE TRANSCEIVERS

Session Chair: Ali Sheikholeslami, *University of Toronto, Toronto, Canada*
Associate Chair: Tatsuya Saito, *Hitachi, Kokubunji, Japan*

8.1 A 47×10Gb/s 1.4mW/(Gb/s) Parallel Interface in 45nm CMOS

8:30 AM

F. O'Mahony, J. Kennedy, J. E. Jaussi, G. Balamurugan, M. Mansuri, C. Roberts, S. Shekhar, R. Mooney, B. Casper

Intel, Hillsboro, OR

A 47×10Gb/s chip-to-chip interface consuming 660mW is demonstrated in 45nm CMOS. A dense interconnect topology allows clocking to be shared across multiple lanes to reduce power. Receiver power is reduced by 93% during standby and an integrated wake-up timer indicates that all lanes return reliably to active mode in <5ns. The active circuitry occupies $3.2mm^2$.

8.2 A 6.8mW 7.4Gb/s Clock-Forwarded Receiver with up to 300MHz Jitter Tracking in 65nm CMOS

9:00 AM

M. Hossain, A. Chan Carusone

University of Toronto, Toronto, Canada

The clock path in a 65nm CMOS receiver comprises two injection-locked oscillators to frequency-multiply, deskew, and track correlated jitter on a pulsed clock forwarded from the transmitter. Latency mismatch and data rates are accommodated by controlling jitter tracking up to 300MHz. Each receiver consumes 0.92pJ/b at 7.4Gb/s with a jitter tolerance of 1.5UI at 200MHz.

8.3 A 4.5mW/Gb/s 6.4Gb/s 22+1-Lane Source-Synchronous Link RX Core with Optional Cleanup PLL in 65nm CMOS

9:30 AM

R. Reutemann[1], M. Ruegg[1], F. Keyser[2], J. Bergkvist[2], D. Dreps[3], T. Toifl[4], M. Schmatz[4]

[1]Miromico, Zürich, Switzerland   [2]IBM STG, Burlington, VT
[3]IBM STG, Austin, TX   [4]IBM Zurich Research Laboratory, Rüschlikon, Switzerland

A 23-lane (22 data+1 clk) source-synchronous RX PHY for server systems is realized in 65nm CMOS supporting multiple link protocols at 4.8 to 6.4Gb/s. To minimize jitter, either a polyphase filter or a cleanup PLL can be selected for I/Q clock generation. Power consumption of 4.5mW/(Gb/s) is achieved in the product-level design by a pulsed CDR using dithering to avoid excess jitter.

Break   10:00 AM

8.4 A 16Gb/s 1st-Tap FFE and 3-Tap DFE in 90nm CMOS

10:15 AM

H. Sugita, K. Sunaga, K. Yamaguchi, M. Mizuno

NEC, Sagamihara, Japan

A 16Gb/s 1st-tap FFE and 3-tap DFE is developed featuring 33% faster operation than conventional DFEs. The presented technique is employed for high-speed 1st-tap ISI equalization and for jitter reduction in equalized edges. By-path feedback and a voltage swing limiter have been developed to speed-up both 2nd-tap and 3rd-tap equalization. The DFE is fabricated in a 90nm CMOS process, occupies $227×276\mu m^2$, and consumes 69mW from a 1.4V supply operating at a BER of $<10^{-12}$ over a channel with 22B loss at 8GHz.

8.5   A 12Gb/s 39dB Loss-Recovery Unclocked-DFE Receiver with Bi-dimensional Equalization

M. Pozzoni[1], S. Erba[1], D. Sanzogni[1], M. Ganzerli[2], P. Viola[1], D. Baldi[1], M. Repossi[1], G. Spelgatti[3], F. Svelto[3]

[1]STMicroelectronics, Cornaredo, Italy

[2]University of Modena and Reggio Emilia, Modena, Italy

[3]University of Pavia, Pavia, Italy

A 45nm CMOS receiver based on an unclocked DFE is presented. A bi-dimensional equalization simultaneously adapts the DFE tap value and feedback delay, optimizing both the vertical and horizontal eye opening at the sampler input. Realized prototypes show error free operation at 12Gb/s with 39dB backplane loss. The receiver core occupies $0.1mm^2$ and consumes 130mW.

8.6   A Fractional-Sampling-Rate ADC-Based CDR with Feedforward Architecture in 65nm CMOS

O. Tyshchenko[1], A. Sheikholeslami[1], H. Tamura[2], Y. Tomita[2], H. Yamaguchi[2], M. Kibune[2], T. Yamamoto[2]

[1]University of Toronto, Toronto, Canada

[2]Fujitsu Laboratories, Kawasaki, Japan

This paper presents a fractional-sampling-rate (FSR) CDR that blindly samples the received signal with an ADC at 1.45× the data rate and estimates the data phase using a feedforward architecture for clock and data recovery. The presented architecture reduces the ADC power by 27.3% compared to a 2× CDR. Measurements confirm that the FSR CDR recovers data with BER<10^{-13} at 6.875Gb/s from samples taken at 10GS/s. The test-chip, implemented in 65nm CMOS, occupies $0.3683mm^2$, and consumes 175.2mW.

8.7   A 5Gb/s Transceiver with an ADC-Based Feedforward CDR and CMA Adaptive Equalizer in 65nm CMOS

H. Yamaguchi[1], H. Tamura[1], Y. Doi[1], Y. Tomita[1], T. Hamada[1], M. Kibune[1], S. Ohmoto[2], K. Tateishi[2], O. Tyshchenko[3], A. Sheikholeslami[3], T. Higuchi[2], J. Ogawa[1], T. Saito[1], H. Ishida[4], K. Gotoh[4]

[1]Fujitsu Laboratories, Kawasaki, Japan   [2]Fujitsu LSI Solutions, Kawasaki, Japan

[3]University of Toronto, Toronto, Canada   [4]Fujitsu Microelectronics, Akiruno, Japan

An SSC-compliant 5Gb/s transceiver in 65nm CMOS is developed and tested. The receiver uses an ADC-based front-end that samples the incoming signal without adjusting the phase difference between the sampling clock and the signal. The phase tracking of the input signal and the data decision are performed entirely in the numerical domain.

8.8   A 20Gb/s 40mW Equalizer in 90nm CMOS Technology

S. A. Ibrahim, B. Razavi

University of California, Los Angeles, CA

A linear equalizer with 9dB of boost and a 1-tap speculative half-rate DFE compensate for 24dB of channel loss at 10GHz, generating an output with a BER less than 10^{-12} and an eye opening of 0.32UI. The circuit consumes 40mW from a 1V supply at 20Gb/s.

Conclusion 12:15 PM

SESSION 9

Session Chair: Shannon Morton, *Icera, Bristol, United Kingdom*
Associate Chair: Joshua Friedrich, *IBM, Austin, TX*

9.1 Within-Die Variation-Aware Dynamic-Voltage-Frequency Scaling Core Mapping and Thread Hopping for an 80-Core Processor

8:30 AM

S. Dighe[1], S. Vangal[1], P. Aseron[1], S. Kumar[2], T. Jacob[2], K. Bowman[1], J. Howard[1], J. Tschanz[1], V. Erraguntla[2], N. Borkar[1], V. De[1], S. Borkar[1]

[1]Intel, Hillsboro, OR [2]Intel, Bangalore, India

Measured within-die core-to-core F_{MAX} variation data for an 80-core processor in 65nm is presented. Variation-aware DVFS with optimal core mapping is shown to improve energy efficiency 6 to 35% across a range of compute/communication activity workloads. A dynamic-thread-hopping scheme is boosts performance by 5 to 10% and energy efficiency by 20 to 60%.

9.2 Low-Skew Clock Distribution Using Zero-Phase-Clock-Buffer DLLs

9:00 AM

T. Wu, F. Aryanfar, H-C. Lee, J. Shen, T. Chin, C. Werner, K. Chang

Rambus, Los Altos, CA

A clock distribution scheme based on a zero-phase-clock-buffer (ZPCB) is presented. Each ZPCB generates an equal phase between its input and output by adjusting its resonant frequency to slightly higher than the clock frequency. A testchip fabricated in a 40nm LP process measures sub-psec skew over 500MHz and 800MHz ranges, for a 5GHz single-ended and a 15GHz differential ZPCB, respectively.

9.3 POWER7™ Local Clocking and Clocked Storage Elements

9:30 AM

J. Warnock[1], L. Sigal[2], D. Wendel[3], K. P. Muller[4], J. Friedrich[5], V. Zyuban[2], E. Cannon[6], A. KleinOsowski[6]

[1]IBM Systems and Technology Group, Yorktown Heights, NY
[2]IBM Research, Yorktown Heights, NY
[3]IBM Systems and Technology Group, Boeblingen, Germany
[4]IBM Systems and Technology Group, Poughkeepsie, NY
[5]IBM Systems and Technology Group, Austin, TX [6]Boeing, Seattle, WA

The clocked storage elements and local clocking circuitry for the POWER7™ chip, in 45nm SOI CMOS technology, include special features for enhanced reliability, testability, and debug capability. Multiple design options, including capacitance-optimized multi-bit layouts, allow for fine-grained power/performance tuning.

9.4 A 1.2 TB/s On-Chip Ring Interconnect for 45nm 8-Core Enterprise Xeon® Processor

9:45 AM

C. Park, R. Badeau, L. Biro, J. Chang, T. Singh, J. Vash, B. Wang, T. Wang

Intel, Hudson, MA

A 1.2TB/s ring interconnect implemented with a 9 metal 45nm technology is described. The implementation provides on-die communication for 8 Xeon cores, 8-port parallel-access 24MB L3 cache, and 2 system-interface ports. The efficient, flexible, and modular building-block approach used to construct our design is described.

Break   10:00 AM

9.5   High-Bandwidth and Low-Energy On-Chip Signaling with Adaptive Pre-Emphasis in 90nm CMOS

10:15 AM

J-S. Seo[1], R. Ho[2], J. Lexau[2], M. Dayringer[2], D. Sylvester[1], D. Blaauw[1]
[1]University of Michigan, Ann Arbor, MI   [2]Sun Microsystems, Menlo Park, CA

We present circuits for efficient repeaterless on-chip wires. A transmitter sends RZ pulses to a clockless hysteresis receiver using a 3-tap FIR filter to control ISI. Partly overlapped bits double bandwidth using adaptive pre-emphasis. A 90nm CMOS testchip shows bandwidth density of 4.4Gb/s/µm over 5mm on-chip links with 0.34 pJ/b energy consumption.

9.6   A Microcontroller-Based PVT Control System For A 65nm 72Mb Synchronous SRAM

10:30 AM

S. T. Eid, M. Whately, S. Krishnegowda

Cypress Semiconductor, San Jose, CA

We present a manufacturable scheme for managing PVT variations and controlling speed and power consumption by using an on-chip microcontroller and a temperature sensor. The system varies body-bias and power supplies of the memory core and periphery logic independently. The circuit occupies $0.32mm^2$ (0.4%) of a 72Mb SRAM test-chip in a 65nm CMOS process.

9.7   Accurate Characterization of Random Process Variations Using a Robust Low-Voltage High-Sensitivity Sensor Featuring Replica-Bias Circuit

10:45 AM

M. Meterelliyoz[1], A. Goel[2], J. P. Kulkarni[1], K. Roy[2]

[1]Intel, Hillsboro, OR   [2]Purdue University, West Lafayette, IN

We design a low-voltage high-sensitivity random-process-variations sensor using an on-chip calibration circuit for improved accuracy. The sensor features a replica-biasing circuit that compensates global PVT variations and maintains sensitivity for robust operation. Measurement results from 90nm test hip demonstrate the effectiveness of the sensor.

9.8   In Situ Delay-Slack Monitor for High-Performance Processors Using An All-Digital Self-Calibrating 5ps Resolution Time-to-Digital Converter

11:15 AM

D. Fick, N. Liu, Z. Foo, M. Fojtik, J-S. Seo, D. Sylvester, D. Blaauw

University of Michigan, Ann Arbor, MI

We present a minimally invasive in situ delay-slack monitor that directly measures the timing margins on critical timing signals, allowing margins due to both global and local PVT variations to be removed.

9.9   Early Detection of Oxide Breakdown Through In Situ Degradation Sensing

11:45 AM

P. Singh, Z. Foo, M. Wieckowski, S. Hanson, M. Fojtik, D. Blaauw, D. Sylvester

University of Michigan, Ann Arbor, MI

We present an in situ approach to detect the initial onset of oxide breakdown in large-scale circuits for wearout detection and management. The detection is based on a change in the resistive behavior of the oxide from non-linear to linear. Two 65nm testchips show robustness under temperature variation and capture of the onset of failure after just 0.5% delay increase in a FIR filter.

9.10   A Precise-Tracking NBTI-Degradation Monitor Independent of NBTI Recovery Effect

12:00 PM

E. Saneyoshi, K. Nose, M. Mizuno

NEC, Kanagawa, Japan

We design an on-chip aging monitor that combines the advantages of the small area of a ring-oscillator-type monitor and the short measurement time of a delay-line type monitor. It offers 1) short measurement time (more than 10× faster than conventional aging monitors, 2) small size (1/6 the size of a delay-line monitor), and 3) strong V_{DD} noise immunity.

Conclusion 12:15 PM

SESSION 10

Session Chair: Philip K.T. Mok, *Hong Kong University of Science and Technology, Hong Kong, China*

Associate Chair: Yoshihisa Fujimoto, *Sharp, Abenu, Japan*

10.1 A Two-phase Switching Hybrid Supply Modulator for Polar Transmitters with 9% Efficiency Improvement

8:30 AM

Y. Wu, P. K. Mok

Hong Kong University of Science and Technology, Hong Kong, China

A two-phase switching hybrid amplifier for polar transmitters, implemented in 0.35µm CMOS, lowers output ripple voltage by ripple cancellation, and boosts static efficiency by 9% due to halved switching loss and reduced ripple current flowing through the linear section of the amplifier. Dynamic efficiency improves by 8 to 12% with an on-chip feedforward bandpass filter.

10.2 A Robust Digital DC-DC Converter with Rail-to-Rail Output Range in 40nm CMOS

9:00 AM

E. G. Soenen, A. Roth, J. Shi, M. Kinyua, J. Gaither, E. Ortynska

TSMC, Austin, TX

A DC-DC converter with an embedded digital controller is implemented in 40nm CMOS. The converter including the ADC, decimator, digital filter, and DPWM occupies $0.7mm^2$ of which the area occupied by the output drivers is $0.6mm^2$. It achieves >90% efficiency at 200mA load.

10.3 A PLL-Based High-Stability Single-Inductor 6-channel Output DC-DC Buck Converter

9:30 AM

K-C. Lee[1], C-S. Chae[1], G-H. Cho[2], G-H. Cho[1]

[1]KAIST, Daejeon, Korea   [2]JDA Technology, Daejeon, Korea

A single-inductor 6-channel regulated output DC-DC buck converter employing PLL-based multiple-output bang-bang (PMB) control is presented. A mixture of comparator control and bang-bang control is used for regulating the multiple output channels inside the PLL loop. The fabricated chip occupies $2.5 \times 3mm^2$ in a 0.35µm CMOS process with a switching frequency of 2MHz.

Break   10:00 AM

10.4 A 300mA 14mV-Ripple Digitally Controlled Buck Converter Using Frequency Domain $\Delta\Sigma$ ADC and Hybrid PWM Generator

10:15 AM

H. H. Ahmad, B. Bakkaloglu

Arizona State University, Tempe, AZ

A 0.18µm CMOS digitally controlled DC-DC buck converter is presented. An all-digital 8b frequency-domain $\Delta\Sigma$ ADC is used for the feedback path, and a 9b segmented digital PWM is used for power stage control. A regulated output voltage accuracy of 1% and maximum efficiency of 94% is achieved with less than $14mV_{pp}$ ripple and a settling time of 100µs for a 300mA load transient.

10.5 A 10-MHz 92.1%-Efficiency Green-Mode Automatic Reconfigurable Switching Converter with Adaptively Compensated Single-Bound Hysteresis Control

10:45 AM

C. Zheng, D. Ma

University of Arizona, Tucson, AZ

A green-mode power converter is implemented in 0.13µm CMOS and achieves step-up/down variable output with adaptively optimized efficiency. Single-bound hysteresis control enables high-frequency switching regulation with suppressed error and noise. For V_{in}=1.5V and f_s=10MHz, the output is regulated from 0.9 to 2.2V with an efficiency of >80% over a 400mW power range.

10.6 Digitally Assisted Discontinuous Conduction Mode 5V/100MHz and 10V/45MHz DC-DC Boost Converters with Integrated Schottky Diodes in standard 0.13µm CMOS

11:15 AM

P. Li[1], L. Xue[1], D. Bhatia[1,2], R. Bashirullah[1]

[1]University of Florida, Gainesville, FL   [2]Intel, San Jose, CA

A 100MHz digitally assisted 4-phase switched-inductor boost converter delivers 240mW to load voltages of 3 to 5V with peak efficiency of 64%, and a 45MHz hybrid switched-inductor/capacitor boost converter delivers 20mW over a 6 to 10V output range at peak efficiency of 37%. Implemented in a standard 1.2V 0.13µm CMOS, the converters use integrated schottky diode rectifiers with 10V blocking voltages for DCM switching.

10.7 A 0.16mm^2 Completely On-Chip Switched-Capacitor DC-DC Converter Using Digital Capacitance Modulation for LDO Replacement in 45nm CMOS

11:45 AM

Y. Ramadass[1], A. Fayed[2], B. Haroun[3], A. Chandrakasan[1]

[1]Massachusetts Institute of Technology, Cambridge, MA

[2]Iowa State University, Ames, IA

[3]Texas Instruments, Dallas, TX

A completely on-chip switched-capacitor DC-DC converter that occupies 0.16mm^2 is implemented in a 45nm CMOS process. The converter delivers 8mA output current while maintaining load voltages from 0.8 to 1V from a 1.8V input supply. A digital capacitive modulation scheme is employed to maintain the converter efficiency between 50 to 70% over a wide range of load current levels.

10.8 A 32nm Fully Integrated Reconfigurable Switched-Capacitor DC-DC Converter Delivering 0.55W/mm^2 at 77% Efficiency

12:00 PM

H-P. Le[1], M. Seeman[1], S. R. Sanders[1], V. Sathe[2], S. Naffziger[2], E. Alon[1]

[1]University of California, Berkeley, CA

[2]AMD, Fort Collins, CO

A fully integrated switched-capacitor DC-DC converter with 32-phase interleaving is implemented in 0.374mm^2 of a 32nm SOI process. The converter can be reconfigured into three topologies to support 0.5 to 1.2V output from a 2V input supply, and achieves a maximum efficiency of 77% at an output power density of 0.55W/mm^2.

Conclusion   **12:15 PM**

SESSION 11

RADAR, MM-WAVE, & LOW-POWER TRANSCEIVERS

Session Chair: Yorgos Palaskas , *Intel, Hillsboro, OR*
Associate Chair: Mark Ingels, *IMEC, Leuven , Belgium*

11.1   A 4-Channel 4-Beam 24-to-26GHz Spatio-Temporal RAKE Radar Transceiver in 90nm CMOS for Vehicular Radar Applications

8:30 AM

H. Krishnaswamy[1], H. Hashemi[2]

[1]Columbia University, New York, NY

[2]University of Southern California, Los Angeles, CA

An RF Multibeam Spatio-Temporal RAKE radar architecture uses multi-beam beamforming and waveform diversity to isolate line-of-sight and multipath reflections for enhanced imaging. A 90nm CMOS, 4-channel, 4-beam, 24-to-26GHz vehicular radar prototype integrates a 4-channel mm-Wave front-end, a 4×4 multibeam matrix, and 4 high-speed mixed-signal baseband processors.

11.2   A Fully Integrated 77GHz FMCW Radar System in 65nm CMOS

9:00 AM

Y-A. Li, M-H. Hung, S-J. Huang, J. Lee
National Taiwan University, Taipei, Taiwan

A fully integrated 77GHz FMCW automotive radar system in 65nm CMOS includes clock generation and chip-antenna assembly. Incorporating a full-rate fractional-N synthesizer and a high-performance RF front-end, the radar achieves a maximum detectable distance of 106 meters for a mid-size car while consuming 243 mW from a 1.2V supply.

11.3   A SiGe BiCMOS 16-Element Phased-Array Transmitter for 60GHz Communications

9:30 AM

A. Valdes-Garcia[1], S. Nicolson[2], J-W. Lai[3], A. Natarajan[1], P-Y. Chen[3], S. Reynolds[1], J-H. C. Zhan[3], B. Floyd[1]

[1]IBM T. J. Watson, Yorktown Heights, NY   [2]MediaTek, San Jose, CA

[3]MediaTek, Hsinchu, Taiwan

A 60GHz phased-array transmitter for multi-Gb/s non-line-of-sight links is fully integrated in a 0.12um SiGe BiCMOS process. It consists of an up-conversion chain with synthesizer, a power distribution tree and 16 phase-shifting front-ends. The IC occupies 44mm², draws 1.2W excluding front-ends, and delivers 9 to 13.5dBm OP_{1dB} per element drawing 164 to 313mW per front-end.

Break   10:00 AM

11.4   A Wideband mm-Wave CMOS Receiver for Gb/s Communications Employing Interstage Coupled Resonators

10:15 AM

F. Vecchi[1,2], S. Bozzola[1], M. Pozzoni[3], D. Guermandi[4], E. Temporiti[3], M. Repossi[3], U. Decanis[1], A. Mazzanti[5], F. Svelto[1]

[1]University of Pavia, Pavia, Italy
[2]Istituto Universitario di Studi Superiori di Pavia, Pavia, Italy
[3]STMicroelectronics, Pavia, Italy
[4]STMicroelectronics, now with Broadcom, Bunnik, Netherlands
[5]University of Modena e Reggio Emilia, Modena, Italy

A 65nm CMOS sliding-IF receiver comprising 3 LNA gain stages, RF mixer, quadrature IF mixers, VCO and dividers is presented. Coupled resonators, both in the LNA and RF mixer, allow an important gain-bandwidth extension over conventional single LC neutralization. Realized prototypes show >13GHz RF bandwidth around 60GHz, <6.5dB NF, -21 dBm P_{1dB}, 12.6% VCO frequency range, and -115dBc/Hz phase noise at 10MHz offset from the carrier while drawing 75mW.

11.5   A 2.4GHz/915MHz 51μW Wake-Up Receiver with Offset and Noise Suppression

<div align="right">10:30 AM</div>

X. Huang, S. Rampu, X. Wang, G. Dolmans, H. de Groot

Holst Centre-IMEC, Eindhoven, Netherlands

An envelope detector-based wake-up receiver front-end is presented. A double-sampling technique is implemented to suppress the 1/f noise and DC offset, resulting in a lower output noise level and therefore a better SNR for a given input level. The receiver consumes 51μW and occupies 0.36mm^2 in 90nm CMOS. For 10kb/s OOK reception it achieves -69dBm and -80dBm sensitivity at 2.4GHz and 915MHz respectively.

11.6   A 2.4GHz 830pJ/bit Duty-Cycled Wake-Up Receiver with -82dBm Sensitivity for Crystal-Less Wireless Sensor Nodes

<div align="right">10:45 AM</div>

S. Drago[1,2], D. M. Leenaerts[1], F. Sebastiano[1,3], L. J. Breems[1], K. A. Makinwa[3], B. Nauta[2]

[1]NXP Semiconductors, Eindhoven, Netherlands

[2]University of Twente, Enschede, Netherlands

[3]Delft University of Technology, Delft, Netherlands

A 65nm CMOS 2.4GHz wake-up receiver operating with low-accuracy frequency references has been realized. Robustness to frequency inaccuracy is achieved by employing non-coherent energy detection, broadband-IF heterodyne architecture and impulse-radio modulation. The radio dissipates 415μW at 500kb/s and achieves a sensitivity of -82dBm with an energy efficiency of 830pJ/bit.

11.7   An Ultra-Low-Power Interference-Robust IR-UWB Transceiver Chipset Using Self-Synchronizing OOK Modulation

<div align="right">11:00 AM</div>

M. Crepaldi[1,2], C. Li[1,3], K. Dronson[1], J. Fernandes[1,4], P. Kinget[1]

[1]Columbia University, New York, NY   [2]Politecnico di Torino, Torino, Italy

[3]Peking University, Beijing, China   [4]Instituto Superior Tecnico, Lisbon, Portugal

A short-range 1Mb/s 3.8GHz IR-UWB transceiver in 90nm CMOS uses 1.5pulse/bit synched-OOK modulation, enabling low-complexity 200pJ/b digital demodulation and synchronization. An interference-robust asynchronous energy detector receiver can tolerate interferers up to -5dBm. The power-gated oscillator-based transmitter has a power efficiency of 10.4%.

11.8   A Fully Integrated 802.15.4a IR-UWB Transceiver in 0.13μm CMOS with Digital RRC Synthesis

<div align="right">11:15 AM</div>

S. Joo[1], W-H. Chen[1], T-Y. Choi[1], M-K. Oh[2], J-H. Park[2], J-Y. Kim[2], B. Jung[1]

[1]Purdue University, West Lafayette, IN   [2]ETRI, Daejeon, Korea

An 802.15.4a-compliant fully integrated coherent IR-UWB transceiver with digital RRC synthesis that supports 3 channels in Band Group 1 is presented. The transceiver consists of an RF front-end including frequency synthesizer and a digital back-end implemented in 0.13μm CMOS. It achieves a 20m radio distance (PER<10^{-2}), with <18cm ranging error.

11.9   A 0.92/5.3nJ/b UWB Impulse Radio SoC for Communication and Localization

<div align="right">11:45 AM</div>

Y. Zheng, S-X. Diao, C-W. Ang, Y. Gao, F-C. Choong, Z. Chen, X. Liu, Y-S. Wang, X-J. Yuan

Institute of Microelectronics, A*STAR (Agency for Science, Technology and Research), Singapore, Singapore

A UWB radio SoC, including an RF transceiver and a digital PHY, is presented for both communication and ranging. Realized in 0.18μm CMOS, the TX generates ternary coding and BPSK pulses in the 3-to-5GHz range, and the RX achieves a data rate of 0.25 to 20Mb/s, a noise figure of 7.2 to 8.4 dB, and a sensitivity of -82 to -90 dBm. At 1Mb/s, only 0.92nJ/b and 5.3nJ/b are required for TX and RX. Ranging accuracy of <15cm is realized.

<div align="right">**Conclusion   12:15 PM**</div>

EMERGING MEDICAL APPLICATIONS

Session Chair: Alison Burdett, *Toumaz Technology, Oxford, United Kingdom*
Associate Chair: Kenneth Shepard, *Columbia University, New York, NY*

12.1 Pain Control On Demand Based on Pulsed Radio-Frequency Stimulation of the Dorsal Root Ganglion Using a Batteryless Implantable CMOS SoC

1:30 PM

C-W. Lin[1], H-W. Chiu[2], M-L. Lin[1], C-H. Chang[1], I-H. Ho[2], P. Fang[1], Y. Li[1], C. Wang[1], Y-C. Tsai[1], Y-R. Wen[3], W-P. Shih[1], Y-J. Yang[1], S-S. Lu[1]

[1]National Taiwan University, Taipei, Taiwan

[2]National Taipei University of Technology, Taipei, Taiwan

[3]Shin Kong Wu Ho-Su Memorial Hospital, Taipei, Taiwan

Electrical stimulation can effectively control or reduce the sensation of pain. This paper presents the implementation of a batteryless CMOS SoC with low-voltage pulsed radio-frequency (PRF) stimulation. Its effectiveness is demonstrated by observing the behavior of rats receiving localized bi-polar stimulus to the dorsal root ganglion (DRG) of the lumbar nerve without thermal damage.

12.2 Mixed-Signal Integrated Circuits for Self-Contained Sub-Cubic Millimeter Biomedical Implants

2:00 PM

E. Y. Chow[1], S. Chakraborty[2], W. J. Chappell[1], P. P. Irazoqui[1]

[1]Purdue University, West Lafayette, IN   [2]Texas Instruments, Dallas, TX

This paper presents implantable monitors developed for treatment of glaucoma and cardiac disease. The CMOS chip enables wireless telemetry, powering at 2.4GHz, and digitizes and stores data from a MEMS sensor into FeRAM. A 24µF capacitor array for power storage enables independent operation over a 24-hour period. The system demonstrates a 0.5mmHg resolution over a 0-to-50mmHg range.

12.3 An Implantable 5mW/Channel Dual-Wavelength Optogenetic Stimulator for Therapeutic Neuromodulation

2:30 PM

K. Paralikar[1], P. Cong[1], W. Santa[1], D. Dinsmoor[1], B. Hocken[2], G. Munns[1], J. Giftakis[1], T. Denison[1]

[1]Medtronic, Minneapolis, MN   [2]Medtronic, Tempe, AZ

This paper describes an implantable system prototype capable of delivering optical intensities and modulation patterns suitable to therapeutically modulate neural networks. It leverages the emerging "optogenetic" interface paradigm for exciting or inhibiting neural activity with the advantages of genetically targeted stimulation and enhanced MRI/EMI compatibility.

12.4 Compact Voltage and Current Stimulation Buffer for High-Density Microelectrode Arrays

2:45 PM

P. Livi[1], F. Heer[1], U. Frey[2], D. Bakkum[3], A. Hierlemann[1]

[1]ETH Zurich, Zurich, Switzerland

[2]ETH Zurich (now at IBM Research), Zurich, Switzerland

[3]University of Tokyo, Tokyo, Japan

This paper presents the design and test of a reconfigurable buffer for voltage and current stimulation of electrogenic cells cultured on a CMOS microelectrode array. In voltage mode, the circuit is a high-current class-AB voltage follower, based on a local common-mode feedback. In current mode, the circuit is a current conveyor of type II, using the same amplifier with increased gain.

Break   **3:00 PM**

FREQUENCY & CLOCK SYNTHESIS

Session Chair: Ivan Bietti, *STMicroelectronics, Grenoble, France*
Associate Chair: Mike Keaveney, *Analog Devices, Limerick, Ireland*

13.1   A Low-Area Switched-Resistor Loop-Filter Technique for Fractional-N Synthesizers Applied to a MEMS-Based Programmable Oscillator

3:15PM

M. H. Perrott[1], S. Pamarti[2], E. Hoffman[3], F. S. Lee[1], S. Mukherjee[1], C. Lee[1], V. Tsinker[4], S. Perumal[5], B. Soto[6], N. Arumugam[1], B. W. Garlepp[1]

[1]SiTime, Sunnyvale, CA   [2]University of California, Los Angeles, CA

[3]Global Foundries, Sunnyvale, CA   [4]Invensense, Sunnyvale, CA

[5]Consultant, Sunnyvale, CA   [6]Consultant, Mountain View, CA

A fractional-N synthesizer is used in a programmable 1 to 115MHz MEMS oscillator. A high gain phase detector lowers the impact of loop filter noise, and a switched-resistor loop filter avoids a charge pump and boosts effective resistance to save area. The entire synthesizer with LC-VCO occupies 0.31mm^2 in 0.18μm CMOS. Chip consumption is 3.7mA drawn from a 3.3V supply for a 20MHz output with no load.

13.2   A 45nm SOI-CMOS Dual-PLL Processor Clock System for Multi-Protocol I/O

3:45 PM

D. M. Fischette[1], A. L. Loke[1], M. M. Oshima[1], B. A. Doyle[1], R. Bakalski[2], R. J. DeSantis[1], A. Thiruvengadam[1], C. L. Wang[1], G. R. Talbot[1], E. S. Fang[1]

[1]AMD, Sunnyvale, CA   [2]Global Foundries, Dresden, Germany

A dual-PLL system for 45nm SOI-CMOS processors is designed to clock a multi-protocol wireline I/O for high-speed digital communications covering a frequency range from 1GHz up to 11.1GHz. The two PLLs, based on a ring and LC-tank VCO, achieve 0.99ps and 0.55ps rms jitter, respectively. Circuit and architectural techniques to minimize the impact of SOI floating-body effect on phase jitter are introduced.

13.3   A 0.3mm^2 90-to-770MHz Fractional-N Synthesizer for a Digital TV Tuner

4:15 PM

M. Kondou[1], A. Matsuda[2], H. Yamazaki[1], O. Kobayashi[2]

[1]Fujitsu Laboratories, Yokohama, Japan   [2]Fujitsu Laboratories, Kawasaki, Japan

A 0.3mm^2 fractional-N synthesizer covering the frequency range from 90 to 770MHz needed for a digital TV tuner is presented. The synthesizer achieves the specifications of the ISDB-T/Tsb/Tmm standards while maintaining low spurious signals and small area by combining an FIR filtering technique and a circulating register. The phase noise at 1MHz offset is -119dBc/Hz. The worst spurious signals are below -61.2dBc.

13.4   A Low-Noise Frequency Synthesizer for Infrastructure Applications

4:45 PM

S. Farahvash, W. Roberts, J. Easter, R. Wei, D. Stegmeir, L. Jin

RFMD, San Jose, CA

A 2.2GHz fully integrated SiGe-BiCMOS frequency synthesizer embedding a low-noise VCO and targetting infrastructure applications is presented. A differential Colpitts VCO forms the core of the synthesizer. An initial open-loop calibration which stores the center frequencies of all VCO sub-bands in a RAM obviates the need for incremental calibration. The synthesizer has multiple out-of-loop dividers to synthesize frequencies less than the VCO frequency.

13.5   A 17.5-to-20.94GHz and 35-to-41.88GHz PLL in 65nm CMOS for Wireless HD Applications

5:00 PM

O. Richard[1], A. Siligaris[2], F. Badets[3], C. Dehos[2], C. Dufis[1], P. Busson[1], P. Vincent[2], D. Belot[1], P. Urard[1]
[1]STMicroelectronics, Crolles, France   [2]CEA-LETI-Minatec, Grenoble, France
[3]STMicroelectronics, Grenoble, France

A complete frequency synthesizer occupying 1.1mm^2 in 65nm CMOS is presented. It is composed of a push-push quadrature VCO that delivers two LO signals in 20 and 40GHz bands. The PLL consumes 80mW including buffers, and achieves a phase noise lower than -100 and -97.5dBc/Hz for the 20GHz and the 40GHz signals, respectively.

Conclusion 5:15 PM

SESSION 14

NON-VOLATILE MEMORY
Session Chair: Hideaki Kurata, *Hitachi, Kokubunji, Japan*
Associate Chair: Roberto Gastaldi, *Numonyx, Agrate Brianza, Italy*

14.1 Negative-Resistance Read and Write Schemes for STT-MRAM in 0.13µm CMOS

1:30 PM

D. Halupka[1], S. Huda[1], W. Song[1], A. Sheikholeslami[1], K. Tsunoda[2], C. Yoshida[2], M. Aoki[2]
[1]University of Toronto, Toronto, Canada   [2]Fujitsu Laboratories, Atsugi, Japan

We present a negative-resistance read scheme and write scheme for spin-torque-transfer (STT) MRAM. A negative resistance shunting an STT-MRAM cell performs a non-destructive read operation, and saves power during write compared with the conventional scheme. Measurements show an 8ns non-destructive read-access time and an average write power savings of 10.5% for a 16kb STT-MRAM fabricated in 0.13µm CMOS using a CoFeB/MgO/CoFeB MTJ.

14.2 A 64Mb MRAM with Clamped-Reference and Adequate-Reference Schemes

2:00 PM

K. Tsuchida, T. Inaba, K. Fujita, Y. Ueda, T. Shimizu, Y. Asao, T. Kajiyama, M. Iwayama, K. Sugiura, S. Ikegawa, T. Kishi, T. Kai, M. Amano, N. Shimomura, H. Yoda, Y. Watanabe
Toshiba, Yokohama, Japan

A 64Mb spin-transfer-torque MRAM in 65nm CMOS is developed. A 47mm^2 die uses a 0.3584µm^2 cell with a perpendicular-TMR device. To achieve read-disturb immunity for the reference cell, a clamped-reference scheme is adopted. An adequate-reference scheme is implemented to suppress read-margin degradation due to the resistance variation of reference cells.

14.3 A 0.13µm 64Mb Multi-Layered Conductive Metal-Oxide Memory

2:30 PM

C. J. Chevallier, C. Siau, S. Lim, S. Namala, M. Matsuoka, B. L. Bateman, D. Rinerson
Unity Semiconductor, Sunnyvale, CA

A 64Mb NAND-compatible non-volatile memory testchip based on a conductive metal-oxide technology is developed in 0.13µm technology. The memory cell, which does not require a selection device, occupies 0.17µm^2 and is built at the intersection of two metal lines above the CMOS circuitry. The chip uses 4 layers of cross-point arrays. Decoding and sensing techniques are also described.

Break   **3:00 PM**

14.4 A Scalable Shield-Bitline-Overdrive Technique for 1.3V Chain FeRAM

3:15 PM

D. Takashima, H. Shiga, D. Hashimoto, T. Miyakawa, S. Shiratake, K. Hoya, R. Ogiwara, R. Takizawa, S. Doumae, R. Fukuda, Y. Watanabe, S. Fujii, T. Ozaki, H. Kanaya, S. Shuto, K. Yamakawa, I. Kunishima, T. Hamamoto, A. Nitayama
Toshiba, Yokohama, Japan

A ferroelectric capacitor overdrive with shield-bitline drive for 1.3V chain FeRAM has been verified using a 0.13µm 576Kb test chip with 0.719µm^2 cell. This technique applies 0.24V bias to ferroelectric capacitors without increasing stress and bitline capacitance. The measured tail-to-tail cell signal is improved by 100mV and doubled in 1.3V array operation.

14.5   A 2.5Gb/s/ch 4PAM Inductive-Coupling Transceiver for Non-Contact Memory Card
3:45 PM

S. Kawai, H. Ishikuro, T. Kuroda

Keio University, Yokohama, Japan

A 2.5Gb/s/ch 4PAM inductive-coupling link is developed for non-contact memory cards. The data rate is 12.5× higher than that of a commercial memory card. By using automatic gain and phase control (AGPC), a communication range from 0.5 to 1mm is achieved, which is 10× of that without AGPC. BER <10^{-12} operation is confirmed at a data-rate of 2.5Gb/s.

14.6   A 0.29V Embedded NAND-ROM in 90nm CMOS for Ultra-Low-Voltage Applications
4:00 PM

M-F. Chang[1], S-M. Yang[1], C-W. Liang[1], C-C. Chiang[1], P-F. Chiu[1], K-F. Lin[1], Y-H. Chu[2], W-C. Wu[2], H. Yamauchi[3]

[1]National Tsing Hua University, Hsinchu, Taiwan

[2]Industrial Technology Research Institute, Hsinchu, Taiwan

[3]Fukuoka Institute of Technology, Fukuoka, Japan

A 90nm 256Kb NAND-ROM using read-1 noise elimination and read-0 sensing-margin-expanding schemes is functional at 0.29V and 3MHz with 100% code-coverage and 5% area overhead. This work reduces the delay-per-BL-length, energy-per-bit at V_{DDmin}, and V_{DDmin}-delay-product by 3000×, 4× and 3700×, respectively, compared to previous low-voltage ROMs.

14.7   A 90nm 4Mb Embedded Phase-Change Memory with 1.2V 12ns Read Access Time and 1MB/s Write Throughput
4:15 PM

G. De Sandre[1], L. Bettini[1], A. Pirola[1], L. Marmonier[1], M. Pasotti[1], M. Borghi[1], P. Mattavelli[1], P. Zuliani[1], L. Scotti[1], G. Mastracchio[1], F. Bedeschi[2], R. Gastaldi[2], R. Bez[2]

[1]STMicroelectronics, Agrate Brianza, Italy   [2]Numonyx, Agrate Brianza, Italy

A 90nm 4Mb embedded phase-change memory (PCM) is presented, demonstrating the feasibility of PCM integration with 3 masks overhead in a 6M standard CMOS process. Using a low-voltage NMOS transistor as a cell selector leads to a 0.29µm^2 cell size. A 1.2V low-voltage read operation achieves a 12ns access time. The 3mm^2 macro features a random write throughput of 1MB/s and a mode to increase write throughput to 4MB/s.

14.8   A 45nm 1Gb 1.8V Phase-Change Memory
4:45 PM

C. Villa[1], D. Mills[2], G. Barkley[2], H. Gidutur[2], S. Schippers[1], D. Vimercati[1]

[1]Numonyx, Agrate Brianza, Italy

[2]Numonyx, Folsom, CA

A 45nm 1Gb 1.8V single-level cell (SLC) phase-change memory (PCM) is designed with 85ns random-access time and 9MB/s program throughput, featuring read-while-write and over-write program commands. Sensing techniques to enable wide-temperature-range operation and reject wordline noise are presented. The 37.5mm^2 die size uses a double-gate-oxide and triple-Cu-metal process.

Conclusion   5:15 PM

SESSION 15

15.1 A 390Mb/s 3.57mm[2] 3GPP-LTE Turbo Decoder ASIC in 0.13μm CMOS

1:30 PM

C. Studer[1], C. Benkeser[1,2], S. Belfanti[1], Q. Huang[1,2]

[1]ETH Zürich, Zürich, Switzerland

[2]Advanced Circuit Pursuit, Zollikon, Switzerland

A turbo decoder for the 3GPP-LTE standard is implemented in 0.13μm CMOS technology. The 3.57mm[2] chip exceeds the maximum LTE throughput requirement of 326.4Mb/s and achieves a peak throughput of 390.6Mb/s at an energy efficiency of 0.37nJ/b/iteration.

15.2 A 4.5mW Digital Baseband Receiver for Level-A Evolved EDGE

2:00 PM

C. Benkeser[1,2], A. Bubenhofer[1], Q. Huang[1,2]

[1]ETH Zürich, Zürich, Switzerland

[2]Advanced Circuit Pursuit (ACP), Zollikon, Switzerland

A digital baseband receiver ASIC that supports GSM/GPRS/EDGE and Evolved EDGE is implemented in 0.13μm CMOS technology. The design centers around two main blocks: an adaptive channel equalizer processes GMSK/8PSK/16QAM and 32QAM modulated signals and a flexible channel decoder supports convolutional and turbo codes, as required for Evolved EDGE. The receiver occupies 2.0mm[2] and the average power consumption during burst reception and processing is less than 5mW in each of the modes.

15.3 A 477mW NoC-Based Digital Baseband for MIMO 4G SDR

2:30 PM

F. Clermidy[1], C. Bernard[1], R. Lemaire[1], J. Martin[1], I. Miro-Panades[1], Y. Thonnart[1], P. Vivet[1], N. Wehn[2]

[1]CEA-LETI-Minatec, Grenoble, France

[2]Technical University of Kaiserslautern, Kaiserslautern, Germany

A MIMO 3GPP-LTE digital baseband chip based on a heterogeneous 3×5 array NoC using 3.2GOPS/50mW programmable VLIW cores is presented. It features less than 10μs run-time full physical layer reconfiguration and distributed power management leading to 477mW power consumption on a 4×2 MIMO RX application.

Break   3:00 PM

15.4 A 2Gb/s Network Processor with a 24mW IPsec Offload for Residential Gateways

3:15 PM

Y. Nishida, K. Kawai, K. Koike

NTT, Kanagawa, Japan

A 90nm CMOS network processor comprising dual CPUs, a packet engine (PE), and an embedded LAN switch is developed on a 7.51×7.75mm[2] die. The network processors enable a residential gateway to forward packets at 2Gb/s with IP security and packet filtering. By offloading the packet handling to a packet engine, the power consumption of this function is limited to 24mW.

15.5 A 45nm Resilient and Adaptive Microprocessor Core for Dynamic Variation Tolerance

3:45 PM

J. W. Tschanz, K. Bowman, S-L. Lu, P. Aseron, M. Khellah, A. Raychowdhury, B. Geuskens, C. Tokunaga, C. Wilkerson, T. Karnik, V. De

Intel, Hillsboro, OR

A 45nm 1.3GHz microprocessor core employs error-detection circuits, tunable replica circuits, and error-recovery circuits, to mitigate dynamic variation guardbands for maximum throughput. An adaptive clock controller adjusts the frequency based on error statistics to optimize efficiency. Silicon measurements show resilient operation as well as throughput gains of 12 to 16% at 1.0V and 22 to 23% at 0.8V.

15.6 A Power-Efficient 32b ARM ISA Processor Using Timing-error Detection and Correction for Transient-error Tolerance and Adaptation to PVT Variation

4:15 PM

D. Bull[1], S. Das[1], K. Shivshankar[1], G. Dasika[2], K. Flautner[1], D. Blaauw[2]

[1]ARM, Cambridge, United Kingdom

[2]University of Michigan, Ann Arbor, MI

An ARM ISA processor fabricated in a 65nm CMOS process uses a combination of timing-error detecting circuits and micro-architectural recovery mechanisms to eliminate safety guardbands. Measurements performed on a distribution of 63 samples, including split lots, show a 52% power reduction for the overall distribution, for 1GHz operation.

15.7 A 45nm CMOS 13-Port 64-Word 41b Fully Associative Content-Addressable Register File

4:45 PM

G. Burda, Y. Kolla, J. Dieffenderfer, F. Hamdan

Qualcomm, Raleigh, NC

A 13-port 64-word 41b fully associative content-addressable register file that is part of a dual-issue superscalar ARMv7-architecture CPU is described. The register file is part of the register-renaming function within the CPU, allowing for the resolution of data hazards common to out-of-order superscalar CPUs. The register file occupies $0.062mm^2$ in a 1.1V 45nm CMOS technology and operates at 1.4GHz while consuming 21mW.

15.8 Millimeter-Scale Nearly Perpetual Sensor System with Stacked Battery and Solar Cells

5:00 PM

G. Chen, M. Fojtik, D. Kim, D. Fick, J. Park, M. Seok, M-T. Chen, Z. Foo, D. Sylvester, D. Blaauw

University of Michigan, Ann Arbor, MI

An $8.75mm^3$ sensor system is implemented with a near-threshold ARM Cortex-M3 core, custom 3.3fW leakage-per-bit SRAM, two $1mm^2$ solar cells, a thin-film Li-ion battery, and an integrated power management unit. The 2.1µW system enters a 100pW data-retentive sleep state between sensor measurements and harvests energy from the solar cells to enable nearly perpetual operation.

Conclusion   5:15 PM

ISSCC 2010 TUTORIALS

Sunday, February 7th

Time		
8:00AM	T1: Battery Management for Portable Devices	T2: SoC Integration of RF Front-end Passives
10:00AM	T3: Specifying and Testing ADCs	T4: RF CMOS Power Amplifiers and Linearization Techniques	T5: Design of Energy-Efficient On-Chip Networks
12:30PM	T6: Design of Smart Sensors	T7: High-Speed Memory Interfaces
2:30PM	T8: Power Gating	T9: PLL Design in Nanometer CMOS

ISSCC 2010 FORUMS

Time		
8:00AM	F1: Silicon 3D Integration Technology Systems	F2: Reconfigurable RF and Data Converters

ISSCC 2010 EVENING SESSIONS

8:00 PM ES1: Beyond CMOS: Emerging Technologies	7:45 PM ES2: Student Research Preview

ISSCC 2010 PAPER SESSIONS

Monday, February 8th

Time				
8:15AM	Session 1: Plenary Session			
1:30PM	Session 2: mm-Wave Beamforming & RF Building Blocks	Session 3: Cellular Techniques	Session 4: Analog Techniques	Session 5: Processors	Session 6: Displays & Biomedical Devices
5:15PM	Social Hour: Poster Session - DAC/ISSCC Student-Design-Contest Winners; Author Interviews, Student-Research Preview Speaker Interviews			

ISSCC 2010 EVENING SESSIONS

8:00PM	ES3: Energy-Efficient High-Speed Interfaces	ES4: Fusion of MEMS and Circuits	EP1: Analog Circuits: Stump the Panel

ISSCC 2010 PAPER SESSIONS

Tuesday, February 9th

Time					
8:30AM	**Session 7:** Designing in Emerging Technologies	**Session 8:** High-Speed Wireline Transceivers	**Session 9:** Digital Circuits & Sensors	**Session 10:** DC-DC Power Conversion	**Session 11:** Radar, mm-Wave, & Low-Power Transceivers
1:30PM	**Session 12:** Emerging Medical Applications / **Session 13:** Frequency & Clock Synthesis	**Session 14:** Non-Volatile Memory	**Session 15:** Low-Power Processors & Communication	**Session 16:** High-Performance Data Converters	**Session 17:** Sensors & MEMS
5:15PM	Social Hour: Poster Session - DAC/ISSCC Student-Design-Contest Winners; Author Interviews; University Alumni Events; Women's Networking Reception				

ISSCC 2010 EVENING SESSIONS

Time			
8:00PM	**ES5:** Can RF SoCs (Self) Test Their Own RF?	**ES6:** Can We Rebuild Them? Bionics Beyond 2010	**EP2:** The Semiconductor Industry in 2025

Wednesday, February 10th

ISSCC 2010 PAPER SESSIONS

Time					
8:30AM	**Session 18:** Power Efficient Media Processing	**Session 19:** High-Performance Embedded Memory	**Session 20:** Next-Generation Optical & Electrical Interfaces	**Session 21:** Successive-Approximation ADCs	**Session 22:** Image Sensors
1:30PM	**Session 23:** mm-Wave Transceivers, Power Amplifiers & Sources	**Session 24:** DRAM & Flash Memories	**Session 25:** Wireless Connectivity	**Session 26:** High-Performance & Digital PLLs	**Session 27:** Directions in Health, Energy & RF
5:15 PM	Author Interviews				

Thursday, February 11th

ISSCC 2010 SHORT COURSE

Time	
8:00 AM	CMOS Phase-Locked Loops for Frequency Synthesis

ISSCC 2010 FORUMS

Time				
8:00AM	**F3:** Transceiver Circuits for Optical Communications	**F4:** High-Speed Image Sensor Technologies	**F5:** Circuits for Portable Medical Electronic Systems	**F6:** Signal and Power Integrity for SoCs

SESSION 16

Session Chair: Gabriele Manganaro, *National Semiconductor, Unterhaching , Germany*
Associate Chair: Kong-Pang Pun, *Chinese University of Hong Kong, Hong Kong, China*

16.1 A 16b 250MS/s IF-Sampling Pipelined A/D Converter with Background Calibration

1:30 PM

A. M. Ali, A. Morgan, C. Dillon, G. Patterson, S. Puckett, M. Hensley, R. Stop, P. Bhoraskar, S. Bardsley, D. Lattimore, J. Bray, C. Speir, R. Sneed

Analog Devices, Greensboro, NC

We present a 16b 250MS/s ADC that employs background calibration of the residue amplifier gain errors. It has an integrated input buffer and is fabricated on a 0.18µm BiCMOS process. Without the input buffer, the SNR is 77.5dB and the SFDR is 90dB. With the input buffer, the SNR is 76dB and the SFDR is 95dB. The clock jitter is 60fs. The ADC consumes 850mW and the input buffer consumes 150mW.

16.2 A 16b 100-to-160MS/s SiGe BiCMOS Pipelined ADC with 100dBFS SFDR

2:00 PM

R. Payne, M. Corsi, D. Smith, S. Kaylor, D. Hsieh

Texas Instruments, Dallas, TX

A 16b 160MS/s pipelined ADC built in a complementary SiGe BiCMOS process is presented, with an SFDR of 105dB and an SNR of 77dB at -1dBFS below 160MHz. The fully buffered track-and-hold has circuitry needed to achieve this performance. The internal sub-DAC uses circuits to mitigate the limitations imposed by transistor self-heating, early voltage and impact ionization.

16.3 A 2.6mW 6b 2.2GS/s 4-times Interleaved Fully Dynamic Pipelined ADC in 40nm Digital CMOS

2:30 PM

B. Verbruggen[1,2], J. Craninckx[1], M. Kuijk[2], P. Wambacq[1,2], G. Van der Plas[1]

[1]IMEC, Leuven, Belgium

[2]Vrije Universiteit Brussel, Elsene, Belgium

A 2.2GS/s 4x-interleaved 6b ADC in 40nm digital CMOS is presented. Each ADC slice consists of a 1b folding stage followed by a pipelined binary-search sub-ADC using dynamic nonlinear amplifiers for low power consumption and high speed. Threshold calibration corrects for amplifier and comparator imperfections and 31.6dB SNDR is achieved with 2GHz ERBW for 2.6mW power consumption.

Break   3:00 PM

16.4 A Mostly Digital Variable-Rate Continuous-Time ADC ΔΣ Modulator

3:15 PM

G. Taylor[1,2], I. Galton[1]

[1]University of California, San Diego, CA

[2]Analog Devices, San Diego, CA

A mostly digital variable-rate continuous-time ΔΣ modulator is presented with power dissipation, output sample-rate, bandwidth, and peak SNDR ranges of 8 to 17mW, 0.5 to 1.15GHz, 3.9 to 18MHz, and 67 to 78dB, respectively. The IC is implemented in a 65nm CMOS process with an active area of $0.07mm^2$.

16.5 A 10b 100MS/s 4.5mW Pipelined ADC with a Time Sharing Technique

3:45 PM

Y-C. Huang, T-C. Lee

National Taiwan University, Taipei, Taiwan

A 10b pipelined ADC employs opamp and time-sharing techniques to reduce the power consumption and silicon area. The presented ADC needs only one opamp to complete the 10b conversion. The chip is fabricated in a 90nm digital CMOS process and occupies $0.058mm^2$. It operates at 100MS/s and achieves an SNDR of 55.0dB while the power consumption is 4.5mW from a 1.0V supply.

16.6 A 1.4V Signal Swing Hybrid CLS-Opamp/ZCBC Pipelined ADC Using a 300mV Output Swing Opamp

4:15 PM

B. P. Hershberg, S. T. Weaver, U-K. Moon

Oregon State University, Corvallis, OR

A Hybrid CLS-opamp/ZCBC pipelined ADC is introduced to improve accuracy, robustness, and power efficiency. Fast and accurate residue amplification is achieved by invoking a short ZCBC operation followed by CLS-opamp settling. Measured ENOB is better than 11b at sampling rate of 20MHz.

16.7 A 110dB SNR and 0.5mW Current-Steering Audio DAC Implemented in 45nm CMOS

4:45 PM

R. Hezar[1], L. Risbo[2], H. Kiper[1], M. Fares[1], B. Haroun[1], G. Burra[1], G. Gomez[1]

[1]Texas Instruments, Dallas, TX

[2]Texas Instruments, Copenhagen, Denmark

An oversampled cascaded-modulator audio DAC architecture to reduce out-of-band noise is presented. Pulse-width modulation combined with an analog-FIR filter is used to reduce the impact of circuit mismatch and dynamic glitch errors. Implemented in 45nm CMOS as a current-steering DAC, the $0.045mm^2$ chip delivers 110dB DR while consuming 0.5mW.

Conclusion   5:15 PM

SESSION 17

Session Chair: Makoto Ikeda, *University of Tokyo, Tokyo, Japan*
Associate Chair: Christoph Hagleitner, *IBM Research , Ruschlikon, Switzerland*

17.1 A System-on-Chip EPC Gen-2 Passive UHF RFID Tag with Embedded Temperature Sensor

1:30 PM

J. Yin, J. Yi, M. Law, Y. Ling, M. Lee, K. Ng, B. Gao, H. Luong, A. Bermak, M. Chan, W-H. Ki, C-Y. Tsui, M-F. Yuen

Hong Kong University of Science and Technology, Hong Kong, China

An RFID tag features a temperature sensor with a gain-error compensation, a dual-path clock generator for both accurate link frequency and low power applications, and a zero-mask CMOS OTP memory array for low cost. The tag executes EPC-compliant SENSE-WRITE-READ commands with -6dBm sensitivity and +0.4/-1.1°C error with one-point calibration.

17.2 A CMOS Temperature Sensor with an Energy-Efficient Zoom ADC and an Inaccuracy of ±0.25°C (3σ) from -40°C to 125°C

2:00 PM

K. Souri, M. Kashmiri, K. Makinwa

Delft University of Technology, Delft, Netherlands

A 0.26mm^2 CMOS temperature sensor is realized in a 0.16µm CMOS process. It uses a hybrid SAR/ΔΣ (zoom) ADC to achieve 0.018°C resolution at 10S/s while dissipating 9µW. After a 1-point trim, the sensor achieves an inaccuracy of ±0.25°C (3σ) in the range from −40°C to 125°C.

17.3 A 1.2V 10µW NPN-Based Temperature Sensor in 65nm CMOS with an Inaccuracy of ±0.2°C (3σ) from −70°C to 125°C

2:30 PM

F. Sebastiano[1,2], L. J. Breems[1], K. A. Makinwa[2], S. Drago[1,3], D. M. Leenaerts[1], B. Nauta[3]

[1]NXP Semiconductors, Eindhoven, Netherlands

[2]Delft University of Technology, Delft, Netherlands

[3]University of Twente, Enschede, Netherlands

A temperature sensor utilizing NPN transistors has been realized in a 65nm CMOS process. It achieves a batch-calibrated inaccuracy of ±0.5°C (3σ) and a trimmed inaccuracy of ±0.2°C (3σ) from −70°C to 125°C. The sensor draws 8.3µA from a 1.2V supply and occupies an area of 0.1mm^2.

Break 3:00 PM

17.4 A Thermal-Diffusivity-Based Temperature Sensor with an Untrimmed Inaccuracy of ±0.2°C (3σ) from −55°C to 125°C

3:15 PM

C. P. van Vroonhoven[1], D. d'Aquino[2], K. A. Makinwa[1]

[1]Delft University of Technology, Delft, Netherlands

[2]National Semiconductor, Santa Clara, CA

A temperature sensor based on the thermal diffusivity of IC-grade silicon has a near-linear digital output, which is insensitive to both process spread and packaging stress. Its accuracy is mainly limited by lithographic errors and thus benefits from scaling. An implementation in a 0.18µm CMOS process has an untrimmed inaccuracy of ±0.2°C (3σ) from −55°C to 125°C.

17.5   An In-Situ Temperature Sensing Interface Based on a SAR ADC in 45nm LP Digital CMOS for the Frequency-Temperature Compensation of Crystal Oscillators

3:45 PM

Z. Wang[1], R. Lin[2], E. Gordon[3], H. Lakdawala[2], L. Carley[1], J. Jensen[2]

[1]Carnegie Mellon University, Pittsburgh, PA

[2]Intel, Hillsboro, OR

[3]Intel, Haifa, Israel

A crystal-temperature-sensing interface based on an *in-situ* thermistor and a 1V 12b digitally calibrated SAR ADC in 45nm LP CMOS is presented. The digitized temperature readings are used by an LUT-based compensation scheme to stabilize the frequency of a crystal oscillator through digital capacitive load tuning to achieve ±0.5ppm stability over a -10-to-80°C temperature range.

17.6   A 76dB-Ohm 1.7GHz Tunable Transimpedance Amplifier in 0.18μm CMOS for High-Frequency Lateral Micromechanical Oscillators

4:15 PM

H. Miri Lavasani[1], W. Pan[1], B. Harrington[2], R. Abdolvand[2], F. Ayazi[1]

[1]Georgia Institute of Technology, Atlanta, GA

[2]Oklahoma State University, Tulsa, OK

A 76dB-Ohm 1.7GHz tunable CMOS TIA in 0.18μm CMOS for lateral micromechanical oscillators is presented. The 7.2mW TIA uses a low-power broadband current pre-amplifier for gain boosting (loading > 2pF). The TIA is interfaced with 724MHz and 1.006GHz resonators and achieves phase noise better than -87dBc/Hz and -94dBc/Hz at 1kHz offset, respectively.

17.7   A Closed-Loop SC Interface for a ±1.4g Accelerometer with 0.33% Nonlinearity and 2μg/√Hz Input Noise Density

4:45 PM

M. Yucetas, J. Salomaa, A. Kalanti, L. Aaltonen, K. Halonen

Helsinki University of Technology, Espoo, Finland

A closed-loop SC interface for a ±1.4g accelerometer together with a 1b SC $\Delta\Sigma$ ADC is implemented in 0.35μm CMOS. The active area is 2mm^2 and the supply current and voltage are 2.4mA and 3.6V, respectively. The SC interface, designed for a sensor element with a high quality factor, allows the resonance peak of the element to be damped in such a way that the ADC remains outside the closed-loop accelerometer.

17.8   A 200MHz 300ps 0.5pJ/ns Optical Pulse Generator Array in 0.35μm CMOS

5:00 PM

B. R. Rae[1], J. McKendry[2], Z. Gong[2], E. Gu[2], D. Renshaw[1], M. D. Dawson[2], R. K. Henderson[1]

[1]University of Edinburgh, Edinburgh, United Kingdom

[2]University of Strathclyde, Glasgow, United Kingdom

An 8×8 array of AlInGaN micro-LEDs is bump-bonded to a standard 0.35μm CMOS driver chip. Each pixel can be independently pulsed at a rate of 200MHz with pulsewidths down to 300ps FWHM at optical power levels of 0.5pJ/ns at 370nm. Circuit techniques to minimize pulsewidths are demonstrated. Applications include chip-to-chip communications and lab-on-chip devices.

Conclusion   **5:15 PM**

EVENING SESSIONS

ES5: Can RF SoCs (Self) Test Their Own RF?

Co-Chair/Organizer: R. Bogdan Staszewski, *Delft University of Technology, Delft, The Netherlands*

Co-Chair/Moderator: Jacques C. Rudell, *University of Washington, Seattle, WA*

Testing for RF-parameter compliance of a wireless standard is time-consuming, and commands a significant fraction of the total SoC cost, even though it is only a small percentage of the die area. The same on-die digital logic that is used to calibrate the circuit also can be effective in testing, thereby reducing the complexity of external test equipment, or even eliminating it entirely. RF circuit-and-system designers need to consider how self-testing will affect the selection of RF front-end circuitry and architecture, rather than view it as something confined to the back-end sections of a modem.

Time	Topic
8:00	**RF SoC's Can Test Their Own RF!** R. Bogdan Staszewski, *Delft University of Technology, Delft, The Netherlands*
8:20	**Digital Time-Domain Methods for SoC RF-BIST** Mani Soma, *University of Washington, Seattle, WA*
8:40	**How to do RF-BIST Without Adding Extra Circuitry for RF-SoCs** Donald Y.C. Lie, *Texas Tech University, Lubbock, Texas*
9:00	**Calibration and Self-Test of RF Transceivers and SoCs** Gernot Hueber, *Infineon, Linz, Austria*
9:20	**Testing and Calibration Techniques in Modern WLAN SoCs** Srenik Mehta, *Atheros Communications, Santa Clara, CA*
9:40	**Panel Discussion**

ES6: Can We Rebuild Them? Bionics Beyond 2010

Co-Organizer: Maysam Ghovanloo, *Georgia Tech, Atlanta, GA*

Co-Organizer/Chair: Tim Denison, *Medtronic, Minneapolis, MN*

The goal of this Session is to provide a better understanding of how integrated circuits fit into the overall bionic system. Clearly, in the proper context, interfacing silicon circuits to the patient's neural circuits may achieve profound effects. The speakers will describe several such developments: a cochlear prosthesis, which has helped restore a measure of hearing in over 100,000 patients; neurostimulators, which provide therapy for a variety of neurological diseases including Parkinson's disease; and a retinal prosthesis, which is being deployed in clinical trials.

Time	Topic
8:00	**System Design Challenges in a Very Complex System Indeed** Gerald Loeb, *University of Southern California, Los Angeles, CA*
8:30	**Cochlear Implants – The First 50 Years…and Thoughts for the Future** Hugh McDermott, *University of Melbourne, Melbourne, Australia*
9:00	**Clinical Trials with the First Useful Retinal Implants, Status and Issues** Albrecht Rothermel, *University of Ulm, Ulm, Germany*
9:30	**Neurotechnology to Engage the Brain: Technical Challenges and a Look to the Future** Daryl R. Kipke, *University of Michigan, Ann Arbor, Michigan*

EP2: The Semiconductor Industry in 2025

Co-Organizer: **Azeez Bhavnagarwala,** *IBM, Yorktown Heights, NY*

Co-Organizer: **Takayasu Sakurai**, *University of Tokyo, Tokyo, Japan*

Moderator: **Siva Narendra**, *Tyfone, Protland, OR*

The historic predictability of Moore's Law has spurred innovation and redefined how we build integrated circuits. We have developed an eco-system of specialized entities to resolve specific challenges such as Equipment Development, Foundry Services, Design, EDA, Software, and Consumer Services. While more specialization has been an undisputed trend of the past, we are beginning to see hardware companies becoming less specialized – manufacturing companies entering design, design companies entering services, to name a few. What approach will be the predominant model in 2025? More vertically-integrated companies that enable recurring revenue? Or more horizontally- integrated companies that focus on specialized innovation?

Panelists:
      William Holt, *SVP & GM, Intel, Hillsboro, OR*
      Tadahiro Kuroda, *Keio Univerisity, Yokohama, Japan*
      Pierre-Yves Lesaicherre, *SVP & GM, NXP, San Jose, CA*
      Sreedhar Natarajan, *VP, TSMC, Kanata, Canada*
      Gary Patton, *VP, IBM, Hopewell Junction, NY*
      Walden Rhines, *Chairman & CEO, Mentor Graphics, Willisonville, OR*
      Charles G. Sodini, *MIT, Cambridge, MA*

SESSION 18

POWER EFFICIENT MEDIA PROCESSING

Session Chair: Raney Southerland, *ARM, Austin, TX*
Associate Chair: Vasantha Erraguntla, *Intel, Bangalore, India*

18.1 A 222mW H.264 Full-HD Decoding Application Processor with x512b Stacked DRAM in 40nm

8:30 AM

Y. Kikuchi, M. Takahashi, T. Maeda, H. Hara, H. Arakida, H. Yamamoto, Y. Hagiwara, T. Fujita, M. Watanabe, T. Shimazawa, Y. Ohara, T. Miyamori, M. Hamada, M. Takahashi, Y. Oowaki
Toshiba, Kawasaki, Japan

A 40nm 14-core mobile application processor with a 222mW Full-HD H.264 video decoder and a video/audio multiprocessor is developed. It has 25 power domains. The power switch circuits realize less than 1µs power-up switching while minimizing rush current. The x512b power-efficient stacked DRAM I/F achieves 10.6GB/s bandwidth.

18.2 A 320mV-to-1.2V On-Die Fine-Grained Reconfigurable Fabric for DSP/Media Accelerators in 32nm CMOS

9:00 AM

A. Agarwal, S. K. Mathew, S. K. Hsu, M. A. Anders, H. Kaul, F. Sheikh, R. Ramanarayanan, S. Srinivasan, R. Krishnamurthy, S. Borkar
Intel, Hillsboro, OR

A 32nm on-die fine-grained reconfigurable fabric for DSP/media accelerators is fabricated and occupies a $0.076mm^2$ die. The optimized hybrid arithmetic configurable logic blocks with self-decoded look-up tables, ultra-low voltage PVT-tolerant register file circuits and dual-supply operation help enable a 2.4GHz nominal performance at 1.0V and 320mV-to-1.2V dynamic voltage range. The peak energy efficiency is 2.6TOPS/W when measured at 340mV and 50°C.

18.3 A 59.5mW Scalable/Multi-View Video Decoder Chip for Quad/3D Full HDTV and Video Streaming Applications

9:30 AM

T-D. Chuang, P-K. Tsung, P-C. Lin, L-M. Chang, T-C. Ma, Y-H. Chen, L-G. Chen
National Taiwan Univeristy, Taipei, Taiwan

A 90nm 59.5mW scalable/multi-view/H.264 multi-standard video decoder chip is implemented in a $8.53mm^2$ die. Via a throughput-efficiency architecture with reconfigurable scheduling and a cache system, a low memory bandwidth, high-throughput design is achieved. It has 3.41× throughput with 47% power reduction compared to previous work.

Break   10:00 AM

18.4 A 345mW Heterogeneous Many-Core Processor with an Intelligent Inference Engine for Robust Object Recognition

10:15 AM

S. Lee, J. Oh, M. Kim, J. Park, J. Kwon, H-J. Yoo
KAIST, Daejeon, Korea

A 228GOPS 345mW heterogeneous many-core processor combines bottom-up and top-down attention for high accuracy. It uses analog-digital mixed-mode neuro-fuzzy inference circuits to realize robust object recognition. Weight perturbation learning and workload-aware voltage/frequency control are adopted. The $5×10mm^2$ chip with 96% recognition accuracy contains 4 SIMD vector processing elements and 32 MIMD processors.

18.5   A Scalable Massively Parallel Processor for Real-Time Image Processing

10:45 AM

T. Kurafuji[1], M. Haraguchi[1], M. Nakajima[1], T. Gyoten[1], T. Nishijima[1], H. Yamasaki[1], Y. Imai[2], M. Ishizaki[1], T. Kumaki[2], Y. Okuno[1], T. Koide[2], H. J. Mattausch[2], K. Arimoto[1]

[1]Renesas Technology, Itami, Japan

[2]Hiroshima University, Higashi-Hiroshima, Japan

A processor with 2048 4b grained processor elements (PE) and a 2Mb SRAM is implemented in 65nm CMOS and occupies a $5.29mm^2$ die. It achieves 200MHz operation at 1.0V and outputs peak power efficiency of 310GOPS/W. The peak performance reached 191GOPS at 560MHz and 1.2V in the double frequency mode. The processor can be optimized for both power and area by changing the number of PEs from 256 to 2048.

18.6   A Graphics and Vision Unified Processor with 0.89µW/fps Pose Estimation Engine for Augmented Reality

11:15 AM

J-S. Yoon, J-H. Kim, H-E. Kim, W-Y. Lee, S-H. Kim, K. Chung, J-S. Park, L-S. Kim

KAIST, Daejeon, Korea

A parallel unified processor for graphics and vision is developed. It achieves 371.9GOPS/W in full operation through a 6-way VLIW datapath, reconfigurable processing elements for graphics and vision mode, and a pixel arranger for data-level parallelism. The pose-estimation engine achieves 0.89µW/fps for marker-based augmented reality.

18.7   A Multimedia Semantic Analysis SoC (SASoC) with Machine-Learning Engine

11:45 AM

T-W. Chen, Y-L. Chen, T-Y. Cheng, C-S. Tang, P-K. Tsung, T-D. Chuang, L-G. Chen, S-Y. Chien

National Taiwan University, Taipei, Taiwan

A 671GOPS/W Semantic Analysis SoC (SASoC) is implemented in 90nm CMOS technology. Two stream processing systems are integrated with a power-aware frequency scaling technique to simultaneously accelerate video processing and machine-learning algorithms. The input data rate reaches 76.8Gpixel/s for video processing and 51.2Gdimension/s for machine-learning algorithms.

Conclusion   12:15 PM

SESSION 19

HIGH-PERFORMANCE EMBEDDED MEMORY

Session Chair: Harold Pilo, *IBM, Essex Junction, VT*
Associate Chair: Kevin Zhang, *Intel, Hillsboro, OR*

19.1 A 45nm SOI Embedded DRAM Macro for POWER7™ 32MB On-Chip L3 Cache

8:30 AM

J. Barth[1], D. Plass[2], E. Nelson[1], C. Hwang[2], G. Fredeman[2], M. Sperling[2], A. Mathews[3], W. Reohr[4], K. Nair[2], N. Cao[2]

[1]IBM, Essex Junction, VT

[2]IBM, Poughkeepsie, NY

[3]IBM, Austin, TX

[4]IBM T. J. Watson, Yorktown Heights, NY

This paper presents a 1.7ns-random-cycle SOI embedded-DRAM macro developed for the POWER7™ high-performance microprocessor and introduces enhancements to the micro-sense-amplifier (µSA) architecture. The macro enables a 32MB on-chip L3 cache, eliminating delay, area and power from the off-chip interface.

19.2 A 32kB 2R/1W L1 Data Cache in 45nm SOI Technology for the POWER7™ Processor

9:00 AM

J. Pille[1], D. Wendel[1], O. Wagner[1], R. Sautter[1], W. Penth[1], T. Froehnel[1], S. Buettner[1], O. Torreiter[1], M. Eckert[1], J. Paredes[2], D. Hrusecky[2], D. Ray[2], M. Canada[3]

[1]IBM, Boeblingen, Germany

[2]IBM, Austin, TX

[3]IBM, Burlington, VT

The POWER7™ microprocessor features a 32kB L1 data cache with a 2R and banked-1W functionality using a 6T-SRAM cell. Read/write collision is intercepted inside the array with write-over-read priority. The array-specific power supply improves SRAM cell stability and performance while reducing the logic voltage level. The macro is fabricated in a 45nm CMOS SOI technology.

19.3 A 32nm High-κ Metal-Gate SRAM with Adaptive Dynamic-Stability Enhancement for Low-Voltage Operation

9:30 AM

H. H. Nho, P. Kolar, F. Hamzaoglu, Y. Wang, E. Karl, Y-G. Ng, U. Bhattacharya, K. Zhang

Intel, Hillsboro, OR

A 3.4Mb SRAM macro is developed with a built-in stability sensor for adaptive wordline under-drive (AWLUD) in 32nm HK-MG CMOS technology. By tracking temperature, voltage and process variation of each die, the AWLUD is shown to lower VCCmin by 130mV, increase yield by 9% at a target frequency, and is projected to reduce test time up to 40% by eliminating die-by-die WLUD programming.

Break   10:00 AM

19.4 A Configurable SRAM with Constant-Negative-Level Write Buffer for Low Voltage Operation with 0.149µm² Cell in 32nm High-κ/Metal Gate CMOS

10:15 AM

Y. Fujimura, O. Hirabayashi, T. Sasaki, A. Suzuki, A. Kawasumi, Y. Takeyama, K. Kushida, G. Fukano, A. Katayama, Y. Niki, T. Yabe

Toshiba Semiconductor, Kawasaki, Japan

This paper presents a configurable SRAM with 0.149µm² cell in 32nm high-k metal-gate CMOS. Constant-negative-level write buffer adjusts bitline level automatically for configuration range of four to 512 cells/bitline, improving write margin at low voltage. Measurement results demonstrate that cell-failure-rate improves by two orders of magnitude at 0.5V.

19.5   A 512kb 8T SRAM Macro Operating Down to 0.57V with An AC-Coupled Sense Amplifier and Embedded Data-Retention-Voltage Sensor in 45nm SOI CMOS

10:45 AM

M. Qazi[1], K. Stawiasz[2], L. Chang[2], A. Chandrakasan[1]

[1]Massachusetts Institute of Technology, Cambridge, MA

[2]IBM T. J. Watson, Yorktown Heights, NY

An 8T SRAM fabricated in 45nm SOI CMOS exhibits voltage scalable operation from 1.2V down to 0.57V with access times from 400ps to 3.4ns. Timing variation and the challenge of low-voltage operation are addressed with an AC-coupled sense amplifier. An area efficient data path is achieved with a regenerative global-bitline scheme. Finally, a data-retention-voltage sensor is developed to predict the mismatch-limited minimum-standby voltage without corrupting the content of the memory.

19.6   PVT-and-Aging Adaptive Wordline Boosting for 8T SRAM Power Reduction

11:15 AM

A. Raychowdhury, B. Geuskens, J. Kulkarni, J. Tschanz, K. Bowman, T. Karnik, S-L. Lu, V. De, M. M. Khellah

Intel, Hillsboro, OR

A 16KB 8T register-file macro in a 45nm CMOS process uses on-die PVT-adaptive boosting of read- and write-wordline for minimizing V_{MIN} while reducing boosting overhead for maximum power benefit. Measurements of 1MB 8T arrays in a single-VCC µP core indicate 6 to 27% lower power for arrays access variations by 10% (75pF) to 30% (1nF).

19.7   SRAM Stability Characterization Using Tunable Ring Oscillators in 45nm CMOS

11:45 AM

J. Tsai[1], S. Toh[1], Z. Guo[1], L-T. Pang[1,2], T-J. King Liu[1], B. Nikolic[1]

[1]University of California, Berkeley, CA

[2]IBM T. J. Watson, Yorktown Heights, NY

A method to characterize distributions of read and write margins of an SRAM array using tunable ring oscillators (ROs) is presented. A 45nm CMOS testchip demonstrates a write RO with frequency that correlates well with static wordline write-trip voltage and a read RO that that correlates well with the static-current noise margin as well as with the cell read current.

19.8   A 0.5V 100MHz PD-SOI SRAM with Enhanced Read Stability and Write Margin by Asymmetric MOSFET and Forward Body Bias

12:00 PM

K. Nii[1], M. Yabuuchi[1], Y. Tsukamoto[1], Y. Hirano[2], T. Iwamatsu[2], Y. Kihara[1]

[1]Renesas Technology, Kodaira, Japan

[2]Renesas Technology, Itami, Japan

We present a 0.5V 6T SRAM fabricated in a 90nm PD-SOI technology with asymmetric MOSFET to improve the read and write margin. The design also uses a forward-body-bias technique in the bit-cell and peripheral circuits. The measured minimum operating voltage of the SRAM is 0.45V at 25°C, which is 100mV lower than conventional SRAM. The access time is 6.8ns at 0.5V.

Conclusion   **12:15 PM**

SESSION 20

Session Chair: Michael M. Green, *University of California, Irvine, CA*
Associate Chair: Daniel Friedman, *IBM T.J. Watson, Yorktown Heights, NY*

20.1   10Gb/s 15mW Optical Receiver with Integrated Germanium Photodetector and Hybrid Inductor Peaking in 0.13µm SOI CMOS Technology

8:30 AM

D. Kucharski, D. Guckenberger, G. Masini, S. Abdalla, J. Witzens, S. Sahni

Luxtera, Carlsbad, CA

A 10Gb/s optical receiver with an integrated germanium photodetector is presented. The receiver is fabricated in a silicon-photonics-enabled 0.13µm SOI CMOS technology. The high-speed circuits consume 15mW, achieving sensitivity of 6µA p-p at BER=10^{-12} with less than 5ps of DJ. Photodetector dark current is 3µA at a reverse bias of 1V, and responsivity is 0.8A/W.

20.2   An 8.5Gb/s CMOS OEIC with On-Chip Photodiode for Short-Distance Optical Communications

9:00 AM

D. Lee[1], J. Han[2], E. Chang[1], G. Han[1], S. Park[2]

[1]Yonsei University, Seoul, Korea

[2]Ewha Womans University, Seoul, Korea

An 8.5Gb/s single-chip optoelectronic receiver with on-chip photodiode is realized in a 0.13µm CMOS process, where an adaptive equalizer utilizing a slope-detection algorithm is presented. Measured results demonstrate 120dB-Ω transimpedance gain, 5.9GHz bandwidth, -3dBm sensitivity, and 47mW power dissipation from a single 1.5V supply. The chip core occupies an area of 0.1mm^2.

20.3   A 1.296-to-5.184Gb/s Transceiver with 2.4mW/(Gb/s) Burst-Mode CDR using Dual-Edge Injection-Locked Oscillator

9:30 AM

K. Maruko[1], T. Sugioka[1], H. Hayashi[1], Z. Zhou[1], Y. Tsukuda[1], Y. Yagishita[1], H. Konishi[2], T. Ogata[2], H. Owa[1], T. Niki[1], K. Konda[1], M. Sato[1], H. Shiroshita[1], T. Ogura[1], T. Aoki[1], H. Kihara[1], S. Tanaka[1]

[1]Sony, Tokyo, Japan

[2]Sony LSI Design, Yokohama, Japan

A 1.296-to-5.184Gb/s transceiver with 2.4mW/(Gb/s) burst-mode CDR using a dual-edge injection-locked oscillator is fabricated in 40nm CMOS. The chip operates over a range of 1.296 to 5.184Gb/s. The proposed CDR locks in less than 20b and features continuous-rate capability, with twice the power efficiency of previously reported continuous-rate burst-mode CDRs.

Break   10:00 AM

20.4   A 78mW 11.8Gb/s Serial Link Transceiver with Adaptive RX Equalization and Baud-Rate CDR in 32nm CMOS

10:15 AM

F. Spagna[1], L. Chen[1], M. Deshpande[1], Y. Fan[2], D. Gambetta[1], S. Gowder[1], S. Iyer[1], R. Kumar[1], P. Kwok[1], R. Krishnamurthy[1], C-C. Lin[1], R. Mohanavelu[1], R. Nicholson[1], J. Ou[1], M. Pasquarella[1], K. Prasad[1], H. Rustam[1], L. Tong[1], A. Tran[1], J. Wu[1], X. Zhang[1]

[1]Intel, Santa Clara, CA

[2]Intel, Hillsboro, OR

An 11.8Gb/s transceiver with 3-tap FIR TX and adaptively equalized RX is implemented in a 32nm CMOS process. The RX features a continuous-time LE with AGC, a 4-tap DFE and baud-rate timing recovery. The transceiver achieves a BER<2×10^{-15} with PRBS23 over a 24" PCB trace with 25dB loss at 5.9GHz. The TX/RX lane occupies 0.155mm^2 and consumes 78mW from a 0.95V supply when operating at 11.8Gb/s.

20.5   A 12.3mW 12.5Gb/s Complete Transceiver in 65nm CMOS

<div align="right">10:45 AM</div>

K. Fukuda, H. Yamashita, G. Ono, R. Nemoto, E. Suzuki, T. Takemoto, F. Yuki, T. Saito

Hitachi, Tokyo, Japan

This paper presents a 12.3mW 12.5Gb/s complete transceiver in a 65nm standard digital CMOS process. The chip includes a CDR, MUX/DEMUX, and global clock distribution network. A number of low-power design techniques are described that allow a power efficiency of 0.98mW/(Gb/s).

20.6   A 32mW 7.4Gb/s Protocol Agile Source-Series Terminated Transmitter in 45nm CMOS SOI

<div align="right">11:15 AM</div>

W. D. Dettloff[1], J. C. Eble[1], L. Luo[1], P. Kumar[2], F. Heaton[1], T. Stone[1], B. Daly[1]

[1]Rambus, Chapel Hill, NC

[2]Rambus, Bangalore, India

An SST transmitter is described with ground regulation, P-to-N shunting and partially weighted segments for fine granularity level/equalization. Clocks and datapath dissipate 32mW at 7.4Gb/s with an 800mV eye for a power efficiency of 4.32mW/(Gb/s). Measured total jitter is 209.6mUI or 28.3ps at 10^{-12} BER. Target protocols include PCIe G1/2, XAUI, FC 1/2/4, CEI6 MR and SATA 1/2.

20.7   A 5-to-25Gb/s 1.6-to-3.8mW/(Gb/s) Reconfigurable Transceiver in 45nm CMOS

<div align="right">11:45 AM</div>

G. Balamurugan, F. O'Mahony, M. Mansuri, J. E. Jaussi, J. T. Kennedy, B. Casper

Intel, Hillsboro, OR

A reconfigurable transceiver capable of adapting its signaling mode to the I/O channel is implemented in 45nm CMOS. When configured for single-ended 2/3/4-PAM, it enables 5-to-25Gb/s signaling over on-package interconnect while dissipating 1.6-to-2.6mW/(Gb/s). Over a backplane channel, a differential source series-terminated signaling configuration with TX pre-emphasis and 1-tap DFE allows 10Gb/s signaling with 3.8mW/(Gb/s) power efficiency.

20.8   A 2×25Gb/s Deserializer with 2:5 DMUX for 100Gb/s Ethernet Applications

<div align="right">12:00 PM</div>

K-C. Wu, J. Lee

National Taiwan University, Taipei, Taiwan

A 2×25Gb/s deserializer for 100Gb/s Ethernet is implemented in 65nm CMOS technology. Employing regulated limiting amplifiers, full-rate CDRs, a built-in clock generator, and a 2:5 DMUX, this two-channel prototype achieves BER<10^{-12} with 20mV$_{pp}$ input sensitivity while consuming a total power of 510mW.

<div align="right">**Conclusion   12:15 PM**</div>

SESSION 21

Session Chair: Un-Ku Moon, *Oregon State University, Corvallis, OR*
Associate Chair: Tatsuji Matsuura, *Renesas Technology, Gunma, Japan*

21.1   An 18b 12.5MHz ADC with 93dB SNR

8:30 AM

C. P. Hurrell[1], C. Lyden[2], D. Laing[1], D. Hummerston[1], M. Vickery[1]

[1]Analog Devices, Newbury, United Kingdom

[2]Analog Devices, Cork, Ireland

This paper describes an 18b 12.5MHz ADC that uses a pipeline of 2 successive-approximation ADCs. Both ADCs, one before and one after a closed loop residue amplifier, determine 2 bits plus one redundant bit per bit trial. The converter core consumes 105mW and achieves a dynamic range of 93dB. The chip is implemented in a 0.25µm/0.5µm CMOS process and occupies 6mm^2.

21.2   A 12b 22.5/45MS/s 3.0mW 0.059mm^2 CMOS SAR ADC Achieving Over 90dB SFDR

9:00 AM

W. Liu, P. Huang, Y. Chiu

University of Illinois at Urbana-Champaign, Urbana, IL

A perturbation-based background digital calibration enables the capacitance scaling to the kT/C limit in a 12b SAR ADC. Combined with a dynamic threshold comparison technique, the 0.13µm CMOS prototype measures a 71.1dB peak SNDR, a 94.6dB peak SFDR, and a peak FoM of 31.4fJ/conversion-step while dissipating 3.0mW from a 1.2V supply and occupying 0.059mm^2.

21.3   A 0.06mm^2 8.9b ENOB 40MS/s Pipelined SAR ADC in 65nm CMOS

9:30 AM

M. Furuta, M. Nozawa, T. Itakura

Toshiba, Kawasaki, Japan

An 8.9-ENOB 40MS/s two-stage pipelined SAR ADC for a WLAN receiver is designed and fabricated in a 65nm CMOS technology. The 1st stage is realized by a 1.5b/cycle SAR to mitigate the comparator offset issue. The 2nd stage employs a radix-1.8 SAR to avoid the parasitic capacitance issue. The presented architecture occupies 0.06mm^2 of area despite using a large unit capacitance of 60fF.

Break   10:00 AM

21.4   A 10b 50MS/s 820µW SAR ADC with On-Chip Digital Calibration

10:15 AM

M. Yoshioka, K. Ishikawa, T. Takayama, S. Tsukamoto

Fujitsu Laboratories, Kawasaki, Japan

A 10b 50MS/s SAR ADC is presented that uses comparator offset calibration, CDAC linearity error calibration and internal clock frequency control to compensate for the PVT variation. The prototype in 65nm CMOS achieves 56.9dB SNDR at 50MS/s and consumes 820µW from a 1.0V supply including the digital calibration circuits.

21.5 A 10b 100MS/s 1.13mW SAR ADC with Binary-Scaled Error Compensation

10:45 AM

C-C. Liu[1], S-J. Chang[1], G-Y. Huang[1], Y-Z. Lin[1], C-M. Huang[2], C-H. Huang[2], L. Bu[2], C-C. Tsai[2]

[1]National Cheng-Kung University, Tainan, Taiwan

[2]Himax Technologies, Tainan, Taiwan

This paper presents a 10b SAR ADC with a binary-scaled error compensation technique. The prototype occupies an active area of $155 \times 165 \mu m^2$ in 65nm CMOS. At 100MS/s, the ADC achieves an SNDR of 59.0dB and an SFDR of 75.6dB, while consuming 1.13mW from a 1.2V supply. The FoM is 15.5fJ/conversion-step.

21.6 A 30fJ/Conversion-Step 8b 0-to-10MS/s Asynchronous SAR ADC in 90nm CMOS

11:15 AM

P. Harpe, C. Zhou, X. Wang, G. Dolmans, H. de Groot

Holst Centre-IMEC, Eindhoven, Netherlands

An 8b SAR ADC is presented. The 90nm CMOS prototype achieves an ENOB of 7.8b at a sampling frequency of 10.24MS/s. The use of asynchronous dynamic CMOS logic, custom-designed capacitors, an internal common-mode shift and low-leakage design techniques results in a power consumption of 69µW from a 1V supply. The corresponding FoM equals 30fJ/Conversion-step and is maintained down to 10kS/s.

21.7 A 40GS/s 6b ADC in 65nm CMOS

11:45 AM

Y. M. Greshishchev, J. Aguirre, R. Gibbins, C. Falt, P. Flemke, N. Ben-Hamida, D. Pollex, P. Schvan, S-C. Wang, M. Besson

Nortel, Ottawa, Canada

A 6b 65nm CMOS ADC exceeds the 29GS/s requirement of a 58Gb/s DP-QPSK optical receiver while operating up to 40GS/s. An interleaved architecture combines 16 SAR converters and an array of T/Hs with delay, gain, and offset calibration. A 1V 40mW 2.5GS/s sub-ADC results in a total power of 1.5W, ENOB of 4.5b (3.9b) up to 10GHz (18GHz). An on-chip signal synthesizer simplifies production testing.

Conclusion   **12:15 PM**

SESSION 22

Session Chair: Shoji Kawahito, *Shizuoka University, Hamamatsu, Japan*

Associate Chair: JungChak Ahn, Samsung Electronics, Yongin, Korea

22.1   A 2.1Mpixel 120frame/s CMOS Image Sensor with Column-Parallel ΔΣ ADC Architecture

8:30 AM

Y. Chae[1], J. Cheon[1], S. Lim[1], D. Lee[1], M. Kwon[2], K. Yoo[2], W. Jung[2], D-H. Lee[2], S. Ham[2], G. Han[1]

[1]Yonsei University, Seoul, Korea

[2]Samsung Electronics, Yongin, Korea

A 2.1Mpixel 120frame/s CMOS image sensor with column-parallel ΔΣ ADCs is realized in a 0.13μm CMOS process. Column-parallel ΔΣ ADC architectures improve the conversion speed while reducing the random noise level as well. Inverter-based SC circuits maximize the power efficiency. This sensor achieves a measured noise floor of 1.9e-, while dissipating 180mW.

22.2   A 1.1e- Temporal Noise 1/3.2-inch 8Mpixel CMOS Image Sensor using Pseudo-Multiple Sampling

9:00 AM

Y. Lim, K. Koh, K. Kim, H. Yang, J. Kim, Y. Jeong, S. Lee, H. Lee, S-H. Lim, Y. Han, J. Kim, J. Yun, S. Ham, Y-T. Lee

Samsung Electronics, Yongin, Korea

A pseudo-multiple sampling technique for a low-noise CIS is implemented using a conventional column-parallel single-slope ADC structure with no additional circuitry. It is applied to a 1/3.2-inch 8Mpixel CIS. Measurement results show the technique effectively reduces dark temporal noise from 1.6e- to 1.2e- in 10b ADC mode, and from 1.8e- to 1.1e- in 12b ADC mode.

22.3   A 2.7e- Temporal Noise 99.7% Shutter Efficiency 92dB Dynamic Range CMOS Image Sensor with Dual Global Shutter Pixels

9:15 AM

K. Yasutomi, S. Itoh, S. Kawahito

Shizuoka University, Hamamatsu, Japan

A dual global shutter CIS with pinned storage diode and floating diffusion memory enables a low noise level of 2.7e- and wide dynamic range of 92dB. Dual doping pinned diodes with a shielding structure attain a high shutter efficiency of 99.7%.

22.4   A QVGA 143dB Dynamic Range Asynchronous Address-Event PWM Dynamic Image Sensor with Lossless Pixel-Level Video Compression

9:30 AM

C. Posch, D. Matolin, R. Wohlgenannt

Austrian Institute of Technology, Vienna, Austria

A 0.18μm CIS contains a QVGA array of autonomous pixels that individually detect illumination changes and communicate new gray levels that are PWM encoded after each detected change, ideally realizing optimal lossless pixel-level video compression. Readout is frame-free 18b parallel AER. SNR of >56dB and intra-scene DRs of 143dB static and 125dB at 30fps equivalent have been achieved.

Break   10:00 AM

22.5   A CMOS Image Sensor for 10Mb/s 70m-Range LED-Based Spatial Optical Communication

10:15 AM

S. Itoh[1], I. Takai[2], M. Z. Sarker[1], M. Hamai[1], K. Yasutomi[1], M. Andoh[2], S. Kawahito[1]

[1]Shizuoka University, Hamamatsu, Japan

[2]Toyota Central R&D Labs, Aichi, Japan

A CMOS image sensor for spatial optical communication is presented. A two-transistor optical communication cell with a depleted photodiode and lateral charge overflow drain improves the light pulse response. A weighed summation of 9-point parallel analog outputs and pulse-equalizing technique greatly enhance the bit-rate and communication distance up to 10Mb/s and 70m, respectively.

22.6   A 256×256 14k Range Maps/s 3-D Range-Finding Image Sensor Using Row-Parallel Embedded Binary Search Tree and Address Encoder

10:45 AM

S. Mandai, M. Ikeda, K. Asada

University of Tokyo, Tokyo, Japan

A high-speed 3D range finder uses current-mode subtraction, a row-parallel embedded binary search tree and address encoding, and a mask circuit to achieve 14.4k-range-maps/s, and the maximum and the standard deviation of range error of 0.997mm and 0.258mm, respectively, at a target distance of 400mm.

22.7   An 80×60 Range Image Sensor based on 10µm 50MHz Lock-In Pixels in 0.18µm CMOS

11:15 AM

D. Stoppa, N. Massari, L. Pancheri, M. Malfatti, M. Perenzoni, L. Gonzo

Fondazione Bruno Kessler - IRST, Trento, Italy

A lock-in pixel array based on a fast charge transfer pinned photo-detector for time-of-flight range imaging is presented. Distance measurements at 5-to-20fps on a 6-to-3m range are reported with a linearity error lower than 0.7% and a repeatability of 5-to-16cm, while the best achievable precision is 2.7cm. A demodulation frequency up to 50MHz is demonstrated with a contrast of 29.5%.

22.8   A 2.2/3-inch 4Kx2K CMOS Image Sensor Based on Dual Resolution and Exposure Technique

11:45 AM

T. Azuma[1], T. Imagawa[1], S. Ugawa[1], Y. Okada[1], H. Komobuchi[1], M. Ishii[2], S. Kasuga[2], Y. Kato[2]

[1]Panasonic, Kyoto, Japan

[2]Panasonic, Takatsuki, Japan

A 2.2/3-Inch 4K2K dual resolution and exposure CMOS imager uses motion information to improve the sensitivity by 4 times in comparison to a conventional sensor. The green pixels are read out once every four frames for high sensitivity. Both the red and blue pixels are read out each frame, binned for 2×2 and used for motion compensation.

22.9   A 1/2.3-inch 10.3Mpixel 50 frame/s Back-Illuminated CMOS Image Sensor

12:00 PM

H. Wakabayashi[1], K. Yamaguchi[1], M. Okano[1], S. Kuramochi[1], O. Kumagai[1], S. Sakane[1], M. Ito[1], M. Hatano[1], M. Kikuchi[1], Y. Yamagata[1], T. Shikanai[1], K. Koseki[1], K. Mabuchi[1], Y. Maruyama[1], K. Akiyama[1], E. Miyata[2], T. Honda[2], M. Ohashi[2], T. Nomoto[1]

[1]Sony, Atsugi, Japan

[2]Sony Semiconductor, Nagasaki, Japan

A 1/2.3-inch 10.3Mpixel 50frame/s CMOS image sensor fabricated using a 0.13µm 1P4M CMOS process with back-illumination technology achieves sensitivity of 9890e⁻/lux·s, random noise of 1.7e⁻ and saturation of 8850e⁻. The sensor integrates a 10b/12b analog-to-digital converter, an internal PLL and a 10b serial LVDS interface to enable a data-rate up to 576MHz.

Conclusion 12:15 PM

SESSION 23

MM-WAVE TRANSCEIVERS, POWER AMPLIFIERS, & SOURCES

Session Chair: Michael Zybura, *RFMD Scotts Valley Design Center, Scotts Valley, CA*
Associate Chair: Satoshi Tanaka, *Renesas Technology, Komoro, Japan*

23.1   A Millimeter-Wave Intra-Connect Solution

1:30 PM

K. Kawasaki[1], Y. Akiyama[1], K. Komori[1], M. Uno[1], H. Takeuchi[1], T. Itagaki[1], Y. Hino[1], Y. Kawasaki[1], K. Ito[1], A. Hajimiri[2]
[1]Sony, Tokyo, Japan
[2]California Institute of Technology, Pasadena, CA

An 11Gb/s low-power mm-wave end-to-end solution for short-range wireless Intra-Connect with an active footprint of 0.13mm^2 per channel is demonstrated. Implemented in 40nm CMOS, the 60GHz transmitter and the injection-locked receiver achieve coherent transmission with BER of 10^{-11} over a distance of 14mm.

23.2   A SiGe Quadrature Transmitter and Receiver Chipset for Emerging High-Frequency Applications at 160GHz

2:00 PM

U. R. Pfeiffer, E. Öjefors, Y. Zhao
University of Wuppertal, Wuppertal, Germany

A 158-to-165GHz TX and RX chipset supporting QAM modulation schemes is implemented in SiGe. Double-balanced I/Q mixers are used for direct up-/down-conversion. The LO chain consists of a VCO, a frequency prescaler, a tripler/amplifier chain, and a differential 90deg coupler. The RX further includes an LNA and the TX a PA. The RX system NF is 11 to 14 dB and the TX P$_{sat}$ is up to 5dBm.

23.3   A W-Band 65nm CMOS Transmitter Front-End with 8GHz IF Bandwidth and 20dB IR-Ratio

2:30 PM

D. Sandström, M. Varonen, M. Kärkkäinen, K. A. Halonen
Helsinki University of Technology, Espoo, Finland

A W-band transmitter front-end has been implemented in 65nm CMOS. The output power is higher than +4dBm from 77GHz to 94GHz with an image rejection ratio from 15dB to 25dB. The highest 1dB output compression point is +2.2dBm with + 6.6dBm maximum power at 85GHz. The transmitter draws 100mA from a 1.2V supply.

Break   3:00 PM

23.4   A 90GHz-Carrier 30GHz-Bandwidth Hybrid Switching Transmitter with Integrated Antenna

3:15 PM

A. Arbabian[1], B. Afshar[1], J-C. Chien[1], S. Kang[1], S. Callender[1], E. Adabi[1], S. Toso[2], R. Pilard[3], D. Gloria[3], A. Niknejad[1]
[1]University of California, Berkeley, CA   [2]University of Padova, Padova, Italy
[3]STMicroelectronics, Crolles, France

A fully integrated 90GHz-carrier pulsed transmitter with on-chip antenna and >30GHz measured bandwidth is demonstrated in 0.13µm SiGe BiCMOS. By exploring the benefits of hybrid PA/antenna switching and high-performance digital circuitry, the transmitter generates variable-width carrier-modulated pulses with minimum measured pulse width of 35ps.

23.5   A 13.1% Tuning Range 115GHz Frequency Generator Based on an Injection-Locked Frequency Doubler in 65nm CMOS

3:45 PM

A. Mazzanti[1], E. Monaco[1,2], M. Pozzoni[3], F. Svelto[4]

[1]University of Modena and Reggio Emilia, Modena, Italy

[2]Istituto Universitario di Studi Superiori, Pavia, Italy

[3]STMicroelectronics, Pavia, Italy   [4]University of Pavia, Pavia, Italy

A CMOS frequency multiplier is based on a Pierce oscillator injection-locked by a push-push pair. Compared to traditional stand-alone push-push multipliers driving a selective load, this solution provides a differential output and a larger voltage swing. When driven by a half-frequency VCO, prototypes in 65nm CMOS demonstrate a 13.1% tuning range at 115GHz with a phase noise of -107dBc/Hz @ 10MHz offset for a total power dissipation of 12mW.

23.6   A 1V 17.9dBm 60GHz Power Amplifier in Standard 65nm CMOS

4:15 PM

J-W. Lai[1], A. Valdes-Garcia[2]

[1]MediaTek, Hsinchu, Taiwan   [2]IBM T. J. Watson, Yorktown Heights, NY

A CMOS PA integrating a power detector for all IEEE 802.15.3c bands is demonstrated. A fully synchronous power combiner removes design trade-offs between transformer efficiency and power combining efficiency. At 1V supply, the measured P_{sat}, OP_{1dB}, and peak PAE at 61.5GHz are 17.9dBm, 15.4dBm, and 11.7% respectively. A P_{sat} of +17dBm and an OP_{1dB} of +14dBm are achieved across the 57-to-65GHz band.

23.7   A High-Gain 60GHz Power Amplifier with 20dBm Output Power in 90nm CMOS

4:30 PM

C. Y. Law, A-V. Pham

University of California, Davis, CA

A fully integrated 60GHz power amplifier using a standard 90nm CMOS process is presented. The power amplifier consists of six 2-stage power amplifiers, three 2-way Wilkinson power splitters for parallel amplification, and three 2-way Wilkinson power combiners to combine the output power. The power amplifier achieves a gain of +20dB, a P_{1dB} of +18dBm and a P_{sat} of +20dBm with 1.2V supply.

23.8   A 53-to-68GHz 18dBm Power Amplifier with an 8-Way Combiner in Standard 65nm CMOS

4:45 PM

B. Martineau[1], V. Knopik[2], A. Siligaris[3], F. Gianesello[1], D. Belot[1]

[1]STMicroelectronics, Crolles, France   [2]ST-Ericsson, Crolles, France

[3]CEA-LETI-Minatec, Grenoble, France

A 53-to-68GHz power amplifier with an 8-way combiner in standard 65nm CMOS meeets the wireless HDMI standard. Reliability is improved by solving the issues of time-dependent dielectric breakdown and hot-carrier-injection degradation. The PA output power is 18dBm.

23.9   A 650GHz SiGe Receiver Front-End for Terahertz Imaging Arrays

5:00 PM

E. Öjefors, U. R. Pfeiffer

University of Wuppertal, Wuppertal, Germany

A 650GHz imaging receiver with an on-chip folded-dipole antenna in a SiGe technology is presented. The subharmonic 162.5GHz LO is supplied by an integrated 6dBm LO driver amplifier. The receiver chip occupies $1.2 \times 0.6mm^2$ and provides a bandwidth of 635 to 665 GHz, a -13dBi conversion gain and a 42dB NF.

Conclusion 5:15 PM

SESSION 24

DRAM & FLASH MEMORIES

Session Chair: Ken Takeuchi, *University of Tokyo, Tokyo, Japan*

Associate Chair: Nicky C.C. Lu, *Etron Technology, Hsinchu, Taiwan*

24.1   A 7Gb/s/pin GDDR5 SDRAM with 2.5ns Bank-to-Bank Active Time and No Bank-Group Restriction

1:30 PM

T-Y. Oh, Y-S. Sohn, S-J. Bae, M-S. Park, J-H. Lim, Y-K. Cho, D-H. Kim, D-M. Kim, H-R. Kim, H-J. Kim, J-H. Kim, J-K. Kim, Y-S. Kim, B-C. Kim, S-H. Kwak, J-H. Lee, J-Y. Lee, C-H. Shin, Y-S. Yang, B-S. Cho, S-Y. Bang, H-J. Yang, Y-R. Choi, G-S. Moon, C-G. Park, S-W. Hwang, J-D. Lim, K-I. Park, J. Choi, Y-H. Jun

Samsung Electronics, Gyeonggi, Korea

7Gb/s/pin operation without bank group restriction in a GDDR5 SDRAM is achieved by skewed control logic and current-mode I/O sense amplifiers with regular calibration from replica impedance monitors. The bank-to-bank active time is shortened to 2.5ns by a FIFO-based BLSA enabler, 2.0ns latency V_{PP} generator and active jitter canceler. The chip is fabricated in a 50nm DRAM process in a 61.6mm^2 die area.

24.2   A 1.2V 0.33W 12.8GB/s 4-Channel 1Gb Mobile Wide-I/O DRAM with 512 I/Os

2:00 PM

J-S. Kim, H. Lee, D. Lee, C. Oh, H. Hwang, S. Hwang, B. Na, J. Moon, J-G. Kim, H. Park, J-W. Ryu, K. Park, S. Kang, S-Y. Kim, H. Kim, J-M. Bang, H. Cho, M. Jang, C. Han, J-B. Lee, K. Kyung, J. Choi, Y-H. Jun

Samsung Electronics, Hwasung, Korea

A 1.2V 1Gb mobile SDRAM, having 4 channels with 128 DQ pins per each is fabricated. It exhibits 330.6mW read operating power during 4 channel operation, achieving 12.8GB/s data bandwidth. Test correlation techniques to verify functions through microbumps are also developed. Block-based dual data retention scheme is applied to reduce self-refresh current.

24.3   An 8Tb/s 1pJ/b 0.8mm^2/Tb/s QDR Inductive-Coupling Interface Between 65nm CMOS GPU and 0.1µm DRAM

2:30 PM

N. Miura, K. Kasuga, M. Saito, T. Kuroda

Keio University, Yokohama, Japan

An 8Tb/s 1pJ/b 0.8mm^2/Tb/s inductive-coupling interface between 65nm CMOS GPU and 0.1µm DRAM is developed. BER <10^{-16} operation is examined in 1024-bit parallel links. Compared to the latest wired 40nm DRAM interface, the bandwidth is increased 32×, and the energy consumption and layout area are reduced by 8× and 22×, respectively.

Break   3:00 PM

24.4   A Bitline Sense Amplifier for Offset Compensation

3:15 PM

M. Lee, K. Kyung, H. Won, M. Lee, K. Park

Hynix Semiconductor, Icheon, Korea

We design a DRAM bitline sense-amplifier (BLSA) immune to data-pattern-dependent sensing noise. We fabricate a 68nm DRAM chip using the scheme and the measured results match the simulation results. The BLSA has 15% of the total sensing noise of the fabricated conventional BLSA.

24.5   A 2Gb/s 1.8pJ/b/chip Inductive-Coupling Through-Chip Bus for 128-Die NAND-Flash Memory Stacking

3:30 PM

M. Saito, N. Miura, T. Kuroda

Keio University, Yokohama, Japan

128 NAND Flash memory chips and 1 controller chip are stacked using a spiral stair stacking scheme. The controller accesses a random memory chip at 2Gb/s by inductive-coupling through-chip transmission relayed at every 8th chip. The large coils are placed diagonally over memory core with no area penalty. Energy consumption is reduced to 1.8pJ/b/chip.

24.6   A 159mm² 32nm 32Gb MLC NAND-Flash Memory with 200MB/s Asynchronous DDR Interface

3:45 PM

H. Kim, J-H. Park, K-T. Park, P. Kwak, O. Kwon, C. Kim, Y. Lee, S. Park, K. Kim, D. Cho, J. Lee, J. Song, S. Lee, H. Yoo, S. Kim, S. Yu, S. Kim, S. Lee, K. Kyung, Y-H. Lim, C. Chung

Samsung Electronics, Hwasung, Korea

We present a 159mm² 32Gb MLC NAND Flash that is capable of 200MB/s read and 12MB/s write throughputs in 32nm technology. This performance is achieved by using DDR interface and by using new core memory and data path architecture as well as program algorithm.

24.7   A 3bit/Cell 32Gb NAND Flash Memory at 34nm with 6MB/s Program Throughput and with Dynamic 2b/Cell Blocks Configuration Mode for a Program Throughput Increase up to 13MB/s

4:15 PM

G. G. Marotta[1], A. Macerola[1], A. D'Alessandro[1], A. Torsi[1], C. Ceratogli[1], C. Lattaro[1], C. Musilli[1], D. Rivers[2], E. Sirizotti[1], F. Paolini[1], G. Imondi[1], G. Naso[1], G. Santin[1], L. Botticchio[1], L. De Santis[1], L. Pilolli[1], M. L. Gallese[1], M. Incarnati[1], M. Tiburzi[1], P. Conenna[1], S. Perugini[1], V. Moschiano[1], W. Di Francesco[1], M. Goldman[3], C. Haid[3], D. Di Cicco[1], D. Orlandi[1], F. Rori[1], M. Rossini[1], T. Vali[1], R. Ghodsi[4], F. Roohparvar[4]

[1]Micron, Avezzano, Italy; [2]Micron, Boise, ID
[3]Intel, Folsom, CA; [4]Micron, San Jose, CA

A 3.3V 32Gb NAND-Flash memory with 3b/cell is demonstrated in 34nm technology. The device features a programming throughput of 6MB/s on blocks configured as 3b/cell mode and can dynamically switch up to 13MB/s in 2b/cell mode. A new quad-plane architecture and an optimized programming algorithm are adopted to achieve the design targets.

24.8   A 32Gb MLC NAND-Flash Memory with V_{th}-Endurance-Enhancing Schemes in 32nm CMOS

4:45 PM

C. Lee, S-K. Lee, S. Ahn, J. Lee, W. Park, Y. Cho, C. Jang, C. Yang, S. Chung, I-S. Yun, B. Joo, B. Jeong, J. Kim, J. Kwon, H. Jin, Y. Noh, J. Ha, M. Sung, D. Choi, S. Kim, J. Choi, T. Jeon, J-S. Yang, Y-H. Koh

Hynix Semiconductor, Icheon, Korea

A 32nm 32Gb MLC flash memory, with MSB even page re-program, dramatically improves floating-gate (FG) coupling-induced V_{th}-widening while FG coupling cancellation program verify read minimizes performance loss due to additional program operation allowing throughput of 13.0MB/s. More than 30% improvement in retention-V_{th}-shift and additional 50mV reduction of cell Vth distribution is achieved by moving-read and adaptive code selection. Die size of the device is 146mm² in 3M 32nm CMOS.

Conclusion   5:15 PM

SESSION 25

WIRELESS CONNECTIVITY

Session Chair: Arya Behzad, *Broadcom, San Diego, CA*
Associate Chair: Masoud Zargari, *Atheros, Irvine, CA*

25.1 A Maximally-Digital Radio Receiver Front-End

1:30 PM

F. Opteynde
Audax Technologies, Leuven, Belgium
A radio receiver with reduced analog circuits contains two ADCs placed immediately after the mixers. All filtering, offset compensation and variable gain are realised in the digital domain. The overall receiver chain, including ADCs, consumes 12mW and occupies 0.07mm^2 in a 40nm standard digital CMOS technology.

25.2 A 65nm CMOS 2.4GHz 31.5dBm Power Amplifier with a Distributed LC Power-Combining Network and Improved Linearization for WLAN Applications

1:45 PM

A. Afsahi[1,2], A. Behzad[2], L. Larson[1]
[1]University of California, San Diego, CA   [2]Broadcom, San Diego, CA
A 2.4GHz CMOS power amplifier with a distributed LC power-combining network and improved linearization for high-power WLAN applications is presented. With a 3.3v supply the PA produces a saturated power of 31.5dBm with peak PAE of 25%. By utilizing multiple linearization techniques, an EVM of -25dB is achieved at 25.5dBm for the 2.4GHz band. The PA occupies 2.7mm^2 in 65nm CMOS.

25.3 A MultiStandard, Multiband SoC with Integrated BT, FM, WLAN Radios and Integrated Power Amplifier

2:00 PM

C. P. Lee[1], A. Behzad[1], B. Marholev[2], V. Magoon[1], I. Bhatti[2], D. Li[1], S. Bothra[3], A. Afsahi[1], D. Ojo[1], R. Roufoogaran[2], T. Li[2], Y. Chang[2], K. Rama Rao[1], S. Au[1], P. Seetharam[1], K. Carter[1], J. Rael[2], M. Macintosh[1], B. Lee[2], M. Rofougaran[2], R. Rofougaran[2],

A. Hadji-Abdolhamid[2], M. Nariman[2], S. Khorram[2], S. Anand[2], E. Chien[2], S. Wu[2], C. Barrett[3], L. Zhang[2], A. Zolfaghari[2], H. Darabi[2], A. Sarfaraz[3], B. Ibrahim[2], M. Gonikberg[4], M. Forbes[4], C. Fraser[4], L. Gutierrez[4], Y. Gonikberg[4], M. Hafizi[5], S. Mak[1], J. Castaneda[2], K. Kim[2], Z. Liu[3], S. Bouras[6], K. Chien[2], V. Chandrasekhar[2], P. Chang[2], E. Li[3]

[1]Broadcom, San Diego, CA   [2]Broadcom, Irvine, CA

[3]Broadcom, Santa Clara, CA   [4]Broadcom, Sunnyvale, CA

[5]Qualcomm, San Diego, CA   [6]Broadcom, Athens, Greece

A fully integrated SoC compliant with 802.11a/b/g/ssn, BT, and FM standards is presented. Shared blocks include LNA, PA, crystal, bandgap, and RCAL. The WLAN, BT, and FM receivers achieve sensitivities better than -76dBm (54Mb/s/2.4Ghz), -91dBm, and 1uV$_{rms}$, respectively. The WLAN and BT transmitters achieve linear output powers of 21dBm and 10dBm, respectively.

25.4 A Fully Integrated 2×1 Dual-Band Direct-Conversion Transceiver with Dual-Mode Fractional Divider and Noise-Shaping TIA for Mobile WiMAX SoC in 65nm CMOS

2:30 PM

J. Deguchi, D. Miyashita, Y. Ogasawara, G. Takemura, M. Iwanaga, K. Sami, R. Ito, J. Wadatsumi, Y. Tsuda, S. Oda, S. Kawaguchi, N. Itoh, M. Hamada

Toshiba, Kawasaki, Japan

A fully integrated 2×1 dual-band direct-conversion transceiver for a mobile WiMAX SoC in a 65nm CMOS technology is presented. Inductorless LO distribution by compact dual-mode fractional dividers is introduced. Total NF of 3.8dB is achieved by a noise-shaping transimpedance amplifier. It consumes 214.8mW for 1 TX at +1dBm and 214.1mW for 2 RX, and occupies 2.3×6.72mm^2.

Break   3:00 PM

25.5   A 5mm² 40nm LP CMOS 0.1-to-3GHz Multistandard Transceiver

3:15 PM

M. Ingels[1], V. Giannini[1], J. Borremans[1], G. Mandal[1], B. Debaillie[1], P. Van Wesemael[1], T. Sano[2], T. Yamamoto[3], D. Hauspie[4], J. Van Driessche[1], J. Craninckx[1]

[1]IMEC, Leuven, Belgium

[2]Renesas Technology, Itami, Japan

[3]Renesas Technology, Takasaki, Japan

[4]M4S NV, Leuven, Belgium

A 5mm² 40nm digital CMOS multimode transceiver is presented. The 0.1-to-6GHz RX features 4 LNAs, 25% passive mixer with IIP2 calibration, 5th order baseband filtering and a 50fJ/conversion step ADC. It achieves NF down to 2.4dB, better than -30dB EVM and 50dBm IIP2. A 0.1-to-3Ghz TX with baseband filter, voltage sampled mixer and PPA achieves 3.2% EVM at 0dBm output, with CNR down to -156dBc/Hz. The system uses two dual-VCO 5.9-to-12.8GHz fractional-N PLLs.

25.6   A 65nm CMOS Low-Power Small-Size Multistandard, Multiband Mobile Broadcasting Receiver SoC

3:45 PM

M. Jeong[1], B. Kim[1], Y. Cho[1], Y. Kim[1], S. Kim[1], H. Yoo[1], J. Lee[1], J. Lee[1], K. Jung[1], J. Lee[1], J. Lee[1], H. Yang[1], G. Taylor[2], B-E. Kim[1]

[1]Analog Devices, Seongnam, Korea

[2]Analog Devices, San Diego, CA

A 65nm CMOS multistandard multiband mobile broadcasting receiver SoC that covers DAB/T-DMB, ISDB-T 1seg and FM is introduced. The SoC consists of RF/AFE, power management and demodulator. The power consumption is 35mW with a die size of 2.9x2.9 mm². The RF/AFE area is 2.3 mm². The sensitivities are -103dBm, -98dBm, and 1dBuV for T-DMB, 1seg and FM, respectively.

25.7   A Multistandard Multiband Mobile TV RF SoC in 65nm CMOS

4:15 PM

J-H. Chang, H. Kim, J-H. Choi, H. Chung, J. Heo, S. Kang, J-D. Bae, H. Oh, Y. Kim, T-W. Kwon, R. Kim, W. Choo, D. Rhee, B-H. Park

Samsung Electronics, Yongin, Korea

A multistandard, multiband mobile TV SoC that integrates RF tuner, demodulator, FEC, hardwired MPE-FEC, ARM CPU and SRAM is presented. The RF tuner supports direct and low IF conversion to optimize power consumption and performance of each standard. Implemented in 65nm CMOS, it occupies 23.2mm². For DVB-H/ISDB-T 1-segmentation/TDMB, the total SoC power consumption is 203/101/143mW.

25.8   A 1V RF SoC with an 863-to-928MHz 400kb/s Radio and a 32b Dual-MAC DSP Core for Wireless Sensor and Body Networks

4:45 PM

E. Le Roux, N. Scolari, B. Banerjee, C. Arm, P. Volet, D. Sigg, P. Heim, J-F. Perotto, F. Kaess, N. Raemy, A. Vouilloz, D. Ruffieux, M. Contaldo, F. Giroud, D. Séverac, M. Morgan, S. Gyger, C. Monneron, T-C. Le, C. Henzelin, V. Peiris

CSEM, Neuchâtel, Switzerland

A 150µA/MHz DSP with two MAC/cycle instructions is integrated with a configurable 863-to-928MHz RF transceiver that yields 3.5mW in continuous reception, 2µC per channel sampling and 40mW for 10dBm output. The SoC includes voltage converters that allow 1.0-to-1.8V or 2.7-to-3.6V primary voltage supplies. In sleep mode, it consumes 1µA with a 32kHz crystal-based RTC running.

Conclusion   5:15 PM

SESSION 26

Session Chair: SeongHwan Cho, *KAIST, Daejon, Korea*
Associate Chair: K.R. (Kumar) Lakshmikumar, *Conexant Systems, Red Bank, NJ*

26.1 A 3.5GHz Wideband ADPLL with Fractional Spur Suppression Through TDC Dithering and Feedforward Compensation

1:30 PM

C. Weltin-Wu[1,2], E. Temporiti[3], D. Baldi[3], M. Cusmai[2], F. Svelto[2]

[1]Columbia University, New York, NY

[2]University of Pavia, Pavia, Italy

[3]STMicroelectronics, Pavia, Italy

We present a 3.5GHz fractional-N ADPLL with a 3.4MHz bandwidth operating from a 35MHz reference. Using a dithering algorithm and feedforward compensation around the TDC results in spurious performance better than -58dBc, and in-band phase noise of -101dBc/Hz. The IC with fully integrated calibration logic occupies 0.44mm^2 in 65nm CMOS, and consumes 8.7mW.

26.2 A 2.1-to-2.8GHz All-Digital Frequency Synthesizer with a Time-Windowed TDC

2:00 PM

T. Tokairin[1], M. Okada[2], M. Kitsunezuka[1], T. Maeda[1], M. Fukaishi[1]

[1]NEC, Kawasaki, Japan

[2]NEC Electronics, Kawasaki, Japan

A 2.1-to-2.8GHz low-power all-digital PLL with a time-windowed single-shot pulse-controlling 2-step TDC is presented. The test-chip is implemented in 90nm CMOS and exhibits in-band phase noise of -105dBc/Hz with 500kHz loop-bandwidth and out-of-band noise of -115dBc/Hz at 1MHz offset. The chip draws 8.1mA from a 1.2V supply.

26.3 A Calibration-Free 800MHz Fractional-N Digital PLL with Embedded TDC

2:30 PM

M-W. Chen, D. Su, S. Mehta

Atheros Communications, Santa Clara, CA

An 800MHz digital PLL with its TDC embedded within the DVCO is implemented in 65nm CMOS and occupies 0.027mm^2. The design requires no calibration and achieves the fractional-N operation without a multi-modulus feedback divider. To further improve the TDC linearity, mismatch filtering is used to achieve a DNL of less than 3.5% of LSB.

Break   3:00 PM

26.4 Spur-Reduction Techniques for PLLs Using Sub-Sampling Phase Detection

3:15 PM

X. Gao[1], E. A. Klumperink[1], G. Socci[2], M. Bohsali[2], B. Nauta[1]

[1]University of Twente, Enschede, Netherlands

[2]National Semiconductor, Santa Clara, CA

A low-spur sub-sampling PLL exploits an amplitude-controlled charge pump which is immune to current source mismatch. A DLL/PLL dual-loop architecture and buffering reduces the disturbance of the sampler to the VCO. The 2.2GHz PLL in 0.18μm CMOS achieves -121dBc/Hz in-band phase noise at 200kHz and consumes 3.8mW. The worst-case reference spur measured on 20 samples is -80dBc.

26.5   A 3MHz-BW 3.6GHz Digital Fractional-N PLL with Sub-Gate-Delay TDC, Phase-Interpolation Divider, and Digital Mismatch Cancellation

3:45 PM

M. Zanuso, S. Levantino, C. Samori, A. Lacaita

Politecnico di Milano, Milano, Italy

A 3.6GHz digital fractional-N PLL combines a 4b TDC with digital element shuffling, and a 4b feedback phase interpolator with digital cancellation of mismatches. It achieves maximum in-band fractional spur of -57dBc and in-band noise of -104dBc/Hz at 400kHz offset with 3MHz bandwidth. The PLL draws 67mA from a 1.2V supply and occupies an active area of $0.4mm^2$ in 65nm CMOS.

26.6   A 1.4ps$_{rms}$-Period-Jitter TDC-Less Fractional-N Digital PLL with Digitally Controlled Ring Oscillator in 65nm CMOS

4:15 PM

W. Grollitsch, R. Nonis, N. Da Dalt

Infineon Technologies, Villach, Austria

A fractional-N digital PLL with spread-spectrum capability occupies $190 \times 200 \mu m^2$ in 65nm CMOS. It features a 190-to-4270MHz digitally controlled ring oscillator and does not use any TDC. The period jitter is 1.4ps$_{rms}$ (15ps$_{pp}$) at 3GHz and 8.4ps$_{rms}$ (75ps$_{pp}$) at 375MHz. The PLL dissipates 1.85mW (fixed) and 3.3mW/GHz from 1.3V and 1.1V dual supplies.

26.7   A 86MHz-to-12GHz Digital-Intensive Phase-Modulated Fractional-N PLL Using a 15pJ/Shot 5ps TDC in 40nm Digital CMOS

4:45 PM

J. Borremans[1], K. Vengattaramane[1,2], V. Giannini[1], J. Craninckx[1]

[1]IMEC, Leuven, Belgium

[2]K.U. Leuven, Leuven, Belgium

A 86MHz-12GHz digital-intensive reconfigurable synthesizer is presented with 100kHz to 2MHz bandwidth. It leverages a 15pJ/Shot 5.5ps 14b coarse-fine TDC and a 6-to-12GHz dual-VCO set. The $0.28mm^2$ synthesizer features simple background calibration, $\Delta\Sigma$ noise cancelation, and digital phase modulation, and consumes less than 30mW.

26.8   A 1GHz ADPLL with a 1.25ps Minimum-Resolution Sub-Exponent TDC in 0.18µm CMOS

5:15 PM

S-K. Lee, Y-H. Seo, Y. Suh, H-J. Park, J-Y. Sim

Pohang University of Science and Technology, Pohang, Korea

A sub-exponent TDC performs power-efficient linear phase detection. With a cascaded chain of self-calibrated 2× time amplifiers, TDC generates the sub-exponent-only information for the fractional time difference. The TDC, implemented in a 0.18µm CMOS, shows a minimum resolution of 1.25ps with a total conversion range of 2.5ns. When used in a DPLL, the rms jitter is 5ps at 960MHz output.

Conclusion   5:30 PM

DIRECTIONS IN HEALTH, ENERGY, & RF

Session Chair: Helene Lhermet, *CEA - LETI, Grenoble, France*
Associate Chair: Bill Bidermann, *BK Associates, San Diego, CA*

27.1   A Batteryless Thermoelectric Energy-Harvesting Interface Circuit with 35mV Startup Voltage

1:30 PM

Y. K. Ramadass, A. P. Chandrakasan

Massachusetts Institute of Technology, Cambridge, MA

A batteryless thermoelectric energy-harvesting interface circuit to extract electrical energy from human body heat is implemented in a 0.35μm CMOS process. A mechanically assisted startup circuit enables operation of the system from input voltages as low as 35mV. A control circuit that performs maximal transfer of the extracted energy to a storage capacitor and regulates the output voltage at 1.8V is presented.

27.2   Palm NMR and One-Chip NMR

2:00 PM

N. Sun[1], T-J. Yoon[2], H. Lee[2], W. Andress[1], V. Demas[3], P. Prado[3], R. Weissleder[2], D. Ham[1]

[1]Harvard University, Cambridge, MA

[2]Massachusetts General Hospital, Harvard Medical School, Cambridge, MA

[3]T2 Biosystems, Cambridge, MA

A 0.1kg palm NMR system using a fully integrated CMOS RF transceiver is reported. It is 20× lighter, 30× smaller, yet 2.5× more spin-mass sensitive than our prior system, and 1200× lighter, 1200× smaller, yet 150× more spin-mass sensitive than a commercial system. A one-chip NMR system for on-chip disease screening is also reported, which detects hCG cancer markers and bladder cancer cells.

27.3   A 3.9mW 25-Electrode Reconfigured Thoracic Impedance/ECG SoC with Body-Channel Transponder

2:30 PM

L. Yan, J. Bae, S. Lee, B. Kim, T. Roh, K. Song, H-J. Yoo

KAIST, Daejeon, Korea

An SoC monitors thoracic impedance variance (TIV) and ECG concurrently. TIV of 0.1Ω at $3.17V/\Omega$sensitivity and 8-point ECG signals can be measured with 25 reconfigurable electrodes. The chip with body-channel-transceiver consumes 3.9mW and is integrated on a 4-layer fabric circuit board with flexible battery as a poultice-like plaster.

Break   3:00 PM

27.4   A Multichannel DNA SoC for Rapid Point-of-Care Gene Detection

3:15 PM

D. M. Garner, H. Bai, P. Georgiou, T. G. Constandinou, S. Reed, L. M. Shepherd, W. Wong Jr, K. Lim, C. Toumazou

DNA Electronics, London, United Kingdom

An all-electrical approach for fast genetic testing is developed. The system employs a custom SoC fabricated in unmodified CMOS, which is embedded in a microfluidic cartridge together with proprietary biochemistry and delivers a result within 3 minutes. The system is fully scalable, allowing multiple genetic letters to be identified.

27.5   A Single-Inductor AC-DC Piezoelectric Energy-Harvester/Battery-Charger IC Converting ±(0.35 to 1.2V) to (2.7 to 4.5V)

3:30 PM

D. Kwon, G. A. Rincon-Mora

Georgia Institute of Technology, Atlanta, GA

Energy harvesting in microscale devices is important (because space constrains energy) and challenging (because rectifying small ac piezoelectric signals is lossy and difficult). The 1mm^2 2μm BiCMOS piezoelectric energy harvester-charger IC presented harnesses up to 30μW from a PZT transducer's ±0.35–to-1.2V levels to charge 1.2–to-1 . 5mAh Li Ions with 46–to-81% efficiency .

27.6 A 110µW 10Mb/s eTextiles Transceiver for Body Area Networks with Remote Battery Power

3:45 PM

P. P. Mercier, A. P. Chandrakasan

Massachusetts Institute of Technology, Cambridge, MA

A transceiver for communicating over an electronic textiles medium is implemented for body area networks. A supply-rail-coupled differential signaling scheme permits time-sharing of the eTextiles medium between communication and remote powering circuits. Fabricated in 0.18µm CMOS and operating at 0.9V, the chip consumes 110µW at a data rate of 10Mb/s over a 1m fabric link.

27.7 A 5.4dBm 42mW 2.4GHz CMOS BAW-Based Quasi-Direct Conversion Transmitter

4:15 PM

M. Contaldo, D. Ruffieux, C. Enz

CSEM, Neuchâtel, Switzerland

A 2.4GHz transmitter architecture exploits the combination of an SSB up-converter mixer and a truly co-designed PA and BAW resonators to achieve a clean output spectrum and efficient transmission. Integrated in 0.18µm CMOS, it demonstrates a maximum output power of 5.4dBm and a suppression of all the unwanted components of more than 40dB, while consuming 42mW from a 1.2V supply.

27.8 An 8.6GHz 42ps Pulse-Width Electrical Mode-Locked Oscillator

4:45 PM

M. W. Chen, D. S. Ricketts

Carnegie Mellon University, Pittsburgh, PA

A fully integrated electrical mode-locked oscillator is presented. The oscillator, which produces a periodic train of narrow pulses, is comprised of an on-chip transmission line and a lumped amplifier. The oscillator is fabricated in 0.13µm SiGe BiCMOS and produces pulses with 42ps pulse widths at a repetition rate of 8.6GHz.

27.9 Ultra-Low-Voltage Circuits for Sensor Applications Powered by Free-Space Optics

5:00 PM

T. Kleeburg[1], J. Loo[2], N. J. Guilar[3], E. Fong[1], R. Amirtharajah[1]
[1]University of California, Davis, CA   [2]Cisco Systems, Davis, CA
[3]Agilent Technology, Santa Clara, CA

Ultra-low-voltage circuits powered and clocked by free-space optical links are implemented in 90nm digital CMOS. A CDR circuit powered by 4.6klx illuminance recovers optical data at 50kb/s using interleaved subthreshold oscillators. A passive-filter ΣΔM produces a 47dB peak SNDR at 2.1klx and 256kHz sample rate. The CDR consumes 217nW at 300mV V_{DD} and 200kb/s. The ΣΔM consumes 102nW at 400mV V_{DD} and 1.6MHz for a figure-of-merit of 23fJ/conversion-step.

27.10 Nano-Watt Power Management and Vibration Sensing on a Dust-Size Batteryless Sensor Node for Ambient Intelligence Applications

5:15 PM

*T. Shimamura, M. Ugajin, K. Suzuki, K. Ono, N. Sato, K. Kuwabara, H. Morimura,
S. Mutoh*

NTT, Kanagawa, Japan

Nano-watt-power circuit techniques that accumulate energy from nanoampere-level currents and continuously sense vibration are used for dust-sized batteryless sensor nodes. A chip is fabricated using a 0.35µm CMOS process. The vibration is sensed with 0.7nW and the energy is accumulated from a 1nA current source with voltage monitoring.

Conclusion 5:30 PM

CMOS Phase-Locked Loops for Frequency Synthesis

Organizer: **Ian Galton**, *University of California, San Diego, CA*

Instructors: **Behzad Razavi**, *University of California, Los Angeles, CA*
                     John Cowles, *Analog Devices Northwest Labs, Beaverton, OR*
                     Ian Galton*, University of California, San Diego, CA*
                     Peter Kinget, *Columbia University, New York, NY*

OVERVIEW:

As wireless communication systems evolve toward higher frequencies, higher bandwidths, and multi-standard capabilities, the performance of their phase-locked loops (PLLs) becomes increasingly critical to overall system performance. Additionally, PLLs often must be integrated with large digital blocks, so there is strong and increasing economic pressure to implement them in highly-scaled CMOS technology. This short course provides a tutorial explanation of PLL design at both the system and circuit levels in the context of these issues. Topics include integer-N PLLs, fractional-N PLLs, transistor-level design of critical PLL circuit blocks, and practical application-specific PLL issues in a variety of wireless communication systems. The short course is intended for both entry-level and experienced analog, RF, and mixed-signal circuit designers.

Registration will be filled on a first-come, first-served basis. Use of the ISSCC Web-Registration Site (http://www.isscc.org) is strongly encouraged. Registrants will be provided with immediate confirmation on registration.

Sign-in is at the San Francisco Marriott Marquis Hotel, Level B-2, beginning at 7:00AM on Thursday, February 11, 2010.

DVD of the Short Course & Selected Referenced Papers: A DVD of the Short-Course may be purchased at registration time, or at the on-site registration desk. A substantial price reduction is offered to those who attend the course. The DVD will be mailed approximately four months after the end of the conference. The DVD will include: (1) The visuals of the four Short-Course presentations in PDF format; (2) Audio recordings of the presentations along with written transcriptions; (3) Bibliographies of background papers for all four presentations; and (4) PDF copies of selected relevant background material and important papers in the field (10 to 20 papers per presentation).

OUTLINE:
The Role of Synthesizers in RF Transceivers

This lecture offers a system-level perspective of frequency synthesizers, emphasizing synthesizer/transceiver co-design in modern radios. Examples of radio architectures and their inextricable relation with synthesizers are presented, and various synthesizer requirements in a radio environment are described. The origins and effects of synthesizer non-idealities such as phase noise, spurious components, and injection-pulling are studied and quantified, and examples of synthesizer/PA co-design in transmitters are offered. Finally, it is shown how the wireless standard specifications are translated to synthesizer requirements.

Instructor: Behzad Razavi is Professor of Electrical Engineering at UCLA, where he conducts research on high-speed circuits. Professor Razavi has received numerous awards for his research and teaching, including the Beatrice Winner Award for Editorial Excellence at the 1994 ISSCC, the best paper award at the 1994 European Solid-State Circuits Conference, the best panel award at the 1995 and 1997 ISSCC, the TRW Innovative Teaching Award in 1997, and the best paper award at the IEEE Custom Integrated Circuits Conference in 1998. He and his students received both the Jack Kilby Outstanding Student Paper Award and the Beatrice Winner Award for Editorial Excellence at the 2001 ISSCC. He was also recognized as one of the top 10 authors in the 50-year history of ISSCC and received the Lockheed Martin Excellence in Teaching Award in 2006 and the UCLA faculty Senate Teaching Award in 2007. Professor Razavi is an IEEE Distinguished Lecturer, a Fellow of IEEE, and the author or editor of seven books.

Introduction to Phase-Locked Loops for Frequency Synthesis

After reviewing the impact of synthesizers on communications systems, this lecture explores the high-level characteristics of the building blocks that make up the PLL with the goals of developing useful models and pointing out the effects of non-idealities. A small-signal model is then developed to study the noise and dynamic behavior of PLLs as a function of design parameters, highlighting the fundamental trade-offs in traditional integer-N architectures. The lecture concludes with a challenging design example that will motivate the move to fractional-N PLLs.

Instructor: John Cowles is a design center manager for Analog Devices Northwest Labs in Beaverton, OR. For the last 10 years, Dr. Cowles has been involved in the definition, design and release of a broad portfolio of high performance SiGe bipolar and BiCMOS RFICs for communications, medical and instrumentation applications. Prior to Analog Devices, Dr. Cowles was senior member of technical staff at TRW in Redondo Beach, CA where he helped lead the development effort of III-V technologies for defense and emerging commercial communications systems. Dr. Cowles received his PhD and MSEE from the University of Michigan in 1993 and 1989 and his BSEE from the University of Pennsylvania in 1987.

Fractional-N PLLs

This lecture provides an explanation of the fractional-N PLL as an extension of the integer-N PLL. It builds on the previous lecture by explaining the additional ideas and issues associated with fractional-N PLLs relative to integer-N PLLs. Topics include a self-contained overview of delta-sigma modulation, tradeoffs associated with quantization noise shaping order and PLL bandwidth, non-ideal effects of particular concern in fractional-N PLLs, spurious tone generation mechanisms and mitigation techniques, and recently developed techniques to enhance fractional-N PLL performance. Many of the concepts are presented in the context of fractional-N PLL CMOS IC case studies supported by measurement results.

Instructor: Ian Galton is a professor of electrical engineering at the University of California, San Diego, (UCSD) where he conducts research on mixed-signal integrated circuits. He also consults at several semiconductor companies and teaches industry-oriented short courses on mixed-signal integrated circuits. He has served on a corporate board of directors, on several corporate technical advisory boards, as the Editor-in-Chief of the IEEE Transactions on Circuits and Systems II, and as a member of several IEEE boards and committees including the ISSCC Technical Program Committee. He is an IEEE Solid-State Circuits Society "Distinguished Lecturer," he and his graduate students received the 2008 IEEE Transactions on Circuits and Systems Darlington Best Paper Award and the 2008 ISSCC Jack Kilby Award for Outstanding Student Paper, and he received the 2005-2006 UCSD Electrical and Computer Engineering Department "Best Teacher Award."

Transistor-Level Design of Critical PLL Circuits

In this lecture the system and architecture concepts presented in earlier lectures are translated into transistor-level CMOS designs. In particular, design trade-offs and challenges related to LC VCOs, ring VCOs (briefly), multi-modulus dividers, phase detectors, charge pumps and loop filters are covered in detail with example circuits. Circuit solutions addressing the new challenges related to implementing PLLs in highly scaled nanometer CMOS technologies will also be discussed.

Instructor: Peter Kinget is an Associate Professor of Electrical Engineering at Columbia University in New York City, where he conducts research on the design of analog and RF integrated circuits. He is also a consultant to industry. He has been an Associate Editor for the IEEE Journal of Solid-State Circuits and is currently an Associate Editor for the IEEE Transactions on Circuits and Systems II. He has served on many technical program committees including the ISSCC Technical Program Committee and is an IEEE Solid-State Circuits Society "Distinguished Lecturer." He is a co-recipient of the "Best Student Paper Award - 1st Place" at the 2008 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium and of the First Prize in the 2009 Vodafone Americas Foundation Wireless Innovation Challenge.

FORUMS

F3:   Transceiver Circuits for Optical Communications

Organizer: **Yuriy M. Greshishchev,** *Nortel, Ottawa, Canada*

Committee: **Franz Dielacher**, *Infineon Technologies, Villach, Austria*
Michael Flynn, *University of Michigan, Ann Arbor, MI*
Donhee Ham, *Harvard University, Cambridge, MA*
Naresh Shanbhag, *University of Illinois at Urbana-Champaign, Urbana, IL*
Takuji Yamamoto, *Fujitsu Laboratories, Kawasaki, Japan*

Optical communications have transitioned to a new era were CMOS system integration and electronic signal processing play key roles. Targeted areas have been: equalization and electronic dispersion compensation (EDC); advanced coding and detection techniques, such as FEC, MLSE; Spectral efficient optical modulation with coherent detection modulation formats, such as QPSK, DP QPSK, and so on. While 40Gb/s DP QPSK ASICs are already in most advanced optical systems, developments for 100Gb/s requirements are underway.

The objective of this Forum is to present and discuss with the leading experts from industry and academia recent R&D results in DSP-based optical-tranciever circuits towards 100GE/40GE. The topics span from 40Gb/s ASICs to support new optical- modulation formats in WAN/LAN to critical buliding blocks, (such as ADCs and CMOS integrated RX). In the follow-up pannel discussion, the pros and cons of DSP-based optical transcievers, as well as, future directions in relation to CMOS integration, will be debated. The Forum targets system architects, circuit designers, and students who want to enhance their knowledge of leading-edge transceivers and learn about future challenges in CMOS ASIC design for optical communications.

Forum Agenda:

Time	Topic
8:00	Breakfast
8:45	**Introduction** **Yuriy Greshishchev**, *Nortel, Ottawa, Canada*
9:00	**Advances in Transceiver Circuits to Suit New Optical Modulation Formats - a Historical Perspective** **Naim Ben-Hamida**, *Nortel, Ottawa, Canada*
10:00	**DSP-Based Optical Transceiver Design: Metro to Long-Haul** **Norman Swenson**, *ClariPhy Communications, Irvine, CA*
11:00	Break
11:15	**DSP for Optical WAN Receivers with Advanced Signal Equalization** **Hirotaka Tamura**, *Fujitsu, Kawasaki, Japan*
12:15	Lunch
1:15	**Optical Transceivers for 100GE** **Chris Cole**, *Finisar, Sunnyvale, CA*
2:15	**ADC Front-End for Optical Communications** **Afshin Momtaz**, *Broadcom, Irvine, CA*
3:15	Break
3:30	**CMOS High-Speed Fully Integrated Optical Receivers** **Michiel Steyaert**, *KU Leuven, Leuven, Belgium*
4:30	Panel Discussion
5:00	Conclusion

F4: High-Speed Image-Sensor Technologies

Organizer/Chair: **Johannes Solhusvik,** *Aptina Imaging, Oslo, Norway*

Committee: **Jung-Chak Ahn,** *Samsung, Gyeonggi-Do, Korea*
Jan Bosiers, *DALSA, Eindhoven, The Netherlands*
Boyd Fowler, *Fairchild Imaging, Milpitas, CA,*
Makoto Ikeda, *University of Tokyo, Tokyo, Japan*
Shoji Kawahito, *Shizuoka University, Hamamatsu, Japan*
Jerry Lin, *Ralink Technology, Jhubei City, Taiwan*
Dan McGrath, *Rochester, NY*
Katsu Nakamura, *Analog Devices, Wilmington, MA*
Jun Ohta, *Nara Institute of Science & Technology, Nara, Japan*
Ramchan Woo, *LG Electronics, Seoul, Korea*

High-speed imaging is driven by consumer and industrial applications including HDTV, slow-motion playback, machine vision, 3D, and robotics. Here, "high-speed" refers to fast and high-resolution imagers where capture, readout speed, processing and data-throughput are major challenges. In this Forum, pixels and readout circuits suitable for high-speed CMOS and CCD sensors are presented, as well as image-processing solutions. Moreover, 3D/range-capture and robotics chips including analog and digital interface solutions are discussed.

The Forum concludes with a panel discussion providing the opportunity to ask questions. Targeted participants are circuit designers and engineers working on imaging systems including ADCs, ASPs, power, memory, and interface solutions.

Forum Agenda:

Time	Topic
8:00	Breakfast

8:00   Breakfast

8:30   **Introduction**
       Johannes Solhusvik, *Aptina Imaging, Oslo, Norway*

8:35   **High-Speed CMOS Pixel Physics and Electronics**
       Boyd Fowler, *Fairchild Imaging, Milpitas, CA*

9:20   **High-Speed Imaging with CCDs**
       Jan Bosiers, *DALSA, Eindhoven, The Netherlands*

10:05   Break

10:20   **High-Speed CMOS Image Sensor Architectures**
       Guy Meynants, *CMOSIS, Antwerp, Belgium*

11:05   **Column Readout Circuit Design for High-Speed Low-Noise Imaging**
       Shoji Kawahito, *Shizuoka University, Hamamatsu, Japan*

11:50   Lunch

12:50   **3D Range Image Capture Technologies**
       Makoto Ikeda, *University of Tokyo, Tokyo, Japan*

1:35   **High-Speed Digital Image Processing**
       Levy Gerzberg, *Zoran, Sunnyvale, CA*

2:20   Break

2:35   **Vision Chip and its Applications to Human Interface, Inspection, Bio/Medical Industry, and Robotics**
       Masatoshi Ishikawa, *University of Tokyo, Tokyo, Japan*

3:20   **High-Speed Analog Interfaces for Imagers**
       Katsu Nakamura, *Analog Devices, Wilmington, MA*

4:05   **High-Speed Digital Interfaces for Imagers**
       Jean Dassonville, *Agilent Technologies, Santa Clara, CA*

4:45   Panel Discussion

5:15   Conclusion

FORUMS

F5: Circuits for Portable Medical-Electronic Systems

Co-Organizer/Chair: **Jos Huisken,** *Holst Centre / IMEC, Eindhoven, The Netherlands*
Co-Organizer: **Alice Wang,** *Texas Instruments, Dallas, TX*

Committee: **Andrea Baschirotto,** *University of Milan-Bicocca, Milano, Italy*
Alison Burdett, *Toumaz Technology, Oxford, United Kingdom*
Tim Denison, *Medtronic, Minneapolis, MN*
Maysam Ghovanloo, *Georgia Tech, Atlanta, GA*
Jun Ohta, *NAIST, Nara, Japan*
Zhihua Wang, *Tsinghua University, Beijing, China*

Portable medical electronics face the challenges of both extremely low-power requirements and packaging in a small form-factor. This Forum addresses several aspects of portable medical electronics, beginning with regulatory requirements, and followed by circuit-level challenges in the fields of RF, analog, and digital design. Finally, several real-life integrated solutions will be discussed in which the regulatory and circuit-level design challenges have been addressed.

This Forum offers circuit designers and engineering students a comprehensive overview of portable medical-electronic devices, and describes circuit-level design challenges related to low power. Also the Forum will address the regulatory requirements and opportunities for engineers who are interested in, and trying to understand, the field of medical electronics.

Forum Agenda

Time	Topic
8:00	Breakfast
8:20	**Introduction** **Jos Huisken,** *Holst Centre / IMEC, Eindhoven, Netherlands*
8:30	**Circuit Design Constraints and Methods in a Regulated Medical Environment** **Tim Denison,** *Medtronic, Minneapolis, MN*
9:15	**Bio-to-Bit: Microelectronics for Healthcare** **Bruno Murari,** *ST Microelectronics, Milano, Italy*
10:00	Break
10:15	**An Ultra-Low-Power Analog and ADC Circuit Design** **Akira Matsuzawa,** *Tokyo Institute of Technology, Tokyo, Japan*
11:00	**Digital Processing for Medical Electronics** **Manish Goel,** *Texas Instruments, Dallas, TX*
11:45	**Miniaturized Electronics for Future Wireless Sensors** **Brian Otis** *University of Washington, Seattle, WA*
12:30	Lunch
1:00	**Analog Processing for Medical Electronics** **Refet Firat Yazicioglu,** *Imec, Leuven, Belgium*
1:45	**Wearable Systems for Unobtrusive Healthcare** **Hoi-Jun Yoo,** *KAIST, Daejeon, Korea*
2:30	Break
2:45	**Cochlear Implant Stimulation IC Design for Neural Prostheses** **Soon Kwan An,** *Nurobiosys, Seoul, Korea*
3:30	**Wireless ECG Patch for Portable Health: Potential and Remaining Challenges** **Julien Penders,** *Holst Centre / IMEC, Eindhoven, Netherlands*
4:15	Panel Discussion (Tim Denison, moderator)
5:00	Conclusion

F6: Signal and Power Integrity for SoCs

Organizer/Chair: **Don Draper,** *True Circuits, Los Altos, CA*

Committee: **Fabio Campi,** *ST Microelectronics, Bologna, Italy*
Ram Krishnamurthy, *Intel, Hillsboro, OR*
Takashi Miyamori, *Toshiba, Kawasaki, Japan*
Shannon Morton, *Icera, Bristol, United Kingdom*
Willy Sansen, *K.U. Leuven-ESAT MICAS, Leuven, Belgium*
Vladimir Stojanovic, *MIT, Cambridge, MA*
John Stonick, *Synopsys, Hillsboro, OR*

This Forum is directed toward researchers and designers working in advanced technologies over the next 3-5 years. They will be required to solve emerging issues of signal and power integrity in large, System-on-Chip applications which will raise issues of increasing difficulty. While struggling for higher performance, the designer must battle escalating noise and cross-talk. Interconnect delay and coupling will require new methods of routing and signal transmission. Supply-grid design will take increasing account of limited package and chip metalization through independent power domains, active and passive supply-noise cancellation, and voltage scaling. Increasingly- sensitive analog and RF circuit blocks must counter digital chip noise. Stringent clock-jitter and skew targets, and power-dissipation limitations will be addressed by independent clock domains, resonant clocking, and frequency scaling.

Forum Agenda

Time	Topic
8:00	Breakfast
8:20	**Introduction** **Don Draper,** *True Circuits, Los Altos, CA*
8:30	**Noise and Data Fidelity in On-Chip Interconnect** **Ron Ho,** *Sun Microsystems, Menlo Park, CA*
9:30	**Supply Grid Design and Analysis** **Sam Naffziger,** *AMD, Fort Collins, CO*
10:30	Break
10:45	**On-chip Power Noise Monitoring and Diagnosis** **Makoto Nagata,** *Kobe University, Kobe, Japan*
11:45	Lunch
1:00	**Substrate Noise: A Few Observations** **Marcel Pelgrom,** *NXP Semiconductors, Eindhoven,* *The Netherlands*
2:00	**Asynchronous Network-on-Chip for SoC** **John Bainbridge,** *Silistix, Manchester, United Kingdom*
3:00	Break
3:15	**Clock Generation and Distribution for SoC** **Stefan Rusu,** *Intel, Santa Clara, CA*
4:15	Panel Discussion
5:00	Conclusion

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CONFERENCE INFORMATION

HOW TO REGISTER FOR ISSCC

Online: This is the fastest most-convenient way to register, and will give you immediate email confirmation of your selected events. To register online (which requires a credit card), go to the ISSCC website at www.isscc.org and select Attendee/Conference Registration from the pull-down menus.

By FAX or mail: Use the "2010 IEEE ISSCC Registration Form". All payments must be made in U.S. Dollars, by credit card, or check. Checks must be made payable to "ISSCC 2010". It will take several days before you receive email confirmation when you register using this method. **Registration forms received without full payment will not be processed until payment is received at YesEvents.** The Registration Form can be downloaded from the ISSCC website. Please read the explanations and instructions on the second page of the form, carefully.

Onsite: The Onsite Registration and Advance Registration Pickup Desks at ISSCC 2010 will be located in the Yerba Buena Ballroom Foyer at the San Francisco Marriott Marquis. All participants, except as noted below, should register or pick up their registration materials at these desks as soon as possible. **Pre-registered Presenting Authors and all pre-registered members of the ISSCC Program and Executive Committees must go to the Nob Hill Room, Ballroom level, to collect their conference materials.**

REGISTRATION DESK HOURS:

Saturday,	February 6	4:00 PM to 7:00 PM
Sunday,	February 7	6:30 AM to 8:00 PM
Monday,	February 8	6:30 AM to 3:00 PM
Tuesday,	February 9	8:00 AM to 3:00 PM
Wednesday,	February 10	8:00 AM to 3:00 PM
Thursday,	February 11	7:00 AM to 1:00 PM

Students must present their Student ID at the Registration Desk to receive the student rate. Those registering at the IEEE Member rate must provide their IEEE Membership number.

Deadlines: The deadline for registering at the Early Registration rate is 11:59 PM Pacific Time, **Friday, January 8, 2010.** After January 8th, and on or before 6:00 AM Pacific Time, Tuesday, January 19, 2010, registrations will be processed **at the Late-Registration rate. After January 19th, you must register onsite at the Onsite rate.** You are urged to register early to obtain the lowest rate, and ensure your participation in all aspects of ISSCC 2010.

Cancellations/Adjustments/Substitutions: Prior to 6:00 AM Pacific Time, **Tuesday, January 19th, 2010,** Conference Registration can be cancelled, and fees paid will be refunded (less a processing fee of $75). Registration category or credit card used can also be changed (for a processing fee of $35). Send an email to ISSCCinfo@yesevents.com to cancel or make other adjustments. **No refunds will be made after 6:00 AM Pacific Time, January 19th, 2010.** Paid registrants who do not attend the Conference will be sent all relevant Conference materials. Transfer of registration to someone else is allowed with **WRITTEN** permission from the original registrant.

MEMBERSHIP CAN SAVE YOU MONEY!

Take advantage of reduced ISSCC registration rates by using your IEEE membership number.

If you are an IEEE member and have forgotten your member number, simply phone IEEE at 1(800) 678-4333 and ask. IEEE membership staff will take about 2 minutes to look up your number for you. If you come to register onsite without your membership card, you can phone IEEE then, too. Or you can request a membership number look-up by email. Use the online form at: www.ieee.org/web/aboutus/help/member_technical.html

If you are not an IEEE member, consider joining before you register to reduce your fees! Join online at www.ieee.org/join at any time and you'll receive your member number by email.

Solid-State Circuits Society membership costs $26 with your IEEE membership. Use the onsite IEEE membership registration desk at the hotel to renew or join. This desk is staffed during the same hours as ISSCC registration from Saturday through Wednesday, but closes at 10 AM on Thursday.

CONFERENCE INFORMATION

ITEMS INCLUDED IN REGISTRATION

Technical Sessions: Registration includes admission to all technical and evening sessions starting Sunday evening and continuing throughout Monday, Tuesday, and Wednesday.

Technical Book Displays: A number of technical publishers will have collections of professional books and textbooks on display during the Conference. These books are available for sale or to order onsite. The Book Display will be open on Monday from 12:00 Noon to 6:30 PM; on Tuesday from 10:00 AM to 6:30 PM; and on Wednesday from 10:00 AM to 2:00 PM.

Poster Sessions: The recent ISSCC/DAC student contest winners will display their work in poster form. These students will be available to discuss their posters during the Social Hours on Monday and Tuesday evenings.

Author Interviews: Author Interviews will be held in the Atrium of the hotel, located one level above the lobby, on Monday and Tuesday. On Wednesday, they will be located in the Foyer outside the Yerba Buena Ballroom. All interviews take place after the last afternoon Sessions.

Social Hours: Social Hour refreshments will be available starting at 5:15 PM on Monday and Tuesday in both the Book Display and Author Interview areas.

University Events: Several universities are planning social events during the Conference. Check the University Events display at the Conference for the list of universities, locations and times of these events.

Publications:

Full Conference Registration includes:

-The **Digest of Technical Papers** in both hard copy and on CD (available onsite beginning on Sunday at 4:00 PM, and during registration hours on Monday through Wednesday).

-The **ISSCC 2010 Conference DVD** that includes the Digest and Visuals Supplement (to be mailed in April). **Student Registration does not include the ISSCC 2010 Conference DVD, however it is available for purchase at a reduced fee.**

OPTIONAL EVENTS

Educational Events: Many educational events are available at ISSCC 2010 for an additional fee. There are nine 90-minute Tutorials and two all-day Forums on Sunday. There are four additional all-day Forums on Thursday as well as an all-day Short Course. See the schedule for details of the topics and times.

Women's Networking Reception: ISSCC will be sponsoring a networking event for women in solid-state circuits on **Tuesday evening**. It is an opportunity to get to know other women in the profession and discuss a range of topics including leadership, work-life balance, and professional development. By registering and paying a nominal fee for this event, you will receive a ticket to the reception, a chance to build new friendships, and an opportunity to expand your professional network. Please indicate on your ISSCC registration form if you plan to attend this special event, open to women only.

OPTIONAL PUBLICATIONS

ISSCC 2010 Publications: The following ISSCC 2010 publications can be purchased in advance or onsite:

<u>Additional</u> copies of the **Digest of Technical Papers** in book or CD format.

<u>Additional</u> copies of the **ISSCC 2010 Conference DVD (mailed in April).**

ISSCC 2010 Conference DVD at the special student price **(mailed in April).**

2010 Tutorials DVD: All of the 90 minute Tutorials **(mailed in June).**

2010 Short Course DVD: "CMOS Phase-locked Loops for Frequency Synthesis" **(mailed in June)**.

Short Course and Tutorial DVDs contain audio recordings and written English transcripts synchronized with the presentation visuals; as well as a pdf file of the entire transcription suitable for printing, and a pdf file of key reference material.

Earlier ISSCC Publications: Selected publications from earlier Conferences can be purchased. There are several ways to purchase this material:

-Items listed on the Registration Form can be purchased with registration and picked up onsite at the Conference or mailed to you when available.

-At the ISSCC Publications Desk, located in the registration area, and open during registration hours. With payment by cash, check, or credit card, you can pick up (or order for future delivery) materials at this desk. Tutorial and Short Course DVDs from prior Conferences are available. See the order form for titles and prices.

-Visit the ISSCC website at www.isscc.org and click on the link "Purchase ISSCC Conference Materials", where you can order online or download an order form to mail or fax. For a small shipping fee, this material will be sent to you immediately (or when available), and you will not have to wait until you attend the Conference to get it.

CONFERENCE INFORMATION

HOW TO MAKE HOTEL RESERVATIONS

ALL ATTENDEES WHO NEED A HOTEL ROOM: We are offering this year a $100 Marriott Rebate! If you register for ISSCC 2010 and spend at least three nights at the San Francisco Marriott Marquis, a credit of $100 will be applied to your hotel bill. Enjoy the convenience of staying at the Conference hotel AND save money too!

Online: ISSCC participants are urged to make their hotel reservations at the San Francisco Marriott Marquis online. To do this, go to the conference website at www.isscc.org and click on the "Hotel Reservation" link to make a reservation at the San Francisco Marriott Marquis at the Conference group rate The special ISSCC group rates are $209/single or double; $229/triple; and $249/quad (per night plus tax). In addition, we have negotiated that ISSCC attendees staying at the Marriott receive **in-room Internet access for free**. All online reservations require the use of a credit card. Online reservations are confirmed immediately. You should print the page containing your confirmation number and reservation details and bring it with you when you travel to ISSCC.

Telephone: Call US toll free 800-266-9432 or 506-474-2009.

Changes: Once confirmed, your reservation can be changed online or by telephone. Have your hotel confirmation number ready.

Hotel Deadline: Reservations must be received at the San Francisco Marriott Marquis no later than January 19, 2010 to obtain the special ISSCC rates. A limited number of rooms are available at these rates. **Once this limit is reached or after January 19th, the group rate may no longer be available and reservation requests will be filled at the best available rate.**

REFERENCE INFORMATION
TAKING PICTURES, VIDEOS OR AUDIO RECORDINGS DURING ANY OF THE SESSIONS IS NOT PERMITTED

Conference Website:	www.isscc.org	
ISSCC Email:	ISSCC@ieee.org	
Hotel Information:	San Francisco Marriott Marquis 55 Fourth Street San Francisco, CA 94103	Phone: 415-896-1600
Press Information:	Kenneth C. Smith University of Toronto Email: lcfujino@cs.com	Phone: 416-418-3034 Fax: 416-971-2286
Registration:	YesEvents P.O. Box 32862 Baltimore, MD 21282 Email: issccinfo@yesevents.com	Phone: 410-559-2200 or 800-937-8728 Fax: 410-559-2217

Hotel Transportation: Visit the ISSCC website and select "Attendee/Transportation from Airport" to download a Word document with directions and pictures of how to get from the San Francisco Airport (SFO) to the Marriott. You can get a map and driving directions from the Marriott website at www.marriott.com/hotels/maps/travel/sfodt-san-francisco-marriott/

Next ISSCC Dates and Location: ISSCC 2011 will be held on February 20-24, 2011 at the San Francisco Marriott Marquis Hotel.

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