ISSCC 2009
Conference Overview

- Events
- Paper Statistics
- Plenary Session
- Technical Highlights
- Discussion Sessions
- Short Course
- Tutorials
- Advanced-Circuit-Design Forums

EVENTS

TUTORIALS (SUNDAY, FEBRUARY 8, 2009)

- **10** 90-minute Tutorials, each taught twice, by circuit experts from the Program Committee, serve to meet attendees' needs for introductory material in circuit specialties.

ADVANCED-CIRCUIT-DESIGN FORUMS (SUNDAY, FEBRUARY 8, 2009)

- Circuit experts exchange information on their current research in an all-day informal environment

STUDENT FORUM (SUNDAY, FEBRUARY 8, 2009)

- An opportunity for student networking, in which students present brief overviews or their current research.

TECHNICAL SESSIONS (MON. TO WED., FEBRUARY 9 TO 11, 2009)

- **4 invited talks** presented in the Plenary Session and **203 technical papers** presented in **28** Regular Sessions, highlight the latest circuit developments.

EVENING SESSIONS (SUNDAY, MONDAY & TUESDAY, FEBRUARY8 TO 10, 2009)

- **7** Special-Topic presentations, in which experts provide insight and background on a subject of current importance.

- **2** Panels in which experts debate a selected topic and field audience questions in a semi-formal atmosphere.

SOCIAL HOUR (MONDAY, FEBRUARY 9, 2009)

- Network with experts in a wide range of circuit specialties; meet colleagues in an informal exchange; browse the technical-book exhibits!

SHORT COURSE (THURSDAY, FEBRUARY 12, 2009)

- Intensive All-Day Course on a single topic, taught by world-class instructors, can serve to "jump start" a change in an engineer's circuit specialty.

ADVANCED-CIRCUIT-DESIGN FORUM (THURSDAY, FEBRUARY 12, 2009)

- Circuit experts exchange information on their current research in an all-day informal environment.

PAPER STATISTICS

OVERALL:

- **4** papers invited
- **582** papers submitted to ISSCC 2009
- **203** papers accepted, including:
    - **78** papers from North America, including
        - **31** Industry papers
        - **47** University papers
    - **73** papers from the Far East, including
        - **42** Industry papers
        - **31** University papers
    - **52** papers from Europe, including
        - **23** Industry papers
        - **29** University papers
- **29** Sessions, over 3 days

INTERNATIONAL SCOPE:

	2009	2008	2007
Americas:	**38 %**	**43 %**	**39 %**
Far East:	**36 %**	**28 %**	**31 %**
Europe:	**26 %**	**29 %**	**30 %**

WIDE COVERAGE:

	2009	2008	2007
Analog	**11 %**	**9 %**	**7%**
Data Converters	**7 %**	**10 %**	**7 %**
High-Performance Digital	**4 %**	**7 %**	**13 %**
Imagers, Displays, and MEMs	**12 %**	**11 %**	**12 %**
Low-Power Digital	**6 %**	**5 %**	**4 %**
Memory	**9 %**	**12 %**	**8 %**
RF	**11 %**	**11 %**	**10 %**
Technology Directions	**13 %**	**12 %**	**12 %**
Wireless Communications	**13 %**	**11 %**	**12 %**
Wireline Communications	**14 %**	**11 %**	**13 %**

PLENARY SESSION

Paper 1.1:
Leaner and Greener: Adapting to a Changing Climate Innovation
René Penning de Vries, *CTO, NXP Semiconductors, Eindoven, The Netherlands*

- The semiconductor industry has been a major driver for change in everyday life.
- Energy efficiency and power management are now a major concern necessitating a new vision to meet the challenges of climate change and limited supplies.
- Solutions will depend on characteristics of particular energy sectors - consumer goods, workplace electronics, and transportation.
- For every 1% saved in the world's electricity consumption, roughly 40 fewer power stations are required!
- A new vision for semiconductor technology change is required.
- This presentation will explore how the semiconductor industry can go beyond the traditional to reduce energy demand in the modern world.

Paper 1.2:
Adaptive Circuits for the 0.5V Nanoscale CMOS Era
Kiyoo Itoh, *Fellow, Hitachi Tokyo, Japan*

- Nanoscale supply reduction leads to serious problems in circuit design.
- Problems originate through two unscalable parameters - the limit of V_t below which leakage begins to dominate, and the increase in variability of V_t with reduced nanoscale dimensions.
- Correspondingly, the minimum supply voltage begins to increase as feature size is reduced!
- This implies a 1V barrier at 45nm features sizes.
- For reducing nanoscale features interconnect resistance increases to provide more problems, which also motivate a higher supply voltage!
- A variety of techniques for the reduction of minimum supply voltage toward 0.5V will be presented.

PLENARY SESSION

Paper 1.3:
The New Era of Scaling in an SoC World
Mark Bohr, *Senior Fellow, Intel, Hillsboro, OR*

- Simple scaling began to be troublesome earlier this decade.
- An new era of scaling began with innovations in device materials and transistor structure - copper, strained silicon, high-κ dielectrics and metal-gate transistors. .
- Scaling beyond the natural limits of lithography has led to major innovations - optical-proximity correction, phase-shift masks, and gridded layout.
- Analog circuits have particularly suffered in the nanometer era - degraded transistor gain, reduced dynamic range, and transistor mismatch.
- An adaptive-circuit approach must be employed for circuit improvement.
- These and other techniques for use down to 22nm will be discussed.

Paper 1.4:
Kids Today! Engineers Tomorrow!
John Cohn PhD, *Fellow, IBM Systems and Technology Group, Essex Junction, VT*

- A possible crisis exists in engineering education enrolment.
- World engineering-enrolment trends will be examined.
- What are we doing wrong? What do we need to do?
- How can we motivate kids?
- Grand global challenges to motivate young people.
- Your role as engineers in educating society about engineering.

TECHNICAL HIGHLIGHTS

Analog

- A chopper-stabilized current-feedback instrumentation amplifier with a 1mHz 1/f-noise corner and an AC-coupled ripple-reduction loop **[19.1]**
- A sub-1V bandgap voltage reference in 32nm FinFET technology **[19.6]**
- A 1MHz-bandwidth type-I $\Delta\Sigma$ fractional-N synthesizer for WiMAX applications. **[23.1]**
- A 2.2GHz 7.6mW sub-sampling PLL with -126dBc/Hz in-band phase noise and $0.15ps_{rms}$ jitter in 0.18μm CMOS **[23.2]**
- Single-inductor dual-input dual-output buck-boost fuel-cell-Lithium-ion charging DC-DC converter supply **[26.2]**
- A 20W/channel Class-D amplifiers with zero common-mode radiated emissions **[26.4]**
- A 460W Class-D output stage with adaptive gate drive **[26.6]**

Data Converters

- Pushing the performance envelope with high-speed DACs: 2.9GS/s with high linearity (<-60dBc IM3) and wide bandwidth (1GHz). **[4.1]**
- Virtually all new data converters are digitally enhanced for performance improvement. **[4.2 to 4.7; 9.1; 9.2; 9.5 to 9.8]**
- The trend towards digital enhancement does not favor any one particular converter architecture. **[4.2 to 4.7, 9.1; 9.2; 9.5 to 9.8]**
- Medium-resolution converters, (8 to 10 bits), which are widely used, have migrated upward in speed of conversion. **[4.3; 4.5; 4.6]**
- Migration down to deep-submicron technologies continues, allowing a more economical implementation of digital enhancement techniques. **[4.2 to 4.7; 9.1; 9.2; 9.5 to 9.8]**
- Oversampled converters show a distinct trend toward using continuous-time architectures. **[9.5 to 9.7]**

High-Performance Digital

- High-performance processors continue to push performance and the limits of transistor integration **[3.1]**
- Highest ever transistor count (2.3B) for a microprocessor **[3.1]**
- Highest core count (8) and thread count (16) for an x86 processor **[3.1]**
- Novel technologies for power delivery and dissipation include optimized metal layers and microcontroller-based power management **[3.1; 3.2]**
- Reconfigurable memories offer architectural flexibility using a 3D-stacked system with fine-pitch micro-solder **[3.3]**
- Dynamic frequency switching enables power-frequency optimization within the allowed power envelope. **[3.4]**
- Switched-capacitor methods can secure cryptographic engines from power-analysis attacks **[3.5]**
- Off-chip signaling techniques are integrated into on-chip wire drivers to improve bandwidth at low power **[3.6]**

IMMD

- The first backside-illuminated multi-layer 3D-integrated 1Mpixel CMOS image sensor that is four-side abuttable with only 3-pixel-equivalent seam loss and supports a burst digital data output rate of 1Mpixel in 1ms. **[2.1]**
- An image sensor whose random noise is 30% lower than previous CMOS image sensors with sensitivity doubled by a new column-level charge-addition mode. **[2.6]**
- A piecewise-linear 10b DAC architecture for AMLCD data drivers with drain-current modulation achieves good DNL and excellent channel-to-channel uniformity. **[15.1]**
- A novel digital driving technique for mobile AMOLED displays using $\Delta\Sigma$ modulation mitigates TFT V_t-shifts and solves the false-contour problem. **[15.4]**
- The first bandgap-based temperature sensor at the 32nm node. **[20.1]**
- An interface to a micro-gyroscope that minimizes area and reduces start-up time without compromising performance. **[20.3]**
- The first integrated electrode interface that combines electrical and chemical sensing, allowing researchers to explore the role of both modes of computation in the brain. **[25.2]**
- An integrated multiprocessor IC that extracts information from an array of neural signals for the identification of brain conditions such as epilepsy. **[25.4]**

Low-Power Digital

- The first fully-integrated backend SoC for Blu-ray players includes content decryption, video decode, and display output with Picture-in-Picture (PiP) and HDMI 1.3. **[8.4]**
- A video-encoding chip supporting encoding of multiple views at HD solutions: 1-view (4096 x 2160p), 3-view full-HD (1080p), and 7-view HD (720p) for 3D display applications. **[8.5]**
- The first Full-HD SoC available for handsets: 166MHz Mobile Application Processor is implemented in 65nm to support multistandard video codec at Full-HD resolution. **[8.7]**
- A fully-integrated IR-UWB receiver for communication and sub-cm ranging **[14.1]**
- First non-coherent receiver allowing faster and lower-energy synchronization **[14.2]**
- First IC to achieve 4x4 64-QAM MIMO detection that is easily scalable to 256-QAM **[14.4]**

Memory

- First 4Gb DDR3 highest-density DRAM at 1.2V power supply **[7.1]**
- First 8Gb through-silicon-via 4-stacked DDR3 with master/slave separate chips **[7.2]**
- Fastest-data-rate mobile DDR2 DRAM (4.3GB/s) **[7.3]**
- Fastest GDDR5 DRAM with a data rate of 7Gb/s/pin **[7.4]**
- First-reported 32Gb 34nm MLC NAND Flash Memory with 9MB/s write throughput **[13.1]**
- A 113mm^2 32Gb 3b/cell NAND memory that fits into a microSD memory card **[13.4]**
- Use of inductive coupling for NAND Flash stacking in SSD with 2Gb/s and 15pJ/bit/chip capability **[13.5]**
- First-reported 64Gb 4bit/cell Flash NAND memory with 5.6MB/s write throughput **[13.6]**
- The first 32nm high-density and high-performance SRAM in a Hi-k metal-gate technology **[27.1]**
- The 128Mb FeRAM is the largest-capacity in emerging nonvolatile RAM reported and 1.6GB/s bandwidth is 4 to 8× higher than previously reported **[27.5]**

RF

- A single-gate mixer topology with current reuse consumes just 380μW at 0.6V. **[12.5]**
- A novel technique to vastly reduce harmonic interference in direct-conversion receivers using an analog Walsh shaper **[12.7]** in the RF front-end with further interference cancelation in the digital domain. **[12.9]**
- An all-CMOS integrated transmitter realized with a power-mixer array in 0.13μm CMOS achieving 26dBm output power with 19% power-added efficiency for 16-QAM **[22.2]**
- A 90nm CMOS power amplifier providing 23dBm with 12% power-added efficiency for a 16QAM WiMAX signal, enables long-range high-data low-cost single-chip communications **[22.3]**
- A demonstration of mm-wave power amplifiers at 60GHz to enable Gbit/s communications using low-cost state-of-the-art 65nm and 45nm CMOS at 1V. **[22.4; 22.5]**
- The highest-reported operating frequency (150GHz) for an amplifier in CMOS, enabling new applications from im aging to high-data-rate short-range communications **[29.1]**
- Record gain (26dB) reported for a 100GHz SiGe amplifier using a novel traveling-wave broadband topology **[29.3]**

Technology Directions

- A Spintronic-based oscillator with an operating range of 4GHz to 10GHz co-integrated with a broadband amplifier in 65nm for RF applications **[11.1]**
- 10Mb/s 14μW RFID with 14m operating range based on UWB uplink and UHF downlink in 0.18μm CMOS **[11.2]**
- A 2.5mW pulsed UWB wireless motion control system for a moth. **[11.3]**
- A self-sufficient tire-mounted wireless sensor integrates a Bulk Acoustic Wave-based low-power FSK 2.11GHz transceiver, an energy scavenger and a 3D vertical chip stack. **[17.1]**
- An implantable release-on-demand drug-delivery SoC in CMOS technology monolithically integrates wireless circuitry and 8 addressable 100nl reservoirs fabricated by CMOS-compatible post-IC processing. **[17.2]**
- A stabilized power supply system for low-power 3.3V electronics is realized by monolithically integrated micro fuel cell within an extended CMOS process. **[17.4]**
- A wireless power-transfer system for implanted medical devices uses an antenna area 100 times smaller than previous designs **[17.5]**
- An optically-programmable SoC integrated on a 2.6x2.6mm^2 chip provides the electronics for an autonomous microrobot. **[17.9]**
- Optical I/O architecture achieves data rate of 10Gb/s/channel at 11pJ/b energy efficiency. This technology projects increased optical integration that will reach 20Gb/s at 1pJ/bit**. [28.1]**
- Stretchable circuit sheet using low-voltage CMOS organic technology that enables EMI-distribution measurement by wrapping the flexible surface around electronic equipment with a sensitivity of -70dBm**. [28.3]**
- A proof-of-concept application and methodology based on a cellular-neural-network- contour-generation vision system emulating the processing of part of the brain. **[28.6]**
- Close-proximity inductive coupling data link between 3D-stacked 8-core processor and 1MB SRAM that achieves 19.2Gb/s and 1pJ/b. **[28.7]**

Wireless

- The first multimode single-chip cellular transceivers for 2/2.5G and 3G **[6.2; 6.3; 6.4]**
- First published DOCSIS-3.0 SoC **[6.6]**
- First completely-integrated radio and baseband at 60GHz in CMOS **[18.5]**
- Advances in 45nm CMOS for wireless connectivity **[24.1; 24.6]**
- Highest integration UWB WiMedia PHY in 65nm CMOS **[24.2]**

Wireline

- Subharmonically injection-locked PLLs for ultra-low-noise clock generation **[5.2]**
- A VDSL2 CPE AFE in 0.15μm CMOS with integrated line driver **[5.10]**
- A scalable 3.6-to-5.2mW 5-to-10Gb/s 4-tap DFE in 32nm CMOS **[10.1]**
- A 4-channel 10.3Gb/s backplane transceiver macro with 35dB equalizer and sign-based zero-forcing adaptive control **[10.5]**
- A 40Gb/s multi-data-rate CMOS transceiver with SFI-5 interface for optical transmission systems **[21.1]**
- An 80mW 40Gb/s 7-tap T/2-spaced FFE in 65nm CMOS **[21.4]**

EVENING SESSIONS

SUNDAY

SE1: ***Healthy Radios: Radio & Microwave Devices for the Health Sciences***

SE2: ***Is Fabless MEMS Fabulous?***

MONDAY

SE3: ***Will ADCs Overtake Binary Frontends in Backplane Signaling?***

SE4: ***Highlights of IEDM 2008***

E1: ***Forewarned is Four Armed: Classic Analog Misteakes to Avoid***

SE5: ***Things all RFIC Designers Should Know (But are afraid to ask)***

TUESDAY

SE6: ***Interleaving ADC's – Exploiting the Parallelism***

SE7: ***Next-Generation Energy-Scavenging Systems***

E2: ***MID – 'Scaled Down' PC or 'Souped Up' Handheld?***

SHORT COURSE:

[Thursday, February 12, 2009]

Low-Voltage Analog and Mixed-Signal CMOS Circuit Design

COURSE OBJECTIVE:

The relentless scaling of supply voltage that has accompanied advances in CMOS technology has been great for digital circuits but has made high-performance analog and mixed-signal circuits increasingly challenging to design. Nevertheless, market pressures continue to dictate high levels of integration in mass-market communication and entertainment devices to minimize product cost and size. Increasingly, this necessitates the inclusion of low-noise amplifiers, mixers, filters, and data converters, along with large amounts of digital circuitry in highly-scaled CMOS technology at analog supply voltages of 1.2V or less. Unfortunately, traditional topologies for these analog blocks are not compatible with such low supply voltages, so innovative new techniques for low-voltage analog and mixed-signal CMOS design are required. This short course provides a detailed view of the problems associated with low-voltage analog and mixed-signal design and describes techniques for overcoming these problems. It is intended for both entry-level and experienced analog and mixed-signal circuit designers.

OVERVIEW:

- The Short Course will be offered twice on Thursday, February 12:
  The first offering is scheduled for 8:00AM to 4:30PM.
  The second offering is scheduled for 10:00AM to 6:30PM.

- ***Low-Power Low-Voltage Opamp Design***
  Instructor: Willy Sansen
- ***Low-Voltage Sigma-Delta A/D Converters***
  Instructor: Lucien Breems
- ***The Effect of Technology Scaling on Power Dissipation in Analog CMOS Circuits***
  Instructor: Klaas Bult
- ***Sub-1V RF Design: Challenges and Techniques***
  Instructor: Behzad Razavi

TUTORIALS:

[Sunday, February 8, 2009]

T1: Continuous-Time Filters

T2: Adaptive Power Management Techniques

T3: Turning Bits into Pictures

T4: Fundamentals of Digitally-Assisted RF

T5: Display and RFID-Tag Design Using Organic Transistors

T6: SAR ADCs

T7: Managing Variations Through Adaptive Design Techniques

T8: Variation-Tolerant SRAM Circuit Designs

T9: Managing Linearity in Radio Front-ends

T10: CMOS Circuit Techniques for High-Speed Wireline Transceivers

FORUMS:

[Sunday, February 8, 2009]

F1: SSD, Memory Subsystem Innovation

F2: Medical Image Sensors

F3: GIRAFE: Towards 4G RF Transceivers

F4: Ultra-Low-Voltage Circuit Design

[Thursday, February 12, 2009]

F5: ATAC: High-Speed Interfaces

F6: Multi-Domain Processors

F7: Clock Synthesis Design

F8: Integrated Neural Interfaces

STUDENT FORUM

[Sunday , February 8, 2009]

After the successful launching of the ISSCC Student Forum last year, the International Solid-State Circuits Conference (ISSCC) will continue and expand this student activity at ISSCC 2009. One of the goals of the ISSCC Student Forum is to encourage student participation and networking at ISSCC. In particular, it will provide graduate students (Masters and PhD candidates) with:

- A great opportunity to showcase the directions of their work
- An opportunity to experience ISSCC quality
- An opportunity to interact with others in the ISSCC community
- Encouragement for future regular-paper submissions

More particularly, it will provide graduate students with:

- An opportunity for mutual understanding of academic research styles and cultures
- An opportunity to exchange experiences
- An opportunity to improve communication skills

The ISSCC Student Forum is organized as short presentations of work-in-progress. The presentations will NOT be considered as pre-publication in future ISSCC regular-paper submissions. Results with actual silicon implementation are highly encouraged. Papers that have been accepted at ISSCC will not be considered for the student forum presentation. However, papers that significantly extend a prior ISSCC publication will be considered.

STUDENT FORUM COMMITTEE

CHAIR:	**Anantha Chandrakasan,** *Massachusetts Institute of Technology, Cambridge, MA*
VICE-CHAIR:	**Jan van der Spiegel,** *University of Pennsylvania,Philadelphia, PA*
VICE-CHAIR:	**Chorng-Kuang (C-K) Wang,** *National Taiwan University,Taipei, Taiwan*
SECRETARY:	**Makoto Ikeda,** *University of Tokyo, Tokyo, Japan*
ADVISOR:	**Kenneth C. Smith,** *University of Toronto, Toronto, Canada*
MEDIA/PUBLICATIONS:	**Laura Fujino,** *University of Toronto, Toronto, Canada*
WORKSHOP LOGISTICS:	**Diane Melton,** *Courtesy Associates, Washington, DC*
A/V:	**John Trnka,** *Rochester, MN*

COMMITTEE MEMBERS:
Andrea Baschirotto, *University of Milan-Bicocca, Milano, Italy*
William Bowhill, *Intel, Hudson, MA*
Eugenio Cantatore, *Eindhoven University of Technology, Eindhoven, Netherlands*
Anantha Chandrakasan, *Massachusetts Institute of Technology, Cambridge, MA*
Tzi-Dar Chiueh, *National Taiwan University, Taipei, Taiwan*
Glenn Gulak, *University of Toronto, Toronto, Canada*
Qiuting Huang, *ETH-Zürich, Zürich, Switzerland*
Makoto Ikeda, *University of Tokyo, Tokyo, Japan*
Takayuki Kawahara, *Hitachi, Tokyo, Japan*
Andreas Kaiser, *IEMN-ISEN, Lille, France*
Akira Matsuzawa, *Tokyo Institute of Technology, Toyko, Japan*
Shahriar Mirabbasi, *University of British Columbia,Vancouver, Canada*
Masayuki Mizuno, *NEC, Kanagawa, Japan*
Boris Murmann, *Stanford University, Stanford, CA*
Bram Nauta, *University of Twente, Enschede, Netherlands*
Willy Sansen, *K.U. Leuven-ESAT-MICAS, Leuven, Belgium*
Jan van der Spiegel, *University of Pennsylvania, Philadelphia, PA*
Chorng-Kuang (C-K) Wang, *National Taiwan University, Taipei, Taiwan*
Hoi-Jun Yoo, *KAIST, Daejeon, Korea*