ISSCC 2011 TRENDS REPORT

ISSCC remains the pre-eminent forum for the discussion of the latest state-of-the-art integrated circuit solutions across a variety of application areas including:

- Analog
- Microprocessors
- Imagers, MEMS, Medical, and Display Devices
- Memory
- Radio Frequency
- Technology Directions
- Wireline Communications

Over time, ISSCC has observed a number of trends in these application areas in terms of how technology has developed over time, and where it is headed in the both the near and long terms. This report serves as a summary of these trends, as seen by the industrial and academic experts that make up the International Technical Program Committee of the ISSCC.

ANALOG

With the increasing excitement over the digital world, people often forget that the real world is actually analog. Even though most of our technologies process information via computers and digital circuitry, the signals themselves originate and end up in analog form, such as sound and radio waves. Furthermore, all electronic circuits, whether analog or digital, must be supplied with power, and the power supply circuits are inherently analog. Nevertheless, digital circuits such as microprocessors, drive the market; so, integrated circuit (IC) technology (used in the factories that make integrated circuits) have been optimized relentlessly over the last 40 years to reduce the size, cost, and power consumption of digital circuits. This trend has made analog circuitry increasingly difficult to implement, yet the number of essential analog interface circuits and their performance requirements have increased.

Interestingly, analog designers have turned the curse of this trend away from “analog-friendly” IC technology into a cure. Rather than struggle to overcome the problem with traditional, time-tested analog circuit tricks, they have turned toward the utilization of digital signal-processing circuits, embedded within the analog-circuit blocks, to overcome analog-circuit limitations. This new approach blurs the distinction between analog and digital circuit design, but yields continued advances in the analog state-of-the-art. Increasingly, these techniques have enabled

performance that matches, and now even exceeds, what was possible in traditional high-performance analog IC technology.

MICROPROCESSORS

While process technology continues its onward advancement, enabling integration on massive scales, this year's processors come from wide technological backgrounds. New ground is broken in key areas of transistor integration, performance per unit power, and functional integration. This is accomplished across a wide range of process technologies – 65nm, 45nm, 40nm, and 32nm bulk and SOI CMOS technologies.

The chip-complexity chart (Figure 1) shows the trend in integrating transistors on a single chip over the past two decades. While the 1 billion limit was passed some 5 years ago, this year marks the first commercial product exceeding 3 billion transistors on a single die with the 32nm Intel Itanium Processor. The massive integration continues to drive the inclusion of large caches on-die as we see with 30MB on IBM's zEnterprise, and 54MB on the 32nm Intel Itanium.

Aggressive processor power management and system-wide power optimization has become a requirement as technology has enabled the increasing trend of system integration onto the processor die (Figure 2). The trend of flat-to-down power in these systems continues as engineers leverage low-power design features to squeeze performance within existing power budgets. For example, the IBM zEnterprise system achieves a 20% frequency boost to a mind-numbing 5.2GHz with no power envelope increase over prior generation devices (Figure 3). The Godson-3B processor's focus on power enables that device to consume only 40W. The increased focus on power is helping rein in the immense demands, which PCs, servers, data centers, and similar systems put on power grids. The result will be lower cost, less cooling demands, and a greener product.

As a consequence of lower-power design requirements, system architects have been forced to innovate using multiple processor cores typically running parallel threads at lower frequencies (Figure 4). This enables processors to turn off when not actively doing computations. While ISSCC 2011 does not break ground in maximum core count, the body of work continues to emphasize this growing trend – IBM's zEnterprise is a 4-core machine, the Intel Westmere-EX delivers a 10-core solution, China's Godson-3B features 8 cores, and AMD's Bulldozer also delivers an 8-core CPU. This flexibility and scalability will enable adaptable system power profiles, further reducing power consumption and improving the end-user experience, as our multi-tasking lifestyle evolves.

These trends in integration, power consumption, and parallel computation, bring new challenges to processor development: New techniques are required to ensure robustness to power supply fluctuations; and improvements in power/clock delivery networks are required as multiple voltage domains become de facto on these chips. ISSCC 2011 will highlight many of these new building-block technologies.

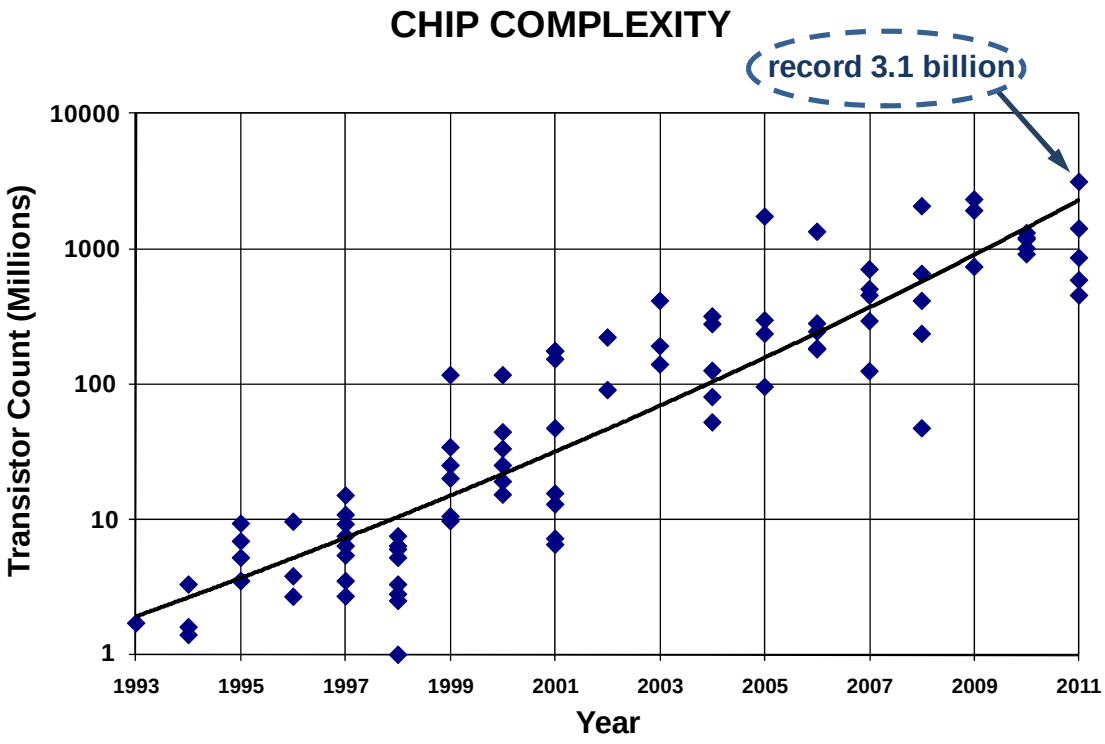

Figure 1: Microprocessor chip complexity vs Year

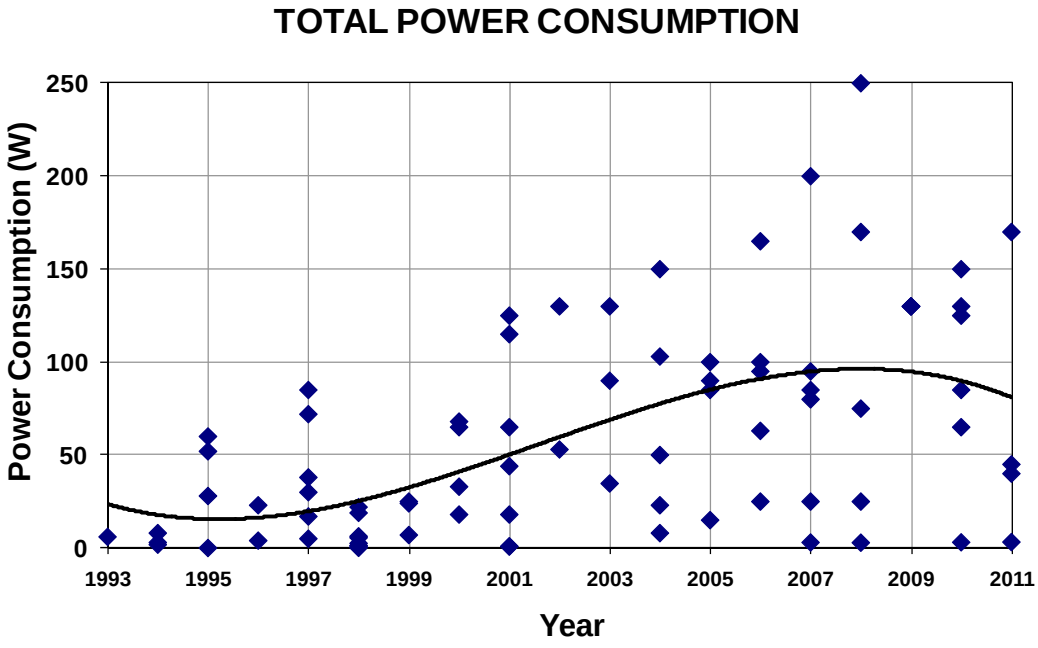

Figure 2: Total microprocessor power consumption vs Year

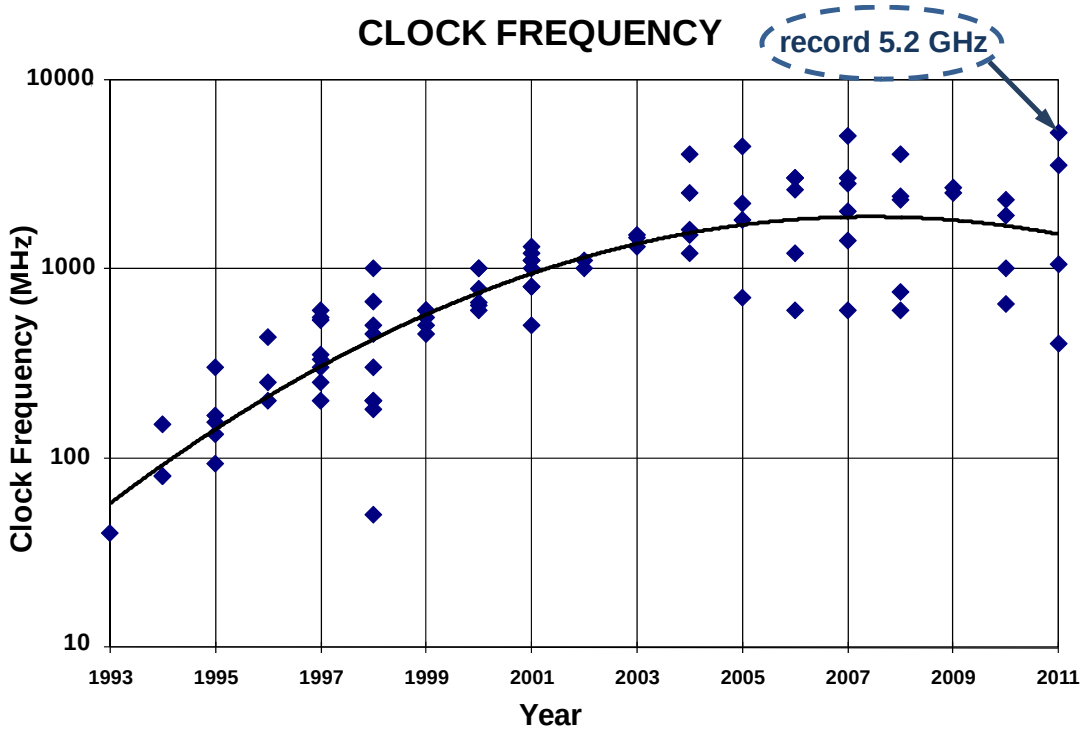

Figure 3 Microprocessor Clock Frequency vs Year

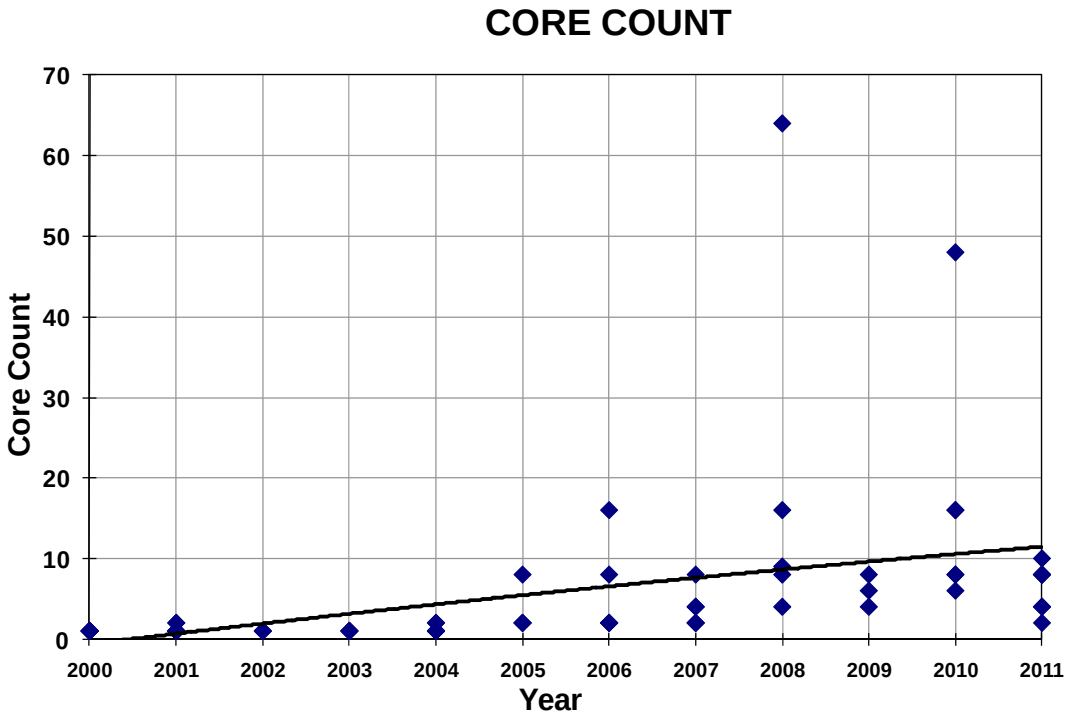

Figure 4 Number of processor cores vs Year

IMMD: Imagers, Mems, Medical, and Display

SENSORS

Recent advances in design, technology, system integration, packaging of sensors together, and increased product volumes, have dramatically reduced the cost of sensors. Cell phones, game consoles, and other consumer products, now integrate multiple sensors such as accelerometers and gyroscopes in a single package, and have spurred-on significant innovation at the application level. The use of multiple sensors, their downscaling in size, and the ever higher levels of integration available, will lead to further growth in the sensor market. Single-packaged multiple-axis accelerometers and gyroscopes have been announced by several companies, including STmicroelectronics, Bosch, and Invensense. 3-axis accelerometers and 3-axis magnetic field sensors are now becoming available.

Silicon MEMS resonators and oscillators are replacing quartz-based solutions. The market uptake for MEMS is growing exponentially.

DISPLAYS

Ongoing trends for LCDs include the drive towards larger, thinner, lower-power, and better quality displays. Structured LED backlights have provided benefits in all of these dimensions. In this technique, solid-state circuits are enabling LED backlight drivers to significantly increase the rate at which LED backlights can operate, and allow extended dynamic range by locally varying brightness. In particular, fast-moving sequences look better on screens that operate at higher frame rates.

Chip-on-Glass (CoG) interfaces are becoming a common choice for high-speed interfaces in notebook applications. In addition, touch and 3D functionality are making their way into notebook PC's and LCD monitors. Small-sized display-driver ICs are seeing increased levels of integration, with the following features becoming commonplace: user-adjustable image enhancements, touch-sensor readouts and handlings, 3D-driving control signals, and temperature-sensor integration to minimize power consumption.

MEDICAL

There is an increased focus on neural applications. There is a huge amount of R&D activities in the field of bio-potential sensors capable of measuring neural activity. Neural techniques continue to propagate into more therapeutic applications. Clinical trials are ongoing for early diagnosis of depression. Chemical sensing is gaining ground in a neurological clinical setting. A pilot study has been completed on monitoring acute activity in the brain.

Longer-term monitoring is facing similar challenges to glucose sensing in diabetes. The need for chronic chemical sensors is critical. The ultimate goal is the development of solutions corresponding to an artificial pancreas.

Cardiac therapies are focusing on ultra-miniaturization of existing devices. The goal is to eventually eliminate the leads, thereby simplifying cardiac surgery, which is currently a very invasive procedure. In addition, there is a push for instrumenting stents with miniaturized technology to add diagnostic capability to these widely-used devices.

IMAGE SENSORS

The CMOS image sensor business is still one of the fastest growing segments of the semiconductor industry due to cell phone cameras and other digital-imaging applications. The cell phone camera adoption rate is expected to be approximately 90% for 2009, and 3G mobile technology is accelerating the utilization of multiple cameras per cell phone. Other digital imaging markets include traditional digital still cameras (DSCs) and camcorders, as well as emerging markets such as web cameras, security cameras, automotive cameras, digital-cinema cameras, and gaming.

The resolution and miniaturization races ongoing, and while the performance requirements stay constant, the pixel size continues to scale down. Pixel resolution over 10M are commercially available employing enhanced small-size pixels. New innovative technologies are constantly being developed in order to compete in this race. These technologies include advanced sub-100 nanometer CMOS image-sensor fabrication processes, backside illumination, digital optics, and wafer-level cameras. The importance of digital-signal-processing technology in cameras continues to grow in order to mitigate sensor imperfections and noise, and to compensate for optical limitations. The level of sensor computation is increasing to thousands of operations per pixel, requiring high-performance and low-power digital-signal-processing solutions. In parallel with these efforts is a trend throughout the image sensor industry toward higher levels of integration to reduce system costs.

Many new achievements occurred in 2010. High Dynamic Range (HDR) is (finally!) introduced in low-cost consumer imaging. High-speed low-power low-noise column-parallel ADCs are becoming a key technology for high-definition video imagers.

Many barriers must be overcome in order to maintain market growth in the image sensor industry. These challenges include better image quality, higher sensitivity, higher-sensor resolution, lower cost, higher data-transfer rate, higher system-level integration, lower power consumption, and 3D imaging. Backside illumination is becoming an indispensable technology for gaining the competitive edge in CMOS imagers, enabling increased market share.

The trends in emerging markets include lower-bandwidth communication for surveillance cameras, wider dynamic range and optical-communication functions for automotive cameras,

faster read-out for digital-cinema cameras, and 3D imaging for gaming. These markets are placing ever increasing functionality and performance demands on today's image sensors, which are in turn delivering an exponential rate of growth in both complexity and performance to ensure they can keep pace. 3D imagers are becoming a very hot R&D topic given the current push toward 3D entertainment. Increasing R&D investment is predicted in forthcoming years for automotive imaging, and for 3-D range-finding and time-of-flight (TOF) applications. Rapid increases in integrated logic functionality are driving a dramatic increase in imager functions and features.

MEMORY

Memory design has seen a number of trends over the years: process technology has steadily reduced its minimum feature size; a wide variety of techniques have been developed to improve packing-density; and a myriad of technology/circuit/system optimizations have been created to improve performance and reduce power dissipation. In addition, emerging technologies such as 3D chip stacking and new physical memory mechanisms are pushing the memory R&D frontier even-further forward. Some current state-of-the-art results from ISSCC 2011 include:

- 28nm 64Gb TLC NAND flash memory
- 7Gb/s-GDDR5 DRAM with 2Gb capacity
- 64Mb SRAM in High-κ Metal-Gate 32nm SOI technology with robust operation
- 28nm SRAM using 6T cells with low-voltage 0.6V operation
- Emerging memory technologies realizing non-volatile RAM: FeRAM (Ferrolectric RAM) with a novel sensing scheme, a fast read/write RRAM (Resistive RAM), and a large bandwidth CBRAM (Conductive-Bridging RAM) at 2.3GB/s.

NON-VOLATILE MEMORY (NVM)

The performance of persistent Non-Volatile RAM (NVRAM) has evolved over time, with ISSCC faithfully tracking these developments over the years. ISSCC 2011 will report the highest read/write bandwidths for emerging NVRAM technologies such as Phase Change Memory (PCRAM) and Resistive RAM (RRAM) resulting from the use of new circuit and device technology (Figure 5). This is presenting new opportunities for extending the memory technology spectrum, together with existing NAND/MRAM/FeRAM/PCRAM technologies, as shown in Figure 6. Commercial uses of these new breeds of NVRAM have been very slow to appear because of the rapid reduction of per-bit costs of conventional flash memory technologies already in the market. However, these new technologies are sure to capture some specific markets for lower-power or zero stand-by system implementation in the coming age of green technology.

HIGH-PERFORMANCE EMBEDDED MEMORY

Embedded memory plays a crucial role in today's VLSI applications from high-performance computing to low-power consumer electronics. While scaling of technology feature size down to 32nm or 28nm has enabled ever- larger and higher-performance on-die memories. However, scaling has also created growing challenges for the embedded memory designer. Growing device variability and power limitations are driving innovative solutions to maintain robustness and area-efficiency in such aggressively scaled memories. In particular, peripheral-circuit-assist features have become the key to maintaining cell read and write margins to enable low-voltage operation for dense SRAM caches. New strategies ranging from circuit-level techniques to fundamental changes in array architecture can also enable significant gains in area and power efficiency.

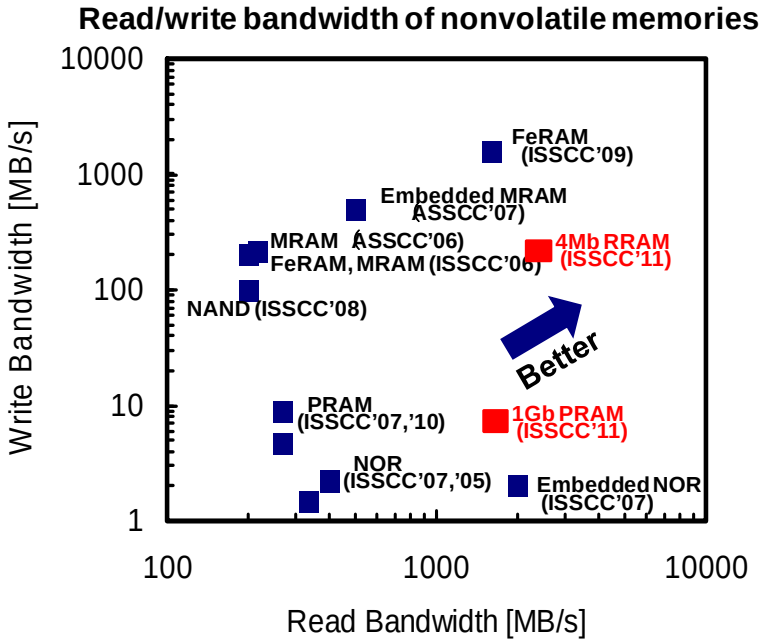

Figure 5. NVRAM Read/Write Bandwidth Trends

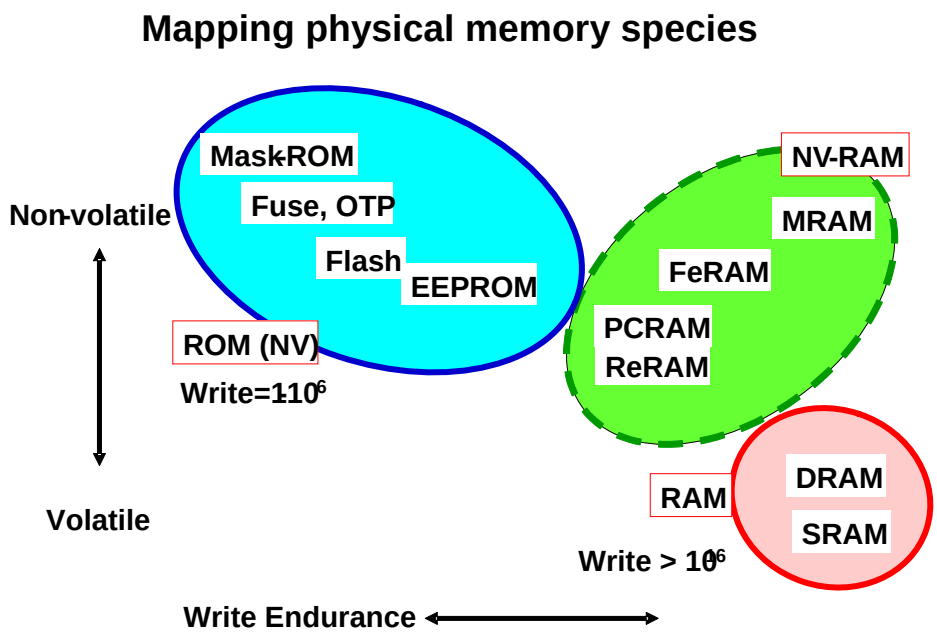

Figure 6. Comparison of NVRAM Technologies

NAND FLASH MEMORY

Significant developments in NAND flash memory over the past few years are resulting in high-density, low-power, and low-cost storage solutions that are enabling the replacement of traditional hard-disk storage with solid-state disks (SSDs). At ISSCC 2011, a 64Gb/die capacity will be demonstrated using 24nm technology with 2b/cell operation. With physical scaling down accompanied by advancing multi-level-storage-cell concepts, a 64Gb/die capacity has been demonstrated in 24nm technology with 2 bits/cell operation. Figure 7 shows the observed trend in NAND flash capacities presented at ISSCC over the past 17 years. Unfortunately, as process feature size shrinks, error rates continue to rise, requiring system designers to develop more-sophisticated controllers to offset this issue, some of which are utilized outside the NAND silicon in the system memory controller.

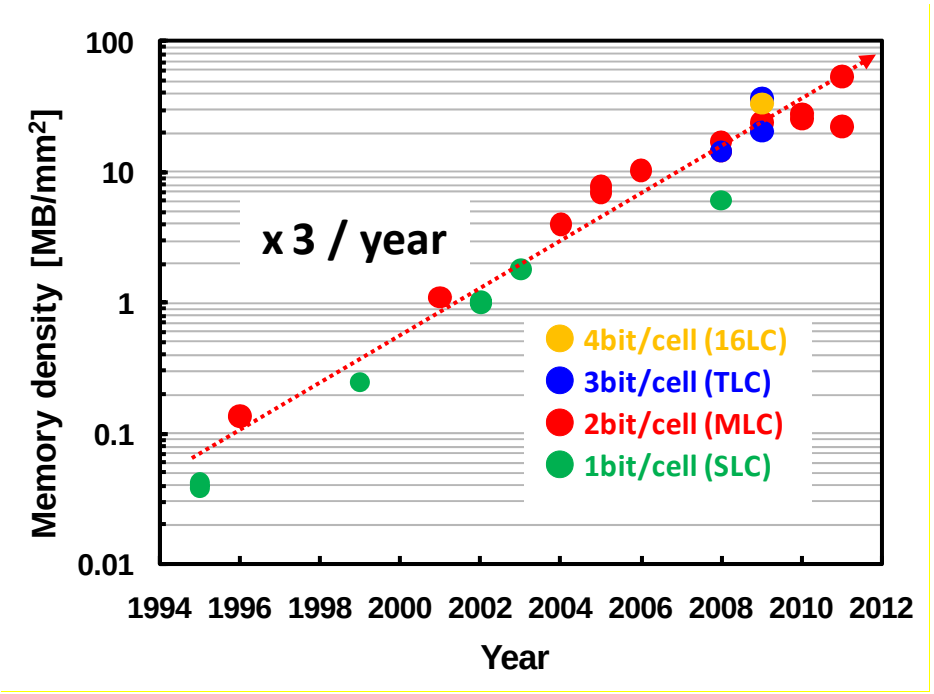

Figure 7 NAND Flash Memory Trends

SRAM BITCELL DESIGN

Historically, a 50% area reduction in bitcell from node to node has been enabled by the scaling of technology feature size, resulting in a 2x improvement in on-die memory integration with each node reduction and continuing improvements in performance. However, the reduction in transistor geometry is increasing device variability, resulting in a slowdown in the scaling trend as shown in Figure 8. Between the 45nm and 32nm technology nodes, bitcell scaling has been reduced to less than the typical 50%. The introduction of High-κ Metal Gate technologies at the 45nm node has provided a significant reduction in the equivalent oxide thickness, thereby reducing the V_T mismatch and allowing further aggressive scaling of device dimensions needed to achieve the scaling of area. However, technology improvements alone are not sufficient to maintain area scaling. SRAM peripheral-circuit-assist features have become the key to maintaining cell stability, readability and write margins, and enable low-voltage operation. New strategies ranging from circuit-level techniques to fundamental changes in array architecture can also enable significant gains in area and power efficiency.

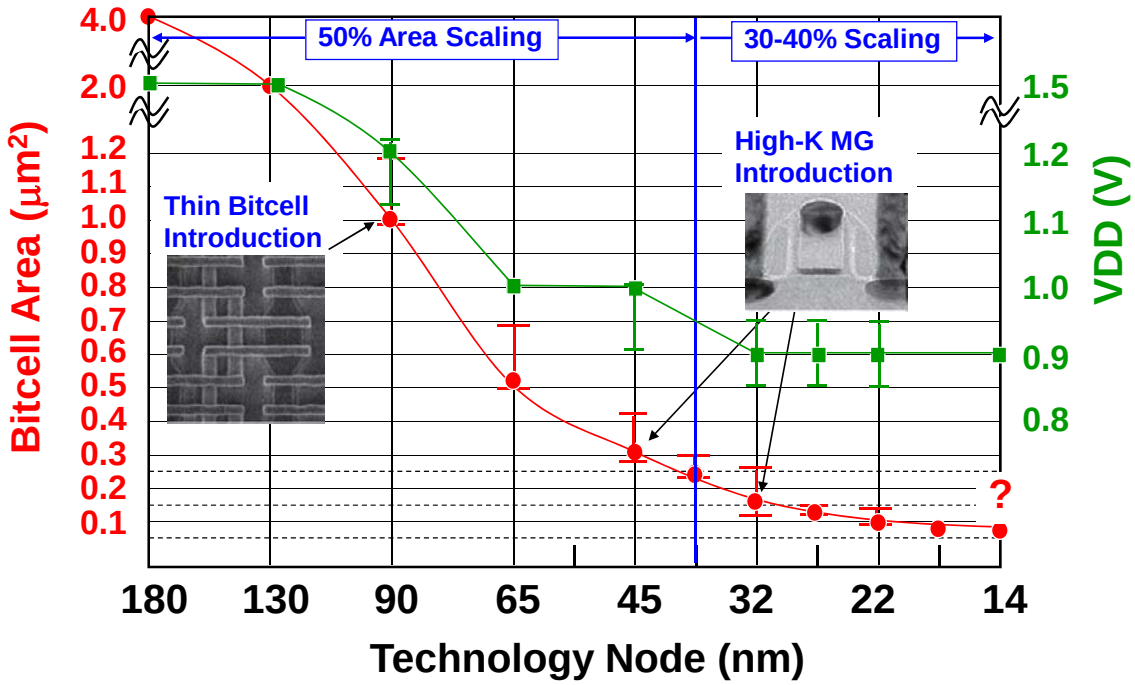

Figure 8 SRAM Bitcell Trends

DRAM & HIGH-SPEED I/O

Unfortunately, the gap between memory-core frequency and external-data rate continues to increase as conventional high-speed wired interface schemes such as DDRx and GDDRx for DRAM and NAND flash memory continue to evolve (Figure 9). This leads to the need for a larger prefetch size, which is emerging as a major problem in modern memory systems. However, alternatives which accommodate high data rates through the use of wider or differential interfaces will face the problem of increased pin-counts, and enlarged silicon areas. Combined with 3D integration of memory and memory/logic in near-future commercial products, new interface technologies will yield more memory stacking, along with lower-power and higher-bandwidth interfaces.

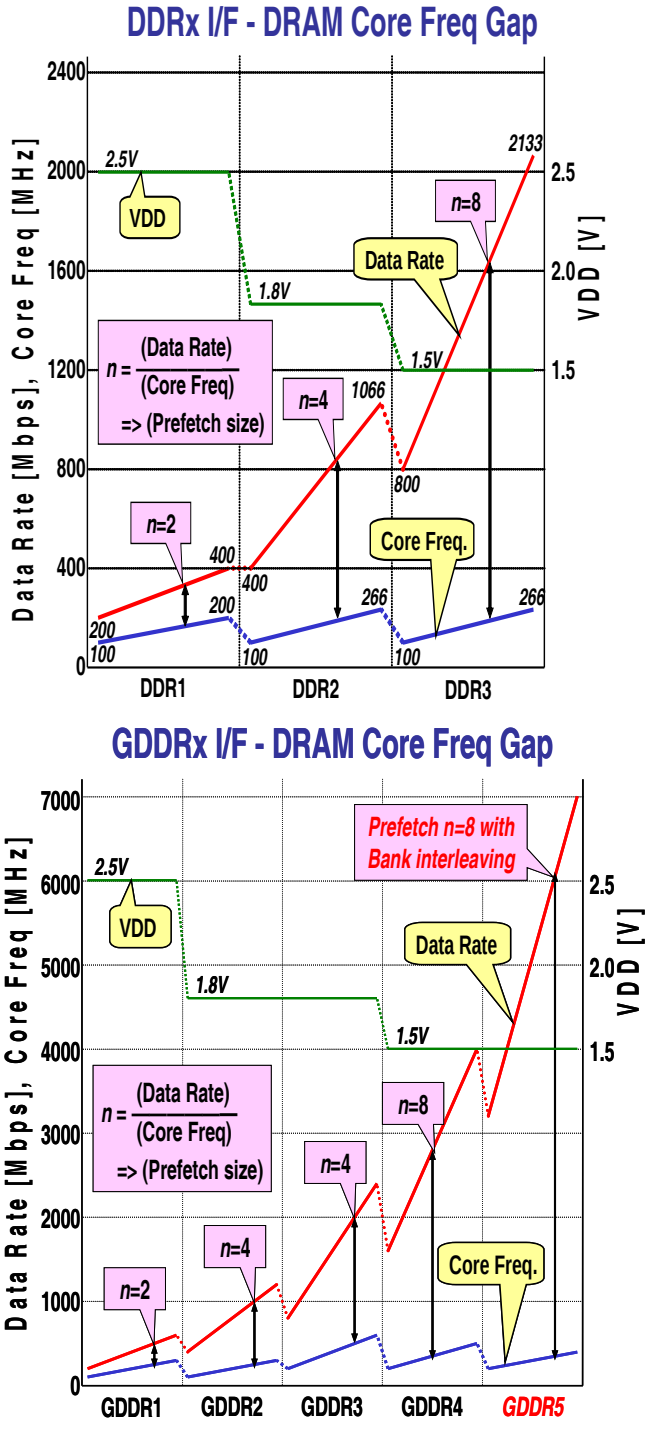

Figure 9 DRAM and High-Speed I/O Trends

RADIO FREQUENCY (RF)

Increasing demand for higher data rates fueled by multimedia applications require communication systems to run at ever-increasing speeds. The bandwidth capabilities of wireline and wireless data communication systems are projected in the data-rate-trend chart shown below. As depicted in Figure 10, millimeter-wave frequency bands in the 120GHz range are enabling a new, potentially-disruptive technology. Using carrier frequencies in the 120GHz band, new wireless transceiver systems allow data rates up to 10Gb/s for short-range wireless data communication. This chart also indicates that wireless links are approaching the data rates traditionally realized with wireline solutions. Advances in wireless-communication data rates are being enabled by advanced nanometer-length CMOS technologies, combined with innovative circuit and radio-architecture implementations.

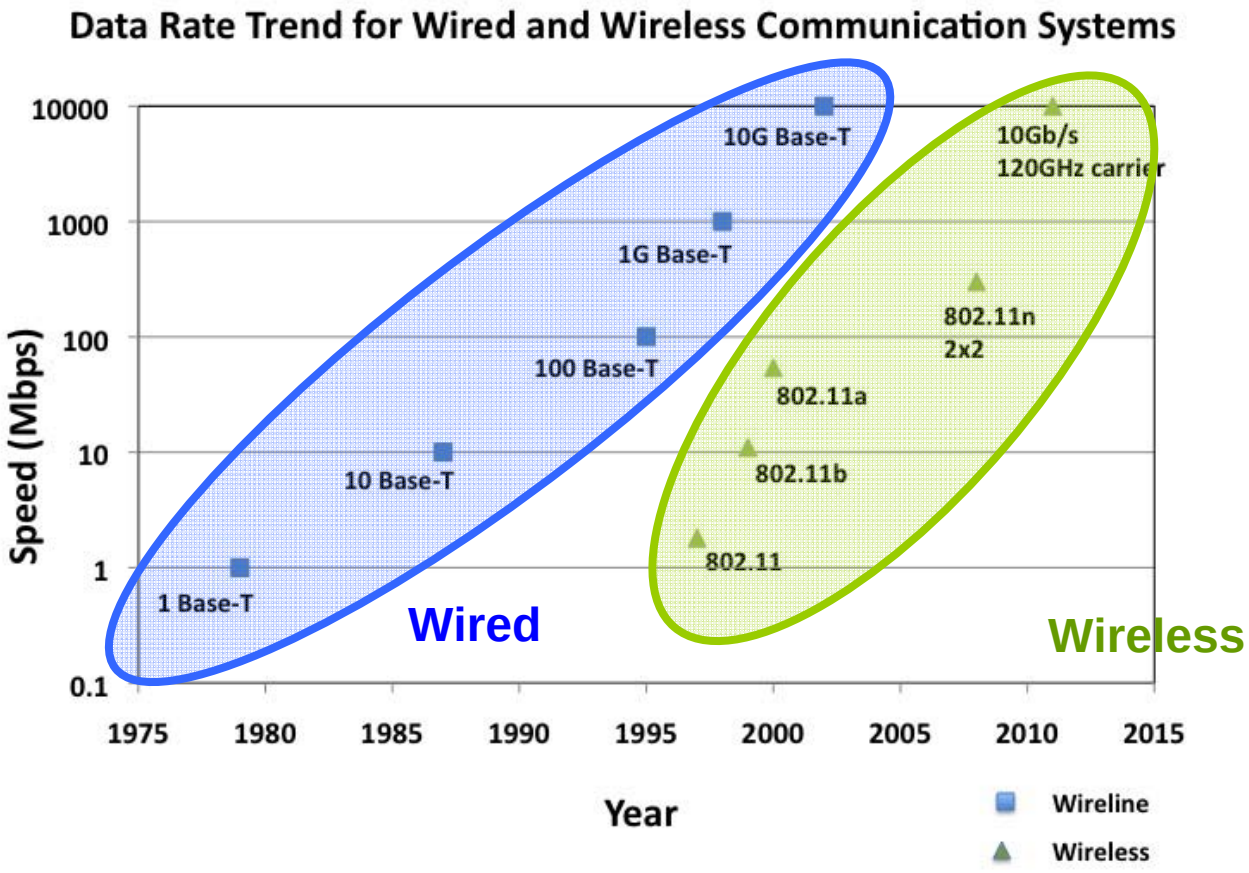

Figure 10 Data rate trends

TECHNOLOGY DIRECTIONS

Body Area Networks (BAN) is an emerging technology that has the potential to revolutionize next-generation healthcare, entertainment, and other personal applications. BAN, compared to other personal-area network solutions, targets a unique region of the power vs. data rate trade-off that makes novel personal applications possible (Figure 11).

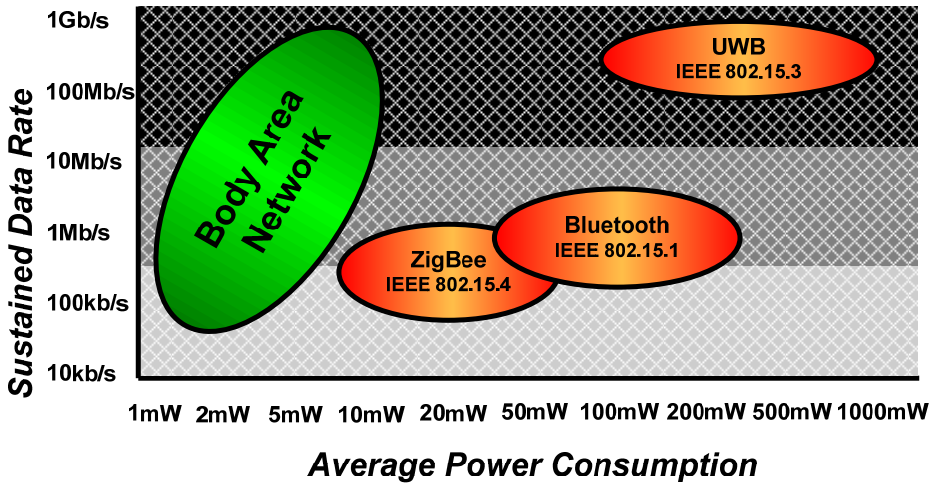

Figure 11 Modern Communication Technologies

Body-Channel Communication (BCC), a type of BAN which uses the human body as the signal-transmission medium, can achieve high-speed communication with low energy consumption compared to other personal-area network (PAN) solutions such as ZigBee, Bluetooth, and UWB (Figure 12).

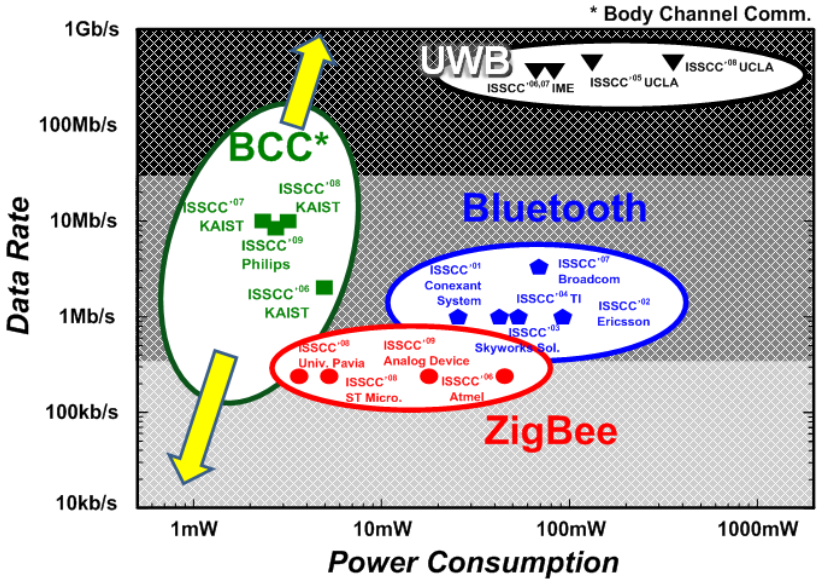

Figure 12 Energy Efficiency of Modern Communication Technologies

WIRELINE

The trends in wireline communications today follow several seemingly conflicting paths. On one hand, there is a strong demand for transceivers that are highly-optimized for low power consumption for use with relatively low-loss channels. Simultaneously, there is a similarly strong demand for transceivers that, while still energy efficient, are optimized to provide signal levels and equalization capabilities that allow for communication over adverse channel conditions at speeds previously deemed impossible. At ISSCC 2011, papers in three sessions [Session 8, Session 20, Session 25] described a number of results that address these issues.

New applications are emerging, such as Internet multi-player gaming, network-based computing/data-storage, transaction-intensive Web 2.0 applications, and high-definition home-entertainment networks. The enabling technologies for these applications are high-performance transceivers for OC-768 (40Gb/s), 100Gb/s Ethernet, and high-speed “green” serial links for data centers. The demands of these applications will drive the advancement in equalization capability and robust-adaptation methodology. Additionally, the deployment of Gigabit Passive Optical Networks (GPON) in the near future will provide home-access data rates beyond 10Gb/s. PON technology reduces system cost by sharing the existing fiber infrastructure between multiple customers, but challenges transceiver designers by requiring burst-mode operation of amplifiers, and clock recovery with low latency at Gb/s data rates. We expect continuing innovation in this area for the foreseeable future.

As shown in Figure 13, up to 100Gb/s data rates are now readily available using CMOS solutions. At these rates, an entire high-definition movie can be transferred in less than a second! Achieving such a high data rate at a reasonable level of power consumption requires advanced energy-efficient clock-and-data recovery, and equalization techniques, to conquer transmission-channel impairments and speed limitations of low-cost CMOS. Papers presented at ISSCC 2011 will cover a large selection of techniques in various CMOS nodes with impressively low power consumption.

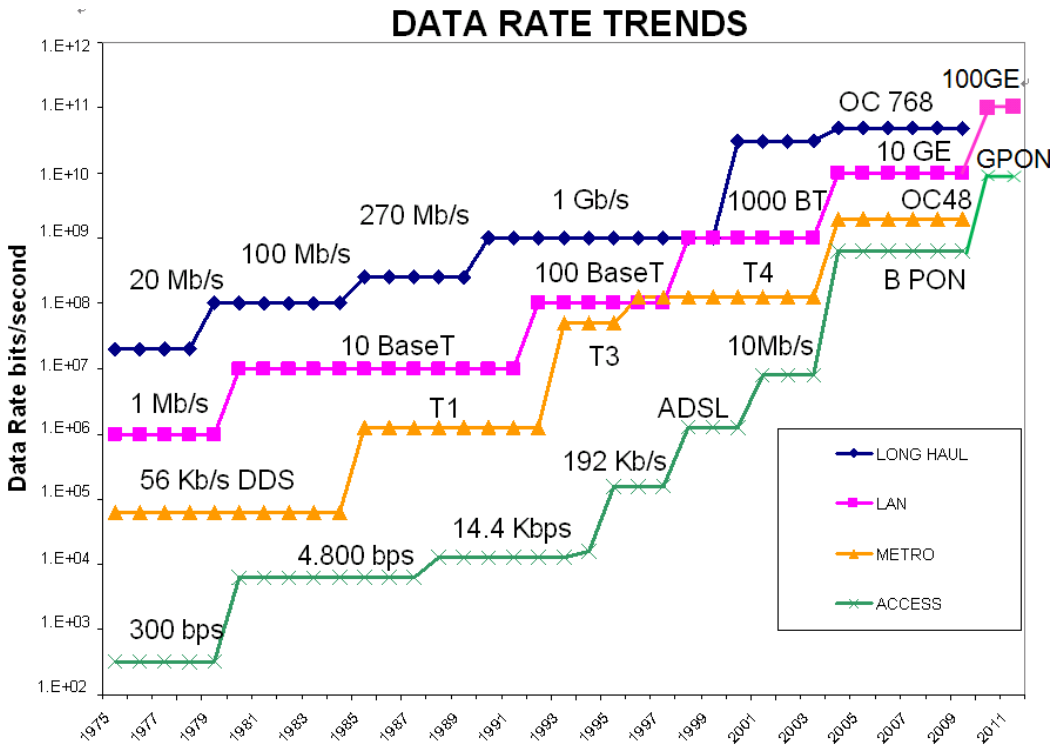

Figure 13 Data Rate Trends