IEEE SOLID-STATE CIRCUITS SOCIETY

ADVANCE PROGRAM

2020 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE

FEBRUARY 16, 17, 18, 19, 20

CONFERENCE THEME:

INTEGRATED CIRCUITS POWERING THE AI ERA

SAN FRANCISCO
MARRIOTT MARQUIS HOTEL

NEW THIS YEAR!
HIGHLIGHTED CHIP RELEASES

5-DAY PROGRAM

SUNDAY ALL-DAY
2 FORUMS: mm-Wave 5G; ML as Killer App

10 TUTORIALS: Integrated Transformers; DCDC Converters; Wearable/Implantable Sensing; Nonvolatile Memories (MRAM, RRAM, PRAM); Time-Interleaved ADCs; Digital Fractional-N Phased Locked Loop; Low-Dropout Integrated Regulators; Capacitive Sensor Interfaces; Wireless Transceiver Circuits/Architectures (2G to 5G); Understand/Evaluate DL Processors

2 EVENING EVENTS: Graduate Student Research in Progress; Rising Stars 2020

THURSDAY ALL-DAY
4 FORUMS:
ML Processors; Electrical/Optical Transceivers; Power Management for Future SoCs; Sensors for Health

SHORT-COURSE: Circuit Design in Advanced CMOS

ISSCC VISION STATEMENT

The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and application to maintain technical currency, and to network with leading experts.

CONFERENCE TECHNICAL HIGHLIGHTS

On Sunday, February 16th, the day before the official opening of the Conference, ISSCC 2020 offers:

- A choice of up to 4 of a total of 10 Tutorials, or
- A choice of 1 of 2 all-day Advanced-Circuit-Design Forums

The 90-minute tutorials offer background information and a review of the basics in specific circuit- and system-design topics. In the all-day Advanced-Circuit-Design Forums, leading experts present state-of-the-art design strategies in a workshop-like format. The Forums are targeted at designers experienced in the technical field.

On Sunday evening, there are two events: A WiC Workshop on "Rising Stars 2020" will be offered starting at 4:00 pm. In addition, the Student-Research Preview, featuring ??? ninety-second introductory presentations followed by a poster session from selected graduate-student researchers from around the world will begin at 7:30 pm. Introductory remarks at the Preview will be provided by a distinguished member of the solid-state circuit community, Tadahiro Kuroda, Professor, University of Tokyo,

On Monday, February 17th, ISSCC 2020 at 8:30 am offers four plenary papers on the theme: "Integrated Circuits Powering the AI ERA ". On Monday at 1:30 pm, there begin five parallel technical sessions, followed by a Social Hour at 5:15 pm open to all ISSCC attendees. The Social Hour, held in conjunction with Book Displays and Author Interviews, will also include a Demonstration Session, featuring posters and live demonstrations of selected papers from industry and academia. On Monday evening there is one event. At 8:00 pm "Industry Showcase" will feature short presentations as well as interactive demonstrations where attendees can have a hands-on experience with each featured innovation

On Tuesday, February 18th, there are five parallel technical sessions, both morning and afternoon. A Social Hour open to all ISSCC attendees will follow. The Social Hour, held in conjunction with Book Displays and Author Interviews, will also include a second Demonstration Session. Tuesday evening includes two events, entitled "Quiz Show: "The Smartest Designer in the Universe" and "Open-Source Hardware Revolution".

On Wednesday, February 19th, there will be five parallel technical sessions, both morning and afternoon, followed by Author Interviews.

On Thursday, February 20th, ISSCC offers a choice of five all-day events:

- A Short Course entitled: "**Circuit Design in Advanced CMOS Technologies — Considerations and Solutions** "
- Four Advanced-Circuit-Design Forums entitled:

"**Machine Learning Processors: From High Performance Applications to Architectures and Benchmarking"**
"**Cutting Edge Advances in Electrical and Optical Transceiver Technologies**"
"**Power Management as an Enabler of Future SoCs"**
"Sensors for Health"

This year, again, there is an option which allows an attendee to sample parts of all 5 Thursday offerings. Registration for educational events on Sunday and Thursday will be filled on a first-come first-served basis. Use of the ISSCC Web-Registration Site (http://www.isscc.org) is strongly encouraged. Registrants will be provided with immediate confirmation on registration for the Conference, Tutorials, Forums, and the Short Course.

Need Additional Information? Go to: www.isscc.org

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There are a total of 10 tutorials this year on 10 different topics. Each tutorial, selected through a competitive process within each subcommittee of the ISSCC, presents the basic concepts and working principles of a single topic. These tutorials are intended for non-experts, graduate students and practicing engineers who wish to explore and understand a new topic.

Ali Sheikholeslami
ISSCC Education Chair

8:30 AM

T1: Fundamentals of Integrated Transformers: From Principles to Applications

Andrea Bevilacqua, *University of Padova, Padova, Italy*

Integrated magnetic transformers are becoming ubiquitous in mm-wave and RF systems, while also finding application in fully integrated DC-DC converters. This tutorial will cover the fundamentals of transformer operation spanning from the underlying physical principles, to the link between the magnetic parameters (inductances and magnetic coupling) and the inductor geometry, to its use in the design of building blocks like LNAs, PAs, VCOs, etc. The advantages and possibilities of using a transformer for the implementation of baluns, impedance transformation networks, higher-order resonant networks, feedback circuits, etc. will be highlighted.

Andrea Bevilacqua received the Laurea and Ph.D. degrees in Electronics Engineering from the University of Padova, Italy. From 2005 to 2015, he was Assistant Professor with the University of Padova, where he is now Associate Professor. His current research interests include the design of analog and RF/microwave integrated circuits and the analysis of wireless communication systems, radars, and DC-DC converters. He is author or coauthor of more than 90 technical papers, and he holds 5 patents. He serves on the ISSCC and ESSCIRC Technical Program Committees and was TPC Co-Chair of ESSCIRC 2014.

8:30 AM

T2: Analog Building Blocks of DC-DC Converters

Bernhard Wicht, *University of Hannover, Hannover, Germany*

System behavior and performance of power management strongly depend on the implementation at the circuit level. This tutorial covers the design of DC-DC converter building blocks such as power switches, gate drivers and their supply, level shifters and error amplifiers, as well as control-loop and current-sensing techniques. Circuits for diagnostics and protection will also be addressed. Increasing switching frequency scales down passive components, but poses a challenge for the design of timing-critical circuits. The tutorial will highlight trade-offs between speed, efficiency, complexity, voltage and current capabilities, etc.

Bernhard Wicht has 20+ years of experience in analog and power-management IC design. He received the Dipl. Ing. degree in electrical engineering from TU Dresden, Germany, in 1996 and the Ph.D. degree from TU Munich, Germany, in 2002. Between 2003 and 2010, he was with Texas Instruments, Germany, responsible for the design of automotive ICs for power management, motor control and transceivers. Between 2010 and 2017, he was a full professor and a member of the Robert Bosch Center for Power Electronics at Reutlingen University. Since April 2017, he has been heading the Chair for Mixed-Signal IC Design at Leibniz University Hannover, Germany.

8:30 AM

T3: Interface Circuits for Wearable and Implantable Sensing Systems

Patrick P. Mercier, *University of California, San Diego, La Jolla, CA*

Wearable and implantable systems offer an exciting means to monitor human physiology in real time. Such devices require careful interaction between transducers and front-end circuits in order to extract the maximum possible signal-to-noise ratio, while also carefully managing system-level size and power trade-offs. This tutorial will introduce front-end design techniques used in electrophysiological sensing applications, along with emerging trends in physiochemical sensing applications.

Patrick Mercier is an Associate Professor of Electrical and Computer Engineering and co-founder/co-director of the Center for Wearable Sensors at UC San Diego. He received his B.Sc. degree from the University of Alberta, and the S.M. and Ph.D. degrees from MIT. His research interests include the design of energy-efficient mixed-signal systems, RF circuits, power converters, and sensor interfaces for wearable, medical, and mobile applications. This has led to over 120 peer-reviewed papers. He has received numerous awards, including the DARPA Young Faculty Award, the NSF CAREER Award, and the 2010 ISSCC Jack Kilby Award. He is an Associate Editor of TBioCAS and SSCL, and is a member of the ISSCC, CICC, and VLSI technical program committees.

10:30 AM

T4: Basics of Non-Volatile Memories: MRAM, RRAM, and PRAM

Fatih Hamzaoglu, *Intel, Hillsboro, OR*

NAND Flash and eFlash have been the workhorse of memory hierarchy for standalone storage and embedded non-volatile memories (NVMs), respectively. But with the ever increasing need for memory capacity and bandwidth, due to new applications in graphics, AI and IoT, device and circuit designers have been heavily investigating alternative memories to fill the need. When it comes storage, there is a big gap between DRAM and NAND in terms of density and speed, which could justify a new memory type. When it comes to NVM, growing IoT requires better performance and more power efficient NVM than eFlash, which can be scaled to 1xnm technologies.

This tutorial will talk about the basic characteristics, circuits and system designs for emerging non-volatile memories such as MRAM, RRAM, and PRAM. The tutorial will present the details of MRAM and RRAM, as well as a comparison of these memory devices, and the applications they target.

After finishing the Ph.D. in EE at the University of Virginia in 2002, Fatih joined Logic Tech. Development at Intel. Since then, he has been working on memory developments, such as SRAM, DRAM, MRAM and RRAM. He has served as technical committee member at VLSI Symp. Circuits and ISSCC. He has co-authored more than 40 papers and he's co-inventor of more than 30 patents.

10:30 AM

T5: Fundamentals of Time-Interleaved ADCs

John P. Keane, *Keysight Technologies, Santa Clara, CA*

In recent years, time-interleaving analog-to-digital converters (ADCs) have become more popular, especially for high sample rate applications such as wireline communications. This tutorial will cover the fundamentals of time-interleaved sampling, including an introduction to aliasing and an explanation of how mismatch in time-interleaved architectures can cause aliasing artifacts to appear. Practical methods to implement time-interleaved ADCs and combat these mismatch-induced effects will also be presented.

John P. Keane received the Ph.D. degree in Electrical Engineering from the University of California, Davis in 2004. Since then, he has been with Keysight Technologies (formerly Agilent Technologies), Santa Clara, CA, where he is engaged in research on high-performance integrated circuits for measurement applications. His research interests include timing recovery and adaptive equalization for high-speed serial transceivers and the design and calibration of high-resolution data converters. Most recently his focus has been on the design of high-bandwidth time-interleaved analog-to-digital converters. He is a co-author of several IEEE papers and US patents on these topics and is currently a member of the ISSCC technical program committee.

10:30 AM

T6: Digital Fractional-N Phase-Locked-Loop Design

Mike Shuo-Wei Chen, *University of Southern California, Los Angeles, CA*

The tutorial overviews the basics of digital fractional-N phase-locked-loop architectures and their design principles from the signal-processing level down to circuit design. We will examine various design constraints and implementation overhead of such architectures due to the inherent digital architecture as well as circuit non-idealities. We will discuss circuit design and calibration techniques. Lastly, some real design examples in silicon with measurement data will be provided.

Mike Shuo-Wei Chen is Associate Professor in the Electrical Engineering Department at the University of Southern California (USC) and holds Colleen and Roberto Padovani Early Career Chair position.

He received the B.S. degree from National Taiwan University, Taipei, Taiwan, in 1998 and the M.S. and Ph.D. degree from University of California, Berkeley, in 2002 and 2006, all in Electrical Engineering. As a graduate student researcher, he proposed and demonstrated the asynchronous SAR ADC architecture, which has been adopted today for low-power high-speed analog-to-digital conversion products in industry. At USC, he leads an analog mixed-signal circuit group. He was the recipient of NSF Faculty Early Career Development (CAREER) Award, DARPA Young Faculty Award (YFA) both in 2014.

1:30 PM

T7: Basics of Digital Low-Dropout (LDO) Integrated Voltage Regulators

Mingoo Seok, *Columbia University, New York, NY*

Systems-on-chips incorporate integrated low-dropout (LDO) voltage regulators (VRs) to improve energy efficiency by allowing each core on a shared input voltage rail to operate at a unique voltage. LDOs enable compact size, low cost, and relatively simple integration. This tutorial introduces the key trade-offs between analog and digital LDOs and covers the primary specifications. Finally, this tutorial presents a wide range of state-of-the-art digital LDOs while highlighting the key design trade-offs.

Mingoo Seok is Associate Professor of Electrical Engineering at Columbia University. He received the B.S. degree with summa cum laude from Seoul National University, South Korea, in 2005, and the M.S. and Ph.D. degrees from the University of Michigan in 2007 and 2011 respectively, all in electrical engineering. His research interest is VLSI hardware, including near-threshold and subthreshold-voltage ultra-low-power hardware, machine-learning hardware, variation-tolerant hardware, on-chip power management, and non-conventional computing such as in-memory computing and hybrid analog-digital computing. He won the 2015 NSF CAREER award. He has been a technical committee member in hardware conferences including the IEEE International Solid-State Circuits Conference (ISSCC).

1:30 PM

T8: Capacitive Sensor Interfaces

Man-Kay Law, *University of Macau, Macau, Macau*

Capacitive sensors for displacement, proximity and pressure sensing are widely deployed in various consumer, medical, automotive, and industrial sectors, with the advantages of zero static power consumption and good compatibility with CMOS circuitry. This tutorial provides an overview of the fundamental principles of capacitive sensor interfaces, as well as the design tradeoffs in terms of accuracy and energy consumption. Recent techniques to achieve low-noise and high-efficiency sensing will also be discussed.

Man-Kay Law received the B.Sc. degree in Computer Engineering and the Ph.D. degree in Electronic and Computer Engineering from Hong Kong University of Science and Technology. Since 2011, he has been with the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macau, China, where he is currently an Associate Professor. His research interests include ultra-low-power sensing circuits and systems, analog and mixed-signal integrated circuits, and energy harvesting techniques. He is a co-recipient of the A-SSCC Distinguished Design Award in 2015, and also the advisor for student awards, including the SSCS Pre-doctoral Achievement Award and the ISSCC Silk-Road Award. He is a member of the Technical Program Committee of ISSCC.

3:30 PM

T9: Fundamentals of Wireless Transceiver Circuits and Architectures (from 2G to 5G)

Venumadhav Bhagavatula, *Samsung Semiconductor, San Jose, CA*

Cellular technology has witnessed five generations of evolution - the mobile UE-era ushered in by 2G (GSM/EDGE), to the future smart-phones that will powered by the enhanced spectral efficiency of 5G. Each 'G' improved the user experience while introducing new hardware design challenges. This tutorial follows a top-down approach - we compare 2/3/4/5G system requirements, derive key TX/RX/LO circuit specifications, and highlight the differences in circuit topologies suited for these contrasting specifications. Using this framework, circuit techniques to handle a diverse range of problems such as low phase-noise oscillators, improved blocker tolerance, single-RB linearity, and digital calibration will be introduced.

Venumadhav Bhagavatula received the B.E. degree in electronics and communication from the University of Delhi, New Delhi, India, the M.Tech. degree in electronic design technology from the Indian Institute of Science, Bangalore, India, and the Ph.D. degree in electrical engineering from the University of Washington, Seattle, WA, USA, in 2005, 2007, and 2013. Since 2014 he has been with the Advanced Circuit Design group at Samsung Semiconductors Inc., San Jose, CA, USA. His research interests include RF/mm-wave and low-power mixed signal circuits. He currently serves on the technical program committee member for the ISSCC.

3:30 PM

T10: How to Understand and Evaluate Deep Learning Processors

Vivienne Sze, *Massachusets Institute of Technology, Cambridge, MA*

There has been a significant amount of specialized hardware being developed for deep learning in both academia and industry. This tutorial aims to highlight the key concepts needed to evaluate and compare deep learning processors. We will discuss existing challenges such as the flexibility and scalability needed to support a wide range of neural networks, as well as design considerations for different platforms. We will also discuss metrics to evaluate and compare existing solutions.

Vivienne Sze is an Associate Professor in the EECS Department at MIT. Her research interests include energy-aware signal processing algorithms, and low-power circuit and system design for applications, such as machine learning, computer vision, autonomous navigation, and video coding. Prior to joining MIT, she was a Member of Technical Staff in the R&D Center at Texas Instruments, where she developed algorithms and hardware for the H.265/HEVC video coding standard, which received the Primetime Engineering Emmy Award. She is a recipient/co-recipient of several awards including the Symposium on VLSI Circuits Best Student Paper Award, the MICRO Top Picks Award, and MIT's Jin-Au Kong Outstanding Doctoral Thesis Prize.

F1: Millimeter-Wave 5G: From Soup to Nuts and Bolts

Organizers: **Arun Natarajan,** *Oregon State University, Corvallis, OR*

Committee: **Krzysztof Dufrêne,** *Intel DMCE, Linz, Austria*
Chan-Hong Chern, *TSMC, San Jose, CA*
Harish Krishnaswamy, *Columbia University, New York, NY*
Jongwoo Lee, Samsung, *Hwaseong, Gyeonggi-do, Korea*
Theodore Georgantas, *Broadcom, Greece*

Millimeter-wave frequencies have emerged as a promising solution to achieve increased wireless capacity and speed in 5G networks. The forum brings together experts who will describe challenges and state-of-the-art in circuits and architectures for 28GHz/38GHz 5G NR transceivers targeting UE, CPE and infrastructure applications. System-level deployment objectives and real-world constraints will be presented to provide the context for mm-wave transceiver designs. Different device technologies will be considered and system-level requirements will be translated to design approaches for critical building blocks for frequency synthesis, power amplification, RF-PA power supply systems and analog-to-digital conversion. Packaging and test considerations play an integral role in mm-wave transceiver design due to the high operating frequency and large number of elements. Low-cost mm-wave antenna and packaging will be presented along with phased array calibration and test approaches for a holistic overview of future mm-wave 5G landscapes.

Agenda

Time	Topic
8:00 AM	Breakfast
8:10 AM	Introduction Arun Natarajan, Oregon State University, Corvallis, OR
8:15 AM	**mm-Wave: From Soup to Nuts Moving it Forward** **Rob Soni,** *Nokia Bell Labs, Randolph, NJ*
9:00 AM	**5G mmWave Front-End Technologies and Architectures** **Bror Peterson,** *Qorvo, Dallas, TX*
9:45 AM	**Transceiver Design for 5G mmWave UE** **Sang Won Son,** *Samsung, San Jose, CA*
10:30 AM	Break
10:45 AM	**Frequency Generation for mm-wave 5G** **Mike Keaveney,** *Analog Devices, Limerick, Ireland*
11:35 AM	**Millimeter-Wave Power Amplifiers for 5G: Status and Prospects** **Peter Asbeck,** *UCSD, San Diego, CA*
12:25 PM	Lunch
1:25 PM	**High Performance ADCs for 5G** **Benjamin Hershberg,** *IMEC, Leuven, Belgium*
2:15 PM	**Scalable Approaches of Organic Substrate Implementation for mmWave Antenna in Package** **Harrison Chang,** *ASE, Kaohsiung, Taiwan*
3:05 PM	Break
3:20 PM	**Beamforming Arrays and their Test and Calibration** **Brian Floyd,** *North Carolina State Universty, Raleigh, NC*
4:10 PM	**Envelope Tracking Modulator for Millimeter-Wave RF Power Amplifiers** **Chen-Yen Ho,** *Mediatek, Hsinchu, Taiwan*
5:00 PM	Conclusion

F2: ML at the Extreme Edge: Machine Learning as the Killer IoT App

Organizer: **Dennis Sylvester,** *University of Michigan, Ann Arbor, MI*

Committee: **Meng-Fan (Marvin) Chang,**
National Tsing Hua University, Hsinchu, Taiwan
James Myers, *Arm, Cambridge, United Kingdom*
Naveen Verma, *Princeton University, Princeton, NJ*

This forum puts a clear focus on machine learning in very low power edge devices (uW to mW), rather than focusing on its use in data centers. While GPUs for training in data centers, and large-scale inference engines are the common case today, the combination of IoT and ML brings new capabilities to edge devices. Speakers will motivate this area and provide insights on the impact of resource constraints on both training and inference in such devices. In addition, key application areas are discussed in depth, namely audio and imaging. The role of new memory-centric design approaches in edge-based ML is also discussed. Finally, the software environment is discussed, to make hardware designers aware of the opportunities for power-constrained ML algorithm implementations.

Agenda

Time	Topic
8:00 AM	Breakfast
8:20 AM	**Introduction** **Dennis Sylvester,** *University of Michigan, Ann Arbor, MI*
8:25 AM	**Machine Learning Meets IoT:** **The Perfect Storm for Innovation in Ultra-Low Power System Design** **Boris Murmann,** *Stanford University, Stanford, CA*
8:50 AM	**TinyML: Ultra-Low Power Edge AI for Autonomous Systems** **Arijit Raychowdhury,** *Georgia Institute of Technology, Atlanta, GA*
9:40 AM	**Bringing Intelligence to Mobile Platforms:** **From Deep Learning to Neuromorphic Computing** **Dongsuk Jeon,** *Seoul National University, Seoul, Korea*
10:30 AM	Break
10:45 AM	**Structured Sparsity and Low-Precision Quantization** **for Energy-/Area-Efficient DNNs** **Jae-sun Seo,** *Arizona State University, Tempe, AZ*
11:35 AM	**TinyML for Audio-Based Applications** **Shih-Chii Liu,** *University of Zurich and ETH Zurich, Switzerland*
12:25 PM	Lunch
1:25 PM	**Machine Learning for Event-Based Vision:** **from Low Power Pixels to Low Power Applications** **Amos Sironi,** *Prophesee, Paris, France*
2:15 PM	**In-Sensor and In-Memory Computing for Constrained Hardware** **for TinyML IoT Applications** **Kea-Tiong Tang,** *National Tsing Hua University, Hsinchu, Taiwan*
3:05 PM	Break
3:20 PM	**Nonvolatile Logic and Smart Nonvolatile Processors** **with CMOS/MTJ Hybrid Technology for IoT and AI (AIoT) Edge System** **Tetsuo Endoh,** *Tohoku University, Sendai, Japan*
4:10 PM	**How TensorFlow Enables the TinyML Ecosystem** **Raziel Alvarez,** *Google, Mountain View, CA*
5:00 PM	Concluding Remarks, **Dennis Sylvester,** *University of Michigan, Ann Arbor, MI*

EE1: Student Research Preview (SRP)

The Student Research Preview (SRP) will highlight selected student research projects in progress. The SRP consists of approximately 21 ninety-second presentations followed by a Poster Session, by graduate students from around the world, which have been selected on the basis of a short submission concerning their on-going research. Selection is based on the technical quality and innovation of the work. This year, the SRP will be presented in three theme sections: Machine Learning & Digital; Biomedical & Analog; Communications & RF.

The Student Research Preview will include an inspirational lecture by Professor Tadahiro Kuroda. The SRP begins at 7:30 pm on Sunday, February 16th. The SRP is open to all ISSCC registrants.

Co-Chair:	Denis Daly	Omni Design Technologies, Billerica, MA
Co-Chair:	Jerald Yoo	National University of Singapore, Singapore
Secretary:	Tinoosh Mohsenin	University of Maryland, Baltimore, MD
Advisor:	Anantha Chandrakasan	MIT, MA
Advisor:	Jan Van der Spiegel	University of Pennsylvania, PA
Media/Publications:	Laura Fujino	University of Toronto, Canada
A/V:	Trudy Stetzler	Halliburton, Houston,TX

Committee Members

Jason Anderson	University of Toronto, Canada
Masoud Babaie	Delft University of Technology, The Netherlands
Andrea Baschirotto	University of Milan-Bicocca, Italy
Hsin-Shu Chen	National Taiwan University, Taiwan
Hayun Chung	Korea University, Korea
Denis Daly	Omni Design Technologies, MA
Shidhartha Das	Arm, United Kingdom
Zeynep Deniz	IBM, NY
Hao Gao	Eindhoven University of Technology, The Netherlands
Minkyu Je	KAIST, Korea
Matthias Kuhl	Hamburg University of Technology, Germany
Seulki Lee	imec-Netherlands, The Netherlands
Yoonmyung Lee	SungKyunKwan University, Korea
Qiang Li	University of Electronic Science & Technology, China
Shih-Chii Liu	University of Zurich/ETH Zurich, Switzerland
Carolina Mora Lopez	IMEC, Belgium
Shahriar Mirabbasi	University of British Columbia, Canada
Tinoosh Mohsenin	University of Maryland, MD
Cormac O'Connell	TSMC, Kanata, Canada
Mondira Pant	Intel, MA
Negar Reiskarimian	MIT, MA
Jae-sun Seo	Arizona State University, AZ
Atsushi Shirane	Tokyo Institute of Technology, Japan
Yildiz Sinangil	Apple, CA
GuoXing Wang	Shanghai Jiao Tong University, China
Jeffrey Weldon	University of Hawaii, HI
Chia-Hsiang Yang	National Taiwan University, Taiwan
Rabia Tugce Yazicigil	Boston University, MA
Jerald Yoo	National University of Singapore, Singapore
Samira Zaliasl	Ferric, NY
Milin Zhang	Tsinghua University, Beijing, China

EE2: Rising Stars 2020 Workshop

Chair: Farhana Sheikh, Intel, Hillsboro, OR
Co-Chair: Rabia Yazicigil, Boston University, Boston, MA

Rising Stars 2020 Workshop Committee:
Zeynep Deniz, IBM
Dina R. El-Damak, University of Southern California
Q. Jane Gu, University of California, Davis
Ulkuhan Guler, Worcester Polytechnic Institute
Alicia Klinefelter, NVIDIA
Rikky Muller, University of California, Berkeley
Negar Reiskarimian, MIT
Yildiz Sinangil, Apple
Trudy Stetzler, Halliburton
Alice Wang, Everactive
Kathy Wilcox, AMD

Advisory Board:
Tsu-Jae K. Liu, U. C. Berkeley
Andrea Goldsmith, Stanford University
Anantha Chandrakasan, MIT

The IEEE SSCS Women in Circuits together with ISSCC will be sponsoring the first "Rising Stars 2020" for young professionals and students. The Rising Stars 2020 is an educational workshop for graduate and undergraduate students, and young professionals who have graduated within the last two years who are interested in learning how to excel at academic and industry careers in computer science, computer and electrical engineering. "*Rising to the Top in Industry*" career panel will touch upon topics such as mentoring, setting career goals, filing patents, management vs. technical tracks, and more. "*Navigating the Assistant Professorship*" will address applying for a faculty position, tenure review, and managing day-to-day life in academia. The panels are open to the all ISSCC 2020 attendees and the public. In addition to the panels, we will be selecting 20 rising stars in academia and industry to attend a special dinner, keynote from a high-profile already "Risen Star", and mentoring session.

Time	Rising Stars 2020
4:00 – 5:00 PM	Welcome, Introductions, Posters, Networking, and Photos
5:00 – 6:30 PM	Dinner, Keynote, and Mentoring
6:30 - 7:30 PM	Navigating the Assistant Professorship (Open to the public)
6:30 - 7:30 PM	Rising to the Top in Industry (Open to the Public)

4:00PM – 5:00PM
Welcome, Posters, and Networking

4:00PM – 5:10PM
Workshop Opening and Introduction
Farhana Sheikh, Intel and Rabia Yazicigil, Boston University

4:10PM – 4:30PM
Poster Introductions
Presented by Rising Stars

4:30PM – 5:00PM
Networking

Rising Stars 2020 Dinner, Keynote, and Mentoring

5:00PM – 5:30PM
Introductions and Dinner
Farhana Sheikh, Intel and Kathy Wilcox, AMD

5:30PM – 6:00PM
Rising Stars 2020 Workshop Dinner Keynote (closed to selected Rising Stars)
Speaker: Anantha Chandrakasan, MIT

6:00PM – 6:30PM
Rising Stars 2020 Workshop Mentoring Session (closed to selected Rising Stars)

6:30PM – 7:30PM
Navigating the Assistant Professorship - Academia Career Panel (open to the public)

Distinguished Panel Speaker:
"Words of Wisdom", Azita Emami, California Institute of Technology

The panel will provide perspectives from professors and rising stars in the academic field on the faculty application process, the necessary steps to increase your chances of being hired, and the requirements at the tenure review. The panel will provide participants with practical information and candid advice on seeking and interviewing for faculty jobs, networking, teaching, speaking, mentoring, funding research, setting up labs, getting tenure, and managing day-to-day life in academia.

Panel Moderators: Dina Reda El-Damak, University of Southern California
Q. Jane Gu, University of California, Davis

Panelists:
Vivienne Sze, MIT
Esther Rodriguez Villegas, Imperial College, London, UK
Jerald Yoo, National University of Singapore
Zhengya Zhang, University of Michigan
Milin Zhang, Tsinghua University

6:30PM – 7:30PM
Rising to the Top in Industry - Industry Career Panel (Open to the Public)

Distinguished Panel Speaker
"Words of Wisdom", Alice Wang, VP, Everactive

The industry career panel will tackle the question of how to become a rising star in the corporate world. Our diverse panelists bring their own experiences and perspectives from small startup organizations to large corporations, including corporate research labs. The panel will touch upon topics such as mentoring, setting career goals, deciding between management and technical tracks, publishing and filing patents, collaborating across diverse teams, and working effectively in a team. The goal is to provide the audience with the know-how to successfully navigate challenges in the corporate world, and rise to the top.

Panel Moderators: Alicia Klinefelter, NVIDIA
Zeynep Deniz, IBM

Panelists:
Wendy Belluomini, IBM
Mike Mulligan, Silicon Labs
Kazuko Nishimura, Panasonic
Walker Turner, NVIDIA
Laura Fick, Mythic AI

Plenary Session — Invited Papers

Chair: ***Jan van der Spiegel,*** *University of Pennsylvania, Philadelphia, PA*
ISSCC Conference Chair

Associate Chair: ***Un-Ku Moon,*** *Oregon State University, Corvallis, OR*
ISSCC International Technical Program Chair

FORMAL OPENING OF THE CONFERENCE **8:30 AM**

1.1 The Deep Learning Revolution and Its Implications for Computer Architecture and Chip Design — 8:45 AM

Jeff Dean, *Google, Mountain View, CA*

The past decade has seen a remarkable series of advances in machine learning, and in particular deep learning approaches based on artificial neural networks, to improve our abilities to build more accurate systems across a broad range of areas, including computer vision, speech recognition, language translation, and natural language understanding tasks. In this talk, I will highlight some of these advances, and their implications on the kinds of computational devices we need to build, especially in an era where general purpose computers are no longer improving their performance significantly year-over-year. I'll also discuss some of the ways that machine learning may also be able to help with some aspects of the circuit design process. Finally, I'll provide a sketch of at least one interesting direction towards much larger-scale multi-task models that are sparsely activated and employ much more dynamic, example- and task-based routing than the machine learning models of today.

1.2 Fertilizing AIoT from Roots to Leaves — 9:20 AM

Kou-Hung Lawrence Loh, *MediaTek, Hsinchu, Taiwan*

Artificial intelligence (AI) creates new opportunities for all kinds of "things" to interface with the universe in unprecedented ways. As IC technology advances, AI has evolved from traditional expert systems toward cognitive intelligence, which involves multidimensional perception, self-learning, decision-making, and interaction. Enabling cognitive AI in everything (AIoT) demands comprehensive circuit technologies to enhance the performance, power dissipation, and form factor of edge devices as well as cloud infrastructure, which forms the roots to support a variety of leaf-applications. The root-technologies are far ranging, including AI Processing Unit (APU), multi-processor computing, 5G, high-speed wireline communication between edge and the cloud, emerging storage technology, human-machine interfaces, and advanced SoC packages. These fundamental technologies enable intelligent applications spanning across mobile devices, smart home, automotive platform, and smart city. This talk will discuss the advancement of these root technologies that are driving the current transition from conventional ICs to AIoT. Through the discussion, technical innovations for Edge AI SoC and Cloud-Edge collaboration enabled by emerging wireless and wireline communication standards will be explored. To reach the vision of over 350 billion connected intelligent devices in 2030, the challenges and opportunities for our industry going forward will be summarized.

ISSCC, SSCS, IEEE AWARD PRESENTATIONS **9:55 AM**

BREAK **10:20 AM**

1.3 Future Scaling: Where Systems and Technology Meet 10:40 AM

Nadine Collaert, *imec, Leuven, Belgium*

In a smart society where everything will be connected, an avalanche of data is coming toward us, with numbers going to several hundreds of zettabytes per year by 2025. This data will need to be sent around, stored, computed and analyzed. At the heart of it all will be innovations at the technology and system level. With Moore's law under pressure, a rethinking of what the semiconductor industry calls scaling will be needed.

In this work, we will show the strong push to technology diversification, blending different technologies together to achieve benefits at the system level. This brings the interaction of technology and design to the next level: System-Technology co-optimization (STCO), with 3D technologies taking a central stage. Furthermore, the growing demand for storage will put an increasing pressure on the memory hierarchy where emerging concepts like MRAM, FeFET.... have the potential to bring new speed and capacity benefits. Next to that, memories like e.g. RRAM are getting a lot of traction for analog in-memory computing to enable energy efficient machine learning at the IoT edge. Finally, we will also briefly review the status of quantum computing, these days gaining a lot of interest as a path to ultra-powerful computing.

1.4 The Future of Computing: Bits + Neurons + Qubits 11:15 AM

Dario Gil, *IBM Thomas J. Watson Research Center, Yorktown Heights, NY*

The laptops, cell phones, and internet applications commonplace in our daily lives are all rooted in the idea of zeros and ones – in bits.

This foundational element originated from the combination of mathematics and Claude Shannon's Theory of Information. Coupled with the 50-year legacy of Moore's law, the bit has propelled the digitization of our world.

In recent years, artificial intelligence systems, merging neuron-inspired biology with information, have achieved superhuman accuracy in a range of narrow classification tasks by learning from labelled data. Advancing from narrow AI to broad AI will encompass the unification of learning and reasoning through neuro-symbolic systems, resulting in a form of AI which will perform multiple tasks, operate across multiple domains, and learn from small quantities of multi-modal input data.

Finally, the union of physics and information led to the emergence of Quantum Information Theory and the development of the quantum bit - the qubit - forming the basis of quantum computers. We have built the first programmable quantum computers, and although the technology is still in its early days, these systems offer the potential to solve problems which even the most powerful classical computers cannot.

The future of computing will look fundamentally different that it has in the past. It will not be based on more and cheaper bits alone, but rather, it will be built upon bits + neurons + qubits. This future will enable the next generation of intelligent mission critical systems and accelerate the rate of science-driven discovery.

PRESENTATION TO PLENARY SPEAKERS **11:50 AM**

CONCLUSION **11:55 AM**

Processors

Session Chair: ***Christopher Gonzalez,*** *IBM, Yorktown Heights, NY*
Session Co-Chair: ***Thomas Burd,*** *Advanced Micro Devices, Santa Clara, CA*

1:30 PM

2.1 Zen 2: The AMD 7nm Energy-Efficient High-Performance x86-64 Microprocessor Core

DS1

T. Singh[1], S. Rangarajan[1], D. John[1], R. Schreiber[1], S. Oliver[1], R. Seahra[2], A. Schaefer[1]
[1]AMD, Austin, TX; [2]AMD, Markham, ON, Canada

2:00 PM

2.2 AMD Chiplet Architecture for High-Performance Server and Desktop Products

S. Naffziger[1], K. Lepak[2], M. Paraschou[1], M. Subramony[2]
[1]AMD, Fort Collins, CO; [2]AMD, Austin, TX

2:30 PM

2.3 A 220GOPS 96-Core Processor with 6 Chiplets 3D-Stacked on an Active Interposer Offering 0.6ns/mm Latency, 3Tb/s/mm² Inter-Chiplet Interconnects and 156mW/mm² @ 82%-Peak-Efficiency DC-DC Converters

P. Vivet[1], E. Guthmuller[1], Y. Thonnart[1], G. Pillonnet[1], G. Moritz[1], I. Miro-Panadès[1], C. Fuguet[1], J. Durupt[1], C. Bernard[1], D. Varreau[1], J. Pontes[1], S. Thuries[1], D. Coriat[1], M. Harrand[1], D. Dutoit[1], D. Lattard[1], L. Arnaud[1], J. Charbonnier[1], P. Coudrain[1], A. Garnier[1], F. Berger[1], A. Gueugnot[1], A. Greiner[2], Q. Meunier[2], A. Farcy[3], A. Arriordaz[4], S. Cheramy[1], F. Clermidy[1]
[1]CEA-LETI-MINATEC, Grenoble, France; [2]Sorbonne University, Paris, France
[3]STMicroelectronics, Crolles, France; [4]Mentor, St. Ismier, France

Break 3:00 PM

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2.4 A 7nm High-Performance and Energy-Efficient Mobile Application Processor with Tri-Cluster CPUs and a Sparsity-Aware NPU

Y. D. Kim, W. Jeong, L. Jung, D. Shin, J. G. Song, J. Song, H. Kwon, J. Lee, J. Jung, M. Kang, J. Jeong, Y. Kwon, N. H. Seong, Samsung Electronics, Hwaseong, Korea

3:45 PM

2.5 A 7nm FinFET 2.5GHz/2.0GHz Dual-Gear Octa-Core CPU Subsystem with Power/Performance Enhancements for a Fully Integrated 5G Smartphone SoC

H. Mair[1], E. Wang[2], A. Nayak[1], R. Lagerquist[1], L. Chou[2], G. Gammie[1], H. Chen[1], L-K. Yong[1], M. Rahman[1], J. Wiedemeier[1], R. Madhavaram[1], A. Chiou[2], B. Li[2], V. Lin[2], R. Huang[2], M. Yang[2], A. Thippana[1], O. Su[2], S. Huang[2], [1]MediaTek, Austin, TX; [2]MediaTek, Hsinchu, Taiwan

4:15 PM

2.6 A 16nm 3.5B Transistor >14TOPS 2-to-10W Multicore SoC Platform for Automotive and Embedded Applications with Integrated Safety MCU, 512b Vector VLIW DSP, Embedded Vision and Imaging Acceleration

R. Venkatasubramanian[1], D. Steiss[1], G. Shurtz[2], T. Anderson[1], K. Chirca[1], R. Santhanagopal[1], N. Nandan[1], A. Reghunath[1], H. Sanghvi[1], D. Wu[1], A. Chachad[1], B. Karguth[1], D. Beaudoin[1], C. Fuoco[1], L. Nardini[1], C. Hu[1], S. Visalli[1], A. Mundra[1], D. Varadarajan[1], F. Cano[2], S. Stelmach[1], M. Mody[3], A. Redfern[1], H. Bilhan[1], M. Sarraj[1], A. Siddiki[1], A. Lell[1], E. Falik[1], A. Hill[1], A. Armstrong[1], T. Beck[1], V. Kanumuri[1], S. Mullinnix[1], D. Moore[1], J. Jones[2], M. Koul[1], S. Agarwala[1]
[1]Texas Instruments, Dallas, TX; [2]Texas Instruments, Houston, TX
[3]Texas Instruments, Bangalore, India

4:45 PM

2.7 IBM z15: A 12-Core 5.2GHz Microprocessor

C. Berry[1], B. Bell[2], A. Jatkowski[1], J. Surprise[1], J. Isakson[3], O. Geva[1], B. Deskin[4], M. Cichanowski[3], D. Hamid[1], C. Cavitt[1], G. Fredeman[1], A. Saporito[1], A. Mishra[5], A. Buyuktosunoglu[6], T. Webel[7], P. Lobo[5], P. Parashurama[5], R. Bertran[8], D. Chidambarrao[9], D. Wolpert[1], B. Bruen[1]
[1]IBM Systems and Technology, Poughkeepsie, NY; [2]IBM Systems and Technology, Rochester, NY
[3]IBM Systems and Technology, Austin, TX; [4]IBM Systems and Technology, Endicott, NY
[5]IBM Systems and Technology, Bangalore, India
[6]IBM T. J. Watson Reseach Center, Yorktown Heights, NY
[7]IBM Systems and Technology, Boeblingen, Germany
[8]IBM Systems and Technology, Yorktown Heights, NY
[9]IBM Systems and Technology, Hopewell Junction, NY

Conclusion 5:15 PM

Analog Techniques I

Session Chair: ***Youngcheol Chae,*** *Yonsei University, Seoul, Korea*
Session Co-Chair: ***Michael Perrott,*** *Texas Instruments, Manchester, NH*

1:30 PM

3.1 An Integrated BAW Oscillator with <±30ppm Frequency Stability Over Temperature, Package Stress, and Aging Suitable for High-Volume Production DS1

D. Griffith[1], E. T-T. Yen[2], K. Tsai[1], H. U. R. Mohammed[1], B. Haroun[1], A. Kiaei[2], A. Bahai[2]
[1]Texas Instruments, Dallas, TX; [2]Texas Instruments, Santa Clara, CA

2:00 PM

3.2 A 0.0088mm² Resistor-Based Temperature Sensor Achieving 92fJ·K² FoM in 65nm CMOS

A. Khashaba, J. Zhu, A. Elmallah, M. Ahmed, P. Hanumolu
University of Illinois, Urbana, IL

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3.3 A 0.51nW 32kHz Crystal Oscillator Achieving 2ppb Allan Deviation Floor Using High-Energy-to-Noise-Ratio Pulse Injection DS1

L. Xu[1], T. Jang[2], J. Lim[1], K. Choo[1], D. Blaauw[1], D. Sylvester[1]
[1]University of Michigan, Ann Arbor, MI; [2]ETH Zürich, Zürich, Switzerland

Break 3:00 PM

3:15 PM

3.4 A 16MHz CMOS RC Frequency Reference with ±400ppm Inaccuracy from -45°C to 85°C after Digital Linear Temperature Compensation

Ç. Gürleyük, S. Pan, K.A.A. Makinwa
Delft University of Technology, Delft, The Netherlands

3:45 PM

3.5 A 34µW 32MHz RC Oscillator with ±530ppm Inaccuracy from -40°C to 85°C and 80ppm/V Supply Sensitivity Enabled by Pulse-Density Modulated Resistors

A. Khashaba, J. Zhu, M. Ahmed, N. Pal, P. K. Hanumolu
University of Illinois, Urbana, IL

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3.6 A CMOS Resistor-Based Temperature Sensor with a 10fJ·K² Resolution FoM and 0.4°C (3σ) Inaccuracy From –55°C to 125°C After a 1-point Trim

S. Pan, K.A.A. Makinwa, Delft University of Technology, Delft, The Netherlands

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3.7 A 620µW BJT-Based Temperature-to-Digital Converter with 0.65mK Resolution and FoM of 190fJ·K²

S. Heidary Shalmany[1], K. Souri[1], U. Sonmez[1], K. Souri[2], M. D'Urbino[1], S. Hussaini[1], D. Tauro[2], S. Tabatabaei[2]
[1]SiTime, Delft, The Netherlands; [2]SiTime, Santa Clara, CA

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3.8 A 23.6ppm/°C Monolithically Integrated GaN Reference Voltage Design with Temperature Range from -50°C to 200°C and Supply Voltage Range from 3.9 to 24V

C-H. Liao[1], S-H. Yang[1], M-Y. Liao[1], K-C. Chung[1], N. Kumari[1], K-H. Chen[1], Y-H. Lin[2], S-R. Lin[3], T-Y. Tsai[2], Y-Z. Juang[4]
[1]National Chiao Tung University, Hsinchu, Taiwan
[2]Realtek Semiconductor, Hsinchu, Taiwan
[3]Realtek Semiconductor, Hsinchu City, Taiwan
[4]Taiwan Semiconductor Research Institute (TSRI), Hsinchu, Taiwan

Conclusion 5:15 PM

mm-Wave Wireless for Communication & Radar

Session Chair: ***Matteo Bassi,*** *Infineon Technologies Austria AG, Villach, Austria*
Session Co-Chair: ***Vito Giannini,*** *Uhnder, Austin, TX*

1:30 PM

4.1 A 39GHz-Band CMOS 16-Channel Phased-Array Transceiver IC with a Companion Dual-Stream IF Transceiver IC for 5G NR Base-Station Applications

H-C. Park, D. Kang, S. M. Lee, B. Park, K. Kim, J. Lee, Y. Aoki, Y. Yoon, S. Lee, D. Lee, D. Kwon, S. Kim, J. Kim, W. Lee, C. Kim, S. Park, J. Park, B. Suh, J. Jang, M. Kim, D. Minn, I. Park, S. Kim, K. Min, J. Park, S. Jeon, A-S. Ryu, Y. Cho, S. T. Choi, K. H. An, Y. Kim, J. H. Lee, J. Son, S-G. Yang, Samsung Electronics, Suwon, Korea

2:00 PM

4.2 An E-Band High-Linearity Antenna-LNA Front-End with 4.8dB NF and 2.2dBm IIP3 Exploiting Multi-Feed On-Antenna Noise-Canceling and G_m-Boosting

S. Li[1], T. Chi[2], D. Jung[1], T-Y. Huang[1], M-Y. Huang[1], H. Wang[1]
[1]Georgia Institute of Technology, Atlanta, GA; [2]Rice University, Houston, TX

2:30 PM

4.3 A 28GHz 4-Element MIMO Beam-Space Array in 65nm CMOS with Simultaneous Spatial Filtering and Single-Wire Frequency-Domain Multiplexing

R. Garg[1], G. Sharma[1], A. Binaie*[2], S. Jain*[1], S. Ahasan*[2], A. Dascurcu[2], H. Krishnaswamy[2], A. Natarajan[1]*
*Equally-Credited Authors (ECAs), [1]Oregon State University, Corvallis, OR
[2]Columbia University, New York, NY

2:45 PM

4.4 A 28/37GHz Scalable, Reconfigurable Multi-Layer Hybrid/Digital MIMO Transceiver for TDD/FDD and Full-Duplex Communication

S. Mondal, L. R. Carley, J. Paramesh, Carnegie Mellon University, Pittsburgh, PA

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4.5 A 64Gb/s 1.4pJ/b/element 60GHz 2×2-Element Phased-Array Receiver with 8b/symbol Polarization MIMO and Spatial Interference Tolerance

A. Chakrabarti, C. Thakkar, S. Yamada, D. Choudhury, J. Jaussi, B. Casper
Intel, Hillsboro, OR

3:45 PM

4.6 Space-Time Modulated 71-to-76GHz mm-Wave Transmitter Array for Physically Secure Directional Wireless Links

X. Lu[1], S. Venkatesh*[1], B. Tang[2], K. Sengupta[1],* *Equally-Credited Authors (ECAs)
[1]Princeton University, Princeton, NJ; [2]Xi'an Jiaotong University, Xi'an, China

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4.7 A Single-Antenna W-Band FMCW Radar Front-End Utilizing Adaptive Leakage Cancellation DS1

M. Kalantari[1,2], H. Shirinabadi[3], A. Fotowat-Ahmadi[2], C. P. Yue[1]
[1]Hong Kong University of Science and Technology, Hong Kong, China
[2]Sharif University of Technology, Tehran, Iran; [3]University of California, Berkeley, CA

4:45 PM

4.8 A Terahertz FMCW Comb Radar in 65nm CMOS with 100GHz Bandwidth DS1

X. Yi[1], C. Wang[1], M. Lu[1], J. Wang[1], J. Grajal[1,2], R. Han[1]
[1]Massachusetts Institute of Technology, Cambridge, MA
[2]Universidad Politécnica de Madrid, Madrid, Spain

Conclusion 5:15 PM

Imagers and ToF Sensors

Session Chair: ***Seong-Jin Kim,*** *Ulsan National Institute of Science and Technology, Ulsan, Korea*
Session Co-Chair: ***Hayato Wakabayashi,*** *Sony Semiconductor Solutions, Atsugi, Japan*

1:30 PM

5.1 DS1 A 240×192Pixel 10fps 70klux 225m-Range Automotive LiDAR SoC Using a 40ch 0.0036mm² Voltage/Time Dual-Data-Converter-Based AFE
S. Kondo[1], H. Kubota[2], H. Katagiri[2], Y. Ota[2], M. Hirono[3], T. T. Ta[1], H. Okuni[1], S. Ohtsuka[2], Y. Ojima[2], T. Sugimoto[2], H. Ishii[2], K. Yoshioka[1], K. Kimura[2], A. Sai[1], N. Matsumoto[2], [1]Toshiba, Kawasaki, Japan [2]Toshiba Electronic Devices & Storage, Kawasaki, Japan; [3]Toshiba, Yokohama, Japan

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5.2 DS1 A 1200×900 6µm 450fps Geiger-Mode Vertical Avalanche Photodiodes CMOS Image Sensor for a 250m Time-of-Flight Ranging System Using Direct-Indirect-Mixed Frame Synthesis with Configurable-Depth-Resolution Down to 10cm
T. Okino, S. Yamada, Y. Sakata, S. Kasuga, M. Takemoto, Y. Nose, H. Koshida, M. Tamaru, Y. Sugiura, S. Saito, S. Koyama, M. Mori, Y. Hirose, M. Sawada, A. Odagawa, T. Tanaka
Panasonic, Nagaokakyo, Japan

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5.3 DS1 An Up-to-1400nm 500MHz Demodulated Time-of-Flight Image Sensor on a Ge-on-Si Platform
C-L. Chen, S-W. Chu*, B-J. Chen*, Y-F. Lyu*, K-C. Hsu*, C-F. Liang*, S-S. Su, M-J. Yang, C-Y. Chen, S-L. Cheng, H-D. Liu, C-T. Lin, K. P. Petrov, H-W. Chen, K-C. Chu, P-C. Wu, P-T. Huang, N. Na, S-L. Chen,* *Equally-Credited Authors (ECAs), Artilux, Hsinchu, Taiwan

2:30 PM

5.4 DS1 A Dynamic Pseudo 4-Tap CMOS Time-of-Flight Image Sensor with Motion Artifact Suppression and Background Light Cancelling Over 120klux
D. Kim[1], S. Lee[2], D. Park[2], C. Piao[1], J. Park[1], Y. Ahn[1], K. Cho[1], J. Shin[3], S. M. Song[3], S-J. Kim[2], J-H. Chun[1], J. Choi[1], [1]Sungkyunkwan University, Suwon, Korea
[2]Ulsan National Institute of Science and Technology, Ulsan, Korea; [3]Zeeann, Hanam, Korea

Break 3:00 PM

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5.5 A 2.1e⁻ Temporal Noise and -105dB Parasitic Light Sensitivity Backside-Illuminated 2.3µm-Pixel Voltage-Domain Global Shutter CMOS Image Sensor Using High-Capacity DRAM Capacitor Technology
J-K. Lee, S. S. Kim, I-G. Baek, H. Shim, T. Kim, T. Kim, J. Kyoung, D. Im, J. Choi, K. Cho, D. Kim, H. Lim, M-W. Seo, J. Kim, D. Kwon, J. Song, J. Kim, M. Jang, J. Moon, H. Kim, C. K. Chang, J. Kim, K. Koh, H. Lim, J. Ahn, H. Hong, K. Lee, H-K. Kang, Samsung Electronics, Hwaseong, Korea

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5.6 A 1/2.65in 44Mpixel CMOS Image Sensor with 0.7µm Pixels Fabricated in Advanced Full-Depth Deep-Trench Isolation Technology
H. Kim, J. Park, I. Joe, D. Kwon, J. H. Kim, D. Cho, T. Lee, C. Lee, H. Park, S. Hong, C. Chang, J. Kim, H. Lim, Y. Oh, Y. Kim, S. Nah, S. Jung, J. Lee, J. Ahn, H. Hong, K. Lee, H-K. Kang
Samsung Electronics, Hwaseong, Korea

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5.7 A 132dB Single-Exposure-Dynamic-Range CMOS Image Sensor with High Temperature Tolerance
Y. Sakano[1], T. Toyoshima[1], R. Nakamura[1], T. Asatsuma[1], Y. Hattori[1], T. Yamanaka[2], R. Yoshikawa[2], N. Kawazu[1], T. Matsuura[1], T. Iinuma[1], T. Toya[1], T. Watanabe[2], A. Suzuki[1], Y. Motohashi[1], J. Azami[1], Y. Tateshita[1], T. Haruta[1], [1]Sony Semiconductor Solutions, Atsugi, Japan
[2]Sony Semiconductor Manufacturing, Kikuyo, Japan

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5.8 A 0.50e^-_{rms} Noise 1.45µm-Pitch CMOS Image Sensor with Reference-Shared In-Pixel Differential Amplifier at 8.3Mpixel 35fps
M. Sato, Y. Yorikado, Y. Matsumura, H. Naganuma, E. Kato, T. Toyofuku, A. Kato, Y. Oike
Sony Semiconductor Solutions, Atsugi, Japan

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5.9 A 0.8V Multimode Vision Sensor for Motion and Saliency Detection with Ping-Pong PWM Pixel
T-H. Hsu, Y-K. Chen*, J-S. Wu, W-C. Ting, C-T. Wang, C-F. Yeh, S-H. Sie, Y-R. Chen, R-S. Liu, C-C. Lo, K-T. Tang, M-F. Chang, C-C. Hsieh,* *Equally-Credited Authors (ECAs)
National Tsing Hua University, Hsinchu, Taiwan

4:45 PM

5.10 DS1 A 1280×720 Back-Illuminated Stacked Temporal Contrast Event-Based Vision Sensor with 4.86µm Pixels, 1.066GEPS Readout, Programmable Event-Rate Controller and Compressive Data-Formatting Pipeline
T. Finateu[1], A. Niwa[2], D. Matolin[1], K. Tsuchimoto[2], A. Mascheroni[1], E. Reynaud[1], P. Mostafalu[3], F. Brady[3], L. Chotard[1], F. LeGoff[1], H. Takahashi[2], H. Wakabayashi[2], Y. Oike[2], C. Posch[1]
[1]PROPHESEE, Paris, France [2]Sony Semiconductor Solutions, Atsugi, Japan
[3]Sony Electronics, Rochester, NY

Conclusion 5:15 PM

Ultra-High-Speed Wireline

Session Chair: ***Amir Amirkhany,*** *Samsung Electronics, San Jose, CA*
Session Co-Chair: ***Andrew Joy,*** *Marvell, Northampton, United Kingdom*

1:30 PM

6.1 DS1 A 112Gb/s PAM-4 Long-Reach Wireline Transceiver Using a 36-Way Time-Interleaved SAR-ADC and Inverter-Based RX Analog Front-End in 7nm FinFET

J. Im[1], K. Zheng[1], A. Chou[1], L. Zhou[1], J. W. Kim[1], S. Chen[1], Y. Wang[2], H-W. Hung[2], K. Tan[2], W. Lin[1], A. Roldan[1], D. Carey[3], I. Chlis[3], R. Casey[3], A. Bekele[1], Y. Cao[1], D. Mahashin[1], H. Ahn[1], H. Zhang[1], Y. Frans[1], K. Chang[1]
[1]Xilinx, San Jose, CA; [2]Xilinx, Singapore; [3]Xilinx, Cork, Ireland

2:00 PM

6.2 DS1 A 460mW 112Gb/s DSP-Based Transceiver with 38dB Loss Compensation for Next-Generation Data Centers in 7nm FinFET Technology

T. Ali[1], E. Chen*[1], H. Park*[1], R. Yousry*[1], Y-M. Ying[1], M. Abdullatif[1], M. Gandara[1], C-C. Liu[2], P-S. Weng[2], H-S. Chen[2], M. Elbadry[1], Q. Nehal[1], K-H. Tsai[2], K. Tan[2], Y-C. Huang[2], C-H. Tsai[2], Y. Chang[2], Y-H. Tung[2,]*
*Equally-Credited Authors (ECAs), [1]MediaTek, Irvine, CA; [2]MediaTek, Hsinchu, Taiwan

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6.3 DS1 A 10-to-112Gb/s DSP-DAC-Based Transmitter with 1.2V_{ppd} Output Swing in 7nm FinFET

E. Groen[1], C. Boecker[1], M. Hossain[2], R. Vu[1], S. Vamvakos[1], H. Lin[1], S. Li[1], M. van Ierssel[3], P. Choudhary[1], N. Wang[1], M. Shibata[3], M. H. Taghavi[3], N. Nguyen[1,4], S. Desai[1]
[1]Rambus, Sunnyvale, CA; [2]University of Alberta, Edmonton, Canada
[3]Rambus, Toronto, Canada; [4]San Jose State University, San Jose

Break 3:00 PM

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6.4 A 56Gb/s 7.7mW/Gb/s PAM-4 Wireline Transceiver in 10nm FinFET Using MM-CDR-Based ADC Timing Skew Control and Low-Power DSP with Approximate Multiplier

B-J. Yoo, D-H. Lim, H. Pang, J-H. Lee, S-Y. Baek, N. Kim, D-H. Choi, Y-H. Choi, H. Yang, T. Yoon, S-H. Chu, K. Kim, W. Jung, B-K. Kim, J. Lee, G. Kang, S-H. Park, M. Choi, J. Shin, Samsung Electronics, Hwaseong, Korea

3:45 PM

6.5 A 6.4-to-32Gb/s 0.96pJ/b Referenceless CDR Employing ML-Inspired Stochastic Phase-Frequency Detection Technique in 40nm CMOS

K. Park, M. Shim, H-G. Ko, D-K. Jeong, Seoul National University, Seoul, Korea

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6.6 Reference-Noise Compensation Scheme for Single-Ended Package-to-Package Links

X. Chen[1], N. Nedovic[1], S. G. Tell[2], S. S. Kudva[1], B. Zimmer[1], T. H. Greer[2], J. W. Poulton[2], S. Song[1], W. J. Turner[2], J. M. Wilson[2], C. T. Gray[2]
[1]NVIDIA, Santa Clara, CA; [2]NVIDIA, Durham, NC

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6.7 An 8Gb/s/μm FFE-Combined Crosstalk-Cancellation Scheme for HBM on Silicon Interposer with 3D-Staggered Channels

H-G. Ko, S. Shin, J. Oh, K. Park, D-K. Jeong, Seoul National University, Seoul, Korea

5:00 PM

6.8 A 100Gb/s NRZ Transmitter with 8-Tap FFE Using a 7b DAC in 40nm CMOS

P-J. Peng[1], S-T. Lai[1], W-H. Wang[1], C-W. Lin[1], W-C. Huang[1], T. Shih[2]
[1]Yuan Ze University, Taoyuan, Taiwan; [2]Teletrx, Taipei, Taiwan

Conclusion 5:15 PM

Demonstration Session 1, Monday February 17th, 5:00-7:00 PM

This year, the Demonstration Session extending in selected regular papers, both Academic and Industrial, will take place on Monday February 17th, and Tuesday February 18th, from 5 pm until 7 pm in the Golden Gate Hall. These demonstrations will feature real-life applications made possible by new ICs presented at ISSCC 2020, as noted by the symbol **DS1**

2.1 Zen 2: The AMD 7nm Energy-Efficient High-Performance x86-64 Microprocessor Core

3.1 An Integrated BAW Oscillator with <±30ppm Frequency Stability Over Temperature, Package Stress, and Aging Suitable for High-Volume Production

3.3 A 0.51nW 32kHz Crystal Oscillator Achieving 2ppb Allan Deviation Floor Using High-Energy-to-Noise-Ratio Pulse Injection

4.7 A Single-Antenna W-Band FMCW Radar Front-End Utilizing Adaptive Leakage Cancellation

4.8 A Terahertz FMCW Comb Radar in 65nm CMOS with 100GHz Bandwidth

5.1 A 240×192Pixel 10fps 70klux 225m-Range Automotive LiDAR SoC Using a 40ch 0.0036mm² Voltage/Time Dual-Data-Converter-Based AFE

5.2 A 1200×900 6µm 450fps Geiger-Mode Vertical Avalanche Photodiodes CMOS Image Sensor for a 250m Time-of-Flight Ranging System Using Direct-Indirect-Mixed Frame Synthesis with Configurable-Depth-Resolution Down to 10cm

5.3 An Up-to-1400nm 500MHz Demodulated Time-of-Flight Image Sensor on a Ge-on-Si Platform

5.4 A Dynamic Pseudo 4-Tap CMOS Time-of-Flight Image Sensor with Motion Artifact Suppression and Background Light Cancelling Over 120klux

5.10 A 1280×720 Back-Illuminated Stacked Temporal Contrast Event-Based Vision Sensor with 4.86µm Pixels, 1.066GEPS Readout, Programmable Event-Rate Controller and Compressive Data-Formatting Pipeline

6.1 A 112Gb/s PAM-4 Long-Reach Wireline Transceiver Using a 36-Way Time-Interleaved SAR-ADC and Inverter-Based RX Analog Front-End in 7nm FinFET

6.2 A 460mW 112Gb/s DSP-Based Transceiver with 38dB Loss Compensation for Next-Generation Data Centers in 7nm FinFET Technology

6.3 A 10-to-112Gb/s DSP-DAC-Based Transmitter with 1.2V_{ppd} Output Swing in 7nm FinFET

24.6 An Instantaneously Broadband Ultra-Compact Highly Linear PA with Compensated Distributed-Balun Output Network Achieving >17.8dBm P_{1dB} and >36.6% PAE_{P1dB} over 24 to 40GHz and Continuously Supporting 64-/256-QAM 5G NR Signals over 24 to 42GHz

28.3 A 5.2Mpixel 88.4dB-DR 12in CMOS X-Ray Detector with 16b Column-Parallel Continuous-Time ΔΣ ADCs

28.4 A CMOS Multimodality In-Pixel Electrochemical and Impedance Cellular Sensing Array for Massively Paralleled Synthetic Exoelectrogen Characterization

29.3 Non-Magnetic 0.18µm SOI Circulator with Multi-Watt Power Handling Based on Switched-Capacitor Clock Boosting

29.5 Sub-THz CMOS Molecular Clock with 43ppt Long-Term Stability Using High-Order Rotational Transition Probing and Slot-Array Couplers

30.3 A SAW-Less NB-IoT RF Transceiver with Hybrid Polar and On-Chip Switching PA Supporting Power Class 3 Multi-Tone Transmission

30.6 A Low-Power BLE Transceiver with Support for Phase-Based Ranging, Featuring 5µs PLL Locking Time and 5.3ms Ranging Time, Enabled by Staircase-Chirp PLL with Sticky-Lock Channel-Switching

34.1 A 64×64 Implantable Real-Time Single-Charged-Particle Radiation Detector for Cancer Therapy

34.2 1225-Channel Localized Temperature-Regulated Neuromorphic Retinal-Prosthesis SoC with 56.3nW/Channel Image Processor

34.6 EEG Dust: A BCC-Based Wireless Concurrent Recording/Transmitting Concentric Electrode

EE3: Industry Showcase

Session Chair: ***Kush Gulati,*** *Omni Design, Milpitas, CA*
Session Co-Chair: ***Alice Wang,*** *Everactive, Santa Clara, CA*

Industry Showcase Committee:

Matteo Bassi, *Infineon Technologies AG, Villach, Austria*
Tom Burd, *Advanced Micro Devices, Santa Clara, CA*
Alison Burdett, *Sensium Healthcare, Oxford, United Kingdom*
Vivek De, *Intel, Hillsboro, OR*
Yohan Frans, *Xilinx, San Jose, CA*
Nagendra Krishnapura, *Indian Institute of Technology, Chennai, India*
Sonia Leon, *Intel, Santa Clara, CA*
Yan Li, *Western Digital, Milpitas, CA*
Patrick Mercier, *University of California, San Diego, CA*
James Myers, *ARM, Cambridge, United Kingdom*
Mijung Noh, *Samsung Electronics, Gyeonggi-do, Korea*
Phillip Restle, *IBM T.J. Watson, Yorktown Heights, NY*
Naveen Verma, *Princeton University, Princeton, NJ*
Long Yan, *Samsung Electronics, Gyeonggi-do, Korea*
Wookyeong Jeong, *Samsung Electronics, Gyeonggi-do, Korea*

ISSCC will hold a plenary Industry Showcase event on the evening of Monday, February 17th, which will highlight how advances in silicon circuits, SoCs and systems are fueling the most innovative industrial applications and products of the future. Following the recognized role of ISSCC as the foremost global forum for advances in solid-state circuits and systems-on-chip (SoCs), the goal of this event will be to highlight the role of silicon in the creation of novel products. It will feature short presentations as well as interactive demonstrations where attendees can have a hands-on experience with each featured innovation. The featured presentations were chosen through a nomination and voting process by members of the Industry Showcase Committee and represent an exciting introduction to the next generation of applications and products enabled by the sustained evolution of solid-state integrated circuits.

Amongst those participating will be:

- **Intel** *(Lakefield: Hybrid Computing with 3D silicon integration)*
- **Wiliot** *(Low-Cost Bluetooth Based Sensor Tags for IoT)*
- **IBM** *(IBM Z15 – A 12 Core 5.2GHz Microprocessor)*
- **Butterfly Network** *(Handheld Whole-Body Imager with Ultrasound-on-Chip)*
- **Weebit Nano** *(Spiking Neural Network using ReRAM)*
- **Samsung Semiconductor** *(Motion-resilient VGA Time-of-Flight Image Sensor)*
- **Samsung Electronics**
  (A 1/1.33-inch 108MP CMOS Image Sensor with 0.8μm Unit Pixels)
- **Samsung Electronics**
  (A Blocker-Tolerant Direct Sampling Receiver for Wireless Multi-Channel Communication)
- **Ferric** *(Fully Programmable Power Converter Chiplet using Ferric Integrated Inductors)*
- **Texas Instruments**
  (Camera Based Perception and 3D Surround View for Autonomous Valet Parking on a 16nm Automotive SoC)
- **Advanced Micro Devices**
  (AMD Radeon RX5700 Graphics Power and Performance Demonstration)
- **Western Digital Research**
  (A Vehicle Security Surveillance Based on Artificial Intelligence of Things (AIoT))
- **MediaTek**
  (A Dual Core Deep Learning Accelerator for Versatile AI Applications in a 7nm 5G Smartphone SoC)
- **Alibaba** *(Hanguang 800, a High Throughput AI Inference Chip)*

High-Performance Machine Learning

Session Chair: ***Geoffrey Burr,*** *IBM Research Almaden, San Jose, CA*
Session Co-Chair: ***Yan Li,*** *Western Digital, Milpitas, CA*

8:30 AM

7.1 A 3.4-to-13.3TOPS/W 3.6TOPS Dual-Core Deep-Learning Accelerator for Versatile AI Applications in 7nm 5G Smartphone SoC

C-H. Lin, C-C. Cheng, Y-M. Tsai, S-J. Hung, Y-T. Kuo, P. H. Wang, P-K. Tsung, J-Y. Hsu, W-C. Lai, C-H. Liu, S-Y. Wang, C-H. Kuo, C-Y. Chang, M-H. Lee, T-Y. Lin, C-C. Chen
MediaTek, Hsinchu, Taiwan

9:00 AM

7.2 A 12nm Programmable Convolution-Efficient Neural-Processing-Unit Chip Achieving 825TOPS

Y. Jiao[1], L. Han[1], R. Jin[2], Y-J. Su[1], C. Ho[1], L. Yin[3], Y. Li[1], L. Chen[1], Z. Chen[1], L. Liu[3], Z. He[3], Y. Yan[3], J. He[3], J. Mao[3], X. Zai[3], X. Wu[3], Y. Zhou[3], M. Gu[1], G. Zhu[1], R. Zhong[1], W. Lee[1], P. Chen[1], Y. Chen[1], W. Li[3], D. Xiao[3], Q. Yan[3], M. Zhuang[3], J. Chen[3], Y. Tian[3], Y. Lin[3], W. Wu[3], H. Li[4], Z. Dou[4]
[1]Alibaba, Sunnyvale, CA
[2]Alibaba, Seattle, WA
[3]Alibaba, Shanghai, China
[4]Alibaba, Hangzhou, China

9:15 AM

7.3 DS2 STATICA: A 512-Spin 0.25M-Weight Full-Digital Annealing Processor with a Near-Memory All-Spin-Updates-at-Once Architecture for Combinatorial Optimization with Complete Spin-Spin Interactions

K. Yamamoto[1,2], K. Ando[1], N. Mertig[3], T. Takemoto[3], M. Yamaoka[3], H. Teramoto[2], A. Sakai[2], S. Takamaeda-Yamazaki[4], M. Motomura[1]
[1]Tokyo Institute of Technology, Yokohama, Japan
[2]Hokkaido University, Sapporo, Japan
[3]Hitachi, Sapporo, Japan
[4]University of Tokyo, Tokyo, Japan

9:30 AM

7.4 DS2 GANPU: A 135TFLOPS/W Multi-DNN Training Processor for GANs with Speculative Dual-Sparsity Exploitation

S. Kang, D. Han, J. Lee, D. Im, S. Kim, S. Kim, H-J. Yoo
KAIST, Daejeon, Korea

Break 10:00 AM

Highlighted Chip Releases

Session Chair: ***Alice Wang,*** *Everactive, Santa Clara, CA*
Session Co-Chair: ***Kush Gulati,*** *Omni Design Technologies, Milpitas, CA*

10:15 AM

8.1 Lakefield and Mobility Compute: A 3D Stacked 10nm and 22FFL Hybrid Processor System in 12×12mm², 1mm Package-on-Package

W. Gomes[1], S. Khushu[2], D. B. Ingerly[1], P. N. Stover[3], N. I. Chowdhury[1], F. O'Mahony[1], A. Balankutty[1], N. Dolev[3], M. G. Dixon[1], L. Jiang[1], S. Prekke[4], B. Patra[4], P. V. Rott[1], R. Kumar[1]
[1]Intel, Hillsboro, OR
[2]Intel, Santa Clara, CA
[3]Intel, Chandler, AZ
[4]Intel, Bangalore, India

10:45 AM

8.2 A Versatile 7nm Adaptive Compute Acceleration Platform Processor

P. K. Raha, T. Knopp, S. Ahmad, A. Ansari, F-H. Ho, T. To, V. Nalluri, M. Sarmah, R. Patwari
Xilinx, San Jose, CA

11:15 AM

8.3 A 3GHz ARM Neoverse N1 CPU in 7nm FinFET for Infrastructure Applications

R. Christy[1], S. Riches[2], S. Kottekkat[3], P. Gopinath[4], K. Sawant[3], A. Kona[1], R. Harrison[3]
[1]ARM, Austin, TX
[2]ARM, Cambridge, United Kingdom
[3]ARM, Sheffield, United Kingdom
[4]ARM, Bangalore, India

11:45 AM

8.4 Radeon RX 5700 Series: The AMD 7nm Energy-Efficient High-Performance GPUs

S. Dasgupta[1], T. Singh[2], A. Jain[2], S. Naffziger[3], D. John[2], C. Bisht[4], P. Jayaraman[1]
[1]AMD, Santa Clara, CA
[2]AMD, Austin, TX
[3]AMD, Fort Collins, CO
[4]AMD, Orlando, FL

Conclusion 12:15 PM

Noise-Shaping ADCs

Session Chair: ***Dominique Morche,*** *CEA-LETI, Grenoble, France*
Session Co-Chair: ***Yun Chiu,*** *University of Texas at Dallas, Richardson, TX*

8:30 AM

9.1 A Current-Sensing Front-End Realized by A Continuous-Time DS2 Incremental ADC with 12b SAR Quantizer and Reset-Then-Open Resistive DAC Achieving 140dB DR and 8ppm INL at 4kS/s
S-H. Wu, Y-S. Shu*, A. Y-C. Chiou, W-H. Huang, Z-X. Chen, H-Y. Hsieh*
*Equally-Credited Authors (ECAs)
MediaTek, Hsinchu, Taiwan

9:00 AM

9.2 A 134µW 24kHz-BW 103.5dB-DR CT ΔΣ Modulator with Chopped Negative-R and Tri-Level FIR DAC
M. Jang, C. Lee, Y. Chae, Yonsei University, Seoul, Korea

9:30 AM

9.3 A 40kHz-BW 90dB-SNDR Noise-Shaping SAR with 4× Passive Gain and 2nd-Order Mismatch Error Shaping
J. Liu[1], X. Wang[1], Z. Gao[1], M. Zhan[1], X. Tang[2], N. Sun[2]
[1]Tsinghua University, Beijing, China; [2]University of Texas, Austin, TX

Break 10:00 AM

10:15 AM

9.4 A 4th-Order Cascaded-Noise-Shaping SAR ADC with 88dB SNDR Over 100kHz Bandwidth
L. Jie, B. Zheng, H-W. Chen, R. Wang, M. P. Flynn
University of Michigan, Ann Arbor, MI

10:45 AM

9.5 A 13.5b-ENOB Second-Order Noise-Shaping SAR with PVT-Robust Closed-Loop Dynamic Amplifier
X. Tang[1], X. Yang[1], W. Zhao[1], C-K. Hsu[1], J. Liu[2], L. Shen[1], A. Mukherjee[1], W. Shi[1], D. Z. Pan[1], N. Sun[1]
[1]University of Texas, Austin, TX; [2]Tsinghua University, Beijing, China

11:15 AM

9.6 A 2.56mW 40MHz-Bandwidth 75dB-SNDR Partial-Interleaving SAR-Assisted NS Pipeline ADC With Background Inter-Stage Offset Calibration
Y. Song[1], Y. Zhu[1], C. H. Chan[1], R. P. Martins[1,2]
[1]University of Macau, Macau, China
[2]Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

11:45 AM

9.7 Background Multi-Rate LMS Calibration Circuit for 15MHz-BW 74dB-DR CT 2-2 MASH ΔΣ ADC in 28nm CMOS
M. Fukazawa[1], T. Oshima[2], M. Fujiwara[1], K. Tateyama[1], A. Raed[1], M. Ito[1], T. Matsumoto[1], T. Matsui[1]
[1]Renesas Electronics, Tokyo, Japan; [2]Hitachi, Tokyo, Japan

12:00 PM

9.8 A Low-Cost 4-Channel Reconfigurable Audio Interface for Car Entertainment Systems
R. van Veldhoven, M. Lammers, L. van der dussen, K. Mabtoul
NXP Semiconductors, Eindhoven, The Netherlands

Conclusion 12:15 PM

High-Performance Transceivers

Session Chair: ***Renaldi Winoto,*** *Mojo Vision, Saratoga, CA*
Session Co-Chair: ***Xin He,*** *NXP Semiconductors, Eindhoven, The Netherlands*

8:30 AM

10.1 A 1.4-to-2.7GHz FDD SAW-Less Transmitter for 5G-NR Using a BW-Extended N-Path Filter-Modulator, an Isolated-BB Input and a Wideband TIA-Based PA Driver Achieving <-157.5dBc/Hz OB Noise

G. Qi[1], H. Shao[1], P-I. Mak[1], J. Yin[1], R. P. Martins[1,2]
[1]University of Macau, Macau, China; [2]University of Lisboa, Lisbon, Portugal

9:00 AM

10.2 A SAW-Less Direct-Digital RF Modulator with Tri-Level Time-Approximation Filter and Reconfigurable Dual-Band Delta-Sigma Modulation

S. Su, M. S-W. Chen, University of Southern California, Los Angeles, CA

9:30 AM

10.3 A 12nm CMOS RF Transceiver Supporting 4G/5G UL MIMO

M-D. Tsai[1], S-Y. Yang[1], C-Y. Yu[1], P-Y. Chen[1], T-H. Wu[1], M. Hassan[2], C-T. Chen[1], C-W. Wang[1], Y-C. Huang[1], L-H. Hung[1], W-H. Chiu[1], A. Lin[1], B-Y. Lin[1], A. Werquin[2], C-C. Lin[1], Y-H. Chen[1], J-C. Tsai[1], Y-Y. Fu[1], B. Tenbroek[2], C-S. Chiu[1], Y-B. Lee[1], G-K. Dehng[1], [1]MediaTek, Hsinchu, Taiwan; [2]MediaTek, Kent, United Kingdom

Break 10:00 AM

10:15 AM

10.4 A 4×4 Dual-Band Dual-Concurrent WiFi 802.11ax Transceiver with Integrated LNA, PA and T/R Switch Achieving +20dBm 1024-QAM MCS11 P_{out} and -43dB EVM Floor in 55nm CMOS

E. Lu[1], W-K. Li[2], Z. Deng[1], E. Rostami[1], P-A. Wu[2], K-M. Chang[2], Y-C. Chuang[2], C-M. Lai[2], Y-C. Chen[1], T-H. Peng[2], T-C. Tsai[2], H-H. Liu[2], C-C. Chiu[2], B. Huang[1], Y-C. Wang[2], J-H. C. Zhan[2], O. Shanaa[1]
[1]MediaTek, San Jose, CA; [2]MediaTek, Hsinchu, Taiwan

10:45 AM

10.5 A Fully Integrated 27dBm Dual-Band All-Digital Polar Transmitter Supporting 160MHz for WiFi 6 Applications

A. Ben-Bassat[1], S. Gross[2], A. Nazimov[1], A. Ravi[3], B. Khamaisi[1], E. Banin[2], E. Borokhovich[2], N. Kimiagarov[2], P. Skliar[2], R. Banin[1], S. Zur[2], S. Reinhold[4], S. Bruker[2], T. Maimon[1], U. Parker[2], O. Degani[1]
[1]Intel, Haifa, Israel; [2]Intel, Petach Tikva, Israel; [3]Intel, Hillsboro, OR
[4]Intel, Munich, Germany

11:15 AM

10.6 A 4G/5G Cellular Transmitter in 12nm FinFET with Harmonic Rejection

M-D. Tsai[1], C-W. Tseng[1], K-J. Tsai[1], S. Andrabi[2], P-C. Huang[1], F. Beffa[3], Y. Chen[3], B. Tenbroek[3], [1]MediaTek, Hsinchu, Taiwan; [2]MediaTek, Cambridge, United Kingdom
[3]MediaTek, Kent, United Kingdom

11:30 AM

10.7 A 0.26mm² DPD-Less Quadrature Digital Transmitter With <-40dB EVM Over >30dB P_{out} Range in 65nm CMOS

S-W. Yoo[1], S-C. Hung[1], J. S. Walling[2], D. J. Allstot[3], S-M. Yoo[1]
[1]Michigan State University, East Lansing, MI; [2]University of Utah, Salt Lake City, UT
[3]Oregon State University, Corvallis, OR

11:45 AM

10.8 A 4-Element 500MHz-Modulated-BW 40mW 6b 1GS/s Analog-Time-to-Digital-Converter-Enabled Spatial Signal Processor in 65nm CMOS

E. Ghaderi, C. Puglisi, S. Bansal, S. Gupta, Washington State University, Pullman, WA

Conclusion 12:15 PM

DC-DC Converters

Session Chair: ***Yan Lu,*** *University of Macau, Taipa, Macau*
Session Co-Chair: ***Makoto Takamiya,*** *University of Tokyo, Tokyo, Japan*

8:30 AM

11.1 A Direct 12V/24V-to-1V 3W 91.2%-Efficiency Tri-State DSD Power Converter with Online V_{CF} Rebalancing and In-Situ Precharge Rate Regulation

K. Wei[1], Y. Ramadass[2], D. B. Ma[1]
[1]University of Texas at Dallas, Richardson, TX
[2]Texas Instruments, Santa Clara, CA

9:00 AM

11.2 A Fully Integrated Resonant Switched-Capacitor Converter with 85.5% Efficiency at 0.47W Using On-Chip Dual-Phase Merged-LC Resonator

P. H. McLaughlin, Z. Xia, J. T. Stauth, Dartmouth College, Hanover, NH

9:30 AM

11.3 A One-Step 325V to 3.3-to-10V 0.5W Resonant DC-DC Converter with Fully Integrated Power Stage and 80.7% Efficiency

C. Rindfleisch, B. Wicht, Leibniz University Hannover, Hannover, Germany

Break 10:00 AM

10:15 AM

11.4 A 48-to-80V Input 2MHz Adaptive ZVT-Assisted GaN-Based Bus Converter Achieving 14% Light-Load Efficiency Improvement

Q. Cheng, L. Cong, H. Lee, University of Texas at Dallas, Richardson, TX

10:45 AM

11.5 A 2-Phase Soft-Charging Hybrid Boost Converter with Doubled-Switching Pulse Width and Shared Bootstrap Capacitor Achieving 93.5% Efficiency at a Conversion Ratio of 4.5

M. Huang[1,2], Y. Lu[1], R. P. Martins[1,3]
[1]University of Macau, Macau, China
[2]South China University of Technology, Guangzhou, China
[3]University of Lisboa, Lisbon, Portugal

11:15 AM

11.6 A 1.46mm² Simultaneous Energy-Transferring Single-Inductor Bipolar-Output Converter with a Flying Capacitor for Highly Efficient AMOLED Display in 0.5µm CMOS

S-W. Hong, Sookmyung Women's University, Seoul, Korea

11:45 AM

11.7 A Voltage-Tolerant Three-Level Buck-Boost DC-DC Converter with Continuous Transfer Current and Flying Capacitor Soft Charger Achieving 96.8% Power Efficiency and 0.87µs/V DVS Rate

J. Baek, T. Nomiyama, S. Park, Y-H. Jung, D. Kim, J. Han, J-S. Bang, Y. Lee, I-H. Kim, J-S. Paek, J. Lee, T. B. Cho
Samsung Electronics, Hwaseong, Korea

12:00 PM

11.8 A 96.8%-Efficiency Continuous Input/Output-Current Step-Up/Down Converter Powering Disposable IoTs with Reconfigurable Multi-Cell-Balanced Alkaline Batteries

M-W. Ko[1], G-G. Kang[1], K-D. Kim[1], J-H. Lee[1], S. Koh[1], T. Kong[2], S-H. Kim[2], S. Lee[2], M. Choi[2], J. Shin[2], G-H. Cho[1], H-S. Kim[1]
[1]KAIST, Daejeon, Korea
[2]Samsung Electronics, Hwaseong, Korea

Conclusion 12:15 PM

Advanced Optical Communication Circuits

Session Chair:
Mounir Meghelli, *IBM Thomas J. Watson Research Center, Yorktown Heights, NY*
Session Co-Chair: ***Takashi Takemoto,*** *Hitachi, Sapporo, Japan*

8:30 AM

12.1 A 3D-Integrated Microring-Based 112Gb/s PAM-4 Silicon-Photonic Transmitter with Integrated Nonlinear Equalization and Thermal Control

H. Li, G. Balamurugan, M. Sakib, R. Kumar, H. Jayatilleka, H. Rong, J. Jaussi, B. Casper
Intel, Hillsboro, OR

9:00 AM

12.2 A 4-Channel 200Gb/s PAM-4 BiCMOS Transceiver with Silicon Photonics Front-Ends for Gigabit Ethernet Applications

E. Sentieri[*1], T. Copani*[*2], A. Paganini[1], M. Traldi[1], A. Palladino[1], A. Santipo[1], L. Gerosa[1], M. Repossi[1], G. Catrini[2], M. Campo[2], F. Radice[1], A. Diodato[1], R. Pelleriti[2], D. Baldi[1], L. Tarantini[1], L. Maggi[1], G. Radaelli[1], S. Cervini[1], F. Clerici[2], A. Moroni[1]*
*Equally-Credited Authors (ECAs)
[1]STMicroelectronics, Agrate, Italy
[2]STMicroelectronics, Catania, Italy

9:30 AM

12.3 A 48GHz BW 225mW/ch Linear Driver IC with Stacked Current-Reuse Architecture in 65nm CMOS for Beyond-400Gb/s Coherent Optical Transmitters

T. Jyo, M. Nagatani, J. Ozaki, M. Ishikawa, H. Nosaka
NTT, Kanagawa, Japan

9:45 AM

12.4 A 700mW 4-to-1 SiGe BiCMOS 100GS/s Analog Time-Interleaver DS2

H. Ramon, M. Verplaetse, M. Vanhoecke, H. Li, J. Bauwelinck, P. Ossieur, X. Yin, G. Torfs
imec - Ghent University, Ghent, Belgium

Break 10:00 AM

Non-Volatile Memories

Session Chair: ***Jongmin Park,*** *SK hynix, Icheon, Korea*
Session Co-Chair: ***Yasuhiko Taito,*** *Renesas Electronics, Kodaira, Japan*

10:15 AM

13.1 A 1Tb 4b/Cell NAND Flash Memory with t_{PROG}=2ms, t_R=110µs and 1.2Gb/s High-Speed IO Rate

D-H. Kim, H. Kim, S. Yun, Y. Song, J. Kim , S-M. Joe, K-H. Kang, J. Jang, H-J. Yoon, K. Lee, M. Kim , J. Kwon, J. Jo, S. Park, J. Park, J. Cho, S. Park, G. Kim , J. Bang, H. Kim, J. Park , D. Lee, S. Lee, H. Jang, H-J. Lee, D. Shin, J. Park, J. Kim , J. Kim, K. Jang, I. H. Park, S. H. Moon, M-H. Choi, P. Kwak, J-Y. Park, Y. Choi, S-L. Kim, S. Lee, D. Kang, J-D. Lim, D-S. Byeon, K. Song, J. Choi, S. J. Hwang, J. Jeong
Samsung Electronics, Hwaseong, Korea

10:45 AM

13.2 A 1Tb 4b/Cell 96-Stacked-WL 3D NAND Flash Memory with 30MB/s Program Throughput Using Peripheral Circuit Under Memory Cell Array Technique

H. Huh, W. Cho, J. Lee, Y. Noh, Y. Park, S. Ok, J. Kim, K. Cho, H. Lee, G. Kim, K. Park, K. Kim, H. Lee, S. Chai, C. Kwon, H. Cho, C. Jeong, Y. Yang, J. Goo, J. Park, J. Lee, H. Kim, K. Jo, C. Park, H. Nam, H. Song, S. Lee, W. Jeong, K-O. Ahn, T-S. Jung
SK hynix, Icheon, Korea

11:15 AM

13.3 A 22nm 32Mb Embedded STT-MRAM with 10ns Read Speed, 1M Cycle Write Endurance, 10 Years Retention at 150°C and High Immunity to Magnetic Field Interference

Y-D. Chih, Y-C. Shih, C-F. Lee, Y-A. Chang, P-H. Lee, H-J. Lin, Y-L. Chen, C-P. Lo, M-C. Shih, K-H. Shen, H. Chuang, T-Y. J. Chang
TSMC, Hsinchu, Taiwan

11:30 AM

13.4 A 22nm 1Mb 1024b-Read and Near-Memory-Computing Dual-Mode STT-MRAM Macro with 42.6GB/s Read Bandwidth for Security-Aware Mobile Devices

T-C. Chang, Y-C. Chiu, C-Y. Lee, J-M. Hung, K-T. Chang, C-X. Xue, S-Y. Wu, H-Y. Kao, P. Chen, H-Y. Huang, S-H. Teng, M-F. Chang
National Tsing Hua University, Hsinchu, Taiwan

11:45 AM

13.5 A 128Gb 1b/Cell 96-Word-Line-Layer 3D Flash Memory to Improve Random Read Latency with t_{PROG}=75µs and t_R=4µs

T. Kouchi[1], N. Kumazaki[1], M. Yamaoka[1], S. Bushnaq[1], T. Kodama[1], Y. Ishizaki[1], Y. Deguchi[1], A. Sugahara[1], A. Imamoto[1], N. Asaoka[1], R. Isomura[1], T. Handa[1], J. Sato[2], H. Komai[1], A. Okuyama[1], K. Naoaki[1], Y. Kajiyama[1], Y. Terada[1], H. Ohnishi[1], H. Yabe[3], C. Hsu[3], M. Kakoi[1], M. Yoshihara[1]
[1]KIOXIA, Yokohama, Japan
[2]KIOXIA Systems, Yokohama, Japan
[3]Western Digital, Milpitas, CA

Conclusion 12:15 PM

Low-Power Machine Learning

Session Chair: ***Jun Deguchi,*** *KIOXIA, Kawasaki, Japan*
Session Co-Chair: ***Rangharajan Venkatesan,*** *NVIDIA, Santa Clara, CA*

1:30 PM

14.1 A 510nW 0.41V Low-Memory Low-Computation Keyword-Spotting Chip Using Serial FFT-Based MFCC and Binarized Depthwise Separable Convolutional Neural Network in 28nm CMOS DS2

W. Shan[1], M. Yang[2], J. Xu[1], Y. Lu[1], S. Zhang[1], T. Wang[1], J. Yang[1], L. Shi[1], M. Seok[3]
[1]Southeast University, Jiangsu, China
[2]EPFL, Neuchâtel, Switzerland
[3]Columbia University, New York, NY

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14.2 A 65nm 24.7μJ/Frame 12.3mW Activation-Similarity-Aware Convolutional Neural Network Video Processor Using Hybrid Precision, Inter-Frame Data Reuse and Mixed-Bit-Width Difference-Frame Data Codec

Z. Yuan[1,2], Y. Yang[1], J. Yue[1,2], R. Liu[1], X. Feng[1], Z. Lin[3], X. Wu[3], X. Li[1], H. Yang[1], Y. Liu[1]
[1]Tsinghua University, Beijing, China
[2]Pi2star Technology, Beijing, China
[3]Anhui University, Hefei, China

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14.3 A 65nm Computing-in-Memory-Based CNN Processor with 2.9-to-35.8TOPS/W System Energy Efficiency Using Dynamic-Sparsity Performance-Scaling Architecture and Energy-Efficient Inter/Intra-Macro Data Reuse

J. Yue[1,2], Z. Yuan[1,2], X. Feng[1], Y. He[1], Z. Zhang[3], X. Si[3], R. Liu[3], M-F. Chang[3], X. Li[1], H. Yang[1], Y. Liu[1]
[1]Tsinghua University, Beijing, China
[2]Pi2star Technology, Beijing, China
[3]National Tsing Hua University, Hsinchu, Taiwan

Break 3:00 PM

SRAM & Compute-In-Memory

Session Chair:
Kyu-Hyoun (KH) Kim, *IBM T. J. Watson Reseach Center, Yorktown Heights, NY*
Session Co-Chair: ***Eric Karl,*** *Intel, Hillsboro, OR*

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15.1 A 5nm 135Mb SRAM in EUV and High-Mobility-Channel FinFET Technology with Metal Coupling and Charge-Sharing Write-Assist Circuitry Schemes for High-Density and Low-V_{MIN} Applications

J. Chang, Y-H. Chen, G. Chan, H. Cheng, P-S. Wang, Y. Lin, H. Fujiwara, R. Lee, H-J. Liao, P-W. Wang, G. Yeap, Q. Li
TSMC, Hsinchu, Taiwan

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15.2 A 28nm 64Kb Inference-Training Two-Way Transpose Multibit 6T SRAM Compute-in-Memory Macro for AI Edge Chips

J-W. Su[1,2], X. Si[1], Y-C. Chou[1], T-W. Chang[1], W-H. Huang[1], Y-N. Tu[1], R. Liu[1], P-J. Lu[1], T-W. Liu[1], J-H. Wang[1], Z. Zhang[1], H. Jiang[3], S. Huang[3], C-C. Lo[1], R-S. Liu[1], C-C. Hsieh[1], K-T. Tang[1], S-S. Sheu[2], S-H. Li[2], H-Y. Lee[2], S-C. Chang[2], S. Yu[3], M-F. Chang[1]
[1]National Tsing Hua University, Hsinchu, Taiwan
[2]Industrial Technology Research Institute, Hsinchu, Taiwan
[3]Georgia Institute of Technology, Atlanta, GA

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15.3 A 351TOPS/W and 372.4GOPS Compute-in-Memory SRAM Macro in 7nm FinFET CMOS for Machine-Learning Applications

Q. Dong[1], M. E. Sinangil[1], B. Erbagci[1], D. Sun[2], W-S. Khwa[2], H-J. Liao[2], Y. Wang[2], J. Chang[2]
[1]TSMC, San Jose, CA
[2]TSMC, Hsinchu, Taiwan

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15.4 A 22nm 2Mb ReRAM Compute-in-Memory Macro with 121-28TOPS/W for Multibit MAC Computing for Tiny AI Edge Devices

C-X. Xue, T-Y. Huang, J-S. Liu, T-W. Chang, H-Y. Kao, J-H. Wang, T-W. Liu, S-Y. Wei, S-P. Huang, W-C. Wei, Y-R. Chen, T-H. Hsu, Y-K. Chen, Y-C. Lo, T-H. Wen, C-C. Lo, R-S. Liu, C-C. Hsieh, K-T. Tang, M-F. Chang
National Tsing Hua University, Hsinchu, Taiwan

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15.5 A 28nm 64Kb 6T SRAM Computing-in-Memory Macro with 8b MAC Operation for AI Edge Chips

X. Si[1,2], Y-N. Tu[1], W-H. Huang[1], J-W. Su[1], P-J. Lu[1], J-H. Wang[1], T-W. Liu[1], S-Y. Wu[1], R. Liu[1], Y-C. Chou[1], Z. Zhang[1], S-H. Sie[1], W-C. Wei[1], Y-C. Lo[1], T-H. Wen[1], T-H. Hsu[1], Y-K. Chen[1], W. Shih[1], C-C. Lo[1], R-S. Liu[1], C-C. Hsieh[1], K-T. Tang[1], N-C. Lien[3], W-C. Shih[3], Y. He[2], Q. Li[2], M-F. Chang[1]
[1]National Tsing Hua University, Hsinchu, Taiwan
[2]University of Electronic Science and Technology of China, Chengdu, China
[3]M31 Technology, Hsinchu, Taiwan

Conclusion 5:15 PM

Nyquist & VCO-Based ADCs

Session Chair: ***Bob Verbruggen,*** *Xilinx, Citywest, Ireland*
Session Co-Chair: ***Takashi Oshima,*** *Hitachi, Tokyo, Japan*

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16.1 A 12b 18GS/s RF Sampling ADC with an Integrated Wideband Track-and-Hold Amplifier and Background Calibration

A. M. A. Ali, H. Dinc, P. Bhoraskar, S. Bardsley, C. Dillon, M. Kumar, M. McShea, R. Bunch, J. Prabhakar, S. Puckett
Analog Devices, Greensboro, NC

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16.2 A 4× Interleaved 10GS/s 8b Time-Domain ADC with 16× Interpolation-Based Inter-Stage Gain Achieving >37.5dB SNDR at 18GHz Input DS2

M. Zhang[1], Y. Zhu[1], C-H. Chan[1], R. P. Martins[1,2]
[1]University of Macau, Macau, China
[2]University of Lisboa, Lisbon, Portugal

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16.3 A Single-Channel 5.5mW 3.3GS/s 6b Fully Dynamic Pipelined ADC with Post-Amplification Residue Generation

Z. Zheng[1,2], L. Wei[1,2], J. Lagos[2], E. Martens[2], Y. Zhu[1], C-H. Chan[1], J. Craninckx[2], R. P. Martins[1,3]
[1]University of Macau, Macau, China
[2]imec, Leuven, Belgium
[3]University of Lisboa, Lisbon, Portugal

Break 3:00 PM

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16.4 A Calibration-Free 71.7dB SNDR 100MS/s 0.7mW Weighted-Averaging Correlated Level Shifting Pipelined SAR ADC with Speed-Enhancement Scheme

T-C. Hung, J-C. Wang, T-H. Kuo, National Cheng Kung University, Tainan, Taiwan

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16.5 A 13b 0.005mm² 40MS/s SAR ADC with kT/C Noise Cancellation

J. Liu[1], X. Tang[2], W. Zhao[2], L. Shen[2], N. Sun[2]
[1]Tsinghua University, Beijing, China
[2]University of Texas, Austin, TX

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16.6 An 800MHz-BW VCO-Based Continuous-Time Pipelined ADC with Inherent Anti-Aliasing and On-Chip Digital Reconstruction Filter

H. Shibata[1], G. Taylor[2], B. Schell[3], V. Kozlov[1], S. Patil[1], D. Paterson[4], A. Ganesan[1], Y. Dong[4], W. Yang[4], Y. Yin[1], Z. Li[1], P. Shrestha[4], A. Gopal[5], A. Bhat[4], S. Pavan[6]
[1]Analog Devices, Toronto, Canada
[2]Analog Devices, San Diego, CA
[3]Analog Devices, Somerset, NJ
[4]Analog Devices, Wilmington, MA
[5]Analog Devices, Greensboro, NC
[6]Indian Institute of Technology Madras, Chennai, India

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16.7 A 40MHz-BW 76.2dB/78.0dB SNDR/DR Noise-Shaping Nonuniform Sampling ADC with Single Phase-Domain Level Crossing and Embedded Nonuniform Digital Signal Processor in 28nm CMOS

T-F. Wu, M-W. Chen, University of Southern California, Los Angeles, CA

Conclusion 5:15 PM

Frequency Synthesizers & VCOs

Session Chair: ***Wanghua Wu,*** *Samsung, San Jose, CA*
Session Co-Chair: ***Jiayoon Ru,*** *XINYI Information Technology, Shanghai, China*

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17.1 A -240dB-FoM$_{jitter}$ and -115dBc/Hz PN @ 100kHz, 7.7GHz Ring-DCO-Based Digital PLL Using P/I-Gain Co-Optimization and Sequence-Rearranged Optimally Spaced TDC for Flicker-Noise Reduction
Y. Lee[1,2], T. Seong*[1,2], J. Lee[1], C. Hwang[1], H. Park[1], J. Choi[1],* *Equally-Credited Authors (ECAs)
[1]KAIST, Daejeon, Korea; [2]Ulsan National Institute of Science and Technology, Ulsan, Korea

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17.2 A 66fs$_{rms}$ Jitter 12.8-to-15.2GHz Fractional-N Bang-Bang PLL with Digital Frequency-Error Recovery for Fast Locking
A. Santiccioli[1], M. Mercandelli[1], L. Bertulessi[1], A. Parisi[1], D. Cherniak[2], A. L. Lacaita[1], C. Samori[1], S. Levantino[1]
[1]Politecnico di Milano, Milan, Italy; [2]Infineon Technologies, Villach, Austria

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17.3 A -58dBc-Worst-Fractional-Spur and -234dB-FoM$_{jitter}$, 5.5GHz Ring-DCO-Based Fractional-N DPLL Using a Time-Invariant-Probability Modulator, Generating a Nonlinearity-Robust DTC-Control Word
T. Seong[1,2], Y. Lee*[1,2], C. Hwang[1], J. Lee[1], H. Park[1], K. J. Lee[2], J. Choi[1]*
*Equally-Credited Authors (ECAs)
[1]KAIST, Daejeon, Korea; [2]Ulsan National Institute of Science and Technology, Ulsan, Korea

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17.4 A 18.6-to-40.1GHz 201.7dBc/Hz FoM$_T$ Multi-Core Oscillator Using E-M Mixed-Coupling Resonance Boosting
Y. Shu, H. J. Qian, X. Luo
University of Electronic Science and Technology of China, Chengdu, China

Break 3:00 PM

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17.5 A 12.5GHz Fractional-N Type-I Sampling PLL Achieving 58fs Integrated Jitter
M. Mercandelli[1], A. Santiccioli[1], A. Parisi[1], L. Bertulessi[1], D. Cherniak[2], A. L. Lacaita[1], C. Samori[1], S. Levantino[1]
[1]Politecnico di Milano, Milan, Italy; [2]Infineon Technologies, Villach, Austria

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17.6 A 21.7-to-26.5GHz Charge-Sharing Locking Quadrature PLL with Implicit Digital Frequency-Tracking Loop Achieving 75fs Jitter and -250dB FoM
Y. Hu[1], X. Chen[1], T. Siriburanon[1], J. Du[1], Z. Gao[1], V. Govindaraj[1], A. Zhu[1], R. B. Staszewski[1,2]
[1]University College Dublin, Dublin, Ireland
[2]Microelectronic Circuits Centre Ireland, Dublin, Ireland

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17.7 DS2 A 12mW 10GHz FMCW PLL Based on an Integrating DAC with 90kHz rms Frequency Error for 23MHz/µs Slope and 1.2GHz Chirp Bandwidth
P. T. Renukaswamy[1,2], N. Markulic[1], S. Park[1,2], A. Kankuppe[1,2], Q. Shi [1], P. Wambacq[1,2], J. Craninckx[1], [1]imec, Leuven, Belgium; [2]Vrije Universiteit Brussel, Brussels, Belgium

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17.8 A 170MHz-Lock-In-Range and -253dB-FoM$_{jitter}$, 12-to-14.5GHz Subsampling PLL with a 150µW Frequency-Disturbance-Correcting Loop Using a Low-Power Unevenly Spaced Edge Generator
Y. Lim[1,2], J. Kim*[1], Y. Jo[1], J. Bang[1], S. Yoo[1,2], H. Park[1], H. Yoon[3], J. Choi[1]*
*Equally-Credited Authors (ECAs), [1]KAIST, Daejeon, Korea
[2]Ulsan National Institute of Science and Technology, Ulsan, Korea
[3]Qualcomm, San Diego, CA

5:00 PM

17.9 A 9mW 54.9-to-63.5GHz Current-Reuse LO Generator with a 186.7dBc/Hz FoM by Unifying a 20GHz 3rd-Harmonic-Rich Current-Output VCO, a Harmonic-Current Filter and a 60GHz TIA
C. Fan[1], J. Yin[1], C-C. Lim[1], P-I. Mak[1], R. P. Martins[1,2]
[1]University of Macau, Macau, China; [2]University of Lisboa, Lisbon, Portugal

Conclusion 5:15 PM

GaN & Isolated Power Conversion

Session Chair: ***Robert Pilawa,*** *UC Berkeley, Berkeley, CA*
Session Co-Chair: ***Harish Krishnamurthy,*** *Intel, Beaverton, OR*

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18.1 A Self-Health-Learning GaN Power Converter Using On-Die Logarithm-Based Analog SGD Supervised Learning and Online T_J-Independent Precursor Measurement
Y. Huang, Y. Chen, D. B. Ma, The University of Texas at Dallas, Richardson, TX

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18.2 A Monolithic E-Mode GaN 15W 400V Offline Self-Supplied Hysteretic Buck Converter with 95.6% Efficiency
M. Kaufmann[1], M. Lueders[2], C. Kaya[3], B. Wicht[1]
[1]Leibniz University Hannover, Hannover, Germany
[2]Texas Instruments, Freising, Germany
[3]Texas Instruments, Dallas, TX

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18.3 A 120mA Non-Isolated Capacitor-Drop AC/DC Power Supply
Y. Ramadass[1], A. Blanco*[2], B. Xiao*[3], J. Cummings[3]*
*Equally-Credited Authors (ECAs)
[1]Texas Instruments, Santa Clara, CA
[2]Texas Instruments, Dallas, TX
[3]Texas Instruments, Tucson, AZ

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18.4 An 11MHz Fully Integrated 5kV Isolated DC-DC Converter Without Cross-Isolation-Barrier Feedback
L. Li[1], X. Fang[1], R. Wu[2]
[1]CoilEasy Technologies, Chongqing, China
[2]University of Electronic Science and Technology of China, Chengdu, China

Break 3:00 PM

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18.5 ZVS Flyback-Converter ICs Optimizing USB Power Delivery for Fast-Charging Mobile Devices to Achieve 93.5% Efficiency
W-H. Chang, K-Y. Lin, C-C. Lee, L-D. Lo, J-Y. Lin, T-Y. Yang, Richtek, Hsinchu, Taiwan

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18.6 A 92.8%-Peak-Efficiency 60A 48V-to-1V 3-Level Half-Bridge DC-DC Converter with Balanced Voltage on a Flying Capacitor
M. Choi[1,2], D-K. Jeong[1]
[1]Seoul National University, Seoul, Korea
[2]Samsung Electronics, Hwaseong, Korea

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18.7 A DC to 35MHz Fully Integrated Single-Power-Supply Isolation Amplifier for Current- and Voltage-Sensing Front-Ends of Power Electronics
S. Takaya, H. Ishihara, K. Onizuka, Toshiba, Kawasaki, Japan

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18.8 A Fully-Generic-Process Galvanic Isolator for Gate Driver with 123mW 23% Power Transfer and Full-Triplex 21/14/0.5Mb/s Bidirectional Communication Utilizing Reference-Free Dual-Modulation FSK
H. Ishihara, K. Onizuka, Toshiba, Kawasaki, Japan

Conclusion 5:15 PM

CRYO-CMOS for Quantum Technologies

Session Chair: ***Edoardo Charbon,*** *EPFL, Neuchatel, Switzerland*
Session Co-Chair: ***Rabia Yazicigil,*** *Boston University, Boston, MA*

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19.1 A Scalable Cryo-CMOS 2-to-20GHz Digitally Intensive Controller for 4×32 Frequency Multiplexed Spin Qubits/Transmons in 22nm FinFET Technology for Quantum Computers

B. Patra[1], J. P. G. van Dijk*[1], S. Subramanian[2], A. Corna[1], X. Xue[1], C. Jeon[2], F. Sheikh[2], E. Juarez-Hernandez[3], B. Perez Esparza[3], H. Rampurawala[2], B. Carlton[2], N. Samkharadze[4], S. Ravikumar[2], C. Nieva[2], S. Kim[2], H-J. Lee[2], A. Sammak[4], G. Scappucci[1], M. Veldhorst[1], L. M. K. Vandersypen[1,2], M. Babaie*[1], F. Sebastiano*[1], E. Charbon*[2,5], S. Pellerano*[2]*
*Equally-Credited Authors (ECAs)
[1]Delft University of Technology, Delft, The Netherlands
[2]Intel, Hillsboro, OR
[3]Intel, Guadalajara, Mexico
[4]TNO, Delft, The Netherlands
[5]EPFL, Neuchatel, Switzerland

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19.2 A 110mK 295μW 28nm FDSOI CMOS Quantum Integrated Circuit with a 2.8GHz Excitation and nA Current Sensing of an On-Chip Double Quantum Dot

L. Le Guevel[1,2], G. Billiot[1], X. Jehl[2], S. De Franceschi[2], M. Zurita[1], Y. Thonnart[1], M. Vinet[1], M. Sanquer[2], R. Maurand[2], A. G. Jansen[2], G. Pillonnet[1]
[1]CEA-LETI-MINATEC, Grenoble, France
[2]CEA-IRIG, Grenoble, France

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19.3 A 200dB FoM 4-to-5GHz Cryogenic Oscillator with an Automatic Common-Mode Resonance Calibration for Quantum Computing Applications

J. Gong[1], Y. Chen[1], F. Sebastiano[1], E. Charbon[2,3], M. Babaie[1]
[1]Delft University of Technology, Delft, The Netherlands
[2]EPFL, Lausanne, Switzerland
[3]Intel, Hillsboro, OR

Break 3:00 PM

Low-Power Circuits for IoT & Health

Session Chair: ***Nick Van Helleputte,*** *imec, Heverlee, Belgium*
Session Co-Chair: ***Munehiko Nagatani,*** *NTT, Atsugi, Japan*

3:15 PM

20.1 A 28µW IoT Tag That Can Communicate with Commodity WiFi Transceivers via a Single-Side-Band QPSK Backscatter Communication Technique

P-H. P. Wang[1,2], C. Zhang[1], H. Yang[1], D. Bharadia[1], P. P. Mercier[1]
[1]University of California, San Diego, La Jolla, CA
[2]Broadcom Inc., San Diego, CA

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20.2 A 57nW Software-Defined Always-On Wake-Up Chip for IoT Devices with Asynchronous Pipelined Event-Driven Architecture and Time-Shielding Level-Crossing ADC

Z. Wang[1], L. Ye[1,2], H. Zhang[1], J. Ru[3], H. Fan[2], Y. Wang[1], R. Huang[1]
[1]Peking University, Beijing, China
[2]Advanced Institute of Information Technology of Peking University, Hangzhou, China
[3]XINYI Information Technology, Shanghai, China

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20.3 A 4.0×3.7×1.0mm³-MEMS CMOS Integrated E-Nose with Embedded 4×Gas Sensors, a Temperature Sensor and a Relative Humidity Sensor

S. H. Lee[1], K. Park[1], J. Lim[1], M. Lee[1], J. Park[1], H. Kim[1], Y. O. Lee[2], H. S. Ahn[2], E. Shin[1], H. Ko[1], S. Yoo[1], H. Ryu[1], Y. Park[1], J. Kim[1], L. Yan[1]
[1]Samsung Electronics, Hwaseong, Korea
[2]Wisol, Osan, Korea

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20.4 3D Surgical Alignment with 100µm Resolution Using Magnetic-Field Gradient-Based Localization DS2

S. Sharma, G. Ding, A. Telikicherla, F. Aghlmand, A. Hashemi Talkhooncheh, M. Wang, M. G. Shapiro, A. Emami
California Institute of Technology, Pasadena, CA

Conclusion 5:15 PM

Demonstration Session 2, Tuesday, February 18th, 5:00-7:00 PM

This year, the Demonstration Session extending in selected regular papers, both Academic and Industrial, will take place on Monday February 17th, and Tuesday February 18th, from 5 pm until 7 pm in the Golden Gate Hall. These demonstrations will feature real-life applications made possible by new ICs presented at ISSCC 2020, as noted by the symbol DS2

7.3 STATICA: A 512-Spin 0.25M-Weight Full-Digital Annealing Processor with a Near-Memory All-Spin-Updates-at-Once Architecture for Combinatorial Optimization with Complete Spin-Spin Interactions

7.4 GANPU: A 135TFLOPS/W Multi-DNN Training Processor for GANs with Speculative Dual-Sparsity Exploitation

9.1 A Current-Sensing Front-End Realized by A Continuous-Time Incremental ADC with 12b SAR Quantizer and Reset-Then-Open Resistive DAC Achieving 140dB DR and 8ppm INL at 4kS/s

12.4 A 700mW 4-to-1 SiGe BiCMOS 100GS/s Analog Time-Interleaver

14.1 A 510nW 0.41V Low-Memory Low-Computation Keyword-Spotting Chip Using Serial FFT-Based MFCC and Binarized Depthwise Separable Convolutional Neural Network in 28nm CMOS

16.2 A 4× Interleaved 10GS/s 8b Time-Domain ADC with 16× Interpolation-Based Inter-Stage Gain Achieving >37.5dB SNDR at 18GHz Input

17.7 A 12mW 10GHz FMCW PLL Based on an Integrating DAC with 90kHz rms Frequency Error for 23MHz/µs Slope and 1.2GHz Chirp Bandwidth

20.4 3D Surgical Alignment with 100µm Resolution Using Magnetic-Field Gradient-Based Localization

21.1 A Fully Integrated Genetic Variant Discovery SoC for Next-Generation Sequencing

25.3 A 65nm Edge-Chasing Quantizer-Based Digital LDO Featuring 4.58ps-FoM and Side-Channel-Attack Resistance

26.1 A 4.5mm^2 Multimodal Biosensing SoC for PPG, ECG, BIOZ and GSR Acquisition in Consumer Wearable Devices

26.3 A Closed-Loop Neuromodulation Chipset with 2-Level Classification Achieving 1.5V$_{pp}$ CM Interference Tolerance, 35dB Stimulation Artifact Rejection in 0.5ms and 97.8% Sensitivity Seizure Detection

26.4 A Cell-Capacitance-Insensitive CMOS Sample-and-Hold Chronoamperometric Sensor for Real-Time Measurement of Small Molecule Drugs in Whole Blood

26.5 A 20µW Heartbeat Detection System-on-Chip Powered by Human Body Heat for Self-Sustaining Wearable Healthcare

26.8 A Trimodal Wireless Implantable Neural Interface System-on-a-Chip

26.9 A 0.19×0.17mm^2 Wireless Neural Recording IC for Motor Prediction with Near-Infrared-Based Power and Data Telemetry

27.1 A 65nm Energy-Harvesting ULP SoC with 256kB Cortex-M0 Enabling an 89.1µW Continuous Machine Health Monitoring Wireless Self-Powered System

27.2 M0N0: A Performance-Regulated 0.8-to-38MHz DVFS ARM Cortex-M33 SIMD MCU with 10nW Sleep Power

27.3 EM and Power SCA-Resilient AES-256 in 65nm CMOS Through >350× Current-Domain Signature Attenuation

29.1 A 0.42THz 9.2dBm 64-Pixel Source-Array SoC with Spatial Modulation Diversity for Computational Terahertz Imaging

29.4 High-Performance Isolators and Notch Filters Based on N-Path Negative Transresistance

30.8 A 3.5mm×3.8mm Crystal-Less MICS Transceiver Featuring Coverages of ±160ppm Carrier Frequency Offset and 4.8-VSWR Antenna Impedance for Insertable Smart Pills

33.1 A 74 TMACS/W CMOS-RRAM Neurosynaptic Core with Dynamically Reconfigurable Dataflow and In-situ Transposable Weights for Probabilistic Graphical Models

33.2 A Fully Integrated Analog ReRAM Based 78.4TOPS/W Compute-In-Memory Chip with Fully Parallel MAC Computing

34.5 Human-Body-Coupled Power-Delivery and Ambient-Energy-Harvesting ICs for a Full-Body-Area Power Sustainability

TIMETABLE OF ISSCC 2020 SESSIONS

ISSCC 2020 • Sunday February 16th

Tutorials

8:30 AM	**T1:** Fundamentals of Integrated Transformers	**T2:** Analog Building Blocks of DC-DC Converters	**T3:** Interface Circuits for Wearable and Implantable Sensing Systems
10:30 AM	**T4:** Basics of Non-Volatile Memories: MRAM, RRAM, and PRAM	**T5:** Fundamentals of Time-Interleaved ADCs	**T6:** Digital Fractional-N Phase-Locked-Loop Design
1:30 PM	**T7:** Basics of Digital Low-Dropout (LDO) Integrated Voltage Regulators	**T8:** Capacitive Sensor Interfaces	
3:30 PM	**T9:** Fundamentals of Wireless Transceiver Circuits and Architectures (from 2G to 5G)	**T10:** How to Understand and Evaluate Deep Learning Processors	

Forums

8:00 AM	**F1:** Millimeter-Wave 5G: From Soup to Nuts and Bolts	**F2:** ML at the Extreme Edge: Machine Learning as the Killer IoT App

Events Below in Bold Box are Included with your Conference Registration

Evening Events

7:30 PM EE1: Student Research Preview: Short Presentations with Poster Session

6:30 PM EE2a: "Navigating the Assistant Professorship" (open to the public)
6:30 PM EE2b: "Rising to the Top in Industry" (open to the public)

ISSCC 2020 • Monday February 17th • Paper Sessions

8:30 AM	**Session 1:** Plenary Session				
1:30 PM	**Session 2:** Processors	**Session 3:** Analog Techniques I	**Session 4:** mm-Wave Wireless for Communication & Radar	**Session 5:** Imagers and ToF Sensors	**Session 6:** Ultra-High-Speed Wireline

12noon to 7:00 PM – Book Displays • 5:00 PM to 7:00 PM – Demonstration Session • 5:15 PM – Author Interviews • Social Hour

Evening Events

8:00 PM EE3: Industry Showcase

ISSCC 2020 • Tuesday February 18th • Paper Sessions

8:30 AM	**Session 7:** High-Performance Machine Learning **Session 8:** Highlighted Chip Releases	**Session 9:** Noise-Shaping ADCs	**Session 10:** High-Performance Transceivers	**Session 11:** DC-DC Converters	**Session 12:** Advanced Optical Communication Circuits **Session 13:** Non-Volatile Memories
1:30 PM	**Session 14:** Low-Power Machine Learning **Session 15:** SRAM & Compute-In-Memory	**Session 16:** Nyquist & VCO-Based ADCs	**Session 17:** Frequency Synthesizers & VCOs	**Session 18:** GaN & Isolated Power Conversion	**Session 19:** CRYO-CMOS for Quantum Technologies **Session 20:** Low-Power Circuits for IoT & Health

10:00 AM to 7:00 PM – Book Displays • 5:00 PM to 7:00 PM – Demonstration Session • 5:15 PM – Author Interviews • Social Hour

Evening Events

8:00 PM **EE4:** Quiz Show: "The Smartest Designer in the Universe"

EE5: Is an Open-Source Hardware Revolution on the Horizon?

ISSCC 2020 • Wednesday February 19th • Paper Sessions

8:30 AM	**Session 21:** Domain Specific Processors **Session 22:** DRAM & High-Speed Interfaces	**Session 23:** Analog Techniques II	**Session 24:** RF & mm-Wave Power Amplifiers	**Session 25:** Digital Power Delivery & Clocking Circuits	**Session 26:** Biomedical Innovations
1:30 PM	**Session 27:** IoT & Security **Session 28:** User Interaction & Diagnostic Technologies	**Session 29:** Emerging RF & THz Techniques	**Session 30:** Efficient Wireless Connectivity	**Session 31:** Digital Circuit Techniques for Emerging Applications **Session 32:** Power Management Techniques	**Session 33:** Non-Volatile Devices for Future Architecture **Session 34:** Biomedical Sensing, Stimulation & Harvesting

10:00 AM to 3:00 PM – Book Displays • 5:15 PM – Author Interviews

ISSCC 2020 • Thursday February 20th

8:00 AM	**Short Course:** Circuit Design in Advanced CMOS Technologies — Considerations and Solutions	**F3:** Machine Learning Processors: From High Performance Applications to Architectures and Benchmarking	**F4:** Cutting Edge Advances in Electrical and Optical Transceiver Technologies	**F5:** Power Management as an Enabler of Future SoC's	**F6:** Sensors for Health

EE4: The Smartest Designer in The Universe

Organizers:
Massimo Alioto, National University of Singapore, Singapore
Denis Daly, Omni Design Technologies, US
Tinoosh Mohsenin, University of Maryland, US
Alex Moreno, University of California at Berkeley, US
Mandy Pant, Intel, US
Tim Piessens, ICsense, Belgium
Mahmoud Sawaby, Stanford University, US
Farhana Sheikh, Intel, US
Tom Van Breussegem, ICsense, Belgium

Good silicon engineering is like practicing sports on an Olympic scale. Be the best and be known being the best. But who is actually the smartest designer of the universe? Who is capable of combining endless creativity with superb knowledge and insight? And where will we find this person: in industry or in academia? Or will the students rise up and show the former generation their tail?

In this interactive quiz show, three teams representing industry, academia and students will compete for the honor and the prestigious title: "The Smartest Designer in the Universe". In several rounds, he contestants will solve questions and puzzles covering all parts of electrical engineering.

They will baffle you with their knowledge, surprise your with their wit and entertain you with their to the point remarks. This all topped with a gentle sauce of made of irony, since the smartest designer in the universe should be smart enough to appreciate the special relativity of it all.

Join this session not only to support your own team but enroll in the game. Everybody will be able to actively participate using an app. Show your strength and support your team!

EE5: "Is an Open-Source Hardware Revolution on the Horizon?"

Organizers:
Naveen Verma, Princeton University, Princeton, NJ
Tanay Karnik, Intel, Hillsboro, OR
Kush Gulati, Omni Design Technologies, Milpitas, CA
Sudip Shekhar, UBC, Vancouver, Canada
Rabia Yazicigil, Boston University, Boston, MA

Open-source has revolutionized software, fostering innovation and enhancing productivity. Hardware design is complex in distinct ways, which, on the one hand, makes such progression necessary, but, on the other hand, institutes completely new challenges. Are the challenges show stoppers, or just new ways of thinking and engineering? If open-source hardware could be attained, what would it look like, and would there be significant up-side (e.g., compared to today's IP licensing)? Whatever the answers, the success of open-source hardware will require alignment, partnership, and collective will across the hardware ecosystem, from design, to methodologies, to business models. This evening session brings together panelists representing and debating from these different perspectives, to make and break the case.

Moderator:
Denis Daly, Omni Design Technologies, Billerica, MA

Panelists:
Rob Aitken, Arm, San Jose, CA
Elad Alon, UCB and Blue Cheetah Analog Design, Berkeley, CA
Brucek Khailany, NVIDIA, Austin, TX
Sailesh Kottapalli, Intel, Hillsboro, OR
Shichin Ouyang, MediaTek, San Jose, CA
David Patterson, UCB and Google, Berkeley and Mountain View, CA
Davide Rossi, UNIBO, Bologna, Italy

Domain-Specific Processors

Session Chair: ***Massimo Alioto,*** *National University of Singapore, Singapore*
Session Co-Chair: ***Ingrid Verbauwhede,*** *KU Leuven, Leuven, Belgium*

8:30 AM

21.1 A Fully Integrated Genetic Variant Discovery SoC for Next-Generation Sequencing DS2

Y-C. Wu[*1], *Y-L. Chen*[*1], *C-H. Yang*[1], *C-H. Lee*[2], *C-Y. Yu*[3], *N-S. Chang*[3], *L-C. Chen*[3], *J-R. Chang*[3], *C-P. Lin*[3], *H-L. Chen*[3], *C-S. Chen*[3], *J-H. Hung*[2], *C-H. Yang*[1]
*Equally-Credited Authors (ECAs)
[1]National Taiwan University, Taipei, Taiwan
[2]National Chiao Tung University, Hsinchu, Taiwan
[3]Taiwan Semiconductor Research Institute (TSRI), Hsinchu, Taiwan

9:00 AM

21.2 A 1.5μJ/Task Path-Planning Processor for 2D/3D Autonomous Navigation of Micro Robots

C. Chung, C-H. Yang
National Taiwan University, Taipei, Taiwan

9:30 AM

21.3 A 5.69mm² 0.98nJ/Pixel Image-Processing SoC with 24b High-Dynamic-Range and Multiple Sensor Format Support for Automotive Applications

C-C. Ju, T-M. Liu, Y-C. Chang, C-M. Wang, C-H. Tsai, Y-J. Chen, T. Wu, H-M. Lin, H-L. Chou, A. Chen, A-H. Wang, W. Gu, W. Hsieh, J-Y. Chang, S-C. Liao, C. Ho, L. Chu, S. Wei, C. Wang, K. Jou
MediaTek, Hsinchu, Taiwan

Break 10:00 AM

DRAM & High-Speed Interfaces

Session Chair: ***Dong Uk Lee,*** *SK hynix, Icheon, Korea*
Session Co-Chair: ***Seung-Jun Bae,*** *Samsung, Hwaseong, Korea*

10:15 AM

22.1 A 1.1V 16GB 640GB/s HBM2E DRAM with a Data-Bus Window-Extension Technique and a Synergetic On-Die ECC Scheme

C-S. Oh, K. C. Chun, Y-Y. Byun, Y-K. Kim, S-Y. Kim, Y. Ryu, J. Park, S. Kim, S. Cha, D. Shin, J. Lee, J-P. Son, B-K. Ho, S-J. Cho, B. Kil, S. Ahn, B. Lim, Y. Park, K. Lee, M-K. Lee, S. Baek, J. Noh, J-W. Lee, S. Lee, S. Kim, B. Lim, S-K. Choi, J-G. Kim, H-I. Choi, H-J. Kwon, J. J. Kong, K. Sohn, N. S. Kim, K-I. Park, J-B. Lee
Samsung Electronics, Hwaseong, Korea

10:45 AM

22.2 An 8.5Gb/s/pin 12Gb-LPDDR5 SDRAM with a Hybrid-Bank Architecture using Skew-Tolerant, Low-Power and Speed-Boosting Techniques in a 2nd generation 10nm DRAM Process

H-J. Chi, C-K. Lee, J. Park, J-S. Heo, J. Jung, D. Lee, D-H. Kim, D. Park, K. Kim, S-Y. Kim, J. Park, H. Cho, S. Lim, Y. Choi, Y. Lim, D. Moon, G. Park, J-H. Jang, K. Lee, I. Hwang, C. Kim, Y. Son, G-Y. Kang, K. Park, S. Lee, S-Y. Doo, C-H. Shin, B. Na, J. Kwon, K. R. Kim, H. Choi, S-K. Choi, S. Chang, W-I. Bae, H-J. Kwon, Y-S. Sohn, S-J. Bae, K-I. Park, J-B. Lee
Samsung Electronics, Hwaseong, Korea

11:15 AM

22.3 A 128Gb 8-High 512GB/s HBM2E DRAM with a Pseudo Quarter Bank Structure, Power Dispersion and an Instruction-Based At-Speed PMBIST

D. U. Lee, H. S. Cho, J. Kim, Y. J. Ku, S. Oh, C. D. Kim, H. W. Kim, W. Y. Lee, T. K. Kim, T. S. Yun, M. J. Kim, S. Lim, S. H. Lee, B. K. Yun, J. I. Moon, J. H. Park, S. Choi, Y. J. Park, C. K. Lee, C. Jeong, J-S. Lee, S. H. Lee, W. S. We, J. C. Yun, D. Lee, J. Shin, S. Kim, J. Lee, J. Choi, Y. Ju, M-J. Park, K. S. Lee, Y. Hur, D. Shim, S. Lee, J. Chun, K-W. Jin
SK hynix, Icheon, Korea

11:30 AM

22.4 A 32Gb/s Digital-Intensive Single-Ended PAM-4 Transceiver for High-Speed Memory Interfaces Featuring a 2-Tap Time-Based Decision Feedback Equalizer and an In-Situ Channel-Loss Monitor

P-W. Chiu, C. Kim
University of Minnesota, Minneapolis, MN

11:45 AM

22.5 An 8nm 18Gb/s/pin GDDR6 PHY with TX Bandwidth Extension and RX Training Technique

S-M. Lee, K. Seong, J. Shin, H. Kim, J. Jeong, S. Yi, J. Kim, E. Kim, S. Jung, S. Hwang, J. Oh, K. Chae, K-H. Koo, S. Park, J. Shin, J. Park
Samsung Electronics, Hwaseong, Korea

12:00 PM

22.6 A 0.8-to-2.3GHz Quadrature Error Corrector with Correctable Error Range of 101.6ps Using Minimum Total Delay Tracking and Asynchronous Calibration On-Off Scheme for DRAM Interface

S. Shin[1], H-G. Ko[1], S. Jang[2], D. Kim[2], D-K. Jeong[1]
[1]Seoul National University, Seoul, Korea
[2]SK hynix, Icheon, Korea

Conclusion 12:15 PM

Analog Techniques II

Session Chair: ***Yiannos Manoli,*** *University of Freiburg - IMTEK, Freiburg, Germany*
Session Co-Chair: ***Taeik Kim,*** *Samsung Electronics, Seongnam, Korea*

8:30 AM

23.1 A 4GS/s 80dB DR Current-Domain Analog Front-End for Phase-Coded Pulse-Compression Direct Time-of-Flight Automotive LiDAR
M. Kashmiri, B. Behroozpour, V. Petkov, K. Wojciechowski, C. Lang
Robert Bosch, Sunnyvale, CA

9:00 AM

23.2 A 70µW 1.19mm² Wireless Sensor with 32 Channels of Resistive and Capacitive Sensors and Edge-Encoded PWM UWB Transceiver
Y. Luo, Y. Li, A. V-Y. Thean, C-H. Heng, National University of Singapore, Singapore

9:30 AM

23.3 A 0-to-60V-Input V_{CM} Coulomb Counter with Signal-Dependent Supply Current and ±0.5% Gain Inaccuracy from -50°C to 125°C
C. van Vroonhoven, Analog Devices, Ismaning, Germany

Break 10:00 AM

10:15 AM

23.4 A 28W -108.9dB/-102.2dB THD/THD+N Hybrid ΔΣ-PWM Class-D Audio Amplifier with 91% Peak Efficiency and Reduced EMI Emission
S. Karmakar[1], H. Zhang[1], R. Van Veldhoven[2], L. Breems[2], M. Berkhout[3], Q. Fan[1], K.A.A. Makinwa[1]
[1]Delft University of Technology, Delft, The Netherlands
[2]NXP Semiconductors, Eindhoven, The Netherlands
[3]NXP Semiconductors, Nijmegen, The Netherlands

10:45 AM

23.5 A 0.41mA Quiescent Current, 0.00091% THD+N Class-D Audio Amplifier with Frequency Equalization for PWM-Residual-Aliasing Reduction
S-H. Chien, T-H. Kuo, H-Y. Huang, H-B. Wang, Y-Z. Qiu
National Cheng Kung University, Tainan, Taiwan

11:15 AM

23.6 A 2pA/√Hz Transimpedance Amplifier for Miniature Ultrasound Probes with 36dB Continuous-Time Gain Compensation
E. Kang[1], M. Tan[1], J-S. An[1], Z-Y. Chang[1], P. Vince[2], N. Sénégond[2], T. Mateo[2], C. Meynier[2], M. Pertijs[1]
[1]Delft University of Technology, Delft, The Netherlands
[2]VERMON, Tours, France

11:45 AM

23.7 A 130dB CMRR Instrumentation Amplifier with Common-Mode Replication
S. Zhang, C. Gao, X. Zhou, Q. Li
University of Electronic Science and Technology of China, Chengdu, China

12:00 PM

23.8 A 41µW 16MS/s 99.2dB-SFDR Capacitively Degenerated Dynamic Amplifier with Nonlinear-Slope-Factor Compensation
Y. Kim[1,2], S. Park [1,2], S. Song[1], S. Lee[1], M. Jang[1], C. Lee[1], Y. Chae[1]
[1]Yonsei University, Seoul, Korea
[2]Samsung Electronics, Hwaseong, Korea

Conclusion 12:15 PM

RF & mm-Wave Power Amplifiers

Session Chair: ***Swaminathan Sankaran,*** *Texas Instruments, Dallas, TX*
Session Co-Chair: ***Yves Baeyens,*** *Nokia - Bell Labs, Murray Hill, NJ*

8:30 AM

24.1 A 24-to-30GHz Watt-Level Broadband Linear Doherty Power Amplifier with Multi-Primary Distributed-Active-Transformer Power-Combining Supporting 5G NR FR2 64-QAM with >19dBm Average P_{out} and >19% Average PAE

F. Wang, H. Wang, Georgia Institute of Technology, Atlanta, GA

9:00 AM

24.2 A Reconfigurable Series/Parallel Quadrature-Coupler-Based Doherty PA in CMOS SOI with VSWR Resilient Linearity and Back-Off PAE for 5G MIMO Arrays

N. S. Mannem, M-Y. Huang, T-Y. Huang, S. Li, H. Wang
Georgia Institute of Technology, Atlanta, GA

9:30 AM

24.3 A 28GHz Current-Mode Inverse-Outphasing Transmitter Achieving 40%/31% PA Efficiency at P_{sat}/6dB PBO and Supporting 15Gbit/s 64-QAM for 5G Communication

S. Li, M-Y. Huang, D. Jung, T-Y. Huang, H. Wang
Georgia Institute of Technology, Atlanta, GA

Break 10:00 AM

10:15 AM

24.4 A Watt-Level Multimode Multi-Efficiency-Peak Digital Polar Power Amplifier with Linear Single-Supply Class-G Technique

S-W. Yoo, S-C. Hung, S-M. Yoo, Michigan State University, East Lansing, MI

10:45 AM

24.5 A 15b Quadrature Digital Power Amplifier with Transformer-Based Complex-Domain Power-Efficiency Enhancement

D. Zheng, Y. Yin, Y. Zhu, L. Xiong, Y. Li, N. Yan, H. Xu, Fudan University, Shanghai, China

11:15 AM

24.6 DS1 An Instantaneously Broadband Ultra-Compact Highly Linear PA with Compensated Distributed-Balun Output Network Achieving >17.8dBm P_{1dB} and >36.6% PAE_{P1dB} over 24 to 40GHz and Continuously Supporting 64-/256-QAM 5G NR Signals over 24 to 42GHz

F. Wang, H. Wang, Georgia Institute of Technology, Atlanta, GA

11:45 AM

24.7 A 15dBm 12.8%-PAE Compact D-Band Power Amplifier with Two-Way Power Combining in 16nm FinFET CMOS

B. Philippe, P. Reynaert, KU Leuven, Leuven, Belgium

12:00 PM

24.8 A W-Band Power Amplifier with Distributed Common-Source GaN HEMT and 4-Way Wilkinson-Lange Combiner Achieving 6W Output Power and 18% PAE at 95GHz

W. Wang[1,2], F. Guo[2], T. Chen[2], K. Wang[1]
[1]Tianjin University, Tianjin, China
[2]Science and Technology on Monolithic Integrated Circuits and Modules Laboratory, Nanjing, China

Conclusion 12:15 PM

Digital Power Delivery & Clocking Circuits

Session Chair: ***Keith Bowman,*** *Qualcomm, Raleigh, NC*
Session Co-Chair: ***Yvain Thonnart,*** *CEA-Leti, Grenoble, France*

8:30 AM

25.1 A Fully Synthesizable Distributed and Scalable All-Digital LDO in 10nm CMOS

S. Bang, W. Lim, C. Augustine, A. Malavasi, M. Khellah, J. Tschanz, V. De
Intel, Hillsboro, OR

9:00 AM

25.2 A 480mA Output-Capacitor-Free Synthesizable Digital LDO Using CMP-Triggered Oscillator and Droop Detector with 99.99% Current Efficiency, 1.3ns Response Time, and 9.8A/mm² Current Density

J. Oh, J-E. Park, Y-H. Hwang, D-K. Jeong, Seoul National University, Seoul, Korea

9:30 AM

25.3 A 65nm Edge-Chasing Quantizer-Based Digital LDO Featuring 4.58ps-FoM and Side-Channel-Attack Resistance DS2

Y. He, K. Yang, Rice University, Houston, TX

9:45 AM

25.4 A Scalable 20GHz On-Die Power-Supply Noise Analyzer with Compressed Sensing

P. Zhai, X. Zhou, Y. Cai, Z. Zhu, F. Zhang, Q. Li
University of Electronic Science and Technology of China, Chengdu, China

Break 10:00 AM

10:15 AM

25.5 A Self-Calibrated 1.2-to-3.8GHz 0.0052mm² Synthesized Fractional-N MDLL Using a 2b Time-Period Comparator in 22nm FinFET CMOS

S. Kundu, L. Chai, K. Chandrashekar, S. Pellerano, B. Carlton, Intel, Hillsboro, OR

10:45 AM

25.6 A 5.25GHz Subsampling PLL with a VCO-Phase-Noise Suppression Technique

H-H. Ting, T-C. Lee, National Taiwan University, Taipei, Taiwan

11:00 AM

25.7 Time-Borrowing Fast Mux-D Scan Flip-Flop with On-Chip Timing/Power/V_{MIN} Characterization Circuits in 10nm CMOS

A. Agarwal[1], S. Hsu[1], S. Realov[1], M. Anders[1], G. Chen[1], M. Kar[1], R. Kumar[1], H. Sumbul[1], P. Knag[1], H. Kaul[1], S. Mathew[1], M. Kumashikar[2], R. Krishnamurthy[1], V. De[1]
[1]Intel, Hillsboro, OR; [2]Intel, Bangalore, India

11:15 AM

25.8 A Near-Threshold-Voltage Network-on-Chip with a Metastability Error Detection and Correction Technique for Supporting a Quad-Voltage/Frequency-Domain Ultra-Low-Power System-on-a-Chip

C. Lin[1], W. He[1], Y. Sun[1], B. Pei[1], Z. Mao[1], M. Seok[2]
[1]Shanghai Jiao Tong University, Shanghai, China; [2]Columbia University, New York, NY

11:45 AM

25.9 Reconfigurable Transient Current-Mode Global Interconnect Circuits in 10nm CMOS for High-Performance Processors with Wide Voltage-Frequency Operating Range

M. A. Anders, H. Kaul, S. Kim, G. K. Chen, R. Kumar, H. E. Sumbul, P. C. Knag, M. Kar, S. K. Hsu, A. Agarwal, V. Suresh, S. K. Mathew, R. K. Krishnamurthy, V. De
Intel, Hillsboro, OR

Conclusion 12:15 PM

Biomedical Innovations

Session Chair: ***Jerald Yoo,*** *National University of Singapore, Singapore*
Session Co-Chair: ***Esther Rodriguez-Villegas,*** *Imperial College London, London, United Kingdom*

8:30 AM

26.1 A 4.5mm² Multimodal Biosensing SoC for PPG, ECG, BIOZ and GSR Acquisition in Consumer Wearable Devices DS2

Y-S. Shu, Z-X. Chen*, Y-H. Lin, S-H. Wu, W-H. Huang, A. Y-C. Chiou, C-Y. Huang, H-Y. Hsieh, F-W. Liao, T-F. Zou, P. Chen,* *Equally-Credited Authors (ECAs), MediaTek, Hsinchu, Taiwan

9:00 AM

26.2 A Neuromorphic Multiplier-Less Bit-Serial Weight-Memory-Optimized 1024-Tree Brain-State Classifier and Neuromodulation SoC with an 8-Channel Noise-Shaping SAR ADC Array

G. O'Leary[1], J. Xu[1], L. Long[1], J. Sales Filho[1], C. Tejeiro[1], M. ElAnsary[1], C. Tang[1], H. Moradi[2], P. Shah[1], T. A. Valiante[3], R. Genov[1]
[1]University of Toronto, Toronto, Canada; [2]Krembil Neuroscience Center, Toronto, ON, Canada
[3]Toronto Western Hospital, Toronto, Canada

9:30 AM

26.3 A Closed-Loop Neuromodulation Chipset with 2-Level Classification Achieving 1.5V_{pp} CM Interference Tolerance, 35dB Stimulation Artifact Rejection in 0.5ms and 97.8% Sensitivity Seizure Detection DS2

Y. Wang[1], Q. Sun[1], H. Luo[1], X. Chen[2], X. Wang[3], H. Zhang[1]
[1]Xi'an Jiaotong University, Xi'an, China; [2]Hangzhou Nuowei Medical Technology, Hangzhou, China
[3]Xi'an Aerosemi Technology, Xi'an, China

Break 10:00 AM

10:15 AM

26.4 A Cell-Capacitance-Insensitive CMOS Sample-and-Hold Chronoamperometric Sensor for Real-Time Measurement of Small Molecule Drugs in Whole Blood DS2

J-C. Chien, H. T. Soh, A. Arbabian, Stanford University, Stanford, CA

10:30 AM

26.5 A 20μW Heartbeat Detection System-on-Chip Powered by Human Body Heat for Self-Sustaining Wearable Healthcare DS2

S. Bose, B. Shen*, M. L. Johnston*
*Equally-Credited Authors (ECAs), Oregon State University, Corvallis, OR

10:45 AM

26.6 A 6.5μW 10kHz-BW 80.4dB-SNDR Continuous-Time ΔΣ Modulator with G_m-Input and 300mV_{pp} Linear Input Range for Closed-Loop Neural Recording

C. Lee[1], T. Jeon[1], M. Jang[1], S. Park[2], Y. Huh[3], Y. Chae[1]
[1]Yonsei University, Seoul, Korea; [2]University of Science and Technology, Daejeon, Korea
[3]Catholic Kwandong University, Incheon, Korea

11:15 AM

26.7 A 280μW 108dB DR Readout IC with Wireless Capacitive Powering Using a Dual-Output Regulating Rectifier for Implantable PPG Recording

F. Marefat, R. Erfani, K. L. Kilgore, P. Mohseni, Case Western Reserve University, Cleveland, OH

11:45 AM

26.8 A Trimodal Wireless Implantable Neural Interface System-on-a-Chip DS2

Y. Jia[1], U. Guler[2], Y-P. Lai[3], Y. Gong[4], A. Weber[4], W. Li[4], M. Ghovanloo[5]
[1]North Carolina State University, Raleigh, NC; [2]WPI, Worcester, MA
[3]Georgia Institute of Technology, Atlanta, GA; [4]Michigan State University, East Lansing, MI
[5]Bionic Sciences, Atlanta, GA

12:00 PM

26.9 A 0.19×0.17mm² Wireless Neural Recording IC for Motor Prediction with Near-Infrared-Based Power and Data Telemetry DS2

J. Lim[1], E. Moon[1], M. Barrow[1], S. R. Nason[1], P. R. Patel[1], P. G. Patil[1], S. Oh[1], I. Lee[1], H-S. Kim[1], D. Sylvester[1], D. Blaauw[1], C. A. Chestek[1], J. Phillips[1], T. Jang[2]
[1]University of Michigan, Ann Arbor, MI; [2]ETH Zürich, Zürich, Switzerland

Conclusion 12:15 PM

IoT & Security

Session Chair: ***Hirofumi Shinohara,*** *Waseda University, Fukuoka, Japan*
Session Co-Chair: ***James Myers,*** *Arm, Cambridge, United Kingdom*

1:30 PM

27.1 A 65nm Energy-Harvesting ULP SoC with 256kB Cortex-M0 Enabling an DS2 89.1µW Continuous Machine Health Monitoring Wireless Self-Powered System

J. K. Brown[1], D. Abdallah[2], J. Boley[3], N. Collins[1], K. Craig[2], G. Glennon[2], K-K. Huang[3], C. J. Lukas[2], W. Moore[3], R. K. Sawyer[2], Y. Shakhsheer[2,4], F. B. Yahya[2], A. Wang[3], N. E. Roberts[2], D. D. Wentzloff[1], B. H. Calhoun[2]
[1]Everactive, Ann Arbor, MI
[2]Everactive, Charlottesville, VA
[3]Everactive, Santa Clara, CA
[4]now with Analog Devices, Fort Collins, CO

2:00 PM

27.2 M0N0: A Performance-Regulated 0.8-to-38MHz DVFS ARM Cortex-M33 DS2 SIMD MCU with 10nW Sleep Power

P. Prabhat[1], B. Labbe[1], G. Knight[1], A. Savanth[1], J. Svedas[1], M. J. Walker[1], S. Jeloka[2], P. M-Y. Fan[1], F. García-Redondo[1], T. Achuthan[1], J. Myers[1]
[1]ARM, Cambridge, United Kingdom
[2]ARM, Austin, TX

2:15 PM

27.3 EM and Power SCA-Resilient AES-256 in 65nm CMOS Through >350× DS2 Current-Domain Signature Attenuation

D. Das[1], J. Danial[1], A. Golder[2], N. Modak[1], S. Maity[1], B. Chatterjee[1], D. Seo[1], M. Chang[2], A. Varna[3], H. Krishnamurthy[4], S. Mathew[4], S. Ghosh[4], A. Raychowdhury[2], S. Sen[1]
[1]Purdue University, West Lafayette, IN
[2]Georgia Institute of Technology, Atlanta, GA
[3]Intel, Chandler, AZ
[4]Intel Labs, Portland, OR

2:30 PM

27.4 Physically Unclonable Function in 28nm FDSOI Technology Achieving High Reliability for AEC-Q100 Grade 1 and ISO26262 ASIL-B

Y. Choi, B. Karpinskyy, K-M. Ahn, Y. Kim, S. Kwon, J. Park, Y. Lee, M. Noh
Samsung Electronics, Hwaseong, Korea

Break 3:00 PM

User Interaction & Diagnostic Technologies

Session Chair: ***Masayuki Miyamoto,*** *Wacom, Shinjuku, Japan*
Session Co-Chair: ***Johan Vanderhaegen,*** *Google, Mountain View, CA*

3:15 PM

28.1 A Capacitive Touch Chipset with 33.9dB Charge-Overflow Reduction Using Amplitude-Modulated Multi-Frequency Excitation and Wireless Power and Data Transfer to an Active Stylus

J-S. An[1], J-H. Ra[2], E. Kang[1], M. A. P. Pertijs[1], S-H. Han[3]
[1]Delft University of Technology, Delft, The Netherlands
[2]SK hynix, Icheon, Korea
[3]Leading UI, Anyang, Korea

3:30 PM

28.2 A 51dB-SNR 120Hz-Scan-Rate 32×18 Segmented-VCOM LCD In-Cell Touch-Display-Driver IC with 96-Channel Compact Shunt-Sensing Self-Capacitance Analog Front-End

H. Jang, H. Shin, J. Lee, C. Yoo, K. Chun, I. Yun
Sentron, Daejeon, Korea

4:00 PM

28.3 A 5.2Mpixel 88.4dB-DR 12in CMOS X-Ray Detector with 16b Column-Parallel Continuous-Time ΔΣ ADCs DS1

S. Lee[1], J. Jeong[2], T. Kim[1], C. Park[1], T. Kim[2], Y. Chae[1]
[1]Yonsei University, Seoul, Korea
[2]Rayence, Hwaseong, Korea

4:30 PM

28.4 A CMOS Multimodality In-Pixel Electrochemical and Impedance Cellular Sensing Array for Massively Paralleled Synthetic Exoelectrogen Characterization DS1

D. Jung[1], S. R. Kumashi[1], J. Park[2], S. T. Sanz[3], S. Grijalva[4], A. Wang[1], S. Li[1], H. C. Cho[4], C. Ajo-Franklin[5], H. Wang[1]
[1]Georgia Institute of Technology, Atlanta, GA
[2]Intel, Hillsboro, OR
[3]Lawrence Berkeley National Laboratory, Berkeley, CA
[4]Emory University, Atlanta, GA
[5]Rice University, Houston, TX

Conclusion 4:45 PM

Emerging RF & THz Techniques

Session Chair: ***Hua Wang,*** *Georgia Institute of Technology, Atlanta, GA*
Session Co-Chair: ***Shuhei Amakawa,*** *Hiroshima University, Hiroshima, Japan*

1:30 PM

29.1 A 0.42THz 9.2dBm 64-Pixel Source-Array SoC with Spatial Modulation Diversity for Computational Terahertz Imaging DS2

R. Jain, P. Hillger, J. Grzyb, U. R. Pfeiffer, University of Wuppertal, Wuppertal, Germany

2:00 PM

29.2 A 0.59THz Beam-Steerable Coherent Radiator Array with 1mW Radiated Power and 24.1dBm EIRP in 40nm CMOS

K. Guo, P. Reynaert, KU Leuven, Leuven, Belgium

2:30 PM

29.3 Non-Magnetic 0.18μm SOI Circulator with Multi-Watt Power Handling Based on Switched-Capacitor Clock Boosting DS1

A. Nagulu, T. Chen, G. Zussman, H. Krishnaswamy
Columbia University, New York, NY

2:45 PM

29.4 High-Performance Isolators and Notch Filters Based on N-Path Negative Transresistance DS2

M. Khorshidian[1], N. Reiskarimian*[1,2], H. Krishnaswamy[1]*
*Equally-Credited Authors (ECAs), [1]Columbia University, New York, NY
[2]Massachusetts Institute of Technology, Cambridge, MA

Break 3:00 PM

3:15 PM

29.5 Sub-THz CMOS Molecular Clock with 43ppt Long-Term Stability Using High-Order Rotational Transition Probing and Slot-Array Couplers DS1

C. Wang, X. Yi, M. Kim, R. Han
Massachusetts Institute of Technology, Cambridge, MA

3:45 PM

29.6 A 660-to-676GHz 4×2 Oscillator-Radiator Array with Intrinsic Frequency-Filtering Feedback for Harmonic Power Boost Achieving 7.4dBm EIRP in 40nm CMOS

G. Guimaraes, P. Reynaert, KU Leuven, Leuven, Belgium

4:15 PM

29.7 A 490GHz 32mW Fully Integrated CMOS Receiver Adopting Dual-Locking FLL

K-S. Choi[1], D. R. Utomo[1], K-M. Kim[1], B-H. Yun[1], S-G. Lee[1], I-Y. Lee[2]
[1]KAIST, Daejeon, Korea; [2]Chosun University, Gwangju, Korea

4:45 PM

29.8 THzID: A 1.6mm² Package-Less Cryptographic Identification Tag with Backscattering and Beam-Steering at 260GHz

M. I. Ibrahim[1], M. I. W. Khan[1], C. S. Juvekar[2], W. Jung[1], R. T. Yazicigil[3], A. P. Chandrakasan[1], R. Han[1]
[1]Massachusetts Institute of Technology, Cambridge, MA
[2]Analog Devices, Boston, MA; [3]Boston University, Boston, MA

5:00 PM

29.9 A 4×4 Distributed Multi-Layer Oscillator Network for Harmonic Injection and THz Beamforming with 14dBm EIRP at 416GHz in a Lensless 65nm CMOS IC

H. Saeidi, S. Venkatesh, C. R. Chappidi, T. Sharma, C. Zhu, K. Sengupta
Princeton University, Princeton, NJ

Conclusion 5:15 PM

Efficient Wireless Connectivity

Session Chair: ***Yao-Hong Liu,*** *imec-Netherlands, Eindhoven, The Netherlands*
Session Co-Chair: ***Yuu Watanabe,*** *Waseda University, Atsugi, Japan*

1:30 PM

30.1 A Temperature-Robust 27.6nW -65dBm Wakeup Receiver at 9.6GHz X-Band
P. Bassirian, D. Duvvuri, D. S. Truesdell, N. Liu, B. H. Calhoun, S. M. Bowers
University of Virginia, Charlottesville, VA

2:00 PM

30.2 NB-IoT and GNSS All-in-One System-on-Chip Integrating RF Transceiver, 23dBm CMOS Power Amplifier, Power Management Unit and Clock Management System for Low-Cost Solution
J. Lee, J. Han, C. Lo, J. Lee, W. Kim, S. Kim, B. Kang, J. Han, S. Jung, T. Nomiyama, J. Lee, T. B. Cho, I. Kang, Samsung Electronics, Hwaseong, Korea

2:30 PM

30.3 DS1 A SAW-Less NB-IoT RF Transceiver with Hybrid Polar and On-Chip Switching PA Supporting Power Class 3 Multi-Tone Transmission
H. Guo, T. F. Chan, Y. T. Lai, K. C. Wan, L. Chen, W. P. Wong
Hong Kong Applied Science and Technology Research Institute, Hong Kong, China

Break 3:00 PM

3:15 PM

30.4 A 370µW 5.5dB-NF BLE/BT5.0/IEEE 802.15.4-Compliant Receiver with >63dB Adjacent Channel Rejection at >2 Channels Offset in 22nm FDSOI
B. J. Thijssen[1], E. A. M. Klumperink[1], P. Quinlan[2], B. Nauta[1]
[1]University of Twente, Enschede, The Netherlands; [2]Analog Devices, Cork, Ireland

3:30 PM

30.5 A 0.5V BLE Transceiver with a 1.9mW RX Achieving -96.4dBm Sensitivity and 4.1dB Adjacent Channel Rejection at 1MHz Offset in 22nm FDSOI
M. Tamura[1], H. Takano[1], S. Shinke[1], H. Fujita[1], H. Nakahara[1], N. Suzuki[1], Y. Nakada[1], Y. Shinohe[1], S. Etou[1], T. Fujiwara[2], Y. Katayama[1]
[1]Sony Semiconductor Solutions, Atsugi, Japan; [2]Sony LSI Design, Atsugi, Japan

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30.6 DS1 A Low-Power BLE Transceiver with Support for Phase-Based Ranging, Featuring 5µs PLL Locking Time and 5.3ms Ranging Time, Enabled by Staircase-Chirp PLL with Sticky-Lock Channel-Switching
E. Bechthum[1], J. Dijkhuis[1], M. Ding[1], Y. He[1], J. Van den Heuvel[1], P. Mateman[1], G-J. van Schaik[1], K. Shibata[2], M. Song[1], E. Tiurin[1], S. Traferro[1], Y-H. Liu[1], C. Bachmann[1]
[1]imec-Netherlands, Eindhoven, The Netherlands; [2]Renesas Electronics, Tokio, Japan

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30.7 A Crystal-Less BLE Transmitter with -86dBm Frequency-Hopping Back-Channel WRX and Over-the-Air Clock Recovery from a GFSK-Modulated BLE Packet
A. Alghaihab[1], X. Chen[1], Y. Shi[1], D. S. Truesdell[2], B. H. Calhoun[2], D. D. Wentzloff[1]
[1]University of Michigan, Ann Arbor, MI; [2]University of Virginia, Charlottesville, VA

5:00 PM

30.8 DS2 A 3.5mm×3.8mm Crystal-Less MICS Transceiver Featuring Coverages of ±160ppm Carrier Frequency Offset and 4.8-VSWR Antenna Impedance for Insertable Smart Pills
M. Song[1], M. Ding[1], E. Tiurin[1], K. Xu[1,2], E. Allebes[1], G. Singh[1], P. Zhang[1], S. Traferro[1], H. Korpela[1], N. van Helleputte[3], R. B. Staszewski[2], Y-H. Liu[1], C. Bachmann[1]
[1]imec-Netherlands, Eindhoven, The Netherlands; [2]University College Dublin, Dublin, Ireland
[3]imec, Heverlee, Belgium

Conclusion 5:15 PM

Digital Circuit Techniques for Emerging Applications

Session Chair: ***Alicia Klinefelter,*** *Nvidia, Durham, NC*
Session Co-Chair: ***Mijung Noh,*** *Samsung Electronics, Yong-in, Korea*

1:30 PM

31.1 A 65nm 8.79TOPS/W 23.82mW Mixed-Signal Oscillator-Based NeuroSLAM Accelerator for Applications in Edge Robotics
J-H. Yoon, A. Raychowdhury
Georgia Institute of Technology, Atlanta, GA

2:00 PM

31.2 CIM-Spin: A 0.5-to-1.2V Scalable Annealing Processor Using Digital Compute-In-Memory Spin Operators and Register-Based Spins for Combinatorial Optimization Problems
Y. Su, H. Kim*, B. Kim*
*Equally-Credited Authors (ECAs)
Nanyang Technological University, Singapore

2:30 PM

31.3 A Compute-Adaptive Elastic Clock-Chain Technique with Dynamic Timing Enhancement for 2D PE-Array-Based Accelerators
T. Jia, Y. Ju, J. Gu
Northwestern University, Evanston, IL

Break 3:00 PM

Power Management Techniques

Session Chair: ***Chanhong Chern,*** *TSMC, Hsinchu, Taiwan*
Session Co-Chair: ***Li Geng,*** *Xi'an Jiaotong University, Xi'an, China*

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32.1 A 13.56MHz Current-Mode Wireless Power and Data Receiver with Efficient Power Extracting Controller and Energy-Shift Keying Technique for Loosely Coupled Implantable Devices

S-W. Hong
Sookmyung Women's University, Seoul, Korea

3:45 PM

32.2 Self-Tunable Phase-Shifted SECE Piezoelectric Energy-Harvesting IC with a 30nW MPPT Achieving 446% Energy-Bandwidth Improvement and 94% Efficiency

A. Morel[1], A. Quelen[1], C. A. Berlitz[1], D. Gibus[1], P. Gasnier[1], A. Badel[2], G. Pillonnet[1]
[1]CEA-LETI-MINATEC, Grenoble, France
[2]Université Savoie-Mont Blanc, Annecy, France

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32.3 Electromagnetic Mechanical Energy-Harvester IC with No Off-Chip Component and One Switching Period MPPT Achieving up to 95.9% End-to-End Efficiency and 460% Energy-Extraction Gain

A. Quelen, G. Pillonnet, P. Gasnier, F. Rummens, S. Boisseau
CEA-LETI-MINATEC, Grenoble, France

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32.4 A 0.4-to-1.2V 0.0057mm^2 55fs-Transient-FoM Ring-Amplifier-Based Low-Dropout Regulator with Replica-Based PSR Enhancement

J-E. Park, J. Hwang, J. Oh, D-K. Jeong
Seoul National University, Seoul, Korea

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32.5 A Scalable and PCB-Friendly Daisy-Chain Approach to Parallelize LDO Regulators with 2.613% Current-Sharing Accuracy Using Dynamic Element Matching for Integrated Current Sensing

B. Talele[1], R. Magod[2], K. Kunz[3], S. Manandhar[2], B. Bakkaloglu[1]
[1]Arizona State University, Tempe, AZ
[2]Texas Instruments, Dallas, TX
[3]Texas Instruments, Tucson, AZ

Conclusion 5:15 PM

Non-Volatile Devices for Future Architecture

Session Chair: ***Munehiko Nagatani,*** *NTT, Atsugi, Japan*
Session Co-Chair: ***Nick Van Helleputte,*** *imec, Heverlee, Belgium*

1:30 PM

33.1 A 74 TMACS/W CMOS-RRAM Neurosynaptic Core with Dynamically Reconfigurable Dataflow and In-situ Transposable Weights for Probabilistic Graphical Models

DS2

W. Wan[1], R. Kubendran[2], S. B. Eryilmaz[1], W. Zhang[3], Y. Liao[3], D. Wu[3], S. Deiss[2], B. Gao[3], P. Raina[1], S. Joshi[4], H. Wu[3], G. Cauwenberghs[2], H-S. P. Wong[1]
[1]Stanford University, Stanford, CA
[2]University of California, San Diego, CA
[3]Tsinghua University, Beijing, China
[4]University of Notre Dame, Notre Dame, IN

2:00 PM

33.2 A Fully Integrated Analog ReRAM Based 78.4TOPS/W Compute-In-Memory Chip with Fully Parallel MAC Computing

DS2

Q. Liu[1], B. Gao[1], P. Yao[1], D. Wu[1], J. Chen[1], Y. Pang[1], W. Zhang[1], Y. Liao[1], C-X. Xue[2], W-H. Chen[2], J. Tang[1], Y. Wang[1], M-F. Chang[2], H. Qian[1], H. Wu[1]
[1]Tsinghua University, Beijing, China
[2]National Tsing Hua University, Hsinchu, Taiwan

2:30 PM

33.3 Via-Switch FPGA: 65nm CMOS Implementation and Architecture Extension for AI Applications

M. Hashimoto[1], X. Bai[2], N. Banno[2], M. Tada[2], T. Sakamoto[2], J. Yu[1], R. Doi[1], Y. Araki[3], H. Onodera[3], T. Imagawa[4], H. Ochi[4], K. Wakabayashi[5], Y. Mitsuyama[6], T. Sugibayashi[2]
[1]Osaka University, Suita, Japan
[2]NEC, Tsukuba, Japan
[3]Kyoto University, Kyoto, Japan
[4]Ritsumeikan University, Kusatsu, Japan
[5]NEC, Kawasaki, Japan
[6]Kochi University of Technology, Kami, Japan

Break 3:00 PM

Biomedical Sensing, Stimulation & Harvesting

Session Chair: ***Rabia Yazicigil,*** *Boston University, Boston, MA*
Session Co-Chair: ***Edoardo Charbon,*** *EPFL, Neuchatel, Switzerland*

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34.1 A 64×64 Implantable Real-Time Single-Charged-Particle Radiation DS1 Detector for Cancer Therapy

K. Lee[1], J. Scholey[2], E. B. Norman[1], I. K. Daftari[2], K. K. Mishra[2], B. A. Faddegon[2], M. M. Maharbiz[1], M. Anwar[2]
[1]University of California, Berkeley, CA
[2]University of California, San Francisco, CA

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34.2 1225-Channel Localized Temperature-Regulated Neuromorphic Retinal-DS1 Prosthesis SoC with 56.3nW/Channel Image Processor

J. H. Park[1], J. S. Y. Tan [1], H. Wu[1], J. Yoo[1,2]
[1]National University of Singapore, Singapore
[2]N.1 Institute for Health, Singapore

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34.3 An 8.2mm³ Implantable Neurostimulator with Magnetoelectric Power and Data Transfer

Z. Yu, J. C. Chen*, B. W. Avants, Y. He, A. Singer, J. T. Robinson, K. Yang*
*Equally-Credited Authors (ECAs)
Rice University, Houston, TX

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34.4 A 4.5mm³ Deep-Tissue Ultrasonic Implantable Luminescence Oxygen Sensor

S. Sonmezoglu, M. M. Maharbiz
University of California, Berkeley, CA

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34.5 Human-Body-Coupled Power-Delivery and Ambient-Energy-Harvesting DS2 ICs for a Full-Body-Area Power Sustainability

J. Li[1], Y. Dong*[1], J. H. Park[1], L. Lin[1], T. Tang[1], M. Zhang[1], H. Wu[1], L. Zhang[1], J. S. Y. Tan[1], J. Yoo[1,2]*
*Equally-Credited Authors (ECAs)
[1]National University of Singapore, Singapore
[2]N.1 Institute for Health, Singapore

5:00 PM

34.6 EEG Dust: A BCC-Based Wireless Concurrent Recording/Transmitting DS1 Concentric Electrode

T. Tang[1], L. Yan[2], J. H. Park[1], H. Wu[1], L. Zhang[1], H. Y. B. Lee[1], J. Yoo[1,3]
[1]National University of Singapore, Singapore
[2]Samsung Electronics, Suwon, Korea
[3]N.1 Institute for Health, Singapore

Conclusion 5:15 PM

Short Course: Circuit Design in Advanced CMOS Technologies — Considerations and Solutions

Time:	Topic:
8:00 AM	Breakfast
8:20 AM	Introduction by Chair, ***Daniel Friedman*** *IBM Thomas J. Watson Research Center, Yorktown Heights, NY*
8:30 AM	**Device and Physical Design Considerations for Circuits in FinFET Technology** ***Alvin Leng Sun Loke,*** *TSMC, San Diego, CA*
10:00 AM	Break
10:30 AM	**Modeling and RF Design Considerations for Advanced CMOS Technology** ***Ali M. Niknejad,*** *University of California at Berkeley, Berkeley, CA*
12:15 PM	Lunch
1:20 PM	**High-Speed and Mixed-Signal Circuit Design Techniques in FinFET Technology for Wireline and Optical Interface Applications** ***Jonathan E. Proesel,*** *IBM T. J. Watson Research Center, Yorktown Heights, NY*
2:50 PM	Break
3:20 PM	**Embedded Memory and Support-Circuitry Design Considerations in Advanced CMOS Technology** ***Eric Karl,*** *Intel, Portland, OR*
4:50 PM	Conclusion

Introduction

Technology scaling in CMOS has brought with it an ever-growing set of constraints and challenges that must be faced not only by the technologist but also by the circuit designer. Understanding the restrictions imposed by the technology and incorporating strategies to achieve design goals in light of those restrictions are both critical to successful development of state-of-the art CMOS integrated circuits in advanced nodes, especially those using FinFET devices. In this short course, the first presentation will provide a framework for understanding physical design constraints and physical design approaches in the context of FinFET technology and how such constraints will influence circuit design. The second presentation will discuss approaches to RF circuit design in the context of advanced CMOS nodes. The third presentation will cover the design of critical mixed-signal circuits in FinFET technology, including high-speed I/O building blocks and optical interface circuits. Finally, the fourth presentation will cover the design of embedded memory elements in advanced node technology, focusing on SRAM and associated support circuitry.

SC1: Device and Physical Design Considerations for Circuits in FinFET Technology

Alvin Leng Sun Loke, *TSMC, San Diego, CA*

CMOS scaling remains economically lucrative with 7nm mobile SoCs commercialized since late 2018 and 5nm products imminently available. Modest feature-size reduction and process innovations optimized for logic and SRAM scaling continue to offer compelling node-to-node power, performance, area, and cost benefits. This talk provides an overview of the key process technology elements that have enabled the FinFET CMOS nodes and highlights the resulting technology impact on design.

Alvin Loke is a Director in the TSMC San Diego Design Center focusing on analog design methodologies and technology co-optimization in advanced CMOS. He received his PhD from Stanford in 1999, spent several years in CMOS process integration, and worked on wireline/clocking design and design/technology interface at Agilent, AMD, and Qualcomm. Alvin has authored over 50 publications and 28 patents. He is currently a VLSI Symposia TPC member, SSCS Webinar Coordinator for North America, and San Diego SSCS Chapter Chair. He previously served as a Distinguished Lecturer, CICC TPC member, and JSSC and SSCL Guest Editor. Alvin is recipient of the Canadian NSERC 1967 Scholarship, 2005 SSCS Outstanding Chapter Award, and CICC 2018 Best Paper Award.

SC2: Modeling and RF Design Considerations for Advanced CMOS Technology

Ali M. Niknejad, *University of California at Berkeley, Berkeley, CA*

Advanced CMOS technology nodes are extremely complex marvels of engineering, offering nanoscale devices and metallization approaching terahertz speeds. In this tutorial, we will consider fundamental transistor and circuit properties such as gain, bandwidth, noise, and distortion. We will discuss how circuit design is impacted by advanced technology parameters and how to model these effects to design robust RF circuits.

Ali M. Niknejad received the Ph.D. degree in electrical engineering from the University of California, Berkeley. He holds the Donald O. Pederson Distinguished Professorship chair in the EECS department at UC Berkeley and is a faculty co-director of the Berkeley Wireless Research Center (BWRC). He is also the Associate Director of the Center for Converged TeraHertz Communications and Sensing (ComSenTer). Professor Niknejad is the recipient the 2017 IEEE Transactions on Circuits and Systems Darlington Best Paper Award, the 2017 Most Frequently Cited Paper Award (2010 to 2016) from the Symposium on Very Large-Scale Integration Circuits, the CICC 2015 Best Invited Paper Award, and the 2012 ASEE Frederick Emmons Terman Award.

SC3: High-Speed and Mixed-Signal Circuit Design Techniques in FinFET Technology for Wireline and Optical Interface Applications

Jonathan E. Proesel, *IBM T. J. Watson Research Center, Yorktown Heights, NY*

Getting the best possible performance from analog and mixed-signal circuits requires a strong understanding of the underlying IC technology. Advanced FinFET CMOS technologies have the potential for excellent analog and mixed-signal performance. However, these technologies have many pitfalls for the unwary designer: highly restrictive design rules, thin metal layers, and device self-heating, to name a few problems. This talk explores how to capture the benefits and avoid the problems of FinFET technology in high-speed wireline communications circuits. The talk begins with a brief introduction to wireline communications circuits. Then it discusses FinFET technology and the impact to high-speed wireline circuits. A set of example circuit designs in 14nm FinFET are reviewed, studying system, circuit, and layout details. Finally, the talk concludes with a set of tips and techniques to get the most out of FinFET technologies.

Jonathan Proesel is a Research Staff Member at IBM T. J. Watson Research Center, where he has conducted circuit design research since 2010. He has designed analog and mixed-signal circuits in many silicon technologies, such as 130nm SiGe BiCMOS, 90nm SOI CMOS with monolithically integrated Si photonics, and 14 and 7nm FinFET. His primary research focus is high-speed optical and electrical wireline communications, and his other interests include silicon photonics, data converters, AI hardware, and design-technology co-optimization. He received the Ph.D. degree from Carnegie Mellon University in 2010. He is a co-recipient of the 2010 IEEE CICC Best Student Paper Award and the 2018 IEEE Photonics Technology Journal Best Paper Award. At IBM, he has received multiple technical awards. He serves on the technical program committee for the Symposium on VLSI Circuits.

SC4: Embedded Memory and Support-Circuitry Design Considerations in Advanced CMOS Technology

Eric Karl, *Intel, Portland, OR*

Rapidly accelerating compute requirements are driving the need for improved bandwidth, reduced latency, higher density and better energy efficiency from the memory hierarchy. Embedded memories play a critical role in mitigating the latency and bandwidth limitations of accessing external, storage-class memories. This course will explore the challenges of embedded SRAM, DRAM, MRAM and RRAM in advanced technologies and focus on state-of-the-art-circuit techniques used to assist memory functionality and performance.

Eric Karl (S'03–M'08) received B.S.E., M.S.E. and Ph.D. degrees in Electrical Engineering from the University of Michigan, Ann Arbor, Michigan in 2002, 2004 and 2008, respectively. Dr. Karl held positions at Intel Circuit Research Lab, IBM T.J. Watson Research Center and Sun Microsystems prior to 2008. In 2008, he joined Intel Logic Technology Development, where he is a Senior Principal Engineer engaged in the development of memory circuit technology for low-power and high-performance SoC applications. Dr. Karl has published 27 conference papers and technical journal articles.

F3: Machine Learning Processors: From High Performance Applications to Architectures and Benchmarking

Organizers: **SukHwan Lim**, *Samsung S.LSI, Hwaseong, Korea*
Andreas Burg, *EPFL, Lausanne, Switzerland*
Alicia Klinefelter, *Nvidia, Durham, NC*
Muhammad Khellah, *Intel, Hillsboro, OR*

Committee: **Vivek De,** *Intel, Hillsboro, Oregon*
Boris Murmann, *Stanford University, Stanford, CA*
Masato Motomura, *Tokyo Tech, Yokohama, Japan*

Custom processors are becoming more ubiquitous in the Machine Learning (ML) space, but motivating their design through informed application constraints has been challenging in this emerging and rapidly evolving area. Additionally, ML processors range from pure inference devices to general purpose processors with training capabilities and should not be designed at the hardware level in isolation. This forum looks across the HW and SW stacks to focus on 1) analyzing key ML applications, 2) which inference, but also training algorithms are of interest; 3) how custom designed ML processor architectures are driven by applications and algorithms, 4) how ML processors can be benchmarked on applications that matter. As such, the forum gives audience insights on effective ML processor development by shedding light on applications, algorithms, architectures, benchmarking, and time to market perspectives.

Agenda

Time	Topic
8:00 AM	Breakfast
8:15 AM	**Opening & Introduction**
8:20 AM	**Evolution of DNN Accelerators: From Big Cloud to Small Mobile Deep Learning** **Hoi-Jun Yoo**, *KAIST, Daejeon, Korea*
9:05 AM	**Hardware Opportunities in the Machine Learning Lifecycle** **Joseph Gonzales,** *University of California Berkeley, Berkeley, CA*
9:50 AM	Break
10:00 AM	**Towards a Holistic Co-Design Strategy for Efficient ML Processor Architectures** **Gu-Yeon Wei,** *Samsung Research, Seoul, Korea & Harvard University, Cambridge, MA*
10:45 AM	**Tearing Down the Deep Learning Memory Wall: A Roadmap for Low-Power and High-Performance AI** **Francesco Conti,** *ETH Zürich, Switzerland & University of Bologna, Italy*
11:30 AM	**Specializing The Software Stack For Machine Learning** **Greg Diamos**, *Landing AI, Palo Alto, CA*
12:15 PM	Lunch
1:30 PM	**Global-Scale FPGA-Accelerated DNN Inference** **Steven K. Reinhardt,** *Microsoft, Bellevue, WA*
2:15 PM	**Heterogeneous Computing Platforms for Autonomous Vehicles** **Shimpei Kato,** *University of Tokyo, Japan & Tier IV, Japan*
3:00 PM	Break
3:15 PM	**The Vision Behind MLPerf: A Community-Driven ML Benchmark Suite for Software Frameworks and Hardware Accelerators in Cloud and Edge Computing** **Vijay Janapa Reddi,** *Harvard University, Cambridge, MA*
4:00 PM	**Panel Discussion:** **How Should ML Processors be Benchmarked on Applications That Matter?**
4:45 PM	Conclusion

F4: Cutting Edge Advances in Electrical and Optical Transceiver Technologies

Organizers: **Thomas Toifl,** *Cisco Systems, Zurich, Switzerland*
Munehiko Nagatani, *NTT, Atsugi, Kanagawa, Japan*

Committee: **Andrew Joy,** *Marvell, Irvine, CA*
Frederic Giansello, *STMicroelectronics, Crolles, France*
Mounir Meghelli, *IBM, Yorktown Heights, NY*
Sudip Shekhar, *University of British Columbia, Vancouver, Canada*

This forum reviews current state of the art and future prospects of wireline interfaces and electronic-photonic integration technologies for ultrahigh-speed links.

Electrical interface speeds are reaching 112Gb/s but are now facing severe limitations due to channel bandwidth, power consumption and circuit complexity. The first part of the forum discusses standards, modulation formats, signaling and circuit techniques of state-of-the art transceivers and how to potentially overcome these limitations above 112Gb/s.

With increasing demand on bandwidth, optical links are constantly expanding into new territory. The second part of the forum will review electronic-photonic integrated subsystems, which are now commercially produced in high volumes. In particular, silicon photonics technologies, including foundry services, design tools, and packaging, have matured rapidly in the past few years. Also, enabled by electronic-photonic integration technology, coherent optical communication and DWDM become feasible at high volume. Although currently the main application of electronic-photonic integration technology is long-reach optical communications, its application at shorter-reach promises to overcome the bandwidth limitations of electrical links in the future.

Agenda

Time	Topic
8:00 AM	Breakfast
8:15 AM	**Introduction** **Thomas Toifl,** *Cisco Systems, Zurich, Switzerland*
8:20 AM	**Ethernet's Optical Expansion** **John D'Ambrosia,** *Futurewei, Plano, TX*
9:05 AM	**Future Signaling and Coding:** **Channel Limitations and Potential Solutions above 112G** **Amin Shokrollahi,** *Kandou Bus and EPFL, Lausanne, Switzerland*
9:50 AM	Break
10:00 AM	**Advanced Transceiver Design for 112Gb/s and Beyond Electrical Interfaces** **Ronan Casey,** *Xilinx, Cork, Ireland*
10:45 AM	**7nm FinFET DSP-Based High-Speed Low-Power Transceiver Design** **Matteo Pisati,** *eSilicon, Pavia, Italy*
11:30 AM	**Recent Advancement in Silicon Photonics Foundry** **Luo XianShu,** *Advanced Micro Foundry (AMF), Singapore*
12:15 PM	Lunch
1:30 PM	**Integrated Silicon Photonics Components for High-Speed Transceivers** **Yuliya Akulova,** *Intel, Santa Clara, CA*
2:15 PM	**Advanced Optical Coherent Transceivers Based on Electronic-Photonic Integration Technology** **Takashi Saida,** *NTT, Kanagawa, Japan*
3:00 PM	Break
3:15 PM	**Monolithic Silicon-Photonic Platforms in CMOS SOI Processes** **Vladimir Stojanovic,** *Ayar Labs, CA*
4:00 PM	Conclusion

F5: Power Management as an Enabler of Future SoC's

Organizers: **Jason Stauth,** *Dartmouth College, Hanover, NH*
Yogesh Ramadass, *Texas Instruments, Santa Clara, CA*
Li Geng, *Xi'an Jiaotong University, Xi'an, China*

Committee: **Gerard Villar-Pique,** *NXP Semiconductor, Eindhoven, The Netherlands*
Patrick Mercier, *University of California, San Diego, CA*
Mingoo Seok, *Columbia University, NY*

This forum will explore a number of trends, topologies, and technologies in support of high-density and fully-integrated power management. System-level strategies for power integration will be explored, such as fine-grained dynamic voltage and frequency scaling and envelope tracking. New architectures for power conversion will be discussed, based on hybrid-resonant switched capacitor topologies as well as high conversion-ratio multiphase converters for performance computing. The forum will also provide an overview of key limitations such as packaging and heat dissipation in high-density power electronics and next generation integrated circuit passive components including silicon-integrated magnetics.

Agenda

Time	Topic
8:00 AM	Breakfast
8:15 AM	**Opening & Introduction** **Jason Stauth,** *Dartmouth College, Hanover, NH*
8:20 AM	**System-Level Power Management Strategies for Integrated Platforms** **Vivek De,** *Intel, Hillsboro, OR*
9:05 AM	**Next-Generation Circuit Architectures for Power-Supply on Chip** **Hanh-Phuc Le,** *University of California, San Diego, CA*
9:50 AM	Break
10:00 AM	**Distributed Networks of Ultra-Fast Microregulators for Large Scale SoC** **Zeynep Toprak-Deniz,** *IBM, Yorktown Heights, NY*
10:45 AM	**Advanced Supply Modulator Architectures for Envelope Tracking in 5G Mobile Handset** **Dongsu Kim,** *Samsung Electronics, South Korea*
11:30 AM	**Monolithic Multi-Phase Converters for Medium to High-Current Application Processors** **Juha Pennanen,** *Texas Instruments, Oulu, Finland*
12:15 PM	Lunch
1:30 PM	**Integrated Passive Components for Power Supply in Package and Power Supply on Chip - Technology Capabilities and Applications** **Cian Ó Mathúna,** *Tyndall National Institute, University College Cork, Ireland*
2:15 PM	**Packaging Techniques for High Power Density Converter Applications** **Jayden Kim,** *HANA Micron, Korea*
3:00 PM	Break
3:15 PM	**Future Power Passive Components: Chip-Scale Magnetics and High-Q Resonant Structures** **Charles R. Sullivan,** *Dartmouth College, Hanover, NH*
4:00 PM	Conclusion

F6: Sensors for Health

Organizer: ***Matteo Perenzoni,*** *FBK, Trento, Italy*

Committee: ***Bruce Rae,*** *STMicroelectronics, Edinburgh, United Kingdom*
Nick Van Helleputte, *IMEC, Leuven, Belgium*
Patrick Mercier, *University of California, San Diego, CA*
Naveen Verma, *Princeton University, Princeton, NJ*

The forum will discuss application challenges, state-of-the-art and future solutions for health sensing. The talks span the full range from sensor components to applications showing how integrated circuits play a crucial role. Fundamental sensor components, implantable devices, flexible/wearable technology, and advanced circuit design techniques specifically tailored for health sensing will be addressed. Furthermore there will be a clear view on the various emerging sensing techniques and application domains in the health space such as SPAD devices and THz sensing, and how the needs in those domains create opportunities for innovation in ASIC design.

Agenda

Time	Topic
8:00 AM	Breakfast
8:15 AM	**Introduction** **Matteo Perenzoni,** *FBK, Trento, Italy*
8:20 AM	**The Opportunities and Challenges of Silicon ICs in Biosensing Platforms: From mm-Scale Multiplexed Bio-Molecular Sensors to Cell-Based Assays** **Kaushik Sengupta,** *Princeton University, Princeton, NJ*
9:05 AM	**Neural Sensors: Developing Brain-Computer Interfaces** **Arto Nurmikko,** *Brown University, Providence, RI*
9:50 AM	Break
10:00 AM	**Conformal Thin-Film Electronics** **Takao Someya,** *University of Tokyo, Tokyo, Japan*
10:45 AM	**Flexible Electronics for Medical Imaging: From Patches to Large-Area X-Ray Imaging** **Kris Myny,** *IMEC, Leuven, Belgium*
11:30 AM	**SPADs, ISFETs and Photodiodes: Mixed-Mode Sensing for Healthcare** **David Cumming,** *University of Glasgow, Glasgow, United Kingdom*
12:15 PM	Lunch
1:30 PM	**CMOS Sensor Architectures and Circuital Solutions for Nuclear Medicine: From Scintillator-Based dSiPM to Monolithic Detectors** **Nicola Massari,** *FBK, Trento, Italy*
2:15 PM	**CMOS/BiCMOS THz System-on-Chip for Life-Science Applications** **Ullrich Pfeiffer,** *University of Wuppertal, Wuppertal, Germany*
3:00 PM	Break
3:15 PM	**Circuit Design for Ultrasound on a Chip** *(Short demo at the end of presentation)* **Kailiang Chen,** *Butterfly Network, Guilford, CT*
4:00 PM	Conclusion

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Tuesday,	February 18	8:00 am to 3:00 pm
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Demonstration Sessions: Hardware demonstrations will support selected papers on Monday and Tuesday evenings.

Author Interviews: Author Interviews will be held Monday, Tuesday and Wednesday evenings. Authors from each day's papers will be available to discuss their work.

Social Hour: Social Hour refreshments will be available starting at 5:15 pm.

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-The **Digest of Technical Papers** on USB. This year, as part of your Conference registration, the e-Digest of Technical Papers will be provided on a USB, as well as part of the download. The e-Digest will include all 3 pages for each paper. Also, the print Digest will be available at a cost of $75, but does not include the 3rd page (additional figures and references). Note that all 3 pages for each paper will be available on IEEE Xplore.

-**Papers Visuals:** The visuals from all papers presented will be available by download.

-**Demonstration Session Guidebook:** A descriptive guide to the Demonstration Session will be available by download.

-**Note:** Instructions will be provided for access to all downloads. Downloads will be available both during the Conference and for a limited time afterwards.

OPTIONAL EVENTS

Educational Events: Many educational events are available at ISSCC for an additional fee. There are ten 90-minute Tutorials and two all-day Forums on Sunday. There are four additional all-day Forums on Thursday as well as an all-day Short Course. All events include a course handout in color. The Forums and Short Course include breakfast, lunch and break refreshments. The Tutorials include break refreshments. See the schedule for details of the topics and times. A "Thursday All-Access Pass" is available that provides access to all Thursday educational events and a copy of each course handout. Pick just the speakers you want to hear!

OPTIONAL PUBLICATIONS

ISSCC 2020 Publications: The following ISSCC 2020 publications can be purchased in advance or on site:

2020 ISSCC Download USB: All of the downloads included in conference registration, (regular papers and presentations) **(mailed in March).**

2020 Digest of Technical Papers in hard copy**.**

2020 Tutorials USB: All of the 90 minute Tutorials **(mailed in June).**

2020 Short Course USB: Circuit Design in Advanced CMOS Technologies —Considerations and Solutions" **(mailed in June)**.

The Short Course and Tutorial USBs contain audio and written English transcripts synchronized with the presentation visuals. In addition, the USBs contain a pdf file of the presentations and pdf files of key reference material.

Earlier ISSCC Publications: Selected publications from earlier conferences can be purchased. There are several ways to purchase this material:

-Items listed on the registration website can be purchased with registration and picked up at the conference.

-Visit the ISSCC Publications Desk. This desk is located in the registration area and has the same hours as conference registration. With payment by cash, check or credit card, you can purchase materials at this desk. See the posted list at the Conference for titles and prices.

-Visit the ISSCC website at www.isscc.org and click on the link "About/Shop ISSCC/Shop Now" where you can order online or download an order form to mail, email or fax. For a small shipping fee, this material will be sent to you immediately and you will not have to wait until you attend the Conference to get it.

HOW TO MAKE HOTEL RESERVATIONS

Online: ISSCC participants are urged to make their hotel reservations at the San Francisco Marriott Marquis online. Go to the conference website and click on the Hotel Reservation link. **Conference room rates are $285 for a single/double, $310 for a triple and $335 for a quad** (per night plus tax). In addition, ISSCC attendees booked in the ISSCC group receive **in-room Internet access for free**. All online reservations require the use of a credit card. Online reservations are confirmed immediately. You should print the page containing your confirmation number and reservation details and bring it with you when you travel to ISSCC.

Telephone: Call 877-622-3056 (US) or 415-896-1600 and ask for "Reservations." When making your reservation, identify the group as ISSCC 2020 to get the group rate.

Hotel Deadline: Reservations must be received at the San Francisco Marriott Marquis no later than 5 pm Pacific Time January 26, 2020 to obtain the special ISSCC rates. A limited number of rooms are available at these rates. **Once this limit is reached or after January 26th, the group rates may no longer be available and reservations will be filled at the best available rate.** Changes: Before the hotel deadline, your reservation can be changed by calling the telephone numbers above. After the hotel deadline, call the Marriott Marquis at 415-896-1600 (ask for "Reservations"). Have your hotel confirmation number ready.

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Conference Website:	www.isscc.org	
ISSCC Email:	ISSCC@ieee.org	
Registration questions:	ISSCCinfo@yesevents.com	
Hotel Information:	San Francisco Marriott Marquis 780 Mission Street San Francisco, CA 94103	Phone: 415-896-1600
Press Information:	Kenneth C. Smith University of Toronto Email: lcfujino@aol.com	Phone: 416-418-3034
Registration:	YesEvents PO Box 3024 Westminster, MD 21158 Email: issccinfo@yesevents.com	Phone: 800-937-8728 Fax: 410-559-2236

Hotel Transportation: Visit the ISSCC website "Registration/Transportation from Airport" page for helpful travel information and links. You can get a map and driving directions from the hotel website at
www.marriott.com/hotels/travel/sfodt-san-francisco-marriott-marquis/

Next ISSCC Dates and Location:
ISSCC 2021 will be held on February 14-18, 2021
at the San Francisco Marriott Marquis Hotel.

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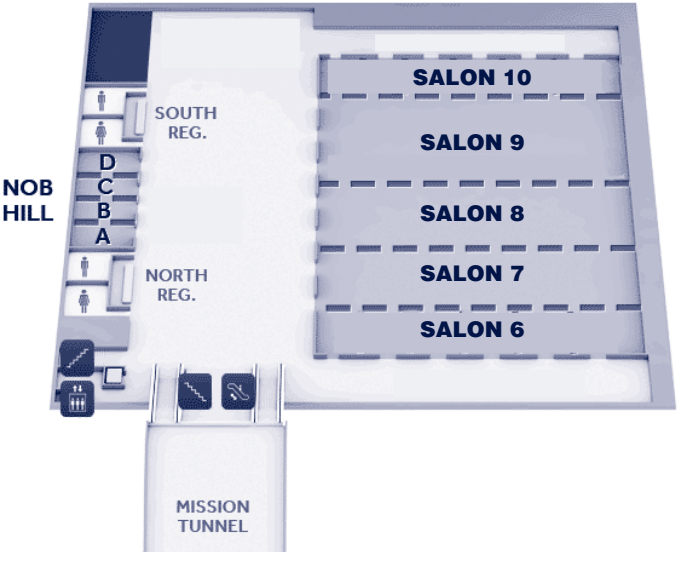
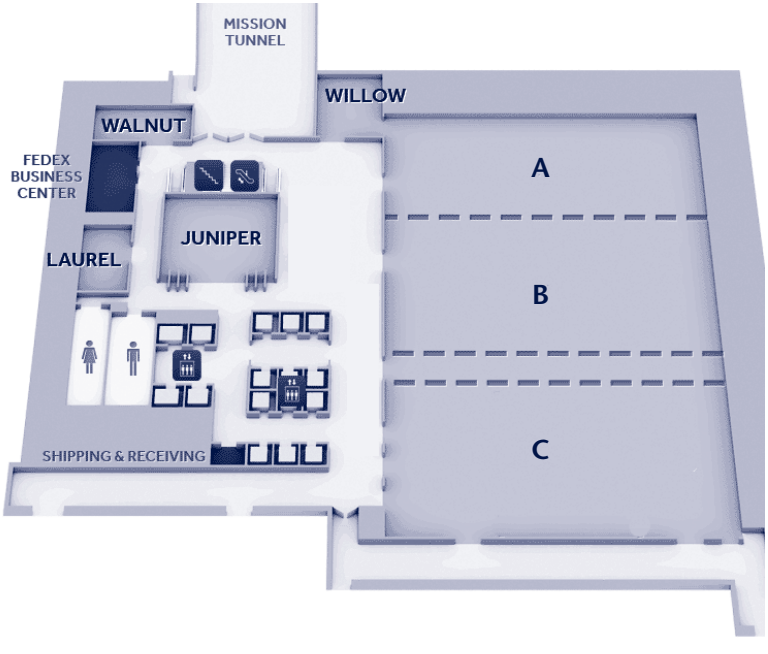
Lower B2 Level - Yerba Buena Ballroom



B2 Level - Golden Gate Hall



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