



2019

PRESS KIT



ISSCC Press Kit Disclaimer

The material presented here is preliminary.

As of November 6, 2018, there is not enough information to guarantee its correctness.

Thus, it must be used with some caution.

ISSCC 2019

VISION STATEMENT

The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and use to maintain technical currency, and to network with leading experts.

Table of Contents

Table of Contents.....	4
Preamble.....	7
FAQ on ISSCC.....	7
Overview: ISSCC 2019 – Envisioning the Future.....	10
Plenary Session (Session 1).....	10
Plenary Session — Invited Papers.....	12
Evening Events.....	15
How to Save Lives with Circuits.....	15
Student Research Preview.....	15
Industry Showcase.....	15
Student Event: Making a Career Choice.....	17
Evening Panel: Moving to 'The Dark Side'!.....	17
Evening Panel: How Can Hardware Designers Reclaim the Spotlight?.....	17
Session Overviews and Highlights.....	18
Conditions of Publication.....	19
PREAMBLE.....	19
FOOTNOTE.....	19
Session 2 Overview: Processors.....	20
Session 2 Highlights: Processors.....	21
Session 3 Overview: Nyquist Rate ADCs.....	22
Session 3 Highlights: Nyquist Rate ADCs.....	23
Session 4 Overview: Power Amplifiers.....	24
Session 4 Highlights: Power Amplifiers.....	25
Session 5 Overview: Image Sensors.....	27
Session 5 Highlights: Image Sensors.....	28
Session 6 Overview: Ultra-High-Speed Wireline.....	29
Session 6 Highlights: Ultra High Speed Wireline.....	30
Session 7 Overview: Machine Learning.....	32
Session 7 Highlights: Machine Learning.....	33
Session 8 Overview: DC-DC converters.....	35
Session 8 Highlights: Hybrid DC-DC Converter.....	36
Session 9 Overview: High-Frequency Transceivers for Radar and Communication.....	37
Session 9 Highlights: High-Frequency Transceivers for Radar and Communications.....	38
Session 10 Overview: Sensor Interfaces.....	39
Session 10 Highlights: Sensor Interfaces.....	40

<i>Session 11 Overview: Diagnostics</i>	41
<i>Session 11 Highlights: Diagnostics</i>	42
<i>Session 12 Overview: Emerging Technologies</i>	43
<i>Session 12 Highlights: Emerging Technologies</i>	44
<i>Session 13 Overview: Nonvolatile Memories</i>	45
<i>Session 13 Highlights: Nonvolatile Memories</i>	46
<i>Session 14 Overview: Machine Learning and Digital LDO Circuits</i>	48
<i>Session 14 Highlights: Machine-Learning and Digital LDO Circuits</i>	49
<i>Session 15 Overview: Power for 5G, Wireless Power, and GaN Converters</i>	51
<i>Session 15 Highlights: Power for 5G, Wireless Power and GaN Converters</i>	52
<i>Session 16 Overview: Frequency Synthesizers</i>	53
<i>Session 16 Highlights: Frequency Synthesizers</i>	54
<i>Session 17 Overview: Technologies for Human Interaction & Health</i>	55
<i>Session 17 Highlights: Technologies for Human Interaction & Health</i>	56
<i>Session 18 Overview: Analog Techniques</i>	57
<i>Session 18 Highlights: Analog Techniques</i>	58
<i>Session 19 Overview: Adaptive Digital and Clocking Techniques</i>	59
<i>Session 19 Highlights: Adaptive Digital and Clocking Techniques</i>	61
<i>Session 20 Overview: Noise-Shaped and VCO-Based ADCs</i>	62
<i>Session 20 Highlights: Noise-Shaped and VCO-Based ADCs</i>	63
<i>Session 21 Overview: 4G/5G Transceivers</i>	64
<i>Session 21 Highlights: 4G/5G Transceivers</i>	65
<i>Session 22 Overview: Physiological Monitoring</i>	67
<i>Session 22 Highlights: Physiological Monitoring</i>	68
<i>Session 23 Overview: DRAM</i>	69
<i>Session 23 Highlights: DRAM</i>	70
<i>Session 24 Overview: SRAM and Computation-in-Memory</i>	72
<i>Session 24 Highlights: SRAM and Computation-In-Memory</i>	73
<i>Session 25 Overview: Circuits Enabling Security</i>	74
<i>Session 25 Highlights: Circuits Enabling Security</i>	75
<i>Session 26 Overview: Frequency Generation and Interference Mitigation</i>	76
<i>Session 26 Highlights: Frequency Generation and Interference Mitigation</i>	77
<i>Session 27 Overview: Energy Harvesting & DC/DC Control Techniques</i>	78
<i>Session 27 Highlights: Energy Harvesting & DC/DC Control Techniques</i>	79
<i>Session 28 Overview: Techniques for Low-Power & High-Performance Wireless</i>	81
<i>Session 28 Highlights: Techniques for Low-Power and High-Performance Wireless</i>	82
<i>Session 29 Overview: Quantum & Photonics Technologies</i>	83

<i>Session 29 Highlights: Quantum & Photonics Technologies</i>	84
<i>Session 30 Overview: Advanced Wireline Techniques</i>	85
<i>Session 30 Highlights: Advanced Wireline Techniques</i>	87
<i>Trends</i>	88
<i>Conditions of Publication</i>	89
<i>PREAMBLE</i>	89
<i>FOOTNOTE</i>	89
<i>Analog – 2019 Trends</i>	91
<i>Power Management – 2019 Trends</i>	92
<i>Data Converters – 2019 Trends</i>	93
<i>RF Subcommittee – 2019 Trends</i>	98
<i>Wireless – 2019 Trends</i>	100
<i>Wireline – 2019 Trends</i>	102
<i>Digital Architectures & Systems (DAS) – 2019 Trends</i>	106
<i>Digital Circuits – 2019 Trends</i>	111
<i>Memory – 2019 Trends</i>	114
<i>IMMD – 2019 Trends (Medical)</i>	120
<i>IMMD – 2019 Trends (Imagers)</i>	121
<i>Technology Directions – 2019 Trends</i>	122
<i>INDEX</i>	124
<i>Technical Topics Mapped to Papers</i>	125
<i>Selected Presenting Companies/Institution Mapped to Papers</i>	125
<i>Contact Information</i>	131

Preamble

FAQ on ISSCC

What is ISSCC?

ISSCC (International Solid-State Circuits Conference) is the **flagship** conference of the IEEE Solid-State Circuits Society. According to the SIA, the Semiconductor industry generated US\$412.2 billion in sales in 2017 and ISSCC continues to be the premier technical forum for presenting advances in solid-state circuits and systems.

Who Attends ISSCC?

Attendance at ISSCC 2019 is expected to be around **3000**. Corporate attendees from the semiconductor and system industries typically represent around **60%**.

Where is ISSCC?

The **66th ISSCC** will be held at the San Francisco Marriott Marquis on February 17th through February 21st 2019.

Are there Keynote Speakers?

After a day devoted to educational events, ISSCC 2019 begins formally on Monday, February 18, 2019 with four exciting plenary talks:

- Yann LeCun, Facebook AI Research & New York University, New York, NY
- Hoi-Jun Yoo, KAIST, Daejeon, Republic of Korea
- Meint K. Smit, Eindhoven University of Technology, Eindhoven, The Netherlands
- Vida Ilderem, Intel, Hillsboro, OR

What is the Technical Coverage at ISSCC?

ISSCC covers a full spectrum of design approaches in advanced technical areas broadly categorized as: (1) Communication Systems, (2) Analog Systems, (3) Digital Systems, and (4) Innovations including micro-machines and MEMS, imagers, sensors, biomedical devices, as well as forward-looking developments that may take three or more years for commercialization.

How are ISSCC Papers Selected?

Currently around 600 submissions are received each year across the broad spectrum of specified topics. Review is by a team of over 150 scientific and industry experts from the Far-East, Europe, and North America. These experts are organized into 11 Sub-Committees that cover the 4 broad areas described earlier:

- **Communication Systems** includes Wireless, RF, and Wireline Subcommittees
- **Analog Systems** includes Analog, Power Management, and Data Converter Subcommittees
- **Digital Systems** includes Memory, Digital Circuits, and Digital Architectures and Systems Subcommittees
- **Innovative Topics** includes Imagers/MEMS/Medical Devices/Displays and Technology Directions Subcommittees

What Companies are Presenting this year?

Companies presenting papers at ISSCC 2019 include Analog Devices, Broadcom, Hitachi, Huawei, IBM, Intel, MediaTek, NXP Semiconductors, Panasonic, Qualcomm, Renesas, Samsung, Sony, Texas Instruments, TSMC and Toshiba, just to name a few. A more complete list can be found in the Index.

Are there educational sessions?

ISSCC features a variety of educational events which include:

- Ten Tutorials (targeted toward participants looking to broaden their horizon)
- Six Forums (targeted toward experts in an information sharing context)
- One Short Course (targeted toward in-depth appreciation of a current hot topic)

Are There Other Events?

A more complete list of all activities at ISSCC 2019:

- Four Plenary Presentations
- Four Invited Talks on System Issues
- Technical Sessions (30 distinct sessions)
- Six Evening Events and Panels, including:
 - Two Evening Panels
 - Industry Showcase
 - Workshop on Circuits for Social Good
 - Student Research Preview (for the introduction of graduate-student research-in-progress)
 - Student Event: Making a Career Choice
- Educational Sessions Featuring:
 - Ten Tutorials
 - Six Forums
 - One Short Course
- Demonstration Sessions from Academia and Industry
- Networking Social Events
- Author Interview Sessions

- *A Number of University Alumni Events*
- *Book Display*

How Do I Use this Press Kit?

The Press Kit provides a PREAMBLE section that features this FAQ and other general information. The kit also includes SESSION OVERVIEWS AND HIGHLIGHTS of all 30 technical sessions into which the 197 papers are grouped, together with brief descriptions and context for each. As well, there is an abstract for each of the Plenary talks. For your convenience, the Kit includes two structural charts in the INDEX section: (a) a list of the 4 Technical Topics and their associated Subcommittees (11) and Sessions (30); (b) a list of contributing companies and institutions with their associated papers. Thus, to located information of interest you can access Chart 4.1 to identify sessions of interest, after which you might logically access its Session's Overview or Highlight section. Alternatively, if your interest is in particular organization then Chart 4.1 will direct you immediately to papers of interest each of which is detailed in its corresponding Session Overview and possibly in the Highlights section. For anyone's interest it is useful to use Chart 4.1 to access the appropriate Trend information which provides a broad historical view of the context of your interest and often includes reference to current ISSCC 2019 papers.

Anything New This Year?

ISSCC will hold an expanded Industry Showcase event the evening of Monday, February 18th, where companies will provide short "pitches" on their technology/product innovation, followed by an interactive session with attendees at individual company booths/tables. That evening ISSCC will also hold an event for students, "Making a Career Choice", where distinguished panelists from industry, start-ups, academia and research will offer career advice and insights and answer audience questions.

Overview: ISSCC 2019 – Envisioning the Future

The relentless progress of solid-state circuits and systems has a profound impact on our daily lives, changing the way we work, communicate, and even socialize. The advancements in Silicon IC technology predicted by Moore's Law have been fueling this progress, but pursuing this trend further becomes increasingly more challenging from technology and economic perspectives. Stimulated by these difficulties, the solid-state circuit community is exploring a multiplicity of paths for further development: from novel technologies (innovative devices and integration techniques, such as qubits, spintronics, 3D, and photonic integration), to original approaches (such as Artificial Intelligence (AI) and Machine Learning (ML)), to new applications (such as wearable electronics, IoT, virtual reality, autonomous driving, robotics, and many more).

Plenary Session (Session 1)

The Plenary Session on the morning of Monday, February 18, 2019, will feature four renowned speakers:

- *Yann LeCun, Facebook AI Research & New York University, New York, NY, will discuss “The Next Challenge in AI: Self-Supervised Learning”, and why self-supervised learning will be built around deep learning architectures that are considerably larger than current ones, requiring vastly more powerful hardware than what we have today.*
- *Hoi-Jun Yoo, KAIST, Daejeon, Republic of Korea, will give his insights into “Intelligence on Silicon: From Deep Neural Network Accelerators to Brain-Mimicking AI-SoCs”, and will explain how mobile learning and brain mimicking will be the two horses driving the carriage called AI, thus opening up new requirements for the next generation deep learning SoCs.*
- *Meint K. Smit, Eindhoven University of Technology, Eindhoven, The Netherlands, will describe “Integration of Photonics and Electronics”, and will describe the current status and future developments of InP-based generic integration platforms.*
- *Vida Ilderem, Intel, Hillsboro, OR, will discuss “5G Wireless Communication: An Inflection Point” and will highlight the disruptive architectures and technology innovations required to make 5G and beyond a reality.*

Highlights of these Plenary talks are provided in the following section.

ISSCC 2019

PLENARY SESSION – INVITED PAPERS

Plenary Session — Invited Papers

Chair: **Jan Van der Spiegel**, University of Pennsylvania, PA
ISSCC Conference Chair

Associate Chair: **Eugenio Cantatore**, Eindhoven University of Technology, Eindhoven, The Netherlands
ISSCC International Technical-Program Chair

1.1 The Next Challenge in AI: Self-Supervised

Yann LeCun, Facebook AI Research & New York University, New York, NY

Deep learning has caused revolutions in computer understanding of images, audio, and text, enabling new applications such as information search and filtering, autonomous driving, radiology screening, real-time language translation, and virtual assistants. But almost all these successes largely use supervised learning, which requires human-annotated data, or reinforcement learning, which requires too many trials to be practical in most real world situations. In contrast, animals and humans seem to learn vast amounts of background knowledge about the world through mere observation and occasional actions in a self-supervised manner. Making progress in self-supervised learning is the main challenge of AI for the next decade. Success may result in machines with some level of common sense. But they will be built around deep learning architectures that are considerably larger than current ones, requiring vastly more powerful hardware than what we have today.

1.2 Intelligence on Silicon: From Deep Neural Network Accelerators to Brain-Mimicking AI-SoCs

Hoi-Jun Yoo, KAIST, Daejeon, Republic of Korea

Deep learning is influencing not only the technology itself but also our everyday lives. Formerly, most AI functionalities and applications were centralized on datacenters. However, the primary platform for AI has recently shifted to mobile devices. With the increasing demand on mobile AI, conventional hardware solutions face their ordeal because of their low energy efficiency on such power hungry applications. For the past few years, dedicated DNN accelerators inference have been under the spotlight. However, with the rising emphasis on privacy and personalization, ability to learn on mobile platform is becoming the second hurdle for “on-device AI.” Going hand in hand, the brain mimicking is also a highlighted field in AI. Fundamentals of neuromorphic architecture start from the synapses and the neurons, which are realized with custom memories including non-volatile memories. The brain mimicking AI is not restricted to the naïve neuron implementation, but it extends further to mimic the behavioral characteristics such as “connectome” or “visual attention.” In conclusion, mobile learning and brain mimicking will be the two horses driving the carriage called AI, thus opening up new requirements for the next generation deep learning SoCs.

1.3 Integration of Photonics and Electronics

Meint K. Smit, Eindhoven University of Technology, Eindhoven, The Netherlands

The application market for Photonic Integrated Circuits (PICs) is rapidly growing. Photonic Integration is the dominant technology in high bandwidth communications and is set to become dominant in many fields of photonics, just like microelectronics in the field of electronics. Photonic integrated circuits offer compelling performance advances in terms of precision, bandwidth and energy efficiency. To enable uptake in new sectors, the availability of highly standardized (generic) photonic integration platform technologies is of key importance as this separates design from technology, reducing barriers for new entrants. The major platform technologies today are InP-based monolithic integration and Silicon Photonics. In this perspective paper we will describe the current status and future developments of InP-based generic integration platforms.

1.4 5G Wireless Communication: An Inflection Point

Vida Ilderem, Intel, Hillsboro, OR

The 5G era is upon us, ushering in new opportunities for technology innovation across the computing and connectivity landscape. 5G presents an inflection point where wireless communication technology is driven by application and expected use cases, and where the network will set the stage for data-rich services and sophisticated cloud apps, delivered faster and with lower latency. This paper will highlight the disruptive architectures and technology innovations required to make 5G and beyond a reality.

ISSCC 2019

EVENING EVENTS

Evening Events

ISSCC 2019 will continue the popular tradition of evening panels and evening sessions, where experts, often of opposing views, discuss topics which range from the lighthearted to the controversial (but always informative and entertaining!). This year's panels are "Moving to 'The Dark Side!'" and "How Can Hardware Designers Reclaim the Spotlight?".

In addition, ISSCC 2019 will include additional evening events including a Workshop on How to Save Lives with Circuits, an Industry Showcase, a Student Research Preview, and a Making a Career Choice event.

How to Save Lives with Circuits

Sunday, February 17

The workshop highlights circuits and their impact on healthcare-related industries. The goal of the panel is to provide perspectives from system architects, security experts and circuit designers on where we should be heading with the large amount of data that is being generated from more-advanced tests and increased monitoring of our current health status.

Security and privacy problems with medical devices and IOT devices in general are in the news on an almost daily basis. One example from 2017 stated: "FDA issues recall of 465,000 pacemakers to patch security holes." Once medical data is obtained reliably and securely, it is stored on remote servers and in remote databases where there are risks of leaks and data breaches of private medical records. However, it is difficult to put the genie back into the bottle! We have asked our distinguished panel to discuss how circuit designers can contribute to bolster our trust in medical devices and in electronic healthcare systems that manage private medical records. We also encourage the audience to propose attacks and countermeasures.

Student Research Preview

Sunday, February 17

The Student Research Preview (SRP) will highlight selected student research projects in progress. The SRP consists of 90 second presentations followed by a Poster Session, by graduate students from around the world, which have been selected on the basis of a short submission concerning their on-going research.

This year, the SRP will be presented in three theme sections. "Digital and Machine Learning Circuits and Systems", "Data Converters and Clocking", and "Analog and Wireless Circuits".

The Student Research Preview will include the talk "Machine Learning: The Next Big Opportunity for Chip Designers" by Marian Verhelst, Professor, KU Leuven

Industry Showcase

Monday, February 18

ISSCC will hold a plenary Industry Showcase event on the evening of Monday, February 18th, which will highlight how advances in silicon circuits, SoCs and systems are fueling the most innovative industrial applications and products of the future.

The event will begin with a Showcase Keynote "Accelerated Platforms: The Future of Computing" by William J. Dally, Chief Scientist and Senior Vice President of Research, NVIDIA Corporation, Santa Clara, CA and Professor (Research) of EE and CS, Stanford University, Palo Alto, CA. With the end of Moore's Law and Dennard Scaling, domain-specific accelerators remain one of the few ways to continue to improve performance and efficiency of computing hardware. A GPU provides an ideal substrate on which to build a domain-specific accelerator. An efficient high-performance memory system, on-chip interconnect, and highly-parallel, general-purpose execution engine supports domain-specific units that can be added for specific applications. NVIDIA's GPUs provide domain-specific

acceleration for graphics, ray tracing, scientific computing, and deep learning. These accelerated GPUs are used to power platforms for gaming, professional graphics, high-performance computing, data analytics, AI, autonomous vehicles, and robotics.

Following the keynote, the Industry Showcase will feature short presentations as well as interactive demonstrations from each of the Industry Showcase participants, and represent an exciting introduction to the next generation of applications and products enabled by advances in solid-state integrated circuits. The table below highlights the preliminary list of participants in the Industry Showcase.

Participant	Title	Highlight
Altia Systems, Inc. Cupertino, CA	180° Real-time Immersive, Intelligent Vision Systems	Features the Altia real-time 180° intelligent vision system, producing 2D Panoramic-4K and 3D 4K video, which includes AI-based people / object detection capabilities.
ams AG Premstätten, Austria	Direct Time-of-Flight Module in CMOS 55nm HV for Mobile Applications	Showcases AMS' Direct Time-of-Flight Module, based on SPAD detectors, which is able to discriminate multiple objects in the field of view with no hinder from the glass covering the sensor.
Ayar Labs Emeryville, CA	TeraPHY: A high-density electronic-photonic chiplet for co-packaged optical I/O	Demonstrates Ayar Labs's TeraPHY: a high-density electronic-photonic chip enabling communication with 16 wavelengths at 25Gbps/wavelength (400Gbps aggregate bandwidth on a fiber) with a reach up to several kilometers.
Healthrian Daejeon, Korea	Impedance-based Sensor Chip for Non-invasive Blood Pressure	Showcases the Healthrian's non-invasive blood pressure monitor, which exploits impedance measurements to enable a wrist-band form factor.
IBM T. J. Watson Research Center Yorktown Heights, NY	Fast channel sounding and beam optimization for 5G using software defined phased array radios	Showcases the IBM Research 28-GHz software defined phased array radio, able to optimize an indoor 5G communication link in the presence of reflectors and interferers thanks to ultrafast electronic beams steering.
NUFRONT Beijing, China	The world's first deployed URLLC wireless communication system and SoCs	Shows Nufont's EUHT (Enhanced Ultra High Throughput) Wireless Communication System, the world's first Ultra Reliable & Low Latency Communication wireless system, which is massively deployed in high speed rail, industry internet and vehicle-to-everything applications in China.
Ouster San Francisco, CA	Native camera imaging on LiDAR and deep learning enablement	Showcases the Ouster 128 channel LiDAR system, which includes a single monolithic laser array chip containing all 128 lasers, and another ASIC containing all 128 photodetectors plus digital signal processing.
PsiKick Santa Clara, CA	PsiKick's Batteryless Sensor Network Platform for the Industrial IoT	Demonstrates PsiKick's ultra-low power state-of-the-art sensor network with completely batteryless edge sensor nodes for continuous industrial monitoring.
Samsung Electronics Hwaseong, Korea	A Fully Integrated 10nm Multi-Mode 5G Modem Chipset Compatible with 3GPP NR Standards	Features Samsung's Exynos Modem 5100, a new multi-mode 5G modem chipset supporting both sub-6GHz and mm-wave 3GPP 5G New Radio standards, together with global cellular Radio Access Technologies.
Samsung Electronics Hwaseong, Korea	Motion Artifact Free Dynamic Vision Sensor for Machine Vision	Features the latest Samsung dynamic vision sensor that removes motion artifacts while tracking fast-moving objects and shows its application in simultaneous localization and mapping on a smart phone

Student Event: Making a Career Choice

Monday, February 18

This evening interactive event will include several distinguished panelists representing a broad variety of career choices in the areas of start-ups, industry, research, and academia available to graduates in electrical and computer engineering. Following short introductory remarks by each panelist, this forum will open for audience interaction in which the audience is invited to express a broad range of questions to the panelists.

Evening Panel: Moving to 'The Dark Side'!

Tuesday, February 19

Many practicing engineers view management and business as 'The Dark Side', and executive decisions often baffle them. Can engineers do a good job on 'The Dark Side' in management and business? Is it possible to return to engineering from 'The Dark Side'?

The relation between business and management on one and engineering on the other side has always been complex. On one hand, innovative engineers often don't understand the limitations imposed on them by more financially driven business managers. On the other hand, business needs solid engineering, within their budgetary boundaries, in order to be successful. Is it possible to transform from a good engineer to a good business manager? Can business managers return to engineering and be successful engineers after having spent time on 'The Dark Side'? Can engineers and business managers peacefully coexist, and are they able to understand each other? Is that a situation we should work towards or, is a world where each side sees the other as a necessary evil perfectly balanced and sustainable?

In an entertaining and educational discussion between the panelists, the audience will get a closer look into the hearts and minds of Captains of Industry, sharing their views on the subject. How do they view the world after moving to 'The Dark Side' and have they truly moved to 'The Dark Side'?

Join this panel discussion with active audience interaction, take a seat in the tribunal and make your vote count!

Evening Panel: How Can Hardware Designers Reclaim the Spotlight?

Tuesday, February 19

Gone seem the heady days when hardware innovation drove entrepreneurship in communications, computing, and other domains. The bar for circuit innovation and design has been inexorably climbing higher even as circuit components are becoming increasingly commoditized and seemingly losing relevance in the larger scheme of things.

Is this trend here to stay? Should we do something about it? What should we do? Are long hardware design cycles to blame? Can we learn something from software design practices? Or, are there new opportunities where hardware innovation can still play a central role? If so, how far out is the horizon? How do we prepare for these opportunities?

This evening panel assembles a galaxy of international experts from academia, government, and both the hardware and software industries to discuss these issues. The experts will diagnose the situation, offer insightful prognoses, and engage in a lively discussion with each other, and with the audience. Come join us to see if you agree with our experts and for an opportunity to enlighten us with your opinion.



ISSCC 2019

**SESSION OVERVIEWS
AND HIGHLIGHTS**

Conditions of Publication

PREAMBLE

The Session Overviews and Highlights to follow serve to capture the context, highlights, and potential impact, of the papers to be presented in each Session at ISSCC 2019 in February in San Francisco

OBTAINING COPYRIGHT to ISSCC press material is EASY!

You may quote the Subcommittee Chair as the author of the text if authorship is required.

You are welcome to use this material, copyright- and royalty-free, with the following understanding:

- That you will maintain at least one reference to ISSCC 2019 in the body of your text, ideally retaining the date and location. For detail, see the FOOTNOTE below.*
- That you will provide a courtesy PDF of your excerpted press piece and particulars of its placement to press_relations@isscc.net*

FOOTNOTE

- From ISSCC's point of view, the phraseology included in the box below captures what we at ISSCC would like your readership to know about this, the 66th appearance of ISSCC, on February 17th to February 21st, 2019, in San Francisco.*

*This and other related topics will be discussed at length at ISSCC 2019, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 17 - February 21, 2019,
at the San Francisco Marriott Marquis Hotel.*

ISSCC Press Kit Disclaimer

The material presented here is preliminary.

As of November 6, 2018, there is not enough information to guarantee its correctness.

Thus, it must be used with some caution.

Session 2 Overview: Processors

Digital Architectures and Systems Subcommittee

Session Chair: Ingrid Verbauwhede, KU Leuven, Belgium

Session Co-Chair: James Myers, Arm Ltd, Cambridge, UK

Interim Subcommittee Chair: Thomas Burd, AMD, Santa Clara, CA, DAS Subcommittee Chair

Processors continue to diversify and specialize for an ever-wider range of applications. The first paper describes a high-performance supercomputer, followed by low-power streaming vision and post-quantum cryptographic processors. A versatile platform for collaborative robotics comes next, followed by very specialized mixed-signal graph processor and a CMOS annealer. The final paper showcases a multi-core automotive MCU with real-time virtualization.

- In invited Paper 2.1, IBM describes two supercomputers, Summit and Sierra, built upon IBM POWER9™ CPUs and NVIDIA Volta™ GPUs. The Summit supercomputer contains 9216 CPUs and 27648 GPUs, achieving 200 PFLOPS in 15MW.
- In Paper 2.2, KU Leuven presents a 22nm 6.4mm² coarse-grain reconfigurable streaming processor with 330 streaming elements, performing real-time dense optical flow in 30fps VGA at 10.7mW.
- In Paper 2.3, MIT shows an IoT targeted lattice processor supporting Kyber, NewHope, R. EMBLEM and LIMA Round 1 post-quantum cryptography proposals, in a 0.28mm² chip in 40nm CMOS.
- In Paper 2.4, Intel presents a platform including a 22nm SoC with path planning and motion control acceleration, for collaborative robotic applications. Wide-range voltage-frequency scaling delivers 37-238mW at 80-365MHz.
- In Paper 2.5, the University of Minnesota introduces a mixed-signal time-domain 65nm application-specific processor for shortest-path problems, scaling across multiple chips and achieving 559 million traversed edges per second at 10⁵× lower energy than an FPGA. The processor operates at 1.79ns per node with a peak power of 26.4mW.
- In Paper 2.6, Hitachi describes a 40nm CMOS annealing processor for combinatorial optimization problems, supporting 50% higher spin count and multichip interfaces. The 24mm² chip achieves a 22μs annealing time, which is 26000× faster than a CPU.
- In Paper 2.7, Renesas reveals a 94mm² 4-core, 600 MHz automotive control processor, supporting virtualization with 0.44μs context switching latency in 28nm CMOS with e-FLASH.

Session 2 Highlights: Processors

[2.1] Summit and Sierra: Designing AI/HPC Supercomputers

Paper 2.1 Authors: Jim Kahle¹, Jaime Moreno², Dan Dreps³

Paper 2.1 Affiliation: ¹IBM, Austin, TX, ²IBM Research, Yorktown Heights, NY, ³IBM Systems, Austin, TX

Interim Subcommittee Chair: Thomas Burd, AMD, Santa Clara, CA, DAS Subcommittee Chair

CONTEXT AND STATE OF THE ART

- Performance leading supercomputers are realized by heterogeneous integration of IBM POWER9™ CPUs, NVIDIA Volta™ GPUs, and massive memory systems.
- System level optimizations in packaging, cooling, and network integration pave the way for energy efficient, large scale, supercomputers.

TECHNICAL HIGHLIGHTS

- **IBM describes the Sierra and Summit supercomputers with up to 200 PFLOPS of processing capability.**
 - IBM partners with NVIDIA and Mellanox to deliver two super computers for the USA national research labs; Summit has 9216 IBM POWER9™ CPUs, 27,648 NVIDIA Volta™ GPUs at 200PFLOPS and Sierra has 8649 IBM POWER9™ CPUs, 17,280 NVIDIA Volta™ GPUs at 125PFLOPs.

APPLICATIONS AND ECONOMIC IMPACT

- IBM delivers the Sierra and Summit supercomputers, as part of the CORAL program providing Oak Ridge National Laboratory and Lawrence Livermore National Laboratory with unparalleled levels of computational ability.
- Driving applications span many industries and include fluid dynamics simulations, defense, and weather modelling.

Session 3 Overview: Nyquist Rate ADCs

Data Converters Subcommittee

Session Chair: Seng-Pan (Ben) U, University of Macau & Synopsys Macau Ltd, Macau

Session Co-Chair: Ahmed Ali, Analog Devices, Greensboro, NC

Subcommittee Chair: Michael Flynn, University of Michigan at Ann Arbor, Ann Arbor MI

Extending the speed and resolution has been a major trend for Nyquist rate ADCs. This session presents Nyquist rate ADCs ranging in resolution from 11 to 16 bits and sample rates from 2MS/s to 5GS/s. Pipelined ADC architectures are primarily used to achieve these high resolutions, with a variety of hybrid approaches involving SAR and TDC stages used to enhance power efficiency. Residue amplification using open-loop Gm-R, dynamic amplifiers, and closed-loop ring-amplifier-based switched-capacitor circuits are employed for achieving high speed and low power. Calibration is widely used in many of these ADCs to enable high resolution with low power and area. Temperature stability is optimized to maintain calibrated performance over a wide temperature range.

- In Paper 3.1, imec describes a 13b, 3.2Gs/s, 4x interleaved ring-amplifier-based pipelined ADC, which introduces a general method for background tracking of signal-to-distortion ratio using a single-comparator stochastic ADC. This 16nm ADC achieves 61.7dB SNDR at 1.6GHz while consuming 61mW.
- In Paper 3.2, the University of Macau describes a single channel 12b, 1GS/s SAR-assisted pipelined ADC. A Gm-R-based residue amplifier with temperature-compensated bias is used. This 28nm ADC achieves >60dB SNDR at Nyquist while consuming 7.6mW.
- In Paper 3.3, KU Leuven describes a 5GS/s 12b passive-sampling 8x-interleaved hybrid ADC with a bandwidth in excess of 6GHz. This 28nm ADC achieves a 58.5dB SNDR at 2.4GHz while consuming 158.6mW.
- In Paper 3.4, the University of Texas Austin describes a 2MS/s, 13b continuous-time pipelined-SAR ADC with a kT/C noise-free input stage. This 40nm ADC achieves a peak SNDR of 73.5dB while consuming 25.2uW
- In Paper 3.5, the University of Macau presents a 20MS/s, 13b, two-step TDC-assisted SAR ADC with PVT tracking and speed enhancing techniques. This 65nm ADC achieves a Walden FoM of 1.4fJ/conversion-step using a 0.6V supply.
- In Paper 3.6, imec presents a single-channel 600MS/s, 11b, pipelined ADC with an asynchronous, event-driven approach to timing control that leads to fully dynamic power consumption. This 16nm ADC achieves 60dB SNDR and 78dB SFDR while consuming 6mW.
- In Paper 3.7, Oregon State University describes a 15MS/s, 16b, two-step SAR ADC using a dual-deadzone ring-amplifier. This 180nm ADC achieves 91dB SNDR while consuming 61mW.

Session 3 Highlights: Nyquist Rate ADCs

[3.3] A 5GS/s 158.6mW 12b Passive-Sampling 8x-Interleaved Hybrid ADC with 9.4 ENOB and 160.5dB FoMs in 28nm CMOS

[3.5] A 0.6V 13b 20MS/s Two-Step TDC-Assisted SAR ADC with PVT Tracking and Speed-Enhanced Techniques

Paper 3.3 Authors: Athanasios Ramkaj¹, Juan Carlos Pena Ramos¹, Yifan Lyu¹, Maarten Strackx², Marcel J.M. Pelgrom¹, Michiel Steyaert¹, Marian Verhelst¹, Filip Tavernier¹

Paper 3.3 Affiliation: ¹KU Leuven, Heverlee, Leuven, Belgium, ²Nokia Bell Labs, Antwerpen, Belgium

Paper 3.5 Authors: Minglei Zhang¹, Chi-Hang Chan¹, Yan Zhu¹, Rui Paulo da Silva Martins^{1,2}

Paper 3.5 Affiliation: ¹University of Macau, Macau, Macau, ²Instituto Superior Tecnico/University of Lisboa, Lisboa, Portugal

Subcommittee Chair: Michael Flynn, University of Michigan, Ann Arbor, MI

CONTEXT AND STATE OF THE ART

- High-speed and low-power ADCs with high linearity and dynamic range enable more integration, which is required in many emerging applications such as 5G communications, smart sensors, biomedical imaging, and portable instrumentation.
- Circuit non-idealities and variability with technology process, supply and temperature have been a fundamental limitation to achieving high performance with robustness.
- Innovations in hybrid architectures and circuit techniques for ADCs, including meticulous calibration, help break the performance barrier with robustness.

TECHNICAL HIGHLIGHTS

- **KU Leuven introduces a gigahertz ADC for 5G communications in 28nm CMOS achieving much lower power consumption than previous state-of-the-art gigahertz-range high-resolution ADCs.**
 - An 8× Interleaved hybrid multi-stage Pipeline-SAR ADC with input passive-sampling and on-chip digital calibration demonstrates 9.4b-ENOB at 5GS/s with only 158.6mW and a Walden Figure-of-Merit of 46.1fJ/conversion-step.
- **The University of Macau presents a process, voltage, temperature (PVT)-robust hybrid ADC in 65nm CMOS with higher performance efficiency at low supply.**
 - A Two-Step TDC-Assisted SAR ADC achieves 13b 20MS/s at 0.6V with less than 0.8dB SNDR drop across –50°C to 90°C and ±5% power supply variation with a Walden FoM of 1.4fJ/conversion-step.

APPLICATIONS AND ECONOMIC IMPACT

- Advanced circuit techniques for high-accuracy ADCs with robustness make many new applications possible and efficient.
- High performance and low power temperature-insensitive ADCs with self-calibration without factory trimming, thereby reducing manufacturing cost significantly.
- Lower power consumption while preserving performance enables the integration of more channels with improved robustness.

Session 4 Overview: Power Amplifiers

RF Subcommittee

Session Chair: Krzysztof Dufrêne, Intel, Linz, Austria

Session Co-Chair: Harish Krishnaswamy, Columbia University, New York, NY

Subcommittee Chair: Piet Wambacq, imec, Leuven, Belgium, RF Subcommittee

Simultaneously achieving high output power, high peak efficiency, and high efficiency under spectrally efficient modulation schemes has become an important topic of research as the industry prepares for the widespread deployment of 5G technologies. Doherty PAs are being extensively investigated at millimeter-wave frequencies to improve efficiency under back-off. There is a continuing trend at millimeter-waves to blend electronics with antenna design to achieve improved performance. Innovations in digital power amplifiers and broadband power amplifiers are also being seen for sub-6GHz RF applications as well as broadband wireline applications.

- In Paper 4.1, the University of Southern California presents a phase-interleaved, multi-sub-harmonic switching digital power amplifier, providing inherent cancellation of the sub-harmonic components in the power back-off region. The prototype achieves a 30dBm peak power at 1.9GHz with 45.9/41.3/35.3/32.2/24.2% drain efficiency at 0/-3.5/-7/-9.5/-12 dB PBO.
- In Paper 4.2, Fudan University presents a broadband inverter-based class-D power amplifier with a switched-transformer technique to enhance deep back-off efficiency. Implemented in 40nm CMOS and powered from a 1.1V supply, the PA achieves 4 efficiency peaks in 1.3-to-3.5GHz range. It obtains 21.4dBm peak output power and 31.3/27.7/16.6/7.7% PAE at 0/6/12/18dB back-off at 1.5GHz.
- In Paper 4.3, the University of Utah introduces a multiphase interpolating digital power amplifier for TX beamforming, leveraging switched capacitor PA techniques to simultaneously realize high linearity and power and system efficiency. Four transmitters are able to achieve peak P_{out} of 24.4dBm, while achieving <1deg phase resolution and <0.15dB gain error.
- In Paper 4.4, the Georgia Institute of Technology and Skyworks Solutions propose a highly linear, high-power SiGe HBT power amplifier supporting 802.11ac/ax. A compact four-way output transformer with a 2nd-harmonic short is designed to obtain efficient power combining and linear operation without bulky harmonic rejection filters.
- In Paper 4.5, IHP and Technische Universität Berlin present a fully integrated power amplifier at 240GHz. Four PA units are combined with a zero-degree power combiner, achieving P_{sat} of 13.5dBm and 3% drain efficiency. A small-signal gain of 15.5dB is measured across a 3dB 55GHz bandwidth between 200 and 255GHz.
- In Paper 4.6, the Georgia Institute of Technology presents a 3-way series-combining Doherty radiator exploiting dual-antenna coupling and on-antenna current-scaling series combiner for power back-off efficiency enhancement up to 9.6dB with high linearity. It achieves 21.2dBm P_{sat} and 21.8/19.5/18% PAE at 0/6/9dB PBO.
- In Paper 4.7, the University of California, San Diego, describes a compact stacked distributed power amplifier with multi-drive and inter-stack coupling techniques. The amplifier achieves a record 1.525THz gain-bandwidth product and 20.8dBm peak output P1dB. By exploiting complementary nature of NMOS-PMOS to minimize AM-AM and AM-PM distortions, it achieves over 100Gb/s in both 64-QAM and dPAM4 modulations.
- In Paper 4.8, the Georgia Institute of Technology proposes a mixed-signal Doherty power-amplifier architecture. The amplifier achieves 40.1% peak PAE with 32.3dBm P_{sat} and 37.5/33.1% PAE at 5/6dB power back-off. It also achieves -24.5dB rms EVM with an average P_{out} /PAE of +15.6dBm/27.8%.
- In Paper 4.9, the Georgia Institute of Technology presents a cascaded asymmetric distributed active-transformer power amplifier combining 48 differential output ports of 24 PA units to deliver 29.2-to-30.1dBm peak output power with 18.5-to-20.8% peak PAE at 60GHz. The amplifier supports linear amplification of wideband modulations, demonstrating 2Gsymb/s 16-QAM and 64-QAM signals at an average P_{out} of 22.3dBm and 20.9dBm, respectively.

Session 4 Highlights: Power Amplifiers

[4.1] An 88%-Efficiency Supply Modulator Achieving 1.08 μ s/V Fast Transition and 100MHz Envelope-Tracking Bandwidth for 5G New Radio RF Power Amplifier

[4.7] A Compact DC-to-108GHz Stacked-SOI Distributed PA/Driver Using Multi-Drive Inter-Stack Coupling, Achieving 1.525THz GBW, 20.8dBm Peak P1dB, and Over 100Gb/s in 64-QAM and PAM-4 Modulation

[4.8] A Highly Linear Super-Resolution Mixed-Signal Doherty Power Amplifier for High-Efficiency mm-Wave 5G Multi-Gb/s Communications

Paper 4.1 Authors: Aoyang Zhang, Mike Shuo-Wei Chen

Paper 4.1 Affiliation: University of Southern California, Los Angeles, CA

Paper 4.7 Authors: Omar Essam El-Aassar, Gabriel M. Rebeiz

Paper 4.7 Affiliation: University of California, San Diego, La Jolla, CA

Paper 4.8 Authors: Fei Wang, Tso-Wei Li, Hua Wang

Paper 4.8 Affiliation: Georgia Institute of Technology, Atlanta, Georgia

Subcommittee Chair: Piet Wambacq, imec, Leuven, Belgium, RF Subcommittee

CONTEXT AND STATE OF THE ART

Simultaneously achieving high output power, high peak efficiency, and high efficiency under spectrally efficient modulation schemes has become an important topic of research as the industry prepares for the widespread deployment of 5G technologies. Doherty PAs are being extensively investigated at millimeter-wave frequencies to improve efficiency under back-off. There is a continuing trend at millimeter-waves to blend electronics with antenna design to achieve improved performance. Innovations in digital power amplifiers and broadband power amplifiers are also being seen for sub-6GHz RF applications as well as broadband wireline applications.

TECHNICAL HIGHLIGHTS

- **Watt-Level Phase-Interleaved Sub-Harmonic Switching Digital Power Amplifier with Enhanced Power Back-Off Efficiency**
 - A phase-interleaved, multi-sub-harmonic switching digital power amplifier, providing inherent cancellation of the sub-harmonic components in the power back-off region, is presented. The prototype achieves 30dBm peak power at 1.9GHz with 45.9/41.3/35.3/32.2/24.2% drain efficiency at 0/-3.5/-7/-9.5/-12 dB PBO.
- **Ultra-Wideband Distributed Power Amplifier for High-Speed Wireline Communications Links**
 - A compact stacked distributed power amplifier with multi-drive and inter-stack coupling techniques is demonstrated. The amplifier achieves a record 1.525THz gain-bandwidth product and 20.8dBm peak output P1dB. By exploiting complementary nature of NMOS-PMOS to minimize AM-AM and AM-PM distortions, it achieves over 100Gb/s in both 64-QAM and dPAM4 modulations.
- **Doherty PA with Digital Amplifier in the Auxiliary Path for High-Efficiency mm-Wave Multi-Gbit/s Communications**
 - A mixed-signal Doherty power-amplifier architecture is proposed. The amplifier achieves 40.1% peak PAE with 32.3dBm P_{sat} and 37.5/33.1% PAE at 5/6dB power back-off. It also achieves -24.5dB rms EVM with an average P_{out} /PAE of +15.6dBm/27.8%.

APPLICATIONS AND ECONOMIC IMPACT

- *With the continuing advancements in wireless and wireline communications and employment of spectrally efficient modulation schemes, improvements of both linearity and power-back-off efficiency of power amplifiers are critical to enable simultaneously high data-rates and long battery life. The techniques presented in this session are steps towards achieving those goals.*

Session 5 Overview: Image Sensors

IMMD Subcommittee

Session Chair: Kazuko Nishimura, Panasonic Corporation, Moriguchi, Japan

Session Co-Chair: Jun Deguchi, Toshiba Memory Corporation, Kawasaki, Japan

Subcommittee Chair: Chris Van Hoof, IMEC, Leuven, Belgium, IMMD

This session presents advances in image sensors covering 3D-stacked BSI, global shutter, motion/object detection, novel-column ADC architecture, coded exposure, data-compressive imaging, vertical APD, high dynamic range, SPAD, LiDAR and THz imaging. The first paper by SmartSens presents a BSI global shutter with 99% shutter efficiency. This is followed by the University of Michigan who present a low-power image sensor with energy efficient SAR ADCs for IoT applications. Stanford University presents a 127pJ/pixel image sensor for HOG-based object detection. A VGA CMOS image sensor with time-stretched single-slope ADCs is presented by Yonsei University, while the University of Toronto presents a 2-tap coded-exposure image sensor with a tap contrast ratio of 99% at 180fps. Panasonic presents a CMOS image sensor with vertical avalanche photodiodes (VAPDs) with “relaxation-quenching”. The University of Edinburgh presents a stacked SPAD array for LiDAR applications. Finally, Hokkaido University presents a THz image sensor with pixel-parallel ADCs.

- In Paper 5.1, SmartSens presents a global shutter BSI 3D-stacked 1.3Mpixel 1/4” CMOS image sensor. High dynamic range of 110dB and low dark current are achieved at 99% shutter efficiency operating at 120fps consuming 205mW.
- In Paper 5.2, the University of Michigan presents a low-power image sensor for IoT applications using a 65nm CIS process to implement 1.5 μ m 4T pixels along with a column-parallel capacitor array-assisted charge-injection SAR ADC. The energy-efficient SAR ADC architecture achieves a noise floor of 226 μ V_{rms} or 106 μ V_{rms} using multiple sampling to facilitate power-efficient motion detection.
- In Paper 5.3, Stanford University presents an image sensor with 127pJ/pixel for HOG-based object detection. Captured images are compressed to 1.5b and 2.75b logarithmic gradients to reduce backend data by 25 \times compared to an 8b image. Despite the low-resolution logarithmic gradients, the robustness to illumination is comparable to images with 9b linear gradients.
- In Paper 5.4, Yonsei University presents a VGA CMOS image sensor with a frame rate of 500fps, a random noise level of 1.95e_{rms} and power consumption of 76mW using 110nm 1P4M CMOS process. A low figure of merit of 0.96e \cdot nJ is achieved with 8 \times analog gain and time-stretched single-slope ADCs. A horizontal conversion time of only 4 μ s is facilitated using a low-rate 100MHz counter clock.
- In Paper 5.5, the University of Toronto presents a 2-tap coded-exposure-pixel image sensor for computational imaging application with a tap contrast ratio of 99% at 180sub-fps. A small pixel size of 11.2 μ m is realized with a fill factor of 45.3%. The sensor is demonstrated in single-frame structured-light and photometric-stereo applications.
- In Paper 5.6, Panasonic presents a VAPD CMOS image sensor. A new method of “relaxation-quenching” enables operation with variable gain from unity to 80000 with fast and clean (after-pulse-suppressed) quenching. Synthesis of gradation and direct ToF binary images are demonstrated under 100Klux sunlight.
- In Paper 5.7, the University of Edinburgh presents a 256 \times 256 array of stacked SPADs at 9.2 μ m pitch for high-dynamic-range photon counting with multiple reconfigurable modes useful for ToF imaging. Using a 40nm/90nm 3D-stacked BSI process, 4096 14b TDCs with time resolution of 35ps are integrated into the bottom-tier CMOS to facilitate the processing of the SPAD array.
- In Paper 5.8, Hokkaido University presents a 32 \times 32 CMOS THz image sensor using 0.18 μ m CMOS for low cost. A responsivity of 218kV/W at 0.93THz, NEP of 91pW/ \sqrt Hz at 31Hz, and 400fps image capturing with digital CDS are achieved by envelope detectors with a square-law-based amplifier and pixel-parallel VCO-based ADCs.

Session 5 Highlights: Image Sensors

[5.7] A 256×256 40nm/90nm CMOS 3D-Stacked 120dB-Dynamic-Range Reconfigurable Time-Resolved SPAD Imager

Paper 5.7 Authors: Robert K Henderson¹, Nick Johnston¹, Sam Hutchings¹, Istvan Gyongy¹, Tarek Al Abbas¹, Neale Dutton², Max Tyler³, Susan Chan³, Jonathan Leach³

Paper 5.7 Affiliations: ¹University of Edinburgh, Edinburgh, United Kingdom, ²STMicroelectronics, Edinburgh, United Kingdom, ³Heriot-Watt University, Edinburgh, United Kingdom

[5.2] Energy-Efficient Low-Noise CMOS Image Sensor with Capacitor Array-Assisted Charge-Injection SAR ADC for Motion-Triggered Low-Power IoT Applications

Paper 5.2 Authors: Kyojin D. Choo, Li Xu, Yejoong Kim, Ji-Hwan Seol, Xiao Wu, Dennis Sylvester, David Blaauw

Paper 5.2 Affiliation: University of Michigan, Ann Arbor, MI

Subcommittee Chair: Chris Van Hoof, IMEC, Leuven, Belgium, IMMD

CONTEXT AND STATE OF THE ART

- SPADs used for direct time-of-flight and other modalities continue to make use of BSI process technology and 3D stacking Edinburgh.
- Image sensors continue to lower power by optimizing architecture and algorithms to support long battery life for IoT applications.

TECHNICAL HIGHLIGHTS

- **The University of Edinburgh presents a 256×256 array of stacked SPADs at 9.2μm pitch for high-dynamic-range photon counting with multiple reconfigurable modes useful for ToF imaging.**
 - Using a 40nm/90nm 3D-stacked BSI process, 4096 14b TDCs with time resolution of 35ps are integrated into the bottom tier CMOS in order to facilitate the processing of the SPAD array.
- **The University of Michigan presents a low-power image sensor for IoT applications using a 65nm CIS process to implement 1.5μm 4T pixels along with a column-parallel capacitor array-assisted charge-injection SAR ADC.**
 - The energy efficient SAR ADC architecture achieves a noise floor of 226μV_{rms} or 106μV_{rms} using multiple sampling to facilitate power-efficient motion detection.

APPLICATIONS AND ECONOMIC IMPACT

- BSI SPAD-based image sensors with high-resolution pixel arrays are applied for direct time-of-flight imaging. The applications anticipated are for gesture recognition, gaming, virtual reality, and augmented reality.
- Energy-efficient image sensor architectures enable always-on imaging with motion-triggering to drive applications for the Internet of Things.

Session 6 Overview: Ultra-High-Speed Wireline

Wireline Subcommittee

Session Chair: Tony Chan Carusone, University of Toronto, Toronto, Canada

Session Co-Chair: Takayuki Shibasaki, Fujitsu Laboratories, Kanagawa, Japan

Subcommittee Chair: Frank O'Mahony, Intel, Hillsboro, OR

Digital traffic is aggregated within and between data centers through ultra-high-speed wireline links, which are poised to reach 100Gb/s line rates as the bandwidth per port in data routers keeps increasing. Thus, four papers in this session describe circuits at or above 100Gb/s. Wireline transceiver research is at the forefront of solid-state circuits technology, integrating high-performance analog and digital in the most advanced nanoscale CMOS. For instance, three of the papers in this session are implemented in 7nm FinFET technology. Increasingly complex signal processing and communication techniques are being brought to bear on these problems, with four of the papers relying on digital signal processing. However, practical constraints on the circuits' power consumption and area remain, so that advances in analog/mixed-signal transceiver circuits are the focus of the four remaining papers.

- In Paper 6.1, IBM Research describes mixed-signal PAM-4 clock and data recovery at 100Gb/s. The analog front-end shapes the channel response to permit an efficient implementation of a speculative DFE consuming only 1.1pJ/bit in 14nm FinFET technology.
- In Paper 6.2, Huawei Technologies reports a 60Gb/s ADC-DSP based transceiver in 7nm FinFET technology that automatically and adaptively minimizes its power consumption based upon the channel loss and crosstalk. Over 30% power savings is achieved when the link loss varies from 38dB to 18dB.
- In Paper 6.3, eSilicon presents a PAM-4 transceiver that incorporates a DAC, ADC, and DSP in 7nm FinFET technology. The transceiver consumes less than 250mW and compensates up to 42dB loss at 56Gb/s.
- In Paper 6.4, MediaTek describes a 56Gb/s transceiver employing low-power techniques for their 7b DAC and ADC-based front ends. The analog power consumption is 180mW/lane in 7nm FinFET technology.
- In Paper 6.5, Inphi reports on a 400Gb/s 4-lane transceiver for optical communication in 16nm FinFET technology. The quad transceiver occupies 6.16mm² while consuming a total of 900mW.
- In Paper 6.6, IBM Research presents a transmitter with reconfigurable 3-tap FFE operating up to 128Gb/s. A 1V_{ppd} output swing is achieved with 1.3pJ/b power consumption in 14nm FinFET technology.
- In Paper 6.7, Yuan Ze University describes a PAM-4 voltage-mode transmitter incorporating automatic phase alignment in a 4:1 multiplexer. A maximum data rate of 112Gb/s is achieved in 40nm CMOS technology.
- In Paper 6.8, the University of Toronto incorporates automatic equalization and timing adaptation into a mixed-signal receiver that uses the same latches for both baud-rate clock recovery and a 1-tap DFE. The 36Gb/s NRZ receiver consumes 106mW for an 18dB-loss channel in 28nm CMOS technology.

Session 6 Highlights: Ultra High Speed Wireline

[6.1] A 100Gb/s 1.1pJ/b PAM-4 RX with Dual-Mode 1-Tap PAM-4 / 3-Tap NRZ Speculative DFE in 14nm CMOS FinFET

[6.3] A Sub-250mW 1-to-56Gb/s Continuous-Range PAM-4 42.5dB IL ADC/DAC-Based Transceiver in 7nm FinFET

[6.6] A 128Gb/s 1.3pJ/b PAM-4 Transmitter with Reconfigurable 3-Tap FFE in 14nm CMOS

Paper 6.1 Authors: Alessandro Cevrero, Ilter Ozkaya, Pier Andrea Francese, Matthias Brandli, Christian Menolfi, Thomas Morf, Marcel Kossel, Lukas Kull, Danny Luu, Martino Dazzi, Thomas Toifl

Paper 6.1 Affiliation: IBM Research, Ruschlikon, Switzerland

Paper 6.3 Authors: Matteo Pisati, Fernando De Bernardinis, Paolo Pascale, Claudio Nani, Marco Sosio, Enrico Pozzati, Nicola Ghittori, Federico Magni, Marco Garampazzi, Giacomino Bollati, Antonio Milani, Alberto Minuti, Fabio Giunco, Paola Uggetti, Ivan Fabiano, Nicola Codega, Alessandro Bosi, Nicola Carta, Demetrio Pellicone, Giorgio Spelgatti, Massimo Cutrupi, Roberto Massolini, Andrea Rossini, Giovanni Cesura, Ivan Bietti

Paper 6.3 Affiliation: eSilicon Italy, Pavia, Italy

Paper 6.6 Authors: Zeynep Toprak-Deniz, Jonathan E. Proesel, John F. Bulzacchelli, Herschel A. Ainspan, Timothy O. Dickson, Michael P. Beakes, Mounir Meghelli

Paper 6.6 Affiliation: IBM T. J. Watson Research Center, Yorktown Heights, NY

Subcommittee Chair: Frank O'Mahony, Intel, Hillsboro, OR

CONTEXT AND STATE OF THE ART

- State-of-the-art serial interfaces for chip-to-chip or chip-to-optics interconnects now achieve 112-to-128Gb/s to meet increasing bandwidth demands in data centers and telecommunication infrastructures. Power and area efficiencies will continue to improve in order to meet the demand for higher bandwidth and achieve better energy efficiencies, particularly in data centers.
- Rapid adoption of new 7nm FinFET technology is allowing for denser and lower power digital logic. At the same time, the energy efficiency of analog front ends is also improving at 56Gb/s.

TECHNICAL HIGHLIGHTS

- **A low-power 100Gb/s PAM-4 receiver in 14nm FinFET.**
 - In paper 6.1, IBM Zurich Research Laboratory presents a 100Gb/s PAM-4 design with BER < 1e-12 across a 19dB loss channel. The receiver achieves the lowest power design reported at 1.1pJ/b power efficiency. The CTLE topology uses a dual-path concept to generate high frequency boost and long-tail equalization. A PAM-4 DFE circuit implementation with 1+0.5D response to reduce power is reported.
- **A low-power 56Gb/s PAM-4 ADC/DAC-based transceiver in 7nm FinFET.**
 - In paper 6.3, eSilicon presents an ADC/DAC DSP based long reach transceiver. The transceiver operates from 1-to-30Gb/s in NRZ mode and 3.5-to-56Gb/s in PAM-4 mode. It consumes less than 250mW and compensates up to 42dB loss at 56Gb/s PAM-4.

- **First 128Gb/s PAM-4 transmitter in 14nm FinFET.**
 - In paper 6.6, IBM T. J. Watson Research Center presents a 128Gb/s transmitter which employs fully reconfigurable 3-tap baud-spaced FFE. Energy efficiency is 1.3pJ/b and 1.0pJ/b with 128Gb/s $1V_{ppd}$ and 112Gb/s $0.6V_{ppd}$ PAM-4 output signals respectively.

APPLICATIONS AND ECONOMIC IMPACT

- Continued performance scaling for data centers and high-performance computing requires dense, power- and cost-efficient high-bandwidth data communication. Paper 6.6 and three others in this session are operating at a serial data rate at or above 100Gb/s.
- The cost of R&D for wireline transceivers is high due to the increasing complexity of the signal processing required. Therefore, paper 6.3 focuses upon demonstrating IP that is suitable for a wide variety of channels.
- Rapid deployment of the latest 7nm FinFET technology is enabling new architectures of wireline transceivers. Paper 6.3 and two others in this session employ 7nm FinFET technology to allow for complex DSP in the transceiver.
- Papers 6.3 and 6.6 along with five others in this session employ PAM-4 signaling. This is now the industry's predominant modulation format for wireline $\geq 50\text{Gb/s}$ and above to reduce system cost by reducing the requirements for improved channel materials and repeaters.
- Low-power techniques remain a focus of research in this area, including paper 6.6. Lower-power techniques are necessary to scale networking bandwidth within practical power envelopes.

Session 7 Overview: Machine Learning

Digital Architectures and Systems Subcommittee

Session Chair: Dejan Marković, University of California, Los Angeles, Los Angeles, CA

Session Co-Chair: Mahesh Mehendale, Texas Instruments, Dallas, TX

Interim Subcommittee Chair: Thomas Burd, AMD, Santa Clara, CA, DAS Subcommittee

Architectures supporting machine learning for embedded perception and cognition are continuing their rapid evolution, inspired by modern data analytics and enabled by the low energy cost of CMOS processing. This makes it feasible to migrate data analytics toward edge and wearable devices.

This session covers trends in machine learning for modern image and speech recognition and video processing for next-generation mobile/edge devices used in automotive, robotics, and other inference applications. The session features programmable accelerators for Convolutional Neural Networks (CNNs), Deep Reinforcement Learning (DRL), Recurrent Neural Networks (RNNs), and neuromorphic algorithms.

- In Paper 7.1, Samsung introduces an energy-efficient neural processing unit for a mobile product. Their dual-core neural processing unit features 1,024 highly utilized MAC units with in-place feature selection and a butterfly-structure architecture. The processor core is integrated in 5.5mm² in 8nm CMOS and achieves 6.94TOPS at 0.8V, and 11.5TOPS/W at 0.5V, on full-layer neural networks.
- In Paper 7.2, Toshiba presents an image recognition SoC for ADAS applications. The SoC performs ASIL-B-compliant high-performance image recognition and ASIL-D-compliant high-reliability control processes. The 16nm SoC is 94.52 mm² and achieves peak performance of 20.5TOPS at 0.8V, and 217.3 GOPS/mm² with 10 processors, 4 DSPs, and 8 accelerator variants.
- In Paper 7.3, the University of Michigan describes a low-power real-time CNN-SLAM processor that implements full-visual SLAM on a single chip. SLAM performance is tested on the industrial standard KITTI benchmark that renders a large-scale realistic automobile trajectory over 1km. The processor supports large-scale automotive evaluation with >1000 CNN-keypoints/frame on VGA (640×480) resolution in real-time at 80fps, occupies 10.92mm², and consumes 243.6mW from a 0.9V supply in 28nm CMOS.
- In Paper 7.4, KAIST proposes a deep reinforcement learning (DRL) SoC, supporting both CNNs and learning-optimized RNNs. The reusability of weights and inputs allows for reconfiguration of PE mapping with a 49% reduction in memory accesses. Encoding and decoding techniques reduce external data bandwidth by 37% and overall power by 31%. The 65nm 16mm² chip achieves a peak 2.16TFLOPS/W at 0.67V, and 204 GFLOPS at 1.1V with 16b data.
- In Paper 7.5, Tsinghua University unveils a unified block-circulant chip supporting CNN/FC/RNN transpose-domain acceleration. The design features a global-parallel local-serial FFT module and a TRAM-based 2D reuse architecture that shows 16×/12.9× on/off-chip memory access reduction. The 65nm 7.5mm² chip achieves a 0.39-to-140.3TOPS/W with 1-to-12b data at 0.54 to 1.15V.
- In Paper 7.6, Seoul National University describes an on-chip-trainable neuromorphic processor for classification tasks. Training energy of 254.3nJ/image is achieved through a hardware-oriented direct feedback algorithm, out-of-order weight updates, and an update-skipping mechanism. During prediction, the processor achieves 97.83% MNIST recognition accuracy with 236.5 nJ/prediction. The 65nm 10mm² processor delivers 3.42TOPS/W at 0.8V.
- In Paper 7.7, KAIST presents a DNN learning processor that incorporates: 1) fine-grained mixed precision (FGMP) weights and data to reduce external memory access and increase throughput, while retaining learning accuracy, 2) a sparse DNN learning/inference core for high throughput, 3) an input load balancer (ILB) to improve PE utilization. The fabricated chip occupies 16mm² in 65nm CMOS and 25.3TFLOPS/W at 0.78V.

Session 7 Highlights: Machine Learning

[7.1] An 11.5TOPS/W 1024-MAC Butterfly Structure Dual-Core Sparsity-Aware Neural Processing Unit in 8nm Flagship Mobile SoC

[7.3] An 879GOPS 243mW 80fps VGA Fully Visual CNN-SLAM Processor for Wide-Range Autonomous Exploration

[7.4] A 2.1TFLOPS/W Mobile Deep RL Accelerator with Transposable PE Array and Experience Compression

Paper Authors: Jinook Song¹, Yunkyo Cho¹, Jun-Seok Park¹, Jun-Woo Jang², Sehwan Lee², Jon-Ho Song², Inyup Kang¹

Paper Affiliation: ¹Samsung Electronics, Hwaseong, Korea, ²Samsung Advanced Institute of Technology, Suwon, Korea

Paper Authors: Ziyun Li, Yu Chen, Luyao Gong, Lu Liu, Dennis Sylvester, David Blaauw, Hun-Seok Kim

Paper Affiliation: University of Michigan, Ann Arbor, MI

Paper Authors: Changhyeon Kim, Sanghoon Kang, Youngwoo Kim, Dongjoo Shin, Hoi-Jun Yoo

Paper Affiliation: KAIST, Daejeon, Korea

Subcommittee Chair: Thomas Burd, AMD, Santa Clara, CA, DAS Subcommittee Chair

CONTEXT AND STATE OF THE ART

- There is growing demand for accelerating machine intelligence.
- In addition to inferencing, on-chip training is required to enhance mobile/edge machine capabilities.
- Spiking neuromorphic algorithms are emerging as alternative to DNNs to provide machine intelligence.

TECHNICAL HIGHLIGHTS

- **8nm Flagship Mobile SoC for Sparsity-Aware Neural Processing**
 - Samsung unveils their 8nm dual-core neural processing unit for a mobile product, incorporating 1,024 MAC units with in-place feature selection and a butterfly-structure architecture, allowing processing on full layers of neural networks, and a 10× increase in performance over previous state of the art.
- **Fully Visual CNN-SLAM Processor for Wide Range Autonomous Exploration**
 - The University of Michigan demonstrates the first full-visual real-time CNN-SLAM processor, evaluated on the industrial standard KITTI automotive benchmark that renders large-scale realistic automobile trajectory over 1km.
- **Mobile Deep Reinforcement Learning (RNL) Accelerator**
 - KAIST presents a deep-reinforcement-learning (DRL) SoC that supports both CNNs and RNNs with reduced external data bandwidth for power reduction.

APPLICATIONS AND ECONOMIC IMPACT

- Deep-neural-network (DNN) algorithms are outperforming conventional techniques in a variety of “smart” application domains (e.g. virtual assistance, automotive, robotics, etc.), including video, image, and speech processing owing to higher prediction/inference accuracies.

- *DNN computational requirements are distinctively different from conventional workloads, and hence new processing architectures, with superior performance and energy efficiency, are being developed in both industry and academia.*

Session 8 Overview: DC-DC converters

Power Management Subcommittee

Session Chair: Gerard Villar Piqué, NXP Semiconductors, Eindhoven

Session Co-Chair: Jason Stauth, Dartmouth University, Hanover, NH

Subcommittee Chair: Yogesh Ramadass, Texas Instruments, Santa Clara, CA

DC-DC converters are rapidly evolving towards more efficient and compact solutions. In this sense, hybrid converters bring interesting benefits by the smart combination of inductors and capacitors to efficiently transfer energy from input to output. At the same time, full integration of DC-DC converters is enabled by small technology nodes down to 14nm. On the other hand, this session will also reflect the increasing interest towards automotive applications and their demands in terms of wide input voltage range and EMI.

- In Paper 8.1, Intel presents a 4-level flying capacitor multilevel converter that operates from a 5V supply and delivers up to 10A load current with a wide output voltage range. Using a 22nm process, a 10nH inductor, and 5MHz switching frequency, the design is able to achieve up to 93.8% efficiency at a 1.8V output voltage.
- In Paper 8.2, the University of California, San Diego presents an input-passive-stacked buck DC-DC converter that processes power via a stack of two inductors and one capacitor connected to the input. Using small off-chip passive components the design achieves 86.6% conversion efficiency at 0.7W/mm² power density.
- In Paper 8.3, the University of Colorado presents a step-down hybrid converter that uses an input flying inductor and a switched-capacitor network, suitable for charging one- or two-cell batteries from a 9V input. Parasitic inductance of a USB cable is utilized in place of a discrete inductor, reducing on-board power dissipation to 630mW while delivering 7.2W.
- In Paper 8.4, Washington State University describes a fully integrated DC-DC hybrid converter in standard 65nm CMOS technology. The implemented topology reduces the amount of current flowing through the inductor, making it more suitable to lower-quality fully integrated inductors. The converter is able to provide 730mW/mm² while running at 450MHz.
- In Paper 8.5 Intel presents a fully integrated voltage regulator in 14nm CMOS with a 2.5nH package-embedded air-core inductor and using variable ON-time discontinuous conduction mode (DCM) operation. Operating at 70MHz, the design achieves conversion efficiencies between 75% and 88% with 500mA load current at a range of output voltages, and improved light- load efficiency.
- In Paper 8.6, Leibniz University Hannover introduces a fully integrated hybrid multi-ratio resonant DC-DC converter with on-chip inductance and capacitors, suitable for wearable applications. It supports 3.0V-to-4.5V input, 500μA-to-120mA output current and achieves a peak efficiency of 85%. The dynamic load range is 19× wider and the efficiency enhancement factor is 12.8% better than prior art.
- In Paper 8.7, Analog Devices presents a 2MHz 4-to-60V_{IN} automotive-use silent-switcher buck-boost converter. The converter achieves CISPR 25 Class-5 limits. Balanced peak-current mode control minimizes both switching and conduction loss, resulting in 95% power efficiency and >2.5× power density with 10× switching frequency.

Session 8 Highlights: Hybrid DC-DC Converter

[8.3] A 10.9W 93.4%-Efficient (27W 97%-Efficient) Flying-Inductor Hybrid DC-DC Converter Suitable for 1-Cell (2-Cell) Battery Charging

Paper Authors: C. L. Hardy, H-P. Le

Paper Affiliation: University of Colorado, Boulder, CO

Subcommittee Chair: Yogesh Ramadass, Texas Instruments, Santa Clara, CA, Power Management

CONTEXT AND STATE OF THE ART

- *Mobile products are driving the need for low-cost, efficient, and small-form-factor battery chargers with fast charging time and robust operation.*
- *Passive components, especially inductors, are often the primary limitation on size and cost; thus, there is a compelling need to eliminate or shrink magnetic components or leverage energy storage that is embedded in the existing system.*

TECHNICAL HIGHLIGHTS

- ***A USB-powered battery charger eliminates on-board inductors and can operate efficiently using inductance of a USB-C cable through the use of a hybrid, switched capacitor approach.***
 - *The converter can deliver 10.9W of charging power to a single 3V-to-4.2V cell at 93.4% peak efficiency from a 9V supply.*
 - *The converter can also support charging two cells connected in series with 27.4W power and 97% peak efficiency...*

APPLICATIONS AND ECONOMIC IMPACT

- *Highly efficient converter suitable for battery charging with very small size, leveraging USB cable for the inductor component.*
- *Functionality demonstrated in real-world USB operation opens the door to commercial applications.*

Session 9 Overview: High-Frequency Transceivers for Radar and Communication

Wireless Subcommittee

Session Chair: Nagendra Krishnapura, Indian Institute of Technology Madras, Chennai, India.

Session Co-Chair: Yuu Watanabe, Waseda University, Kanagawa, Japan.

Subcommittee Chair: Stefano Pellerano, Intel, Hillsboro, OR, Wireless

Radars, beamforming systems, and mm-wave radios are at the cutting edge of present-day integrated circuit design. This session opens with an invited paper that outlines technological challenges in developing automotive surround-view radar and describes the implementation of a 79GHz FMCW radar system. This is followed by papers describing state-of-the-art transceivers for automotive FMCW radars, UWB radars for vital sign detection, mm-wave beamforming systems, and an ultra-high-data-rate 300GHz transceiver.

- In Paper 9.1, MediaTek describes future trends and technological challenges in developing automotive surround-view radar systems. A 79GHz FMCW radar transceiver integrated with DSP enables a full radar system in a 16mm×25mm package.
- In Paper 9.2, Uhnder describes a 77/79GHz MIMO radar SoC with 12 transmitters and 8×2 receivers resulting in 192 virtual receivers. A radar system using the 28nm CMOS IC demonstrates 6cm range resolution, 1° angular resolution, and 0.099km/h Doppler resolution.
- In Paper 9.3, imec, Delft University of Technology, and Eindhoven University of Technology describe a UWB radar for occupancy and vital sign detection. The proposed burst-chip operation and time-domain pre-distortion enable 100× power reduction and a fast chirp slope of 0.7GHz/40ms with a 0.5MHz rms error. The radar detects heart rate at 5 meters and respiration at 15 meters while consuming only 680μW.
- In Paper 9.4, imec describes a 28nm CMOS transceiver front-end with integrated antennas for 145GHz FMCW radars. The transmitter has a peak effective isotropic radiated power of 11dBm with a 3dB bandwidth of 127 to 154GHz. The receiver has an effective isotropic noise figure of 6dB and a 3dB bandwidth of 138 to 151GHz.
- In Paper 9.5, Hiroshima University, the National Institute of Information and Communication Technology, and Panasonic describe a 300GHz transceiver in 40nm CMOS. A data rate of 80Gb/s over a distance of 3cm is demonstrated using a pair of transceiver ICs with 24dBi horn antennas at each end.
- In Paper 9.6, Intel describes a 60GHz digital polar transmitter with on-chip pulse shaping. The 28nm CMOS IC with an on-PCB dual polarization antenna transmits spectrally-shaped 28.2Gb/s data with 5.6dBm average power and -21.3dBm EVM while consuming 136mW.
- In Paper 9.7, Intel describes a 71-to-76GHz 64-element phased array with a direct-conversion 2×2 transceiver in 22nm FinFET CMOS technology. In this work, which is the first demonstration of a phased-array in FinFET technology, 4 ICs are co-packaged in a single module that includes 16 patch antennas, and 4 such modules are tiled on a PCB to form the 64-element array. The array has a measured EVM of -20dB for 7.2Gb/s 16QAM at 35dBm effective isotropic radiated power.
- In Paper 9.8, KAIST and Hanbat National University describe a 28GHz beamforming front-end IC in 65nm CMOS. It has 6b phase control resolution with 1.5° rms phase error, a 16dB gain control range with 1.4° peak phase variation. The transmitter has a P_{1dB} of 13.9dBm and a peak efficiency of 20.3%, and the receiver has a 4.58dB noise figure.

Session 9 Highlights: High-Frequency Transceivers for Radar and Communications

[9.1] Toward Automotive Surround-View Radars

[9.2] A 192-Virtual-Receiver 77/79GHz GMSK Code-Domain MIMO Radar System-on-Chip

Paper 9.1 Authors: Chih-Ming Hung¹, Alex TC Lin¹, BC Peng¹, Hua Wang¹, Jui-Lin Hsu¹, Yen-Ju Lu¹, Weishow Hsu¹, Jing-Hong Conan Zhan¹, Brian Juan¹, Chi-Hang Lok¹, Sam Lee¹, PC Hsiao¹, Qiang Zhou¹, Mark Wei¹, Hanfei Liu², Hsiang-Yun Chu¹, Yu-Lun Chen¹, Chao-Ching Hung¹, Kevin Fong¹, Po-Chun Huang¹, Pierce Chen¹, Sheng-Yuan Su¹, Yan-Jiun Chen¹, Kehou Chen¹, Chun-Chao Tung¹, Yi-Jhan Hsieh¹, Tzung-Chuen Tsai¹, Yi-Fu, Chen¹, Wei-Kuo Hsin¹, Liang Guo², Dapeng Jin²

Paper 9.1 Affiliation: ¹MediaTek, Hsinchu, Taiwan, ²MediaTek, Hefei, China

Paper 9.2 Authors: Vito Giannini, Marius Goldenberg, Aria Eshraghi, James Maligeorgos, Lysander Lim, Ryan Lobo, Dave Welland, Chung-Kai Chow, Andrew Dornbusch, Tim Dupuis, Struan Vaz, Fred Rush, Paul Bassett, Hong Kim, Monier Maher, Otto Schmid, Curtis Davis, Manju Hegde

Paper 9.2 Affiliation: Uhnder, Austin, TX

Subcommittee Chair: Stefano Pellerano, Intel, Hillsboro, OR, Wireless

CONTEXT AND STATE OF THE ART

- *Autonomous driving needs both short- and long-range radar systems with fine resolution. FMCW radar has been mainly applied for long-range sensing.*
- *The industry faces tremendous challenges in realizing compact, high-frequency and affordable automotive radars.*

TECHNICAL HIGHLIGHTS

- **Surround-View Radar enables 360 degree proximity sensing for vehicles**
 - *In Paper 9.1, MediaTek describes future trends and technological challenges in developing automotive surround-view radar systems. A 79GHz FMCW radar transceiver integrated with DSP allows a full radar sensor in a 16mm×25mm package.*
- **Highly integrated digital-friendly radar provides millimeter-wave sensing with precise ranging and angular resolution.**
 - *In Paper 9.2 Uhnder describes a 77/79GHz MIMO radar SoC with 12 transmitters and 8×2 receivers resulting in 192 virtual receivers. A radar system using the 28nm CMOS IC demonstrates 6cm range resolution, 1° angular resolution, and 0.099 km/h Doppler resolution.*

APPLICATIONS AND ECONOMIC IMPACT

- *Surround-view radar systems will provide better traffic awareness leading to higher levels of automation in driving.*
- *Highly integrated radar chips with precise range and angular resolution will open up new wireless sensing applications.*

Session 10 Overview: Sensor Interfaces

Analog Subcommittee

Session Chair: Tim Piessens, ICsense, Leuven, Belgium

Session Co-Chair: Wen-Chieh Wang, Mediatek, Taiwan

Subcommittee Chair: Kofi Makinwa, Delft University of Technology, Delft, The Netherlands, Analog

This session highlights advances in state-of-the-art sensor interfaces. In the first paper, a highly-integrated energy measurement system is shown that uses self-calibration to achieve high robustness. A second paper describes a high-resolution accelerometer that achieves a noise floor of $22\text{ng}/\sqrt{\text{Hz}}$. The system consists of a MEMS accelerometer, an HV driver ASIC and a low-voltage signal processing ASIC. Next, two integrated resistor-based temperature sensors are presented, one that operates over the largest reported temperature range (-40°C to 180°C) and one that achieves a state-of-the-art energy efficiency of $20\text{fJ}/\text{K}^2$.

- *In Paper 10.1, Analog Devices presents an energy measurement system that measures both line voltages and currents. The system continually monitors its accuracy by injecting reference stimuli. It overcomes the dynamic range challenge associated with detecting these stimuli in the presence of unknown loads, achieving better than 1000ppm inaccuracy for both voltage and current measurements.*
- *In Paper 10.2, Hitachi presents a 17mW MEMS accelerometer. By using a servo-signal-leakage cancellation scheme, and a high-linearity 1b DSM DAC, it achieves a very low noise floor of $22\text{ng}/\sqrt{\text{Hz}}$.*
- *In Paper 10.3, Delft University of Technology describes a Wien bridge temperature sensor that is used to explore the temperature and stress dependence of various on-chip resistors. It achieves an inaccuracy of 0.1°C from -40°C to 180°C .*
- *In Paper 10.4, Delft University of Technology presents an FIR-DAC resistor-based temperature sensor. It achieves $140\mu\text{K}$ resolution, and a state-of-the-art energy efficiency of $20\text{fJ}/\text{K}^2$.*

Session 10 Highlights: Sensor Interfaces

[10.1] An Energy Measurement Front-End with Integrated In-Situ Background Full System Accuracy Monitoring Including the Current and Voltage Sensors

Paper 10.1 Authors: Seyed Danesh¹, William Holland¹, Joe Spalding¹, Michael Guidry², J.E.D. Hurwitz¹

Paper 10.1 Affiliations: ¹Analog Devices, Edinburgh, United Kingdom, ²Analog Devices, Wilmington, NC

Subcommittee Chair: Kofi Makinwa, Delft University of Technology, Delft, The Netherlands, Analog

CONTEXT AND STATE OF THE ART

- Millions of utility electricity meters are deployed globally each year.
- Their accuracy needs to be guaranteed over their full lifetime to accurately calculate billable energy consumption. At present, the accuracy cannot be verified while the meters are online.

TECHNICAL HIGHLIGHTS

- **Complete energy-measurement front-end for electricity meters enables uninterrupted integrated accuracy monitoring over lifetime.**
 - Paper 10.1 describes how the new front-end overcomes the large dynamic range challenges of accurately measuring the monitoring stimuli in the presence of an unknown load signal, achieving accuracies below 1000ppm on voltage and current measurement.

APPLICATIONS AND ECONOMIC IMPACT

- Currently, millions of perfectly accurate meters are replaced annually, since their accuracy cannot be monitored while online. This can be avoided using the concepts presented in paper 10.1.

Session 11 Overview: Diagnostics

IMMD Subcommittee

Session Chair: Joonsung Bae, Kangwon National University, Chuncheon, Korea

Session Co-Chair: Michael Kraft, KU Leuven, Leuven, Belgium

Subcommittee Chair: Chris Van Hoof, IMEC, Leuven, Belgium, IMMD

This session comprises five papers about medical diagnostic systems-on-chip that advance the state-of-the-art for biosensing, neural and ultrasound imaging. The first paper describes an ultrasound ASIC for an echocardiography system with low power consumption and extremely high integration density. The second paper presents a biosensor array based on a 3-electrode system used for voltammetry measurements for DNA analysis. The third paper demonstrates a biosensor for cancer diagnostics based on bio-functionalized microneedles using highly sensitive capacitive detection techniques. The fourth paper describes a frontend circuit for a magnetoresistive biosensor that can tolerate high mismatch between sensors. The fifth paper presents a minimally invasive CMOS fluorescence neural imaging probe based on 512 single-photon-avalanche diodes.

- *In Paper 11.1, KAIST, University of California at Berkeley, National University of Singapore and Singapore Institute of Neurotechnology present a pitch-matched ultrasound ASIC for an intracardiac echocardiography (ICE) system. The presented work achieves high integration density with a $250 \times 250 \mu\text{m}^2$ unit cell and the low power consumption of 5.37mW with 5Vpp TX.*
- *In Paper 11.2, InSilixa Inc. describes a CMOS 32×32 biosensor array with integrated 3-electrode voltammetry $100 \times 100 \mu\text{m}^2$ pixels, including a CMOS-compatible amorphous carbon electrode and temperature control. It achieves $280 \text{fA}_{\text{rms}}$ input-referred noise in a 0.1-to-20Hz bandwidth and 93dB dynamic range.*
- *In Paper 11.3, Yonsei University presents a capacitive 0.87mm^2 biosensor that detects a cancer biomarker using an electrochemical reaction on functionalized microneedles. Employing an ADC consuming 0.1fJ/step, it measures the capacitance between the microneedles with 13.7b resolution from 1 to 100nF and can detect the biomarker with 15fM (rms) resolution from 0.1pM to 1nM.*
- *In Paper 11.4, the University of California San Diego demonstrates a fast-readout 180nm 0.249mm^2 CMOS front-end ASIC for a magnetoresistive biosensor with high mismatch insensitivity. Consuming 1.39mW/ch, it achieves 22.7× faster readout time, better than 22× lower baseline, and 2.3× lower power compared to the state of the art, while being able to tolerate up to 10% mismatch between sensors.*
- *In Paper 11.5, the Korea Institute of Science and Technology, Columbia University and the California Institute of Technology present a minimally invasive fluorescence neural imager displacing only 0.012mm^2 tissue. It is based on two $70 \mu\text{m}$ thin and 3.2mm long shanks with 256 single-photon-avalanche diodes each with $25 \mu\text{m}$ pitch achieving spatial reconstruction of light sources as small as $60 \mu\text{m}$ apart using angle sensitive gratings.*

Session 11 Highlights: Diagnostics

[11.1] A 5.37mW/Channel Pitch-Matched Ultrasound ASIC with Dynamic-Bit-Shared SAR ADC and 13.2V Charge-Recycling TX in Standard CMOS for Intracardiac Echocardiography

Paper 11.1 Authors: Jihee Lee¹, Kyoung-Rog Lee¹, Benjamin E. Eovino², Jeong Hoan Park³, Liwei Lin², Hoi-Jun Yoo¹, Jerald Yoo^{3,4}

Paper 11.1 Affiliation: ¹KAIST, Daejeon, Korea, ²University of California at Berkeley, CA, ³National University of Singapore, Singapore, ⁴Singapore Institute for Neurotechnology, Singapore

Subcommittee Chair: Chris Van Hoof, imec, Heverlee, Belgium, IMMD

CONTEXT AND STATE OF THE ART

- Intracardiac echocardiography (ICE) visualizes the anatomical structure of the heart in real time, with a mm-scale catheter inserted through the intracardiac vessels, and guides surgical intervention for atrial septal defect (ASD) closure.
- A piezoelectric micromachined ultrasound transducer (pMUT) is suitable for implantable ICE applications, but pMUT devices suffer from process variation reducing image quality.

TECHNICAL HIGHLIGHTS

- **KAIST, the University of California Berkeley, the National University of Singapore, and the Singapore Institute for Neurotechnology presents an ultrasound ASIC for an ICE system with TX, RX, and ADC integrated into a 250×250μm² unit cell.**
 - A charge-recycling 13.2V TX is compatible with a standard CMOS process and calibrates itself according to the transducer's process variation per pixel.
 - A dynamic bit-shared (DBS) ADC is shared among four (2×2) adjacent channels for lower power consumption.

APPLICATIONS AND ECONOMIC IMPACT

- As an interventional procedure in structural heart disease and cardiac arrhythmias, ICE does not require general anesthesia. From an economic point of view, low-cost ICE devices enable shorter procedure times, avoid general anesthesia and complications, leading ultimately to shorter hospital stays and reduced cost.

Session 12 Overview: Emerging Technologies

Technology Directions Subcommittee

Session Chair: Wim Dehaene, KU Leuven, Leuven, Belgium

Session Co-Chair: Sriram Vangal, Intel Corporation, Hillsboro, OR

Subcommittee Chair: Makoto Nagata, Kobe University, Kobe, Japan, Technology Directions

This session highlights advances in non-volatile memory integration, battery protection circuits, and flexible thin-film transistor-based memories. Paper 12.1 demonstrates the first-known integrated non-volatile FPGA, CPU and STT-MRAM with the lowest average power consumption. A novel internal short-circuit detector presented in Paper 12.2 that enables Li-ion battery protection and safety using c-axis aligned crystalline IGZO FETs. Paper 12.3 advances the state-of-the-art of TFT-IGZO memory design by increasing SRAM speed by 5.5× and its storage capacity by 4×.

- *In Paper 12.1, Tokohu University describes a fully nonvolatile FPGA-accelerated microcontroller. In addition to the embedded FPGA, it integrates a nonvolatile 32b ARM-Cortex-M0 CPU and a 64kB STT-MRAM fabricated using a 40nm CMOS/MTJ-hybrid process resulting in 47.14 μ W power consumption at 200MHz operating frequency.*
- *In Paper 12.2, Semiconductor Energy Laboratory presents a micro short-circuit detector for battery protection using n-channel c-axis aligned crystalline IGZO FETs. It has a S/H circuit capable of voltage retention for more than 1hr and an analog current load comparator with 52dB gain.*
- *In Paper 12.3, KU Leuven presents a flexible IGZO SRAM and LEPROM with integrated decoder and timing circuitry. The circuits presented are: a 512b SRAM with 242kb/s throughput, a 1kb LEPROM operated at 140k/s, compliant with the ISO NFC standard, and an 8kb self-timed LEPROM accessed at 44kb/s.*

Session 12 Highlights: Emerging Technologies

[12.2] Micro Short-Circuit Detector Including S/H Circuit for 1hr Retention and 52dB Comparator Composed of C-Axis Aligned Crystalline IGZO FETs for Li-Ion Battery Protection IC

Paper 12.2 Authors: Hiroki Inoue, Takeshi Aoki, Fumika Akasawa, Toshiki Hamada, Toshihiko Takeuchi, Kousei Nei, Takako Seki, Yuto Yakubo, Kei Takahashi, Shuji Fukai, Takahiko Ishizu, Munehiro Kozuma, Takanori Matsuzaki, Takayuki Ikeda, Shunpei Yamazaki

Paper 12.2 Affiliation: Semiconductor Energy Laboratory, Atsugi, Japan

Subcommittee Chair: Makoto Nagata, Kobe University, Kobe, Japan, Technology Directions.

CONTEXT AND STATE OF THE ART

- Safety and protection of Li-ion batteries is a serious issue throughout the world.
- Repetitive occurrence of micro short-circuits in Li-ion batteries will cause heat generation eventually leading to a fire accident or explosion.
- Expensive battery monitoring systems with AI are required to prevent fire accidents with Li-ion batteries.

TECHNICAL HIGHLIGHTS

- **An advanced micro short-circuit detector in c-axis aligned IGZO thin-film transistor technology on top of a CMOS battery protection IC is described.**
 - A short circuit detector with an S/H circuit capable of voltage retention for more than 1 hour and an analog current load comparator with high gain improves Li-Ion battery safety.

APPLICATIONS AND ECONOMIC IMPACT

- Safer batteries for smart phones and electric vehicles worldwide.
- Use of IGZO TFT technology enables cost-effective battery-protection ICs.

Session 13 Overview: Nonvolatile Memories

Memory Subcommittee

Session Chair: Yan Li, Western Digital, Milpitas, California

Session Co-Chair: Jongmin Park, SK Hynix, Icheon, Korea

Subcommittee Chair: Jonathan Chang, TSMC, Hsinchu, Taiwan

The five papers in this session include the most advanced non-volatile memory technologies. With large 3D NAND cells, the 4bits/cell flash is going mainstream in many applications. In the 3D NAND memory, the memory stack grows up to 128 layers to achieve higher density. The new 4-plane architecture of putting circuits under the array to gain the highest write throughput of 132MB/s is presented. 1.2Gbps IO speed is achieved in the 6th Generation VNAND. In the emerging memory, an embedded non-volatile ReRAM macro is done using 22nm FinFET technology. A 7Mb embedded STT-MRAM macro is designed in 22FFL FinFET technology.

- In Paper 13.1, Toshiba Memory Corp delivers the highest capacity flash memory chip. A 1.33Tb 4-bit/cell (QLC) 3D-Flash memory in a 96-Word-Line-Layer technology that achieves 8.5Gb/mm² is developed.
- In Paper 13.2, Intel Corp reveals array design in 22nm FinFET process with an array density of 10.1Mb/mm² with all thin gate periphery, leveraging a low voltage ReRAM technology. ReRAM eNVM technology enables superior read performance and byte writability feature.
- In Paper 13.3, Intel Corp demonstrates Write-Verify-Write (WvW) scheme and offset cancellation sensing technique to achieve 7Mb STT-MRAM arrays in 22FFL FinFET Technology. Die by die tuning of a thin film precision resistor used as reference provides large sensing margin.
- In Paper 13.4, Samsung Electronics presents a 512Gb 3b/cell 3D V-NAND flash memory featuring 6th generation V-NAND technology. To improve read and write performance, wordline and bitline setup time reduction techniques are developed.
- In Paper 13.5, Western Digital presents the A 512Gb 3b/cell 3D-flash memory on 128-word-line-layer technology. 4 planes architecture had been proposed to attain performance of 132MB/s with CMOS under array architecture.

Session 13 Highlights: Nonvolatile Memories

[13.5] Paper Title: A 512Gb 3-bit/Cell 3D Flash Memory on 128-Wordline-Layer with 132MB/s Write Performance Featuring Circuit-Under-Array Technology

[13.2] A 3.6Mb 10.1Mb/mm² Embedded Non-Volatile ReRAM Macro in 22nm FinFET Technology with Adaptive Forming/Set/Reset Schemes Yielding Down to 0.5V with Sensing Time of 5ns at 0.7V

Paper 13.5 Authors: Chang Siau¹, Kwnag-Ho Kim¹, Katsuaki Isobe², Noboru Shibata², Kapil Verma¹, Takuya Arikai¹, Jason Li¹, Jong Yuh¹, Anirudh Amarnath¹, Qui Nguyen¹, Ohwon Kwon¹, Stanley Jeong¹, Huguang Li¹, Hua-Ling Hsu¹, Tai-yuan Tseng¹, Steve Choi¹, Siddhesh Darne¹, Pradeep Anantula¹, Alex Yap¹, Seungpil Lee¹, Hardwell Chibvongodze¹, Hitoshi Miwa¹, Minoru Yamashita¹, Mitsuyuki Watanabe¹, Koichiro Hayashi¹, Yosuke Kato¹, Toru Miwa¹, Jang Yong Kang¹, Masatoshi Okumura¹, Naoki Ookuma¹, Muralikrishna Balaga¹, Venky Ramachandra¹, Aki Matsuda¹, Swaroop Kulkani¹, Raghavendra Rachineni¹, Manjunath Pai K¹, Masahito Takehara¹, Toshiki Hisada², Ryo Fukuda², Naoya Tokiwa², Kazuaki Kawaguchi², Masashi Yamaoka², Hiromitsu Komai², Takatoshi Minamoto², Masaki Unno², Susumu Ozawa², Hiroshi Nakamura²

Paper 13.5 Affiliation: ¹Western Digital, Milpitas, CA, ²Toshiba Memory Corporation, Yokohama, Japan

Paper 13.2 Authors: Pulkit Jain¹, Umut Arslan¹, Meenakshi Sekhar¹, Blake C. Lin¹, Liqiong Wei¹, Tanaya Sahu¹, Juan Alzate-vinasco¹, Ajay Vangapaty¹, Mesut Meterelliyo¹, Nathan Strutt¹, Albert B. Chen¹, Patrick Hentges¹, Pedro A. Quintero¹, Chris Connor¹, Oleg Golonzka¹, Kevin Fischer¹, Fatih Hamzaoglu¹

Paper 13.2 Affiliation: ¹Intel, Hillsboro, OR

Subcommittee Chair: Jonathan Chang, TSMC, Hsinchu, Taiwan

CONTEXT AND STATE OF THE ART

- In the 3D NAND memory, the memory stack grows rapidly to 128 layer.
- Paper 13.5 demonstrated the new architecture of putting circuits under the array.
- Demonstration of embedded ReRAM in scaled 22nm FinFet technology with high bit density
- Satisfying wide temperature range operation at high speed read/write time

TECHNICAL HIGHLIGHTS

- **Western Digital introduces the highest 3D memory stack with 128 layers and smallest die density with circuits under the array (Paper 13.5)**
 - With 4 plane architecture, this chip achieved highest write throughput of 132MB/s in TLC write.
 - A new innovative peak power management technique is introduced to improve system-level performance.
- **Intel introduces a high-density ReRAM in 22nm FinFet technology at Mbit level and across a wide temperature range. (Paper 13.2)**
 - Intel Corp. applied a Write-Verify-Write scheme in Forming/Set/Reset to achieve good low and high resistance distributions and applied an offset-cancellation sense amp. technique merged with Precision Resistor Reference to achieve high Read Yield.

APPLICATIONS AND ECONOMIC IMPACT

- *The most advanced 128-layer 3D NAND enhanced write throughput to meet ever increasing demand of flash applications. It also demonstrated continued physical scaling and cost reduction in the Flash memory industry.*
- *Shows ReRAM can be a viable candidate for next-generation MCUs with lower-cost adder and higher speed.*
- *IoT, Wearables, low-cost/low-power SoCs, MCUs.*

Session 14 Overview: Machine Learning and Digital LDO Circuits

Digital Circuits Subcommittee

Session Chair: Vivek De, Intel, Hillsboro, OR

Session Co-Chair: Ping-Ying Wang, CMOS-Crystal Technology, Hsinchu, Taiwan

Subcommittee Chair: Edith Beigne, Facebook, Menlo Park, CA, Digital Circuits

In this session, seven papers highlight developments in machine learning and digital low-dropout (LDO) linear regulators. The papers demonstrate a hybrid digital and mixed-signal computing platform for swarm robotics, bi-directional memory delay lines to perform time-domain MAC operations, hybrid in-/near-memory compute SRAM and resistive RAM for/with resilience techniques. The digital LDO papers present a computational regulation scheme, a sub-nA wide-dynamic-range implementation and a universal modular hybrid LDO in 14nm CMOS.

- In Paper 14.1, Georgia Institute of Technology presents a 1.1-to-9.1TOPS/W unified computation platform fabricated in 65nm CMOS for swarm robotics. It demonstrates an energy-efficient hybrid-digital-mixed-signal (HDMS) circuit architecture, to enable energy-resolution scalability across a variety of swarm algorithms and swarm sizes. The chip consumes 0.3 to 3.4 μ W and occupies 2mm² area.
- In Paper 14.2, the Univ. of Texas Austin describes a 12.08TOPS/W energy-efficient CNN engine implemented in a 40nm CMOS featuring bi-directional memory delay lines to perform time-domain MAC operations with multi-precision kernel weight and pooling support. The design is all-digital without requiring any capacitors, A/D converters, and supports near-threshold voltage operation and 16 \times performance boost with 4 input encoding modes. The chip consumes 31 μ W and occupies 0.124mm² area.
- In Paper 14.3, the University of Michigan introduces a general-purpose hybrid in-/near-memory compute SRAM (CRAM) that combines an 8T transposable bit cell with vector-based bit-serial in-memory arithmetic to accommodate a wide range of bit-widths, from single to 32 or 64b, and operation types, including integer and floating point addition, multiplication and division, providing the flexibility and programmability necessary for evolving software algorithms, ranging from neural networks to graph and signal processing. The energy efficiency is 0.55TOPS/W for multiply and 5.27TOPS/W for addition.
- In Paper 14.4, Stanford University demonstrates a non-volatile microcontroller through on-chip monolithic integration of Resistive RAM and silicon CMOS. It achieves fine-grained temporal power gating (average transition of 4.7 μ s active to shutdown, 200ns back); average active energy of 43pJ/cycle; multiple bits-per-cell RRAM in a complete chip. New resilience techniques achieve a 10-year lifetime of continuous inference. The chip area is 2.5 \times 4.5mm².
- In Paper 14.5, the University of Washington describes computational power regulation, exploiting computing for high-speed regulation. Measurements indicate a 2.79-cycle mean settling time under nominal conditions.
- In Paper 14.6, the University of Virginia demonstrates a 65nm sub-nA, wide-dynamic-load-range digital LDO with a hybrid asynchronous binary-searching and synchronous linear-searching control scheme. The hybrid DLDO achieves 3.8 \times 10⁵ dynamic load range, 99.99% current efficiency, and 2mV output voltage ripple, consuming 745pA quiescent current.
- In Paper 14.7, Intel presents a universal modular hybrid LDO in 14nm CMOS that can be efficiently configured to provide any desired combination of PSRR and load transient response. Measurement results demonstrate up to 42dB of PSR, drawing 27 μ A with zero ripple.

Session 14 Highlights: Machine-Learning and Digital LDO Circuits

[14.1] A 65nm 1.1-to-9.1TOPS/W Hybrid-Digital-Mixed-Signal Computing Platform for Accelerating Model-Based and Model-Free Swarm Robotics

Paper 14.1 Authors: Arijit Raychowdhury

Paper 14.1 Affiliation: Georgia Institute of Technology, Atlanta, GA

[14.5] A 0.6-to-1.1V Computationally Regulated Digital LDO with 2.79-Cycle Mean Settling Time and Autonomous Runtime Gain Tracking in 65nm CMOS

Paper 14.5 Authors: Xun Sun

Paper 14.5 Affiliation: University of Washington, Seattle, WA

Subcommittee Chair: Edith Beigne, Facebook, Menlo Park, CA, Digital Circuits

CONTEXT AND STATE OF THE ART

- Robotics devices require a low-power, yet computationally capable, processing platform for their unique workloads, such as navigation.
- Recently, the concept of multiple collaborative robots, a.k.a. swam robotics, has been proposed to extend the capabilities robots.
- The hybrid digital and mixed-signal computing paradigm has demonstrated state-of-the-art computing energy-efficiency and throughput.
- Systems-on-chip require a number of voltage domains that provide optimal supply voltages to different parts of the chip.
- A digital LDO has emerged as a preferred choice for generating multiple voltage domains on-die. Recent works have demonstrated various circuit techniques to scale size and delay. To further improve the area footprint, more computational/algorithmic-centric approaches can be combined.

TECHNICAL HIGHLIGHTS

- **Georgia Institute of Technology presents a hybrid digital and mixed-signal computing platform for swarm robotics.**
 - In Paper 14.1, Georgia Institute of Technology presents a 1.1-to-9.1TOPS/W unified computation platform fabricated in a 65nm CMOS for swarm robotics, which: 1) supports both model-free and model-based swarm applications with dedicated nonlinear and linear processing blocks, and 2) demonstrates energy-efficient hybrid digital mixed-signal circuits, to enable energy-resolution scalability across a variety of swarm algorithms and swarm sizes.
- **The University of Washington presents a digital LDO having significant computational capability to reduce settling time.**
 - In Paper 14.5, the University of Washington presents computational power supply regulation (CR), exploiting computing for high-speed regulation. CR relies on deriving accurate regulator models, and solving resulting equations at runtime. The CR technique is incorporated into a digital LDO prototype in 65nm with a 2.79-cycle mean settling time.

APPLICATIONS AND ECONOMIC IMPACT

- *With the increasing interest of IoT and robotic devices, designing computing hardware that consumes low power has become an important issue. Low-power, yet computationally-capable hardware, is essential to extend the markets for the IoT and robotics.*
- *Modern processors and SoCs increasingly deploy multiple voltage domains to push the envelope of energy efficiency and performance. A low-dropout regulator is one of the most popular circuits to create a voltage domain. A miniaturized yet fast regulator is attractive within a range of processors from high-performance, to mobile, to embedded applications.*

Session 15 Overview: Power for 5G, Wireless Power, and GaN Converters

Power Management Subcommittee

Session Chair: Min Chen, Analog Devices, Milpitas, CA

Session Co-Chair: Johan Janssens, ON Semiconductor, Mechelen, Belgium

Subcommittee Chair: Yogesh Ramadass, Texas Instruments, Santa Clara, CA, Power Management

Power converters are widely used in many emerging applications like 5G communication, high-power wireless transfer, galvanically isolated systems and high-voltage automotive and offline systems. Efficiency, bandwidth, high frequency, low EMI, and high reliability are all key to these high-performance power converters. This session presents recent advances in high-bandwidth supply modulators for 5G systems, high-efficiency wireless power transfer, single-chip isolated power converters with on-chip transformers, and low-EMI high-reliability GaN power converters.

- In Paper 15.1, Samsung describes a supply modulator IC supporting 100MHz-envelope-tracking bandwidth for 5G sub-6GHz new radio transmitters. The proposed control scheme with a feed-forward fast-switching buck enables 88% of maximum efficiency with 5.8dB PAPR LTE modulated signal while achieving low output noise and output impedance.
- In Paper 15.2, Samsung presents a power management IC for a 5G mm-wave new radio (NR) phased-array transceiver. A novel symbol-power-tracking system is proposed featuring a fast transition of 90ns/V and 110ns/V for up- and down-tracking.
- In Paper 15.3, National Chiao Tung University describes a 13.56MHz GaN-based differential Class-E wireless power-transfer system delivering up to 100W of output power. A differential impedance-matching technique and reverse-conduction calibration technique provides a peak efficiency of 91%.
- In Paper 15.4, Analog Devices presents an isolated power-transfer system using fully integrated transformer with magnetic core. A fully symmetric power stage is utilized to achieve a peak efficiency of 52%, output power of 1.1W and passes CISPR 22 EMI limit by 5.8dB.
- In Paper 15.5, Analog Devices presents an 800mW isolated power-transfer system using an on-chip coreless transformer. Various circuit techniques reduce emissions to meet EMI standard CISPR 22 Class B with a 6dB margin.
- In Paper 15.6, the University of Texas, Dallas, presents a failure self-prognosis GaN power converter achieving in-situ aging condition monitoring using switch R_{ON} as precursor. To eliminate the effect of junction temperature, a gate-leakage-based, aging-independent junction temperature sensor is developed.
- In Paper 15.7, the University of Texas, Dallas, presents an 8.3MHz GaN power converter implementing Markov continuous spread-spectrum modulation, achieving the lowest EMI noise floor of 27dB μ V. One-cycle T_{ON} rebalancing suppresses output voltage jittering by 27.6dB.
- In Paper 15.8, Toshiba presents an active slew-rate-controlling gate driver with discrete-time background feedback. In combination with an initial boost pulse, the technique enables dV/dt maximization for robust minimization of switching loss and turn-on delay.

Session 15 Highlights: Power for 5G, Wireless Power and GaN Converters

[15.1] An 88%-Efficiency Supply Modulator Achieving 1.08 μ s/V Fast Transition and 100MHz Envelope-Tracking Bandwidth for 5G New Radio RF Power Amplifier

Paper Authors: J. S. Paek, D. Kim, and B. Cho

Paper Affiliation: Samsung Electronics

Subcommittee Chair: Yogesh Ramadass, Texas Instruments, Santa Clara, CA , Power Management

CONTEXT AND STATE OF THE ART

- *With the advent of 5G new radios, the supply modulator for the power amplifier needs to track much higher frequency envelope signal and achieve faster transition time with higher power efficiency.*

TECHNICAL HIGHLIGHTS

- ***In Paper 15.1 Samsung Electronics describes an 88% efficiency supply modulator with 1.08 μ s/V transition time and 100MHz envelope tracking bandwidth for 5G New Radio***
 - *Samsung describes a supply modulator IC supporting 100MHz envelope tracking bandwidth for a 5G sub-6GHz new radio transmitter. The proposed control scheme with a feed-forward fast-switching buck enables 88% of maximum efficiency with a 5.8dB PAPR LTE modulated signal while achieving low output noise and output impedance.*

APPLICATIONS AND ECONOMIC IMPACT

- *Improves overall efficiency of 5G new radio RF power amplifier for next generation cell phones*
- *Enables high efficiency, fast transition time, and 100MHz envelope tracking bandwidth*

Session 16 Overview: Frequency Synthesizers

RF Subcommittee

Session Chair: Xiang Gao, Zhejiang University, Hangzhou, China

Session Co-Chair: Jaehyouk Choi, Ulsan National Institute of Science and Technology, Ulsan, Korea

Subcommittee Chair: Piet Wambacq, imec, Leuven, Belgium, RF

This session presents the latest advances in digital and analog frequency synthesizers generating frequencies from 0.5 to 30GHz and covering diverse topics, such as ultra-low-power DPLLs, ultra-low-jitter sub-sampling PLLs, multi-loop BBPLL, FMCW synthesizers, and spurious tone mitigation techniques.

- In Paper 16.1, the Tokyo Institute of Technology describes a fractional-N DPLL with a mechanism to automatically switch between the subsampling and sampling modes. Implemented in 65nm CMOS, it achieved an ultra-low power of $265\mu\text{W}$ with a -237dB FoM and a -52dB worst-case fractional spur.
- In Paper 16.2, UNIST presents a 28-to-31GHz frequency synthesizer cascading subsampling PLL and injection-locking frequency multiplier. This design achieved an ultra-low jitter of 76fs_{RMS} in 65nm CMOS.
- In Paper 16.3, the University of Macau demonstrates a calibration-free PLL with discrete-time phase noise cancellation technique. The 2.4GHz-PLL design consumed 4.1mW while achieving -63dBc reference spur and $248\text{fs}_{\text{RMS}}$ integrated jitter.
- In Paper 16.4, UCLA describes an open loop frequency synthesizer with a digital spur cancellation technique. Designed with 28nm CMOS, it achieved an integrated rms jitter $<90\text{fs}$ and spurious tones $<-106\text{dBc}$ at a 2.42GHz carrier frequency.
- In Paper 16.5, UCLA presents a 28nm-CMOS fractional-N synthesizer for 802.11ax utilizing a background-calibrated reference quadrupler. It achieved a jitter of $110\text{fs}_{\text{RMS}}$, while consuming 22.8mW .
- In Paper 16.6, UCLA demonstrates a heterodyne fractional-N frequency synthesizer consisting of three loops: classical CP PLL, sub-sampling PLL, and BBPLL. It achieved $131\text{fs}_{\text{RMS}}$ jitter and -70dBc fractional spurs while consuming 13.4mW .
- In Paper 16.7, Politecnico di Milano describes a 30.6-to-34.2GHz fractional-N DTC-based PLL with sub-sampling bang-bang phase detection and a phase switching technique that halves the required DTC range. Fabricated in a 65nm LP process, it achieved $198\text{fs}_{\text{RMS}}$ jitter at 35mW power.
- In Paper 16.8, the University of Macau presents a sub-sampling PLL with an improved sub-sampling phase detector for better VCO isolation and low reference spur. Designed in 65nm CMOS, it achieved $71.16\text{fs}_{\text{RMS}}$ jitter with 10.4mW and a PLL FoM of -252.9dB at 26.4GHz.
- In Paper 16.9, University College Dublin demonstrates a fractional-N frequency synthesizer utilizing a divider controller with a nested MASH digital delta-sigma modulator and a probability mass redistributor for low fractional spur. Implemented in $0.18\mu\text{m}$ SiGe BiCMOS, it achieves a -80dBc in-band fractional spur at 2.5kHz offset at 4.48GHz output.

Session 16 Highlights: Frequency Synthesizers

[16.1] A 265 μ W Fractional-N Digital PLL with Seamless Automatic Switching Subsampling/Sampling Feedback Path and Duty-Cycled Frequency-Locked Loop in 65nm CMOS

[16.2] A 76fs_{rms} Jitter and -40dBc Integrated-Phase-Noise 28-to-31GHz Frequency Synthesizer Based on Digital Sub-Sampling PLL Using Optimally Spaced Voltage Comparators and Background Loop-Gain Optimization

Paper 16.1 Authors: H. Liu, Z. Sun, H. Huang, W. Deng, T. Siriburanon, J. Pang, Y. Wang, R. Wu, T. Someya, A. Shirane, K. Okada

Paper 16.1 Affiliation: Tokyo Institute of Technology

Paper 16.2 Authors: J. Kim*, H. Yoon*, Y. Lim, Y. Lee, Y. Cho, T. Seong, J. Choi

Paper 16.2 Affiliation: Ulsan National Institute of Science and Technology

* Equally credited authors

Subcommittee Chair: Piet Wambacq, imec, Leuven, Belgium, RF

CONTEXT AND STATE OF THE ART

- Lowering phase noise/jitter and power consumption are always important objectives when designing CMOS frequency synthesizers.
- The advent of the era of IoT demands frequency synthesizers with ultra-low power.
- 5G communication systems demand frequency synthesizers with ultra-low jitter.

TECHNICAL HIGHLIGHTS

- **265 μ W ultra-low-power LC-DCO based fractional-N DPLL (Paper 16.1)**
 - A fractional-N DPLL with a mechanism to automatically switch between the subsampling and sampling modes is described. Implemented in 65nm CMOS, it achieved an ultra-low power of 265 μ W with a -237dB FoM and a -52dB worst-case fractional spur.
- **28GHz frequency synthesizer with 76fs_{rms} jitter (Paper 16.2)**
 - UNIST presents a 28-to-31GHz frequency synthesizer cascading subsampling PLL and injection-locking frequency multiplier. This design achieved an ultra-low jitter of 76fs_{RMS} in 65nm CMOS.

APPLICATIONS AND ECONOMIC IMPACT

- PLLs achieving ultra-low power and integrated phase noise are presented.
- These PLLs will be the best solution for ultra-low-power wireless connectivity and 5G communication systems

Session 17 Overview: Technologies for Human Interaction & Health

Technology Directions Subcommittee

Session Chair: Patrick P. Mercier, University of California San Diego, La Jolla, CA

Session Co-Chair: Shuichi Nagai, Panasonic, Osaka, Japan

Subcommittee Chair: Makoto Nagata, Kobe University, Kobe, Japan, Technology Directions

Innovations in sensors, actuators, computation, and communication circuits are enabling new and exciting applications in human interaction and healthcare. This session begins with an invited system paper that describes how advances in artificial intelligence and processors, networks, and actuators have enabled new classes of human-interacting robots. The next three papers then describe innovations in voice-activity detection, large-scale tactile sensing, and low-power embedded motion detection systems for human-interactive applications. Subsequent papers introduce ultra-low-power body-area networking circuits, dual optical/electrical tomographic imaging circuits, and ultra-low-power PPG sensing for health-related applications.

- In Invited Paper 17.1, Sony presents key technological developments in processors, sensors, actuators, and wireless communications towards innovative new applications in AI and robotics. These are combined in a demonstration robotic platform called, *aibo*, which is a fully autonomous entertainment robot embedded with AI-based behavior control.
- In Paper 17.2, the University of Michigan demonstrates a voice and acoustic activity detector using mixer-based architecture and an ultra-low power neural network-based classifier. Due to 4× and 12× power reduction in feature extraction and neural processing, a 91.5%/90% speech/non-speech hit rate at 10dB SNR with power consumption of only 142nW is achieved.
- In Paper 17.3, Princeton University introduces an architecture for high-spatial-resolution tactile-sensing skins based on LAE-CMOS hybrid systems with compressed sensing. By readout and control with a resistive force-sensing array using ZnO TFTs, an acquisition error of $0.7k\Omega_{rms}$ over a 100k Ω -to-15k Ω sensing range, at energy and rate of 1.2 μ J/frame and 31fps is realized.
- In Paper 17.4, Texas Instruments presents a 0.13 μ m 16MHz FRAM micro-controller with an embedded piezoelectric strain sensor using an array of thin film Lead Zirconium Titanate (PZT) capacitors for motion detection. The sensor requires only 650nA and occupies an area of 0.6mm².
- In Paper 17.5, the University of California, Berkeley describes a 0.8mm³ neural recording system that is powered by and communicates via ultrasound. A linear AM backscatter technique is introduced that enables operation at a depth of up to 5cm while operating a small power-efficient LNA with -44dB THD over a 20mV_{pp} input range.
- In Paper 17.6, the University of California, San Diego presents a transceiver design to exploit the low path loss enabled by magnetic human body communication (mHBC). A test chip demonstrates reliable trans-body communication at 5Mb/s at TX and RX power consumptions of 18.56 and 6.3 μ W, respectively.
- In Paper 17.7, KAIST describes a portable lightweight (3g) system that can simultaneously image the skin in the electrical and optical domains to help improve skin disease diagnostics. Incorporation of diffused optical and electrical impedance tomography enables achieving 0.5mm sensitivity and 2mm selectivity.
- In Paper 17.8, EPFL presents a photoplethysmography (PPG) sensor that utilizes an array of dedicated pinned-photodiodes in a 0.18 μ m CIS process. Thanks to improved sensitivity offered by the diodes, the total power of the PPG sensor is 4.6 μ W.

Session 17 Highlights: Technologies for Human Interaction & Health

[17.6] A Sub-40 μ W 5Mb/s Magnetic Human Body Communication Transceiver Demonstrating Trans-Body Delivery of High-Fidelity Audio to a Wearable In-Ear Headphone

Paper 17.6 Authors: Jiwoong Park, Patrick P. Mercier

Paper 17.6 Affiliation: University of California San Diego, La Jolla, CA

Subcommittee Chair: Makoto Nagata, Kobe University, Kobe, Japan, Technology Directions

CONTEXT AND STATE OF THE ART

- Human Body Communication (HBC) is highly desirable for emerging wearables where high-throughput wireless data communication at ultra-low-power is needed.
- HBC based on capacitive-coupling has been demonstrated, however, magnetic-coupled HBC (mHBC), which is insensitive to posture, has not been shown until now.

TECHNICAL HIGHLIGHTS

- **5Mb/s mHBC transceiver to enable high-fidelity audio streaming across the body, for example from hand to ear in the provided demonstration.**
 - The presented transceiver exploiting the low path loss offered by mHBC consumes only 18.56 μ W (TX) and 6.3 μ W (RX).
 - A power oscillator is used to efficiently generate OOK-modulated magnetic yields via Q=50 mHBC coils, communicating at 5Mb/s at a carrier frequency of 40MHz despite the high Q via an injection-locked kick-start circuit.

APPLICATIONS AND ECONOMIC IMPACT

- mHBC provides much more reliable wireless connectivity among on-body wearables and mobile devices with an order of magnitude less energy consumption.

Session 18 Overview: Analog Techniques

Analog Subcommittee

Session Chair: David Blaauw, University of Michigan, Ann Arbor, MI

Session Co-Chair: Byungsub Kim, Pohang University of Science and Technology, Pohang, Korea

Subcommittee Chair: Kofi Makinwa, Delft University of Technology, Delft, Analog

This session presents advances in audio amplifiers, auto-zeroed buffers and capacitance-to-digital converters, followed by three papers describing low-power and fast-startup crystal oscillators and two papers describing new voltage references. The audio amplifier (Paper 18.1) achieves -105dBc THD+N. The auto-zeroed buffer (Paper 18.2) incurs a $\sqrt{2}$ noise penalty, which approaches the theoretical limit. The capacitance-to-digital converter (Paper 18.3) achieves a resolution of 0.29fF resolution with 16fJ/conversion-step. Two fast startup crystal oscillators (Papers 18.4 and 18.5) use dynamic frequency and phase locking, respectively, to achieve $\sim 20\mu\text{s}$ startup time. A 32kHz crystal oscillator (Paper 18.6) consumes only 0.55nW. The final two papers (Paper 18.7 and 18.8) present advances in low-power and sub-1V voltage references.

- In Paper 18.1, MediaTek describes an audio decoder that shifts reference noise to the sub-audio band and a new frequency compensation scheme that allows its load capacitance to be increased from 390pF to 22nF. The decoder achieves -105dBc THD+N (-114dBc HD2) at 2.8V peak-peak swing and 120dB dynamic range
- In Paper 18.2, Delft University of Technology describes an auto-zeroed voltage buffer with a novel chopped stabilization loop. This allows its low-frequency noise density to be lowered from $\sqrt{(5)} \times$ white noise to nearly $\sqrt{(2)} \times$. It also achieves an offset of 0.4 μV and 0.8pA input current which is nearly constant over input voltage.
- In Paper 18.3, the University of Texas, Austin describes a two-step capacitance-to-digital converter that combines a coarse SAR ADC and a fine time-domain-based Delta-Sigma Modulator. It achieves a resolution of 0.29fF and energy consumption of 16fJ per conversion-step.
- In paper 18.4, the University of California at Los Angeles describes a 32kHz crystal oscillator that uses an up/down-conversion technique that allows its sustaining amplifiers to operate near DC. The oscillator achieves 0.55nW at 0.5V supply and an Allan deviation floor of 14ppb.
- In Paper 18.5, the University of Illinois at Urbana-Champaign describes a fast crystal startup technique that uses a two-step signal-injection technique based on an RC oscillator that is subsequently precisely tuned by a PLL. The 54MHz oscillator achieves 20 μs startup time across a temperature range of -40°C to 85°C.
- In Paper 18.6, Dialog Semiconductor describes a fast crystal startup technique that uses dynamic phase alignment to allow quasi-synchronized signal injection. The 32MHz oscillator achieves 24 μs startup time and 20.2nJ startup energy and demonstrates operation across -40°C to 140°C.
- In Paper 18.7, Taiwan Semiconductor Manufacturing Company describes a sub-1V bandgap voltage reference that uses a current-controlled feedback loop to improve current-mirror matching. It achieves an average temperature coefficient of 40.5ppm at 0.7V and a 3σ accuracy of 2.35% at 25°C across 0.7V-to-0.9V supply.
- In Paper 18.8, Pohang University of Science and Technology describes a hybrid V_t and bandgap voltage reference that uses a process compensation scheme to achieve less than 0.52% variation across corners. With a 0.69V reference voltage, it consumes 192pW and has a temperature coefficient of 33ppm/°C and a line sensitivity of 0.02%/V.

Session 18 Highlights: Analog Techniques

[18.4] A 0.55nW/0.5V 32kHz Crystal Oscillator Based on a DC-Only Sustaining Amplifier for IoT.

[18.5] A 54MHz Crystal Oscillator with >30× Start-Up Time Reduction Using 2-Step Injection in 65nm CMOS

Paper 18.4 Authors: Hani Esmaeelzadeh

Paper 18.4 Affiliation: University of California at Los Angeles, Los Angeles, CA

Paper 18.5 Authors: Karim Megawer

Paper 18.5 Affiliation: University of Illinois at Urbana-Champaign, Urbana, IL

Subcommittee Chair: Kofi Makinwa, Delft University of Technology, Delft, Analog

CONTEXT AND STATE OF THE ART

- *Internet of things (IoT) devices require low power and fast-starting crystal oscillators to provide accurate timing references for radio communication and sensor interfacing. There is a continuing quest to improve device performance for IoT applications.*

TECHNICAL HIGHLIGHTS

- **New record low-power crystal oscillator with precise timing for IoT applications**
 - *In paper 18.4, the University of California at Los Angeles describes a 32kHz crystal oscillator that uses up/down-conversion and two low-bandwidth 50pW amplifiers to sustain its oscillation. The oscillator draws only 0.55nW from a 0.5V supply and achieves a 14ppb Allan deviation floor.*
- **Crystal oscillator approaches fast startup theoretical minimum and enables power savings for IoT**
 - *In Paper 18.5, the University of Illinois at Urbana-Champaign describes a fast crystal startup technique that uses a two-step signal injection technique based on an RC oscillator, which is subsequently precisely tuned by a PLL. The 54MHz oscillator achieves 20μs startup time across a temperature range of -40°C to 85°C.*

APPLICATIONS AND ECONOMIC IMPACT

- *By lowering the power for starting and sustaining crystal oscillators, sensors and mobile devices intended for the internet of things (IoT) can operate at lower energy, thereby extending their battery life and enabling new applications.*

Session 19 Overview: Adaptive Digital and Clocking Techniques

Digital Circuit Techniques Subcommittee

Session Chair: John Maneatis, True Circuits, Los Altos, CA

Session Co-Chair: Alicia Klinefelter, Nvidia, Durham, NC

Subcommittee Chair: Edith Beigne, Facebook, Menlo Park, CA, Digital Circuits

This session focuses on circuits that adapt to PVT, workload, and precision requirements, including novel techniques in clocking and digital regulators. The presented adaptive digital and clocking circuits demonstrate minimum energy/power-point tracking, adaptivity and unified clock and voltage control schemes, instruction-based dynamic clock scaling, digital leakage compensation for clocking circuits, adaptive forward/back biasing, and time-series processing for energy-efficient processing. The first two papers introduce novel techniques to track minimum energy and power in the system to adjust the body bias or supply voltage. The next paper unifies the output clock and the voltage supply control generation into a single loop to reduce voltage margins and increase response times. The following paper exploits instruction-level dynamic timing slack to guide elastic pipeline timing redistribution guiding clock period adjustment. The last three papers cover clocking and biasing schemes to improve performance. The first of these papers focuses on reducing static phase offset and reference spurs that can degrade performance. The next paper explores back biasing in FDSOI to maximize power efficiency. The final paper uses a novel multi-bit time flip-flop to improve energy efficiency in time series classification.

- In Paper 19.1, the University of Washington presents a fully integrated digital technique for total energy-per-cycle minimization under performance constraints demonstrated on a switched-capacitor-based 0.38-to-0.58V microprocessor in 65nm CMOS. Post-silicon measurements show minimum-energy-point (MEP) tracking within 5mV of the actual MEP across operating conditions, and seamless transition to performance-constrained operation.
- In Paper 19.2, the University of Michigan makes a key observation that at the optimal energy operating point, the ratio of leakage to dynamic power is a constant value across temperature, process, and workload. A Cortex-M0 processor incorporates a control loop with a custom DC-DC converter to dynamically measure the leakage ratio and automatically adjust the body bias and supply voltage to achieve 6.4pJ/cycle at 0.55V and 200kHz.
- In Paper 19.3, Qualcomm presents a 7nm all-digital fast response 2-phase buck regulator with 3 turns and 6 metal-level package inductors that unifies the clock and voltage supply control generation into a single loop to reduce voltage margins arising from dynamic parameter variations with an area of 0.0067mm². Measurements show a fast response time of 60ns from a 178mA output current step with maximum FOVT measured at 3.4GHz, and VOUT is regulated from 0.45 to 0.9V with loads from 1 to 900mA.
- In Paper 19.4, Northwestern University introduces an instruction-based hierarchical adaptive clocking scheme to exploit instruction-level deterministic dynamic-timing slack for out-of-order multicore deep-pipeline graphic processors. Critical-path messengers and elastic pipeline timing redistribution are used to guide the clock period adjustment with additional enhancement for machine learning applications and the proposed clocking scheme achieves 18.2% performance improvement or 35.8% energy savings in benchmark programs.
- In Paper 19.5, Intel presents a digital leakage compensation circuit for an analog PLL in 10nm FinFET CMOS technology to overcome the sensitivity to device or defect leakage. The PLL has a frequency range of 0.5 to 5GHz, a power dissipation of 0.32 to 2.65mA, and an area of 0.026mm², and the static phase error, random jitter, and reference spur are reduced from 230ps, 2.23ps, -44.61dB to -8ps, 1.87ps, -55.52dB, respectively, at 3.2GHz with 1.53mA current and an FoM of -233dB.
- In Paper 19.6, Université Catholique de Louvain presents a complete ULP MCU SoC in 28nm FDSOI, including an on-chip dual-loop digital adaptive forward-back-bias generator. It pushes the performance trade-off beyond the state of the art by full exploitation of the FDSOI back-biasing capability with peak efficiency of 280DMIPS/mW at 40DMIPS, an active power dissipation of 3μA/MHz at 48MHz, and an area of 0.7mm².
- In Paper 19.7, Northwestern University proposes a scalable pipelined DTW engine in the time-domain for time-series classification using a novel multi-bit time flip-flop with an area of 1.67mm². It achieves a 25× improvement in processing time

with half of the error rate, leading to the highest reported throughput of 140×10^9 cell-updates/s for DNA applications, and can run at 0.7V with only 2.3% increase in error rate.

Session 19 Highlights: Adaptive Digital and Clocking Techniques

[19.1] Computationally Enabled Total Energy Minimization Under Performance Requirements for a Voltage-Regulated 0.38-to-0.58V Microprocessor in 65nm CMOS

[19.2] A 6.4pJ/Cycle Self-Tuning Cortex-M0 IoT Processor Based on Leakage-Ratio Measurement for Energy-Optimal Operation Across Wide-Range PVT Variation

Paper 19.1 Authors: Fahim ur Rahman, Rajesh Pamula, Akshat Boora, Xun Sun, Visvesh Sathe

Paper 19.1 Affiliation: University of Washington, Seattle, WA

Paper 19.2 Authors: Jeongsup Lee¹, Yiqun Zhang¹, Qing Dong¹, Wooteak Lim¹, Mehdi Saligane¹, Yejoong Kim¹, Seokhyun Jeong¹, Makoto Yasuda², Satoru Miyoshi³, Masaru Kawaminami⁴, David Blaauw¹, Dennis Sylvester¹

Paper 19.2 Affiliation: ¹University of Michigan, Ann Arbor, MI, ²Fujitsu Semiconductor, Tokyo, Japan, ³Fujitsu America, Sunnyvale, CA, ⁴Fujitsu America, Sunnyvale, CA

Subcommittee Chair: Edith Beigne, Facebook, Menlo Park, CA, Digital Circuits

CONTEXT AND STATE OF THE ART

- Processors, ranging from small embedded cores in systems-on-chip to large multicore servers, aim to minimize total energy consumption during workload execution while satisfying a target performance.
- The minimum energy varies during processor operation, depending on changes in the dynamic and leakage currents.

TECHNICAL HIGHLIGHTS

- The University of Washington demonstrates an on-die minimum-energy-operation tracking technique in conjunction with a unified clock frequency and switched-capacitor voltage regulator to minimize total energy for a target performance. (Paper 19.1)**
 - In a single control loop, the unified clock-frequency (Fclk) and switched-capacitor (SC) voltage (VDD) regulator continuously monitor the Fclk and adjusts VDD to lock Fclk to a target reference frequency. The on-die computational minimum-energy-point (MEP) tracking design monitors several key parameters in the SC VDD regulator to search and optimize VDD to balance dynamic and leakage energies for minimum total energy in a Cortex M0 processor and FFT accelerator. Across 20 dies and temperatures ranging from -30 to 120°C, the computation MEP tracking achieves the optimum VDD within 5mV.
- The University of Michigan minimizes the total energy for a Cortex M0 processor by maintaining a constant ratio of the leakage to dynamic currents by optimizing VDD and body bias for a target performance in an SC voltage regulator. (Paper 19.2)**
 - By observing that the minimum energy occurs near a constant ratio of leakage current to dynamic current across process, temperature, and workload variations, an on-die control loop dynamically measures the leakage ratio and processor speed with a critical-path monitor and automatically adjusts V_{DD} and body bias to minimize total energy. Measurements demonstrate the ability to track an optimal ratio across temperature ranging from -20-to-125°C and 5 process corners from split-wafer lots to achieve 6.4pJ/cycle.

APPLICATIONS AND ECONOMIC IMPACT

- Low-power IoT and high-performance systems drive the need for processor energy-efficiency improvements to achieve low cost and increased performance.

Session 20 Overview: Noise-Shaped and VCO-Based ADCs

Data Converter Subcommittee

Session Chair: Yun-Shiang Shu, MediaTek, Hsinchu City, Taiwan

Session Co-Chair: Bob Verbruggen, Xilinx, Dublin, Ireland

Subcommittee Chair: Mike Flynn, University of Michigan, Ann Arbor, MI, Data Converters

Noise-shaping and VCO-based ADCs have been an area of continued interest in the data converter community. This session features 7 designs using these techniques, with bandwidths ranging from 25MHz to 2.5GHz and SNDRs from 45.2dB to 76.6dB, highlighting the wide applicability of these techniques. This session also marks the first 7nm ADC published at ISSCC.

- In Paper 20.1, the Katholieke Universiteit Leuven describes a 28nm time-interleaved VCO-based ADC. It achieves 45.2dB SNDR with a Nyquist input at 5GS/s, while consuming 22.7mW.
- In Paper 20.2, MediaTek demonstrates a technique for passive signal-residue summation in a noise-shaping SAR ADC in 14nm FinFET technology. It achieves 66.6dB SNDR in a 40MHz bandwidth consuming 1.25mW of power.
- In Paper 20.3, the University of Michigan shows how time-interleaving can be combined with noise-shaping for the first time-interleaved noise-shaping SAR ADC. Implemented in 40nm CMOS, the design achieves 70.4dB SNDR in a 50MHz bandwidth while sampling at 400MS/s and consuming 13mW.
- In Paper 20.4, MediaTek shows the first 7nm ADC at ISSCC, using a linearized DAC and digital noise coupling compensation. The design achieves 74dB SNDR in a 25MHz bandwidth while consuming only 3.8mW.
- In Paper 20.5, the University of Macau demonstrates a 4th-order sturdy-MASH DSM using a noise-coupling technique with a zeroth-order second stage. The design achieves 76.6dB SNDR in a 50MHz bandwidth consuming 29.2mW of power, without requiring any DAC calibration or error shaping.
- In Paper 20.6, MediaTek shows a dual-mode delta-sigma including variable gain and filtering for an 802.11ax analog baseband. The 28nm design achieves 64.9dB SNDR in 80MHz bandwidth consuming 7.3mW of power, or 76.8dB SNDR in 10MHz bandwidth consuming 4.15mW of power.
- In Paper 20.7, the University of Macau shows a wideband CTDSM with a preliminary sampling and quantization technique to increase the time available for quantization. The design, implemented in 28nm CMOS achieves 72.6dB SNDR in 100MHz bandwidth consuming 16.3mW of power.

Session 20 Highlights: Noise-Shaped and VCO-Based ADCs

[20.4] An 8 \times -OSR 25MHz-BW 79.4dB/74dB DR/SNDR CT $\Delta\Sigma$ Modulator Using 7b Linearized Segmented DACs with Digital Noise-Coupling-Compensation Filter in 7nm FinFET CMOS

[20.7] A 72.6dB-SNDR 100MHz-BW 16.36mW CTDSM with Preliminary Sampling and Quantization Scheme in Backend Subranging QTZ

Paper 20.4 Authors: Tien-Yu Lo, Chan-Hsiang Weng, Hung-Yi Hsieh, Ting-Yang Wang, Yun-Shiang Shu, Pao-Cheng Chiu

Paper 20.4 Affiliation: MediaTek Inc., Hsinchu, Taiwan

Paper 20.7 Authors: Wei Wang¹, Chi-Hang Chan¹, Yan Zhu¹, Rui P. Martins^{1,2}

Paper 20.7 Affiliation: ¹University of Macau, Macau, ²Instituto Superior Tecnico/University of Lisboa, Lisboa, Portugal

Subcommittee Chair: Michael Flynn, University of Michigan at Ann Arbor, Ann Arbor, MI

CONTEXT AND STATE OF THE ART

- A power-efficient SAR ADC quantizer combined with a mismatch error shaping technique for a segmented DAC in a 7nm process enables a high-resolution multi-bit quantizer in a continuous-time delta-sigma modulator to achieve high power efficiency.
- Preliminary sampling in a sub-ranging ADC minimizes the excess loop delay introduced by a 7b quantizer and allows stable operation of a continuous-time delta-sigma modulator at GHz sampling rate, thereby enabling high signal bandwidth.

TECHNICAL HIGHLIGHTS

- **MediaTek demonstrates a continuous-time delta-sigma modulator in 7nm CMOS with the state-of-the art power efficiency.**
 - The modulator with a 7b DAC achieves 74dB SNDR in 25MHz bandwidth with a Schreier FoM of 172.2dB and a Walden FoM of 18.6fJ/conversion-step.
- **University of Macau introduces a 100MHz bandwidth continuous-time delta-sigma modulator with ~2 \times higher power efficiency compared to state-of-the-art modulators with similar signal bandwidth.**
 - With a preliminary sampling quantizer, the modulator operating at a 2GHz sampling rate achieves 100MHz bandwidth with a Schreier FoM of 170.5dB and a Walden FoM of 23.4fJ/conversion-step.

APPLICATIONS AND ECONOMIC IMPACT

- ADCs designed in deeply scaled CMOS processes can be integrated in digital-intensive SoCs for various applications.
- Wide-bandwidth continuous-time delta-sigma modulators with high power efficiency satisfy the perpetual demand of high data rate in wireless communications.

Session 21 Overview: 4G/5G Transceivers

Wireless Subcommittee

Session Chair: Yiwu Tang, Qualcomm Technologies Inc., San Diego, CA

Session Co-Chair: Kyoohyun Lim, Future Communications IC (FCI), Republic of Korea

Subcommittee Chair: Stefano Pellerano, Intel, Hillsboro, OR, Wireless

Advancement from 4G to 5G transceivers in both sub-6GHz and mm-wave bands provides tremendous opportunities in high data throughput and low latency communications. This session includes advanced wireless technologies showing a 28GHz phased-array beamformer utilizing a neutralized bi-directional technique supporting dual-polarized MIMO, a 27-to-41GHz MIMO receiver with N-Input-N-Output using scalable cascaded autonomous array-based high-order spatial filters, a reconfigurable bidirectional 28/37/39GHz front-end supporting MIMO-TDD, Carrier Aggregation (CA) TDD and FDD/Full-Duplex with self-interference cancellation, an LTE-A transceiver with 4RX/2TX inter-band CA, 2-Carrier 4x4 MIMO and HPUE Capability, a 5G Sub-6GHz ZIF and mm-wave IF transceiver with MIMO and CA, a sub-6GHz 5G New Radio transceiver supporting EN-DC with 3.15Gb/s DL and 1.27Gb/s UL, and a receiver with mixed-signal circuit technique for cancellation of multiple modulated spurs in 4G/5G CA Transceivers.

- In Paper 21.1, the Tokyo Institute of Technology and NEC Corporation present a 28GHz dual-polarized bi-directional beamformer achieving an SC data rate of 15Gb/s/pol. in 64QAM in a 1m OTA measurement. 2x2 DP-MIMO communication in 64QAM with 400MHz 5G NR signal is realized. A saturated EIRP of 57.6dBm can be supported by the 128H+128V array.
- In Paper 21.2, the Georgia Institute of Technology reports a wideband 27-to-41GHz RX with high spatial selectivity by employing several cascaded scalable high-order Autonomous Spatial Filters (ASFs), which autonomously rejects multiple wideband modulated in-band blockers and achieves 3Gb/s 64QAM and 0.8Gb/s 256QAM over full FoV.
- In Paper 21.3, Carnegie Mellon University presents a reconfigurable area-efficient bidirectional 28/37/39GHz front-end with self-interference cancellation in digital and power-efficient fully connected hybrid beamformers supporting MIMO and CA.
- In Paper 21.4, MediaTek presents a 28nm CMOS LTE-A transceiver to support up to 4RX / 2TX inter-band CA and high-power user equipment (HPUE) as well as 2-carrier 4x4 MIMO with 256QAM to provide >2Gb/s downlink capability. The chip consumes 88mA battery current with 25mm² die area in a flip-chip chip-scale package.
- In Paper 21.5, Intel presents a 28nm bulk CMOS 4G/5G transceiver covering sub-6GHz bands in zero-IF while providing a 10.56GHz IF for mm-wave bands. It features an MPHY Gear 3 interface supporting MIMO and up to 800MHz bandwidth with carrier aggregation for a full 5G solution.
- In Paper 21.6, Samsung reports a 14nm FinFET CMOS single-chip RFIC that supports 2G, 3G, LTE, and SA/NSA sub-6GHz 5G NR with EN-DC in die area of 38.4mm². The transceiver with 14 RX and 2 TX paths using on-chip DCXO and high-speed digital data interface with baseband SOC achieves a peak data throughput of 3.15Gb/s DL and 1.27Gb/s UL.
- In Paper 21.7, Johannes Kepler University and Intel present a 28nm CMOS receiver that can cancel multiple blocker-induced distortions without prior knowledge of their carrier frequencies by up to 33dB for blocker power levels of up to -10dBm at the LNA input.

Session 21 Highlights: 4G/5G Transceivers

[21.2] A 27-to-41GHz MIMO Receiver with N-Input-N-Output Using Scalable Cascadable Autonomous Array-Based High-Order Spatial Filters for Instinctual Full-FoV Multi-Blocker/Signal Management

[21.6] A Sub-6GHz 5G New Radio RF Transceiver Supporting EN-DC with 3.15Gb/s DL and 1.27Gb/s UL in 14nm FinFET CMOS

Paper 21.2 Authors: Min-Yu Huang, Hua Wang

Paper 21.2 Affiliation: Georgia Institute of Technology, Atlanta, GA

Paper 21.6 Authors: Jongwoo Lee, Sangwook Han, Joonhee Lee, Byoungjoong Kang, Jeongyeol Bae, Jaehyuk Jang, Seunghyun Oh, Suseob Ahn, Sanghoon Kang, Quang-Diep Bui, Kiyong Son, Hyungsun Lim, Daechul Jeong, Ronghua Ni, Yongrong Zuo, Ilyong Jong, Chih-Wei Yao, Seungchan Heo, Thomas Byunghak Ch

Paper 21.6 Affiliation: Samsung Electronics, Hwaseong, Korea

Subcommittee Chair: Stefano Pellerano, Intel, Hillsboro, OR, Wireless

CONTEXT AND STATE OF THE ART

- 5G New Radio (NR) will deliver significantly faster and more responsive mobile broadband experiences with both sub-6GHz and mm-wave bands deployed to provide wide bandwidth for high data throughput. It will require advanced techniques in carrier aggregation, MIMO, high-order modulation, phased-array beamforming, and interference cancellation to achieve high spectral efficiency.
- These high-data-rate systems require very high signal fidelity, which makes them susceptible to interferers commonly found in dense deployments. Array-based, high-order spatial filtering with automatic notching of multiple blockers promises an intelligent approach to signal quality and interferer management.
- Sub-6GHz 4G + 5G concurrency transceivers pave the way toward 5G NR deployment in existing 4G infrastructure while delivering multi-Gb/s data rates for both downlink and uplink.

TECHNICAL HIGHLIGHTS

- **Scalable spatial blocker filtering enables MIMO reception with reduced power, enabling MIMO architectures at mm-wave.**
 - In paper 21.2, Georgia Institute of Technology presents an approach to extend spatial cancellation to mm-wave frequencies using cascaded spatial filters that support Gb/s MIMO operation at 27-to-41 GHz carrier frequencies.
- **Integrated transceivers simultaneously support 4G and 5G, promising multi-Gb/s data rates in our phones on new 5G networks while being compatible with legacy standards.**
 - In Paper 21.6, Samsung reports a 14nm FinFET CMOS RFIC with 14RX and 2TX paths that supports 2G, 3G, LTE, and SA/NSA sub-6GHz 5G NR with EN-DC achieving peak data throughput of 3.15Gb/s DL and 1.27Gb/s UL.

APPLICATIONS AND ECONOMIC IMPACT

- 5G radio technology promises a 10-to-100 fold increase in data rates with a 10× reduction in latency. This will continue the exponential growth of traditional mobile data traffic and open new opportunities in machine autonomy, virtual reality and pervasive connected devices and sensors.

- *Deployment of 5G infrastructure has begun and estimated current market size exceeds \$10B. The market is expected to grow rapidly and exceed \$100B by 2022.*

Session 22 Overview: Physiological Monitoring

IMMD Subcommittee

Session Chair: Esther Rodriguez-Villegas, Imperial College London, London, UK

Session Co-Chair: Rikky Muller, University of California, Berkeley, Berkeley, CA

Subcommittee Chair: Chris Van Hoof, imec, Leuven, Belgium, IMMD

This session involves wearable and implantable SoCs that record weak biopotential signals in the presence of real-life interference and under stringent power and size constraints. These new SoCs and corresponding techniques pave the way toward robust non-invasive devices that involve direct sensing, multi-sensor fusion and implantable closed-loop sensor/actuator systems. These advancements enable multimode physiological recordings from nearly every major organ system.

- *In Paper 22.1, imec introduces an SoC for concurrent and synchronized ECG, bioimpedance and PPG recording, incorporating accelerators and an ARM Cortex-M4f microprocessor. The SoC also includes cryptography IP and an SRAM-based PUF solution. The $4320 \times 4320 \mu\text{m}^2$ SoC consumes $769 \mu\text{W}$. The total average system power drawn from the battery, including LDO, LEDs and accelerometer is 2mW , allowing an operating time of more than 3 weeks on 2 ZnAir batteries.*
- *In Paper 22.2, the University of California, San Diego presents an active electrode ExG platform achieving 101dB DR and motion artifact resilience, consuming $228 \mu\text{W}$ per channel. The IC has been fabricated in a 65nm technology.*
- *In Paper 22.3, KAIST presents a bio-impedance sensor IC for wearable/implantable blood status monitoring. The sensor IC demonstrates thoracic impedance variation (TIV) and impedance cardiography (ICG), consuming less than $10 \mu\text{W}$ of power.*
- *In Paper 22.4, KAIST presents a biopotential amplifier that has a large tolerance to common-mode interference (CMI) for reliable two-electrode ECG recording. The IC demonstrates suppression of up to 30V of CMI, consuming $27.8 \mu\text{W}$.*
- *In Paper 22.5, imec presents a bio-impedance readout IC for low-noise 2-electrode measurement by implementing a circuit that simultaneously mitigates $1/f$ noise and cancels reference current noise. The IC is demonstrated in measurement on the human body.*
- *In Paper 22.6, Shanghai Jiao Tong University presents an impedance tomography SoC based on frequency division multiplexing, supporting 13 voltage-sensing channels. Data throughput is reduced by $10\times$, while low power ($118 \mu\text{W}$) and area (0.87mm^2) per channel are achieved.*
- *In Paper 22.7, National Cheng Kung University presents a highly integrated SoC that combines a wireless interface, neural signal sensing, computation, and both electrical and optical stimulation in the brain. The system is demonstrated to detect and suppress seizures in rodents.*
- *In Paper 22.8, the University of Toronto presents a system for bidirectional neurostimulation from scalp electrodes utilizing temporally interfering electric fields. EEG recording circuits and a sleep-state classifier trigger responsive neurostimulation.*

Session 22 Highlights: Physiological Monitoring

[22.1] A 769 μ W Battery-Powered Single-Chip SoC with BLE for Multi-Modal Vital Sign Health Patches

Paper 22.1 Authors: Mario Konijnenburg, Roland van Wegberg, Shuang Song, Hyunsoo Ha, Wim Sijbers, Jiawei Xu, Stefano Stanzione, Chris van Liempd, Dwaipayan Biswas, Arjan Breeschoten, Peter Vis, Chris van Hoof, Nick van Helleputte

Paper 22.1 Affiliation: imec - Netherlands; imec, Leuven, Belgium

Subcommittee Chair: Chris Van Hoof, imec, Leuven, Belgium, IMMD

CONTEXT AND STATE OF THE ART

- *Multi-modal physiological monitoring with the form factor of a low-cost easy-to-use wearable patch has the potential to offer improved monitoring and diagnosis of a number of chronic conditions.*
- *Due to usability requirements, stringent constraints are imposed on the system power consumption. The constraints become even more challenging as the number of sensing modalities increase, including ECG, bio-impedance, and photoplethysmogram (PPG).*
- *In addition to the constraints of usability and weak physiological signal acquisition, these systems need to take into account typical constraints of medical devices, including security and reliability of data transmission.*

TECHNICAL HIGHLIGHTS

- **IMEC introduces an SoC with built-in support for concurrent and synchronous dual-channel ECG, bio-impedance and PPG.**
 - *A power management strategy allows operation of the full system drawing only 2mW average power from the battery.*
 - *The SoC includes cryptography IP supporting a wide range of protocols combined with an SRAM-based PUF solution that guarantees a chip-specific unique cryptographic key.*
 - *The chip has several interfaces, including a BLE radio and USB2.*
 - *The high level of integration in 55nm technology allows a compact implementation ($\sim 18\text{mm}^2$) saving area, cost, power and weight.*

APPLICATIONS AND ECONOMIC IMPACT

- *Chronic conditions account for approximately 50% of the total burden of diseases in the world and for over 60% of all causes of deaths. Due to the high cost associated to such conditions, optimum follow up and management is not possible with currently existing healthcare pathways. Wearable vital sign monitoring technologies have the potential to allow remote and/or frequent monitoring of chronic conditions and consequently, change healthcare management pathways, leading to better quality of life for these patients and improved disease outcomes.*

Session 23 Overview: DRAM

Memory Subcommittee

Session Chair: Wolfgang Spirkel, Micron Semiconductor, Munich, Germany

Session Co-Chair: Dong Uk Lee, SK hynix, Icheon, Korea

Subcommittee Chair: Jonathan Chang, TSMC, Hsinchu, Taiwan

First devices for the new DRAM standards LPDDR5 and DDR5 are implementing improvements in bandwidth and power efficiency. The new devices will have a huge impact on a very wide range of applications, from IoT applications and smartphones to server and workstation applications. A new proposal for managed LRDIMM promises to reduce cost and power, and to provide capacities up to 512GB. For next generation DRAM interfaces a PAM-3 transceiver with 27Gb/s/pin on the base of 3 bits per 2 symbols is presented.

- In Paper 23.1, Samsung presents a 1st-generation 10nm class process LPDDR5 with schemes that increase the maximum bandwidth such as WCK clocking and non-target ODT (NT-ODT). It also reduces power consumption using techniques such as dynamic voltage frequency scaling (DVFS), and a deep-sleep mode (DSM).
- In Paper 23.2, SK hynix presents a DDR5 SDRAM to overcome bandwidth, power and capacity limitations of DDR4. This paper presents a 16Gb 6.4Gb/s/pin DDR5 SDRAM with a phase-rotator-based DLL, write-level training, and RX/TX with the enhanced DFE/FFE. The energy efficiency is improved by more than 30% with 1.1V/1.8V VDD and VPP.
- In Paper 23.3, Korea University presents a 3bit/2UI 1.03pJ/bit PAM-3 single-ended TRX. An 18Gbaud/s PAM-3 symbol (equal to 27Gb/s) is generated with an output driver voltage of 0.6V and a 1/3-rate forwarded clock frequency of 9GHz. The RX adopts a 1-tap tri-level DFE, which has the same complexity as for NRZ signaling to equalize the PAM-3 signal. Fabricated in a 28nm CMOS technology, the proposed PAM-3 TRX can be utilized for the next generation memory interface with low power.
- In Paper 23.4, SK hynix presents a Managed DRAM Solution (MDS) DIMM with 512GB capacity. It consists of ODP-structured (Octal Die Package) memory (media) and a media controller with ECC. This paper deals with architecture and ODP structure of the media for cost minimization, and a pre-CMD scheme for power reduction. A net die decrease of 26% compared to conventional DRAM with the same process and same capacity was achieved. The DIMM power consumption is 12W.

Session 23 Highlights: DRAM

[23.1] A 7.5Gb/s/pin LPDDR5 SDRAM with WCK Clocking and Non-Target ODT for High Speed and with DVFS, Internal Data Copy, and Deep Sleep Mode for Low Power

[23.2] A 1.1V 1nm 6.4Gb/s/pin 16Gb DDR5 SDRAM with a Phase-Rotator-Based DLL, High-Speed SerDes and RX/TX Equalization Scheme

Paper 23.1 Authors: Kyung-Soo Ha, Chang-Kyo Lee, Dongkeon Lee, Daesik Moon, Jin-Hun Jang, Hyong-Ryol Hwang, Hyungjoon Chi, Junghwan Park, Seungjun Shin, Dukha Park, Sang-Yun Kim, Sukhyun Lim, Kiwon Park, YeonKyu Choi, Young-Hwa Kim, Younghoon Son, Hyunyocho Cho, Byongwook Na, Hyo-Joo Ahn, Seungseob Lee, Seouk-Kyu Choi, Youn-Sik Park, Seok-Hun Hyun, Soobong Chang, Hyuck-Joon Kwon, Jung-Hwan Choi, Tae-Young Oh, Young-Soo Sohn, Kwang-Il Park, Seong-Jin Jang

Paper 23.1 Affiliation: Samsung Electronics, Hwaseong, Korea

Paper 23.2 Authors: Dongkyun Kim, Minsu Park, Sungchun Jang, Junyong Song, Hankyu Chi, Geunho Choi, Sunmyung Choi, Jaeil Kim, Changhyun Kim, Kyungwhan Kim, Kibong Ku, Seonghwi Song, Yongmi Kim, Donguk Lee, Jaein Lee, Daesuk Kim, Kihun Kwon, Minsik Han, Byeongchan Choi, Hongjung Kim, Sanghyun Ku, Yeonuk Kim, Jongsam Kim, Sanghui Kim, Youngsuk Seo, Seungwook Oh, Dain Im, Haksong Kim, Jonghyuck Choi, Joohwan Cho, Junhyun Chun, Jonghoon Oh

Paper 23.2 Affiliation: SK hynix, Icheon-si, Korea

Subcommittee Chair: Jonathan Chang, TSMC, Hsinchu, Taiwan

CONTEXT AND STATE OF THE ART

- LPDDR5 is a new JEDEC DRAM standard on the basis of discrete components for high-speed mobile and low-power applications.
- It extends the LPDDR4/4X family.
- DDR5 is the successor of DDR4 for increased bandwidth and power efficiency

TECHNICAL HIGHLIGHTS

- **Samsung introduces 7.5Gb/s LPDDR5**
 - 1st-generation 10nm class process LPDDR5 that includes novel schemes which increase the maximum bandwidth such as WCK clocking and non-target ODT (NT-ODT).
 - Reduces power consumption using dynamic voltage frequency scaling (DVFS),
 - Read and write power consumption of LPDDR5 are improved by 21% and 33% compared to LPDDR4X, respectively.
- **SK Hynix introduces a 16Gb 6.4Gb/s/pin DDR5 SDRAM**
 - A DDR5 SDRAM to overcome bandwidth, power and capacity limitations of DDR4.
 - Phase rotator based DLL, write-level training, and RX/TX with the enhanced DFE/FFE.
 - Energy efficiency is improved by more than 30% with 1.1V/1.8V VDD and VPP.

APPLICATIONS AND ECONOMIC IMPACT

- LPDDR5 provides the performance and power efficiency for the next generation 5G communication, on-device artificial intelligence and advanced driver assistance systems (ADAS), as well as for high-resolution displays and for mobile communication devices.

- *DDR5 is intended for server systems, workstations, and desktop PCs.*
- *Replacement of DDR4 and previous standards expected with a large market volume.*

Session 24 Overview: SRAM and Computation-in-Memory

Memory Subcommittee

Session Chair: Shinichiro Shiratake, Toshiba Memory, Yokohama, Japan

Session Co-Chair: Kyu-hyoun Kim, IBM, Yorktown Heights, NY

Subcommittee Chair: Jonathan Chang, TSMC, Hsinchu, Taiwan

Many state-of-the-art systems for machine learning are limited by memory in terms of the energy they require and the performance they can achieve. This session explores how this bottleneck can be overcome by emerging architectures that perform computation inside the memory array. National Tsing Hua University shows the multi-bit input/weight ReRAM as well as SRAM CIM macros. Southeast University shows the new computing architecture, which reduces the number accesses to the memory. On the other hand, SRAM continues to be the critical technology enabler for a wide range of applications from low-power to high-performance computing. This session showcases the leading-edge SRAM developments from the semiconductor industry. TSMC shows the 7nm dual-port SRAM architecture where read-disturb-write issues were mitigated. Samsung shows the dual-rail 7nm SRAM technology, which is tolerant to voltage and temperature variation.

- In Paper 24.1, National Tsing Hua University demonstrates the first ReRAM CIM macro capable of supporting CNN operations using multiple-bit input/weight and multiple-bit MAC output. This device achieved the fastest MAC operations among existing ReRAM-CIM macros ($T_{ac} = 14.6\text{ns}$ at 2b-input-3b-weight with 4b-MACout) and the best measured peak energy efficiency of 53.17 TOPS/W (binary mode).
- In Paper 24.2, TSMC shows the $0.075\mu\text{m}^2$ dual-port SRAM bitcell in a 7nm technology node. It also mitigates the WL-R/C and cross-talk issue in the advanced technology node by process and layout co-optimization. They confirm that the dummy-read-recovery scheme can mitigate read-disturb-write issues in a dual-port SRAM bitcell. Silicon measurement results show $V_{min} < 500\text{mV}$ at FS corner and 2.1GHz operation at SS and -40°C .
- In Paper 24.3, Samsung shows the dual-rail SRAM technology with voltage auto-tracking assist (VATA) and temperature auto-tracking assist (TATA) circuits. VATA and TATA have simpler architectures than others for avoiding additional power and area overhead. Specifically, VATA shows a new concept to cover the dual-rail offset voltage (740mV) to make dynamic and leakage power scaling possible.
- In Paper 24.4, Southeast University shows an energy-efficient in-memory binary-weight network (BWN) architecture with pulse-width modulation. It is the first in-memory BWN processor in which the feature is stored in memory. Its architecture is like a sandwich, memory-computing-memory. More precise analog computing based on pulse-width modulation is presented.
- In Paper 24.5, National Tsing Hua University demonstrates an SRAM-based CIM macro with twin 8T SRAM bitcells. A fabricated 55nm 3840b 8T SRAM-CIM macro achieved a better than 22 \times improvement in FoM (TOPS/W \times GOPS/KB) and the fastest ever multiple-bit MAC operations (5ns for 2b-input, 5b-weight, 5b-MACout).

Session 24 Highlights: SRAM and Computation-In-Memory

[24.1] A 1Mb Multibit ReRAM Computing-In-Memory Macro with 14.6ns Parallel MAC Computing Time for CNN-Based AI Edge Processors

[24.2] A 7nm 2.1GHz Dual-Port SRAM with WL-RC Optimization and Dummy-Read-Recovery Circuitry to Mitigate Read-Disturb-Write Issue

Paper 24.1 Authors: Cheng-Xin Xue, Wei-Hao Chen, Je-Syu Liu, Jia-Fang Li, Wei-Yu Lin, Wei-En Lin, Jing-Hong Wang, Wei-Chen Wei, Tung-Cheng Chang, Ting-Wei Chang, Yen-Cheng Chiu, Chun-Ying Lee, Chung-Chuan Lo, Ya-Chin King, Chong-Jung Lin, Ren-Shuo Liu, Chih-Cheng Hsieh, Kea-Tiong Tang, Meng-Fan Chang

Paper 24.1 Affiliation: National Tsing Hua University, Hsinchu, Taiwan

Paper 24.2 Authors: Hidehiro Fujiwara, Chih-Yu Lin, Hsien-Yu Pan, Cheng-Han Lin, Po-Yi Huang, Kao-Cheng Lin, Jhon-Jhy Liaw, Yen-Huei Chen, Hung-Jen Liao, Jonathan Chang

Paper 24.2 Affiliation: TSMC, Hsinchu, Taiwan

Subcommittee Chair: Jonathan Chang, TSMC, Hsinchu, Taiwan, Memory

CONTEXT AND STATE OF THE ART

- Computation-In-Memory (CIM) improves the energy efficiency of multiplication-and-accumulation (MAC) operations for machine learning hardware
- SRAM continues to be the critical technology enabler for a wide range of applications from low-power to high-performance computing.

TECHNICAL HIGHLIGHTS

- **National Tsing Hua University introduces 1Mb ReRAM-based Computation-In-Memory macro with multiple-bit resolutions (2b-input, 3b-weight and 4b-MACout)**
 - The device achieves the fastest operation latency of 14.6ns among existing ReRAM CIM macros and the best measured peak energy efficiency of 53.17 TOPS/W (binary mode) which is 2.6× improvement in energy-efficiency compared to the previous record.
- **TSMC presents a 7nm 2.1GHz dual-port SRAM with the smallest bitcell of 0.075um²**
 - The chip achieves 2.1GHz operation at less than -40°C or V_{MIN} of 500mV by mitigating read-disturb-write by the novel dummy-read recovery scheme.

APPLICATIONS AND ECONOMIC IMPACT

- Computation-In-Memory with multiple-bit resolution can maximize energy efficiency in ML computation and would allow more complicated problems to be solved by AI hardware.
- Continued SRAM scaling in density, speed and power would enable wide range of SRAM applications from mobile to high-performance computing.

Session 25 Overview: Circuits Enabling Security

Digital Circuit Techniques Subcommittee

Session Chair: Hirofumi Shinohara, Waseda University, Fukuoka, Japan

Session Co-Chair: Dennis Sylvester, University of Michigan, Ann Arbor, MI

Subcommittee Chair: Edith Beigne, Facebook, Menlo Park, CA, Digital Circuits

This session focuses on two important aspects of securing hardware systems: 1) authentication, and 2) attack resistance. The first two papers offer new approaches to physically unclonable functions (PUFs), which provide unique keys for secure authentication of devices. Challenges in this space include achieving very low error rates, providing compact and energy-efficient key generation, and process scalability. These papers employ reconfigurability to ensure more stable key generation and provide gains in native bit error rates and/or energy. The third paper focuses on side-channel-attack resistance: this work leverages desynchronization of the regulator and AES clocks to reduce side-channel information leakage, making attacks significantly more difficult, and less likely to succeed.

- In Paper 25.1, Rice University describes a compact PUF that exploits an analog-biased native NMOS header to provide supply voltage insensitivity. The PUF is also reconfigurable: one can chain together as many stages as needed to ensure stable full rail readout. The design operates across the widest reported temperature range (-55 to 125°C) with very low 0.00182% bit error rate after a new stabilization technique is applied. Total energy efficiency is 15.3fJ/b, and resiliency to aging is demonstrated.
- In Paper 25.2, Tsinghua University, National Tsing Hua University, and Georgia Institute of Technology present a reconfigurable PUF based on a differential resistive RAM (RRAM) structure. The PUF achieves low native bit error rate ($<6\text{E}-6$) and is implemented in $0.13\mu\text{m}$ technology with each bit occupying $2.86\mu\text{m}^2$.
- In Paper 25.3, Georgia Institute of Technology and Intel use a digital low-dropout regulator (LDO) to power 128b AES engines to provide side-channel attack resistance, specifically for power and electromagnetic probe type attacks. Security is further enhanced via injection of random switching noise, as well as pseudo-random clock-edge dithering. Mean-time-to-disclosure of AES keys is increased by 2182 to 3579 \times over a baseline design, with relatively low 10% performance overhead.

Session 25 Highlights: Circuits Enabling Security

[25.2] A Reconfigurable RRAM Physically Unclonable Function Utilizing Post-Process Randomness Source with $<6 \times 10^{-6}$ Native Bit Error Rate

Paper 25.2 Authors: Yachuan Pang¹, Bin Gao¹, Shengyu Yi¹, Qi Liu¹, Wei-Hao Chen², Ting-Wei Chang², Wei-En Lin², Xiaoyu Sun³, Shimeng Yu³, He Qian¹, Meng-Fan Chang², Huaqiang Wu¹

Paper 25.2 Affiliation: ¹Tsinghua University, Beijing, China, ²National Tsing Hua University, Hsinchu, Taiwan, ³Georgia Institute of Technology, Atlanta, GA

Subcommittee Chair: Edith Beigne, Facebook, Menlo Park, CA, Digital Circuits

CONTEXT AND STATE OF THE ART

- Physically unclonable functions (PUFs) provide unique identification for individual chips. They exploit physical sources of randomness and must be highly repeatable and provide uniqueness across chips.
- Common PUF topologies include SRAM cells and configurable delay chains. A key challenge is providing repeatable readout across process/voltage/temperature/aging, with low energy and compact area.

TECHNICAL HIGHLIGHTS

- **Tsinghua University presents a reconfigurable resistive RAM (RRAM)-based physically unclonable function (PUF), demonstrating extremely low intrinsic bit error rate.**
 - In Paper 25.2, Tsinghua University, National Tsing Hua University, and Georgia Institute of Technology present a reconfigurable PUF based on a differential resistive RAM (RRAM) structure. The PUF achieves low native bit error rate ($<6E-6$) and is implemented in a $0.13\mu\text{m}$ technology with each bit consuming $2.86\mu\text{m}^2$.

APPLICATIONS AND ECONOMIC IMPACT

- With the increasing pervasiveness of IoT devices, data and IP security has become an important issue. Hardware encryption for secure data transfer and IP supply-chain protection is essential to prevent economic loss from individual identity theft, as well as attacks on infrastructure.

Session 26 Overview: Frequency Generation and Interference Mitigation

RF Subcommittee

Session Chair: Ramesh Harjani, University of Minnesota, MN

Session Co-Chair: Andrea Mazzanti, Università di Pavia, Italy

Subcommittee Chair: Piet Wambacq, imec, Belgium, RF

This session covers the latest advancements in frequency synthesis for radars, frequency sources, and RX techniques for interference mitigation. The first presentation in the session demonstrates an ultra-wide-band chirping FMCW modulator with a 16GHz synthesizer in 28nm CMOS. The next two presentations cover recent innovations in millimeter-wave CMOS frequency sources for 5G, achieving low phase noise and wide tuning range and exploiting multi-resonance LC tanks. The fourth paper demonstrates strong interference rejection by introducing envelope-based dynamic biasing in a 2.4GHz CMOS receiver. The last paper in the session proposes a low-noise oscillator for IoT operating down to 0.1V supply.

In Paper 26.1, imec and Sony Semiconductors present a 16GHz FMCW radar modulator in 28nm CMOS. The modulator is based on a dividerless DTC subsampling PLL architecture and reaches a 30 μ s sawtooth chirping speed with a 1.5GHz chirping bandwidth. The rms frequency error is below 103kHz, which is less than 0.007% of the chirp bandwidth.

In Paper 26.2, the University of Macau and Instituto Superior Tecnico of the University of Lisboa propose a 25.5-to-29.9GHz VCO based on an RLMC tank with resonances at 1st, 2nd, and 3rd harmonics and tunable with only common-mode capacitors. The VCO, in 65nm CMOS, achieves up to 191.6dBc/Hz FoM@1MHz and demonstrates 1/ f^3 phase noise corner between 130kHz and 230kHz.

In Paper 26.3, the Indian Institute of Technology, Madras, shows a wide-tuning-range millimeter-wave quadrature VCO exploiting a dual-mode resonator realized with 4-port coupled inductors. The VCO, in 65nm CMOS, is tunable from 25 to 38GHz with 17.5-to-21.6mW power dissipation from a 0.65V supply. The phase noise at 3MHz offset ranges from -121 to -112dBc/Hz, corresponding to a 181-to-187 dBc/Hz figure of merit.

In Paper 26.4, Fudan University and the University of Seattle present a 2.4GHz mixer-first receiver for IoT applications where the interference resilience is improved through an inverter-based LNA exploiting dynamic input biasing generated from the input envelope. With 2.05mA current consumption, the 65nm CMOS receiver achieves 66dB in-band interference tolerance and -83dBm sensitivity with 307kb/s OOK modulation.

In Paper 26.5, the University of California, San Diego, proposes an LC DCO based on a folded, transformer-based, circuit topology to improve phase noise performance at low supply voltages. Implemented in 22nm FDSOI, the circuit oscillates from 4.2 to 5GHz with a peak FoM of 197dBc/Hz, -142.1dBc/Hz PN at 10MHz, 40MHz/V pushing from a 0.15V supply. The oscillator can operate down to 0.1V V_{dd} .

Session 26 Highlights: Frequency Generation and Interference Mitigation

[26.1] A Self-Calibrated 16GHz Subsampling-PLL-Based 30 μ s Fast Chirp FMCW Modulator with 1.5GHz Bandwidth and 100kHz rms Error

Paper 26.1 Authors: Qixian Shi(1), Keigo Bunsen(2), Nereo Markulic(1), and Jan Craninckx(1)

Paper 26.1 Affiliation: imec Heverlee Belgium(1), Sony Semiconductor Solutions, Atsugi, Japan(2)

Subcommittee Chair: Piet Wambacq, imec, Leuven, Belgium, RF

CONTEXT AND STATE OF THE ART

- FMCW radars are increasingly important for autonomous driving
- Multiple-GHz chirping bandwidth combined are low jitter and critical for fine range resolution.

TECHNICAL HIGHLIGHTS

- **A 16GHz chirping FMCW modulator for radar applications**
 - The modulator is based on a dividerless DTC subsampling PLL architecture and reaches a 30 μ s sawtooth chirping speed with a 1.5GHz chirping bandwidth. The rms frequency error is below 103kHz, which is less than 0.007% of the chirp bandwidth.

APPLICATIONS AND ECONOMIC IMPACT

- Autonomous driving is rapidly developing and becoming more and more common place
- FMCW radars are critical components for autonomous driving

Session 27 Overview: Energy Harvesting & DC/DC Control Techniques

Power Management Subcommittee

Session Chair: Yuan Gao, IME A*STAR, Singapore

Session Co-Chair: Chan-Hong Chern, TSMC, Taiwan

Subcommittee Chair: Yogesh Ramadass, Texas Instruments, Santa Clara, CA, Power Management

The first four papers in this session focus on energy harvesting. New circuit techniques to enhance power-conversion efficiency, reduce circuit self-startup voltage and achieve adaptive circuit control for a wide range of inputs are presented. The next four papers present control techniques for envelope tracking modulator, DC-DC converter, and battery charger to improve efficiency, speed up settling and load transient response times, improve charging accuracy and charging time, etc.

- In Paper 27.1, Fudan University presents a bipolar-input boost/flyback hybrid converter for thermoelectric energy harvesting. Implemented in $0.18\mu\text{m}$ CMOS, the circuit achieves maximum end-to-end power conversion efficiency of 84% and 79% when $V_{\text{TEG}}=260\text{mV}$ and $V_{\text{TEG}}=-300\text{mV}$, respectively.
- In Paper 27.2, the University of Michigan presents a Sense-and-Set rectifier that performs maximum-power-point-tracking for piezoelectric energy harvester and adapts to different excitation types and levels. The circuit is implemented in $0.18\mu\text{m}$ CMOS with 0.47mm^2 core area and achieved $5.41\times$ and $4.59\times$ power extraction improvement for periodic and shock excitations, compared to an ideal FBR.
- In Paper 27.3, the University of Macau presents a Split-Phase Flipping-Capacitor Rectifier that uses 4 flying capacitors to achieve 21-phase operations and the capacitors are further reused to construct a multi-VCR buck/boost/unity SC DC-DC. Fabricated in $0.18\mu\text{m}$ CMOS, the chip demonstrates a $9.3\times$ improvement on energy extraction compared with a conventional full-bridge rectifier interface.
- In Paper 27.4, Pennsylvania State University presents a self-starting reconfigurable energy harvesting circuit that adaptively operates in voltage and SECE-modes for a custom inertial harvester with multiple flexible beams. Implemented in $0.35\mu\text{m}$ CMOS, the chip can improve harvested energy by 511% compared with a full-wave active rectifier.
- In Paper 27.5, Arizona State University presents an envelope tracking modulator using a hysteresis-control method for 3-level regulator. Fabricated in a 65nm CMOS process with an active area of $1.7\text{mm}\times 1.6\text{mm}$, the chip has $3.2\times$ higher switching frequency than previous PWM-controlled 3-level switching regulators in envelope tracking applications and achieves 91% efficiency for LTE-80MHz BW, ACLR of -32.5dBc at 24dBm P_{out} and 8% PAE improvement at 4dB back-off.
- In Paper 27.6, National Cheng-Kung University proposes background capacitor-current-sensor (CCS) calibration and ADC-calibrated CCS techniques for a buck converter to precisely accelerate load-transient response. Fabricated in a $0.18\mu\text{m}$ CMOS process with an active area of 1.8mm^2 , this chip has the smallest undershoot/overshoot voltage with $2.2\times$ faster settling speed and achieves $6\times$ faster calibration compared with other state of the art.
- In Paper 27.7, Seoul National University proposes a digital adaptive on-time (DAOT) buck voltage regulator using ripple-injection schemes. Fabricated in a 28nm CMOS process with an active area of 0.39mm^2 , this 4-phase voltage regulator achieves stable and fast output regulation under fixed switching frequency and phase synchronization of multiphase operations and exhibits 80mV droop with a recovery time of 80ns under a $1\text{A}/10\text{ns}$ load step up.
- In Paper 27.8, National Chiao-Tung University proposes a buck-boost battery charger using dynamic charging-current scaling (DCCS) techniques to scale the charging current according to the temperature with dual accurate current control (ACC) and temperature-assisted loop (TAL). Fabricated in a $0.18\mu\text{m}$ BCD process with an active area of 3.3mm^2 , the proposed ACC and TAL techniques along with Build-In Resistance-Detection and Adaptive Thermal-Loss-Calibration (ALTC) techniques achieve higher accuracy on charging current up to 99.6% and reducing charging time by 38.6%.

Session 27 Highlights: Energy Harvesting & DC/DC Control Techniques

[27.2] An Adiabatic Sense and Set Rectifier for Improved Maximum-Power-Point Tracking in Piezoelectric Harvesting with 541% Energy Extraction Gain

Paper Authors: Y. Peng, D.K. Choo, S. Oh, I. Lee, T. Jang, Y. Kim, J. Kim, D. Sylvester, D. Blaauw

Paper Affiliation: University of Michigan, Ann Arbor, MI

CONTEXT AND STATE OF THE ART

- *Piezoelectric energy harvesting efficiency is sensitive to the impedance matching between the transducer and the interface circuit. Maximum-power-point tracking is essential to regulate the transducer output voltage dynamically to maintain the harvesting efficiency at different vibration strength.*

TECHNICAL HIGHLIGHTS

- **Piezoelectric energy-harvesting circuit performs maximum-power-point tracking**
 - *The energy harvesting circuit tracks the maximum power point of piezoelectric transducers in the presence of periodic and shock vibrations and achieves 5.41× and 4.59× power extraction improvement for periodic and shock excitations, compared to an ideal FBR.*

APPLICATIONS AND ECONOMIC IMPACT

- *Harvesting from vibration is one of the most promising energy-harvesting solutions. Increased efficiencies for periodic and shock excitations at different vibration levels are the key to enabling energy-autonomous tiny IoT nodes.*

[27.6] Background Capacitor-Current-Sensor Calibration of DC-DC Buck Converter with DVS for Accurately Accelerating Load-Transient Response

Paper Authors: T. Kuo, Y. Huang, P. Wang

Paper Affiliation: National Cheng Kung University, Tainan, Taiwan

Subcommittee Chair: Yogesh Ramadass, Texas Instruments, Santa Clara, CA, Power Management Subcommittee

CONTEXT AND STATE OF THE ART

- *A power regulator to support Dynamic Voltage Scaling (DVS) and to provide a stable voltage under abrupt load change is necessary for a high performance system. However, the performance would be degraded due to aging or temperature drift of the output capacitor. To resolve this issue, the regulator has to operate adaptively according to output capacitance variation.*

TECHNICAL HIGHLIGHTS

- **Capacitor current-sense calibration for fast load transient response of DC-DC converters**
 - *In paper 27.6, NCKU presents the first background capacitor-current-sensor calibration in a buck converter to precisely accelerate load-transient. The background calibration could achieve the smallest undershoot/overshoot even when it's under arbitrary load transient and DVS.*

APPLICATIONS AND ECONOMIC IMPACT

- *A system could operate reliably and better performance could be achieved thanks to the background capacitor-current sensing calibration.*

Session 28 Overview: Techniques for Low-Power & High-Performance Wireless

Wireless Subcommittee

Session Chair: Danielle Griffith, Texas Instruments, Dallas, TX

Session Co-Chair: Alan Wong, EnSilica, UK

Subcommittee Chair: Stefano Pellerano, Intel, Hillsboro, OR, Wireless

Wireless technologies continue to penetrate and support a wide range of application areas. This session includes state-of-the-art improvements in wake-up radios enabling ultra-low-power and increased blocker rejection, a highly efficient Bluetooth Low Energy transmitter, and a wireless power transfer system supporting enhanced data rates. Furthermore techniques to boost wireless performance are presented, including non-magnetic circulators for improved full-duplex communications at mm-wave and RF frequencies, a wideband blocker-tolerant receiver with low LO leakage and a modified Cartesian feedback transmitter that addresses the noise-linearity trade-off of the conventional architecture.

- In Paper 28.1, Columbia University describes a wake-up receiver in 65nm CMOS LP using a 40-stage MOS RF envelope detector and time-domain windowed integrator. The receiver has $-78.3/-79.1$ dBm sensitivity at 151.25/434.4 MHz with 110ms latency, while consuming 370/420 pW from 0.4V.
- In Paper 28.2, the University of California, San Diego describes a BLE-compliant wake-up receiver in 65nm CMOS using single-die 3-channel FBAR-based filtering and a frequency-hopping time-counting majority-voting algorithm providing 4D signature detection. The receiver achieves -85 dBm sensitivity and up to 60 dB blocker rejection while consuming 220 μ W.
- In Paper 28.3, the University of Michigan describes a Bluetooth Low Energy transmitter in 65nm CMOS using a co-designed 3.5×3.5 mm² loop planar antenna and transformer-boost power oscillator for improving output power and transmit efficiency. The transmitter achieves 23.6% overall efficiency with a measured phase noise of -118.5 dBc/Hz at 1 MHz offset, resulting in 2.1% FSK error and <10 kHz frequency drift during BLE packet.
- In Paper 28.4, the University of Southampton describes a 10 kHz-to-2 MHz combined antenna tuner/driver and modulator for high-Q inductively-coupled systems in 0.18μ m CMOS/LDMOS using adaptive-predictive phase-continuous switching fractional-capacitance tuning. The technique enables FSK/PSK modulation beyond normal Q-factor/bandwidth restrictions, achieving 296 kb/s QPSK at 2 MHz with $Q = 50$.
- In Paper 28.5, Columbia University describes a non-magnetic CMOS 60 GHz circulator based on spatio-temporal (ST) modulation across a loss/dispersion-engineered bandpass filter. The circulator achieves 3.6/3.1 dB loss, isolation >40 dB over 1.3 GHz, 3.2 dB NF, $>+19.5$ dBm IP_{1dB} and spurs <-30 dBc.
- In Paper 28.6, Columbia University and Oregon State University describe a 2×2 MIMO full-duplex receiver with integrated N-path-filter-based non-magnetic circulators. The solution features area and power-efficient passive RF and baseband active wideband MIMO cancellation with shared delay elements to address the $O(N^2)$ challenge while enhancing TX power handling by 8 dB.
- In Paper 28.7, the University of California Irvine describes a CMOS wideband blocker-tolerant receiver realizing high-Q RF-input selectivity for linearity improvement while maintaining a low LO leakage. It achieves a noise figure of 2.45 dB, out-of-band $IIP3/IIP2$ are $+14/+60$ dBm respectively and LO leakage is below -80 dBm from 0.2 to 2 GHz.
- In Paper 28.8, the University of California Davis describes an X-band Cartesian error-feedback transmitter with fully integrated PA in 65nm bulk CMOS. The chip achieves 21.4 dBm P_{sat} with 22.3% system efficiency and 21 dBm OP_{1dB} with 20.3% system efficiency.

Session 28 Highlights: Techniques for Low-Power and High-Performance Wireless

[28.1] A 0.42nW 434MHz -79.1dBm Wake-Up Receiver with a Time-Domain Integrator

Paper 28.1 Authors: Vivek Mangal, Peter R. Kinget

Paper 28.1 Affiliation: Columbia University, New York, NY

Subcommittee Chair: Stefano Pellerano, Intel, Hillsboro, OR, Wireless

CONTEXT AND STATE OF THE ART

- Battery-powered wireless sensor nodes with aggressively duty-cycled operation need an ultra-low-power technique to synchronize data transmission between nodes.
- Current state of the art for wake-up radios is 4.5nW with -64dBm sensitivity and >50ms latency.

TECHNICAL HIGHLIGHTS

- **A 420pW, -79.1dBm sensitivity wake-up receiver achieves 110ms latency and 10× lower power consumption compared to state of the art.**
 - In Paper 9.1, Columbia University describes a wake-up receiver in 65nm CMOS LP using a 40-stage MOS RF envelope detector and time-domain windowed integrator. The receiver has a -78.3/-79.1dBm sensitivity at 151.25/434.4MHz with a 110ms latency, while consuming 370/420pW from 0.4V.

APPLICATIONS AND ECONOMIC IMPACT

- This wake-up radio is targeted for any event-driven wireless sensor node application, such as warehouse inventory, smart homes or integrated patient monitoring, where long battery life or battery-free operation is required.
- Reducing the power of such radios below 1nW can eliminate battery replacement and enable energy harvesting systems.

Session 29 Overview: Quantum & Photonics Technologies

Technology Directions Subcommittee

Session Chair: Edoardo Charbon, EPFL, Lausanne, Switzerland

Session Co-Chair: Pui-In Mak, University of Macau, China

Subcommittee Chair: Makoto Nagata, Kobe University, Kobe, Japan

Quantum and photonics technologies are emerging as a major research topic touching several disciplines, including computing, sensing, telecommunications, information technology, security, etc. This session describes important developments in the field and its applications.

- In Paper 29.1, the University of Massachusetts at Amherst, Google, and the University of California at Santa Barbara describe a chip designed to control superconductive qubits by means of 4-to-8GHz signal patterns operating at deep-cryogenic temperatures (3K). The 28nm cryo-CMOS chip generates up to sixteen -10dBm waveforms to perform several operations on qubits, dissipating 2mW per qubit.
- In Paper 29.2, the Massachusetts Institute of Technology proposes an integrated system for the control and readout of a nitrogen vacancy (NV) center in diamond. The approach is based on a hybrid NV-CMOS scalable platform enabling spin control and optical readout featuring MW generation, uniform radiation, and detection.
- In Paper 29.3, Nagoya University proposes an 8×8b superconductor single-flux-quantum logic multiplier integrated in a 1.0μm, 9-layer process featuring 20,251 Josephson junctions. The multiplier operates at 4.2K and reaches a frequency of 48GHz while dissipating 5.6mW.
- In Paper 29.4, the Tokyo Institute of Technology presents a miniaturized atomic clock system based on a cesium-133 gas cell. The system features a vertical-cavity surface-emitting laser (VCSEL), temperature/magnetic controllers, and control circuits; it achieves a long-term Allan deviation of 2.2×10^{-12} at $\tau=105s$ within a volume of 15.4cm³ dissipating 59.9mW.
- In Paper 29.5, the University of California at Berkeley presents an optical phased array implemented in a 3D platform, where photonics and CMOS, independently optimized, are oxide-bonded and connected through high-density vias. With 18.5°/16° steering range and 0.15°/0.6° beamwidth, the system achieves an effective antenna aperture of 500μm×130μm resulting in a lateral resolution of 0.26m×1m at 100m.
- In Paper 29.6, National Chiao Tung University proposes a digital-type GaN driver for sub-nanosecond laser pulses to be used in a LiDAR featuring a resolution of 0.3m and dynamic range higher than 0.75m. The driver achieves a wide range of repetition frequencies up to 200MHz, adjusting the laser current rise and fall times to within hundreds of picoseconds and a pulse width of 0.9ns.
- In Paper 29.7, the University of Edinburgh presents a Visible Light Communication receiver fabricated in 0.13μm CMOS technology. Based on a 64×64 SPAD array with 43% fill factor, the receiver achieves a data rate of 500Mb/s 4-PAM with a sensitivity of -46.1dBm and a 2×10^{-3} BER in a 450nm laser diode free-space link at 1m and 1klux background illumination.
- In Paper 29.8, the Massachusetts Institute of Technology describes a new technique, SHARC (Self-Healing Analog with RRAM and Carbon nanotube), making carbon-nanotube field-effect transistor (CNFET) analog circuits robust to metallic carbon nanotubes (CNTs). The demonstrated circuits in a 3μm technology node include a 4b ADC (2-stage op-amp and switches) and a 4b-SAR ADC (strong-arm latch and switches).

Session 29 Highlights: Quantum & Photonics Technologies

[29.1] A 28nm Bulk-CMOS 4-to-8GHz <2mW Cryogenic Pulse Modulator for Scalable Quantum Computing

Paper 29.1 Authors: Joseph C Bardin^{1,2}, Evan Jeffrey², Erik Lucero², Trent Huang², Ofer Naaman², Rami Barends², Ted White², Marissa Giustina², Daniel Sank², Pedram Roushan², Kunal Arya², Benjamin Chiaro³, Julian Kelly², Jimmy Chen², Brian Burkett², Yu Chen², Andrew Dunsworth³, Austin Fowler², Brooks Foxen³, Craig Gidney², Rob Graff², Paul Klimov², Josh Mutus², Matthew Mcewen³, Anthony Megrant², Matthew Neeley², Charles Neill², Chris Quintana², Amit Vainsencher², Hartmut Neven⁴, John Martinis^{2,3}

Paper 29.1 Affiliations: ¹University of Massachusetts at Amherst, MA, ²Google, Goleta, CA, ³University of California, Santa Barbara, CA, ⁴Google, Los Angeles, CA

Subcommittee Chair: Makoto Nagata, Kobe University, Kobe, Japan, Technology Directions

CONTEXT AND STATE OF THE ART

- Current quantum processors are made of small arrays of quantum bits (qubits) cooled at deep-cryogenic temperatures of a few milli-Kelvins. Qubits are controlled by means of complex room-temperature instrumentation through long interconnect that needs to go through several stages of refrigeration.
- The approach is not suitable for large arrays of qubits that will be required in the future to achieve practical quantum computers, due to the complexity and size of the control apparatus.

TECHNICAL HIGHLIGHTS

- **Cryogenic Low-Power Pulse Modulator for Scalable Quantum Computing**
 - The University of Massachusetts at Amherst describes a chip designed to control superconductive transmon qubits by means of 4-to-8GHz signal patterns operating at deep-cryogenic temperatures (3K). The 28nm cryo-CMOS chip generates up to sixteen -10dBm waveforms to perform several operations on qubits, dissipating 2mW per qubit.

APPLICATIONS AND ECONOMIC IMPACT

- The proposed system is used for the control of transmon qubits, the core of a quantum computer. The system has been conceived in a scalable fashion for large numbers of qubits. Quantum computers hold the promise to solve problems that are intractable in today's most powerful supercomputers.

Session 30 Overview: Advanced Wireline Techniques

WLN Subcommittee

Session Chair: Yohan Frans, Xilinx, San Jose

Session Co-Chair: Friedel Gerfers, Technische Universität Berlin

Subcommittee Chair: Frank O'Mahony, Intel, Hillsboro, OR, WLN

As wireline transceivers become widely adopted in more systems and applications, challenges such as signaling over channels with high-loss/high-reflection and limited link power budget continue to arise. Since these challenges cannot be addressed by process technology advances alone, new design innovations at circuit level as well as link/system level continue to be critical.

This session starts with an invited paper describing the need and challenges of deploying high-speed links for automotive application. The next four papers propose new ideas on link modulation, architecture, coding, and adaption: a 56Gb/s link using discrete multi-tone (DMT) modulation, a ring topology uplink/downlink interface for large-capacity storage systems using cascaded CDRs, a sequence-coded PAM-4 link using a reduced-state trellis, and the use of a genetic algorithm to perform link adaptation. The last three papers in the session highlight innovations at building-block levels: a highly linear silicon photonic driver, a low-power multi-phase clock generator using injection-locked oscillator, a high-performance PLL that operates at 0.65V, and a low-power ring-oscillator-based injection-locked clock multiplier.

- In Paper 30.1, NXP Semiconductors describes emerging automotive Ethernet network standards and solutions enabling future driver-assistance as well as autonomous-driving technologies. Weight-space-cost constraints lead to a new class of high-bandwidth full-duplex interfaces operating over 15m single twisted-pair cabling meeting the stringent automotive requirements in terms of emissions, robustness, reliability, and fail safety.
- In Paper 30.2, École Polytechnique Fédérale de Lausanne demonstrates a 56Gb/s wireline RX employing discrete multi-tone (DMT) modulation that subdivides a data stream into multiples of frequency-domain sub-channels. The RX is implemented in 14nm FinFET technology and achieves an energy efficiency of 2.9pJ/b (1.2pJ/b for the DSP).
- In Paper 30.3, Toshiba Memory Corporation presents an uplink-downlink interface for large-capacity storage systems employing four-channel multiplexing. The interface utilizes 25.6Gb/s PAM-4 signaling with cascaded CDRs in a ring topology, where each TX uses the RX recovered clock. Fabricated in 28nm CMOS technology, it achieves 3.69pJ/b at 25.6Gb/s with a BER 10^{-15} over a channel loss of 1.84dB.
- In Paper 30.4, the University of Alberta describes a 32Gb/s sequence-coded PAM4 transceiver using a self-converging, reduced-state trellis structure. Compared to conventional PAM-4, it provides up to 6dB SNR gain for a 30dB loss channel with 12.5% bandwidth overhead. The prototype, implemented in 28nm FDSOI technology, consumes 2.9pJ/bit at 32Gb/s over a channel loss of 30dB.
- In Paper 30.5, Huawei Technologies presents a 56.25Gb/s analog-mixed signal PAM-4 receiver in 7nm CMOS that employs a genetic algorithm to perform adaptation of its analog front-end frequency response. The RX achieves an energy efficiency of 1.41pJ/b over a channel loss of 22.3dB without a DFE.
- In Paper 30.6, the University of British Columbia presents a 130nm SiGe driver using resistor-based capacitor splitting, zero-peaking as well as source degeneration to obtain 40GHz of bandwidth. The proposed silicon photonic modulator driver achieves a signal swing of $6V_{ppd}$ and a THD of 3.6%.
- In Paper 30.7, MediaTek describes an 8b injection-locked phase rotator that provides multiphase outputs with a peak-to-peak INL of 1.14LSB without the need of a multiphase input clock. The silicon area and power consumption are 0.0043mm² and 11.4mW, respectively.
- In Paper 30.8, the Hong Kong University of Science and Technology presents a 0.65V sub-sampling PLL that uses a hybrid dual-path structure. Fabricated in a 40nm CMOS process, the PLL achieves a frequency range from 12 to 16GHz with 56.4fs_{rms} jitter at 14GHz output, resulting in a FoM of -256.4dB.

- *In Paper 30.9, the Ulsan National Institute of Science and Technology describes an ultra-low reference spur and low-jitter ring-VCO-based injection-locked clock multiplier. Dissipating only 11mW, the measured reference spur level and jitter are -72dBc and 140fs_{rms}, respectively.*

Session 30 Highlights: Advanced Wireline Techniques

[30.2] A 161mW 56Gb/s ADC-Based Discrete Multitone Wireline Receiver Data-Path in 14nm FinFET

Paper 30.2 Authors: Gain Kim^{1,2}, Lukas Kull², Danny Luu^{2,3}, Matthias Braendli², Christian Menolfi², Pier-Andrea Francese², Hazar Yueksel⁴, Cosimo Aprile^{1,2}, Thomas Morf², Marcel Kossel², Alessandro Cevrero², Ilter Ozkaya^{1,2}, Andreas Burg¹, Thomas Toiff², Yusuf Leblebici¹

Paper 30.2 Affiliation: ¹EPFL, Lausanne, Switzerland, ²IBM Zurich Research Laboratory, Rueschlikon, Switzerland, ³ETH Zürich, Zurich, Switzerland, ⁴IBM T. J. Watson Research Center, Yorktown Heights, NY

Subcommittee Chair: Frank O'Mahony, Intel, Hillsboro, OR, WLN

CONTEXT AND STATE OF THE ART

- *The increasing bandwidth demand in data centers and communication infrastructure has driven the need for wireline transceivers operating at 56Gb/s and beyond.*
- *Recent works have demonstrated >56Gb/s PAM4 ADC/DSP-based receivers (RX) that perform well over a legacy channel. However, their power consumption remains relatively high due to heavy arithmetic operations in the DSP. In order to reduce power consumption and to extend signaling rate beyond 56Gb/s, new modulation techniques are currently being explored.*

TECHNICAL HIGHLIGHTS

- **A 56Gb/s receiver using discrete multi-tone modulation technique is implemented in 14nm FinFET.**
 - *In Paper 30.2, École Polytechnique Fédérale de Lausanne demonstrates a 56Gb/s wireline RX data-path employing a discrete multi-tone (DMT) modulation that subdivides a data stream into multiples of frequency-domain sub-channels. The RX is implemented in 14nm FinFET technology and achieves an energy efficiency of 2.9pJ/b (1.2pJ/b for the DSP).*

APPLICATIONS AND ECONOMIC IMPACT

- *Power delivery to networking devices and the associated cooling systems contribute significantly to the overall operational cost of data centers and telecommunication infrastructures.*
- *As a major part of a network device, transceiver power efficiency directly contributes to this cost. The paper demonstrates the feasibility of discrete multi-tone (DMT) modulation at 56Gb/s over a 28dB loss channel with excellent power efficiency, providing a potential alternative for sustaining bandwidth scaling in data-centers and telecommunication infrastructures.*



ISSCC 2019
TRENDS

Conditions of Publication

PREAMBLE

The Trends to follow serve to capture the context, highlights, and potential impact, of the papers to be presented in each Session at ISSCC 2019 in February in San Francisco

OBTAINING COPYRIGHT to ISSCC press material is EASY!

You may quote the Subcommittee Chair as the author of the text if authorship is required.

You are welcome to use this material, copyright- and royalty-free, with the following understanding:

- *That you will maintain at least one reference to ISSCC 2019 in the body of your text, ideally retaining the date and location. For detail, see the FOOTNOTE below.*
- *That you will provide a courtesy PDF of your excerpted press piece and particulars of its placement to press_relations@isscc.net*

FOOTNOTE

- *From ISSCC's point of view, the phraseology included in the box below captures what we at ISSCC would like your readership to know about this, the 66th appearance of ISSCC, on February 17th to February 21st, 2019, in San Francisco.*

*This and other related topics will be discussed at length at ISSCC 2019, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 17 - February 21, 2019,
at the San Francisco Marriott Marquis Hotel.*

ISSCC Press Kit Disclaimer

The material presented here is preliminary.

As of November 6, 2018, there is not enough information to guarantee its correctness.

Thus, it must be used with some caution.

HISTORICAL TRENDS IN TECHNICAL THEMES

ANALOG SYSTEMS

ANALOG SUBCOMMITTEE

POWER MANAGEMENT SUBCOMMITTEE

DATA CONVERTERS SUBCOMMITTEE

Analog – 2019 Trends

Subcommittee Chair: Kofi A. A. Makinwa, Delft University of Technology, Delft, The Netherlands

New approaches are emerging for traditional circuits such as sensors, crystal oscillators, and voltage references. In the case of integrated temperature sensors, Figure 1 reveals how the energy efficiency of resistor-based temperature sensors has rapidly improved over the last decade, and now exceeds that of traditional bipolar-based temperature sensors. In addition, their accuracy is now comparable to that of their bipolar counterparts across a wide range of temperatures. For crystal oscillators, near optimal start-up schemes have been devised that allow sensor systems to be efficiently duty-cycled for higher energy efficiencies. By using precise frequency injection through a PLL-tuned RC oscillator, a crystal oscillator with the fastest reported startup time is demonstrated. In addition, the traditional approach of using a sustaining amplifier operating at the crystal oscillator frequency has been replaced with a method based on I/Q modulation principles that allows amplification to be done near DC in order to reduce power consumption, resulting in the lowest power crystal oscillator reported to-date at ISSCC as demonstrated in Figure 2.

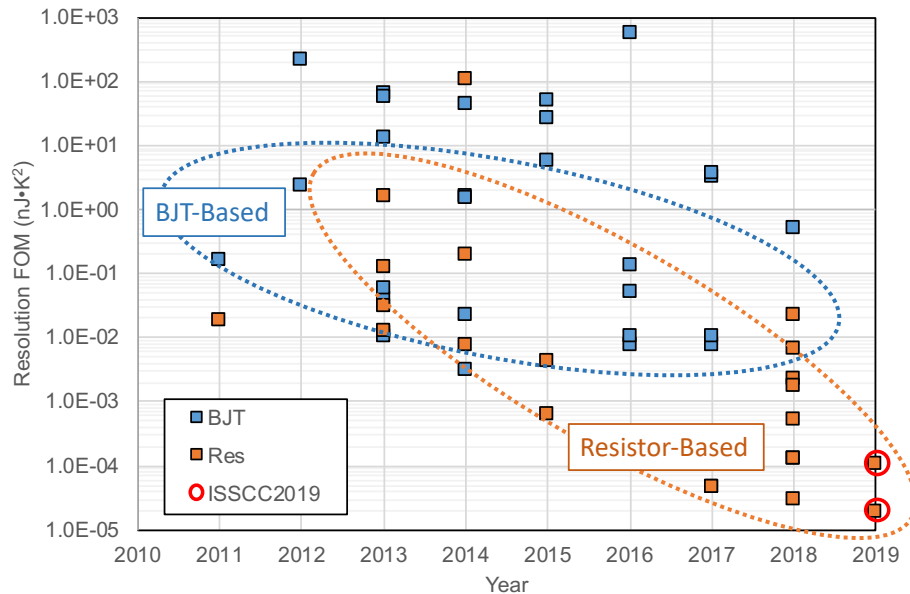


Figure 1 – Trends in the Energy Efficiency of Integrated Temperature Sensors: Resolution FoM versus Time



Figure 2 – Trends in Recent Low Power Fast Startup Crystal Oscillators versus Time

Power Management – 2019 Trends

Subcommittee Chair: Yogesh Ramadass, Texas Instruments, Santa Clara, CA

The efficient control, storage, and distribution of energy are worldwide challenges, and are increasingly important areas of analog circuit research. While the manipulation and storage of information is efficiently performed digitally, the conversion and storage of energy is fundamentally performed with analog systems. Therefore, the key technologies for power management are predominantly analog. For example, there is much interest in wireless power transmission for battery charging applications, ranging from mobile handsets to medical implants: increased performance in wireless power transmission is enabling more efficient power delivery over longer distances. There is also an explosion of technologies that allow energy to be collected from the environment via photovoltaic, piezoelectric, or thermoelectric transducers, with a trend toward the use of multiple sources at the same time. A significant focus here is on analog circuits that are able to harvest sub-microwatt power levels from multiple energy sources at tens of millivolts, to provide autonomy for IoT devices, or to supplement conventional battery supplies in portable devices. To achieve this, the attendant analog circuits have to consume extremely low power, so that some energy is left over to charge a battery or super-capacitor. This trend is captured by movement towards the top-left in the plot shown in Figure 3.

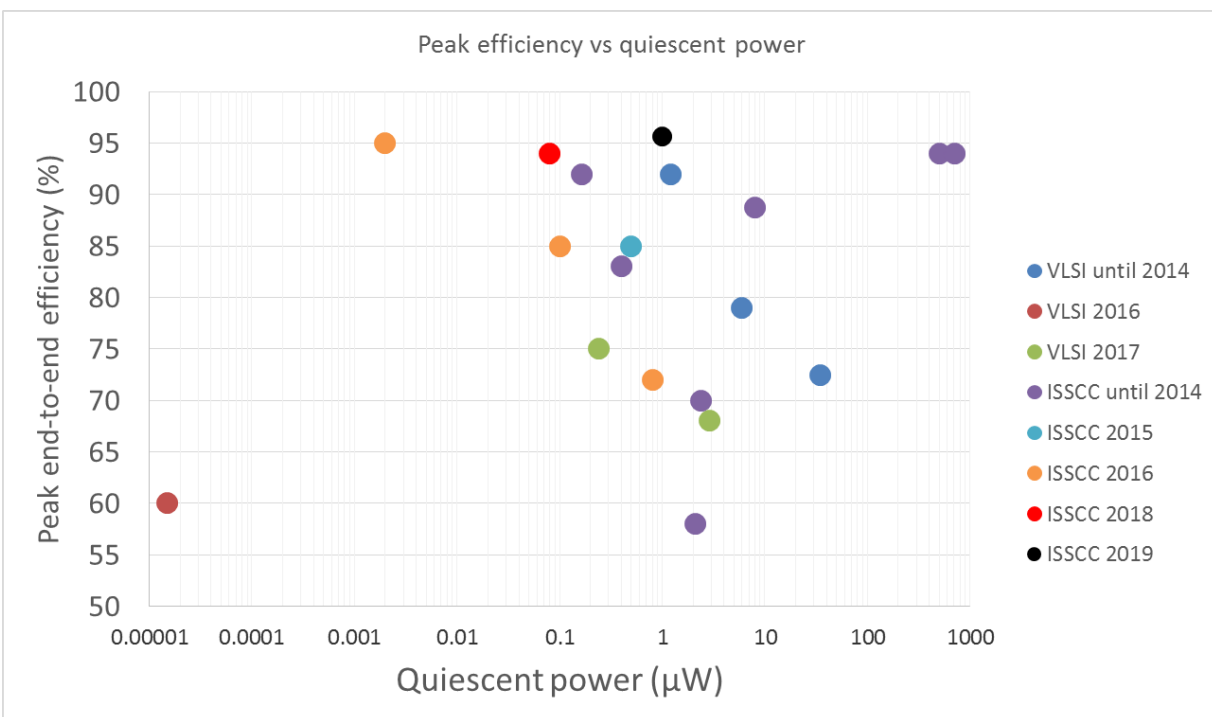


Figure 3 – Comparison of Integrated Energy Harvesting Systems showing End-to-End Efficiency vs Quiescent Power

IC design related to power management is also growing in very different application fields:

- Hybrid converters are becoming more popular and bringing interesting benefits in terms of performance and compactness to DC-DC conversion, due to their ability to relax the requirements of the magnetic components.
- Fully-integrated power converters improve their power density and power efficiency trade-off with the help of hybrid topologies and advanced technology nodes. These allow the push for higher-switching frequencies and enable the use of air-core inductors.
- EMI is a very concerning topic among IC designers for power management, which is being addressed at different levels from gate-drivers up to very effective methods to apply spread-spectrum techniques not only to DC-DC converters but also to high-voltage isolators.

Data Converters – 2019 Trends

Subcommittee Chair: Michael Flynn, University of Michigan, Ann Arbor MI

Data converters form the key link between the analog physical world and the world of digital computing and signal processing prevalent in modern electronics. The need to faithfully preserve the signal across domains continues to pressure data converters to deliver more bandwidth and linearity while continuing to increase power efficiency. This year's ISSCC continues the trend of highly energy-efficient analog-to-digital converters (ADCs) with a combination of successive-approximation-register (SAR), ring-amplifier (RAMP) and noise-shaping based designs.

The three figures below represent traditional metrics to capture innovative progress in ADCs. The first figure plots power dissipated relative to the Nyquist sampling rate (P/f_{nyq}), as a function of signal-to-noise and distortion ratio (SNDR), to give a measure of ADC power efficiency. Note that a lower P/f_{nyq} metric represents a more efficient circuit on this chart. For low-to-medium-resolution converters, energy is primarily expended to quantize the signal; thus the overall efficiency of this operation is typically measured by the energy consumed per conversion and quantization step. The dashed trend-line represents a benchmark of 2fJ/conversion-step. Circuit noise becomes more significant with higher-resolution converters, necessitating a different benchmark proportional to the square of signal-to-noise ratio, represented by the solid line. Designs published from 2009 to 2018 are shown in circles. ISSCC 2019 designs are shown in black dots, continue moving towards the lower right of the figure.

The second figure plots signal fidelity vs. the Nyquist sampling rate normalized to power consumption. At low sampling rates, converters tend to be limited by thermal noise, independent of the sample rate. Higher speeds of operation present additional challenges in maintaining accuracy in an energy-efficient manner, indicated by the roll-off vs. frequency in the dashed line. The last 10 years have resulted in an over 10dB improvement in power-normalized signal fidelity, or a 10× improvement in speed for the same normalized signal fidelity. Of note in this year's ISSCC is that two designs improve upon the thermal noise limited efficiency, using multi-stage pipeline structures.

The final figure plots achieved bandwidth as a function of SNDR. Sampling jitter or aperture errors coupled with an increased noise bandwidth make achieving both high resolution and high bandwidth a particularly difficult task. While 10 years ago a state-of-the-art data converter showed an aperture error of approximately 1ps_{rms} , in recent years designs with aperture errors below $100\text{fs}_{\text{rms}}$ have been published at a wide range of resolutions. ISSCC 2019 further advances the art with the top performing designs exceeding the $100\text{fs}_{\text{rms}}$ trendline with SAR and RAMP based pipeline designs.

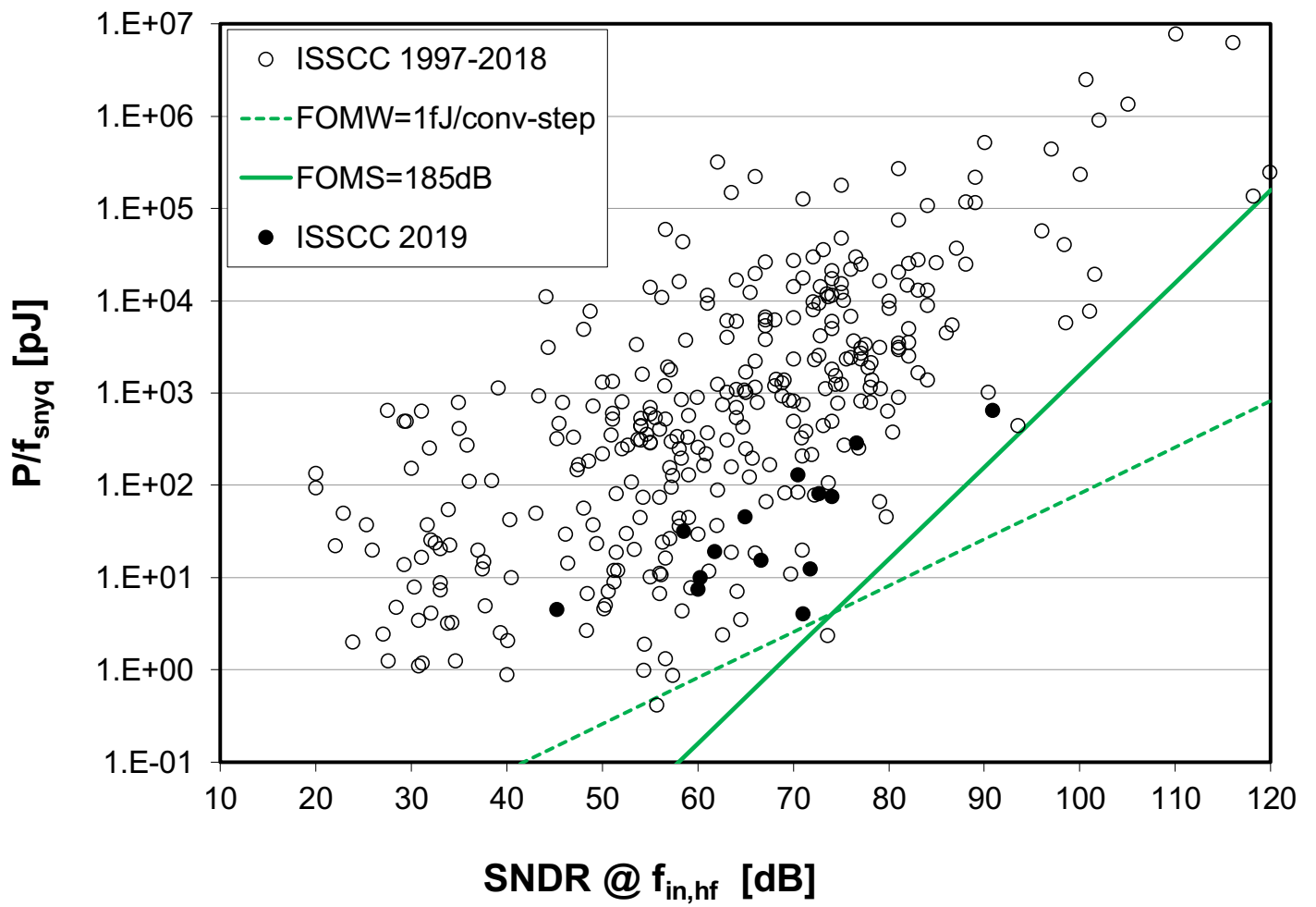


Figure 4: ADC power efficiency (P/f_{snyq}) as a function of SNDR.

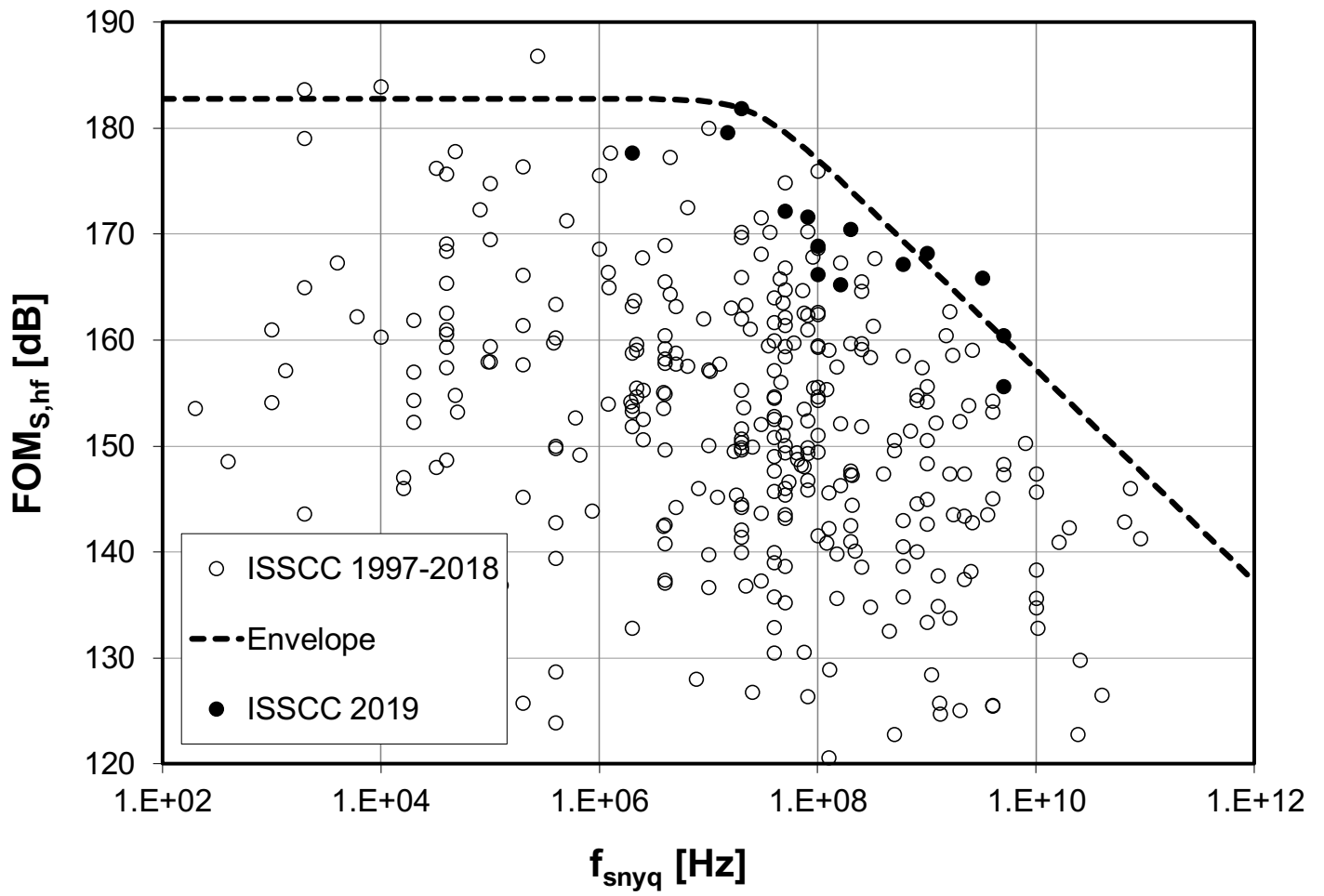


Figure 5: Power normalized noise and distortion vs. the Nyquist sampling rate.

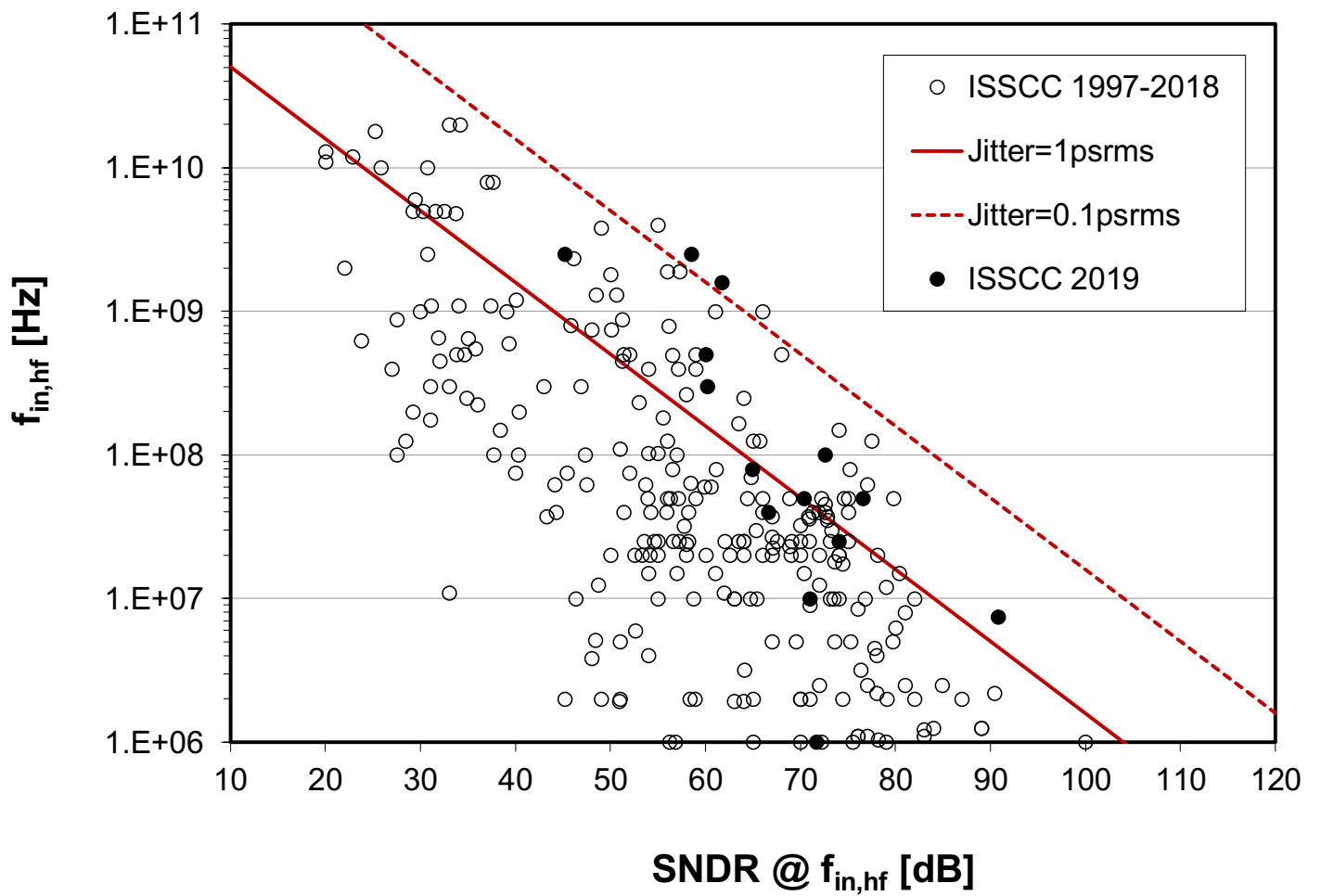


Figure 6: Bandwidth vs. SNDR.

HISTORICAL TRENDS IN TECHNICAL THEMES

COMMUNICATION SYSTEMS

RF SUBCOMMITTEE – WIRELESS SUBCOMMITTEE

WIRELINER SUBCOMMITTEE

RF Subcommittee – 2019 Trends

Subcommittee Chair: Piet Wambacq, imec, Belgium

ISSCC 2019 is dominated by CMOS/BiCMOS power amplifiers, and phase-locked loop (PLL) prototypes. Applications driving the ongoing advancement of building blocks at RF are broadband and 5G communications using massive MIMO and millimeter-wave (mm-wave) technologies, the Internet of Things (IoT), radar and sensing at mm-wave and sub mm-wave frequencies.

Phase-Locked Loop Synthesizers: Visible highlights are PLLs generating 30GHz carrier frequencies directly or via on-chip multipliers, designs offering lower integrated jitter and lower power consumption (e.g., -252.9 dB jitter-power FoM), and sub-systems that are free of calibration circuitry for fast start-up. Sub-sampling PLLs continue to drive the trend to lower power consumption overall, with fully-digital PLLs now almost completely displacing traditional analog designs. As illustrated in Fig. 7, the integrated time jitter (jitter variance) depends upon power consumption of a phase-locked loop frequency source. ISSCC 2019 presents two sub-sampling PLLs with outstanding jitter performance: 1) 25.4 to 29.5GHz, consuming just 10.2mW, and 2) a 28-to-31GHz synthesizer realizing -40dBc integrated phase noise. The timing jitter for both PLLs is $<100\text{fs}_{\text{RMS}}$, far less than previous designs seen on the figure.

Advanced voltage-controlled oscillators operating from supply voltages as low as 0.1V with phase noise and power consumption specifications rivalling state-of-the-art CMOS designs, ensure that advances in frequency synthesis will continue for the foreseeable future.

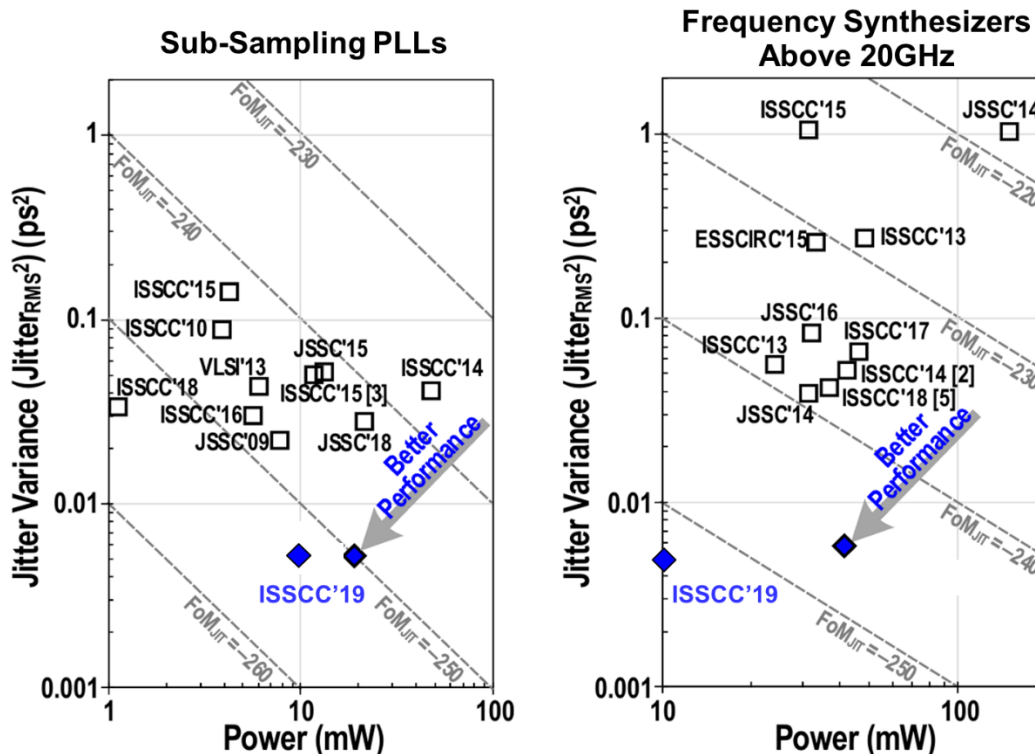


Figure 7. Trends in digital SSPLL and recent SSPLLs (left). Trends of the frequency synthesizers above 20GHz (right).

RF and mm-wave PAs: Doherty power amplifiers on CMOS are demonstrating improved power-added efficiency at the higher peak-to-average power ratios demanded by advanced modulation formats. Watt-level, fully integrated PAs in CMOS are showcased, operating at carrier frequencies up to 60GHz. Wideband PAs using split-path amplification and multi-way power combining on-chip aimed at 802.11ax and emerging 5G communication standards are also featured. Improving peak output power and efficiency in back-off have been major challenges for silicon-based PAs operating from low-voltage supplies. Above 20GHz (see Fig. 8), an asymmetric, distributed-active-transformer minimizes power combining loss in CMOS-SOI to deliver > 1 Watt (30.1dBm) peak output power at

60GHz with practical levels of linearity. A mixed-signal Doherty PA in CMOS-SOI realizes not only 40.1% peak power efficiency, but also 33.1% 6dB-PBO efficiency for 28GHz 5G radios. In the sub-6GHz range, highly digitized, segmented CMOS PAs offer better efficiency in power back-off (PBO) and 5G beamforming. A switched transformer class-G PA, employing an interleaved multi-sub-harmonic switching technique demonstrates 2x efficiency improvement at 12dB PBO.

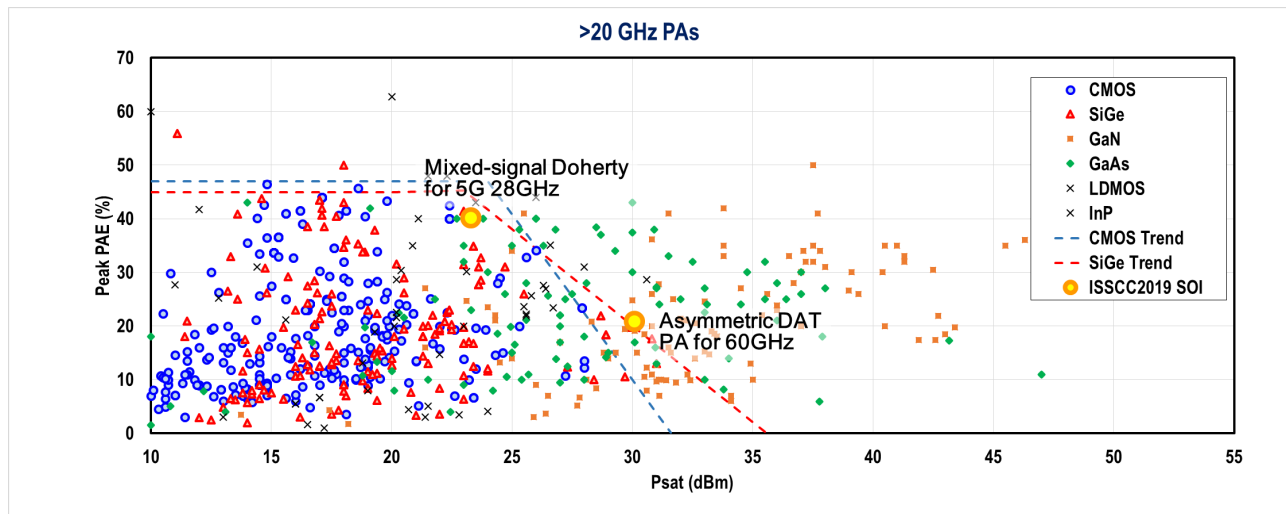


Figure 8: Peak power-added-efficiency (PAE) [%] versus max. output power [dBm] for recent power amplifiers in various technologies. (PA Performance Survey [Online]. Available: gems.ece.gatech.edu/PA_survey.html)

RF Techniques for Communication and Sensing: At ISSCC 2019, papers showcasing fast chirp generation for FMCW radars needed for automotive and indoor sensing, and radio receiver circuits offering vastly improved tolerance to interference are also important developments. A radar chirp generator based on a self-calibrated 16GHz subsampling PLL demonstrates very wide (1.5GHz) bandwidth with the low timing jitter critical for fine range resolution in an FMCW radar. Furthermore, interference is rapidly becoming the dominant problem for wireless receivers as the number of untethered users is increasing exponentially. Techniques demonstrate for a 2.4GHz radio receiver front-end allow for coexistence in the presence of very large (66dB) in-band interfering jammers, while consuming just 2mA of DC current and maintaining a sensitivity of -83dBm.

Wireless – 2019 Trends

Subcommittee Chair: Stefano Pellerano, Intel, Hillsboro, OR

The continuing demand for faster wireless data rates in the context of mobile battery limitations drives the development of high-throughput and power-efficient transceivers. This year, advanced cellular transceivers extend carrier aggregation to support up to 6 inter- and intra-band 3G, 4G and 5G carriers while also enabling NR and LTE protocols with dual connectivity (EN-DC). Data rates of up to 3.55Gb/s downlink and 1.27Gb/s uplink make multi-Gb/s data rates in handsets a reality. Furthermore, carrier aggregation by combining RF and mm-wave spectra in a multiband 5G transceiver achieves up to 6Gb/s, demonstrating the potential of utilizing RF and mm-wave spectra in conjunction.

Figure 9 shows trends in data rates at 28GHz, 60GHz and beyond 100GHz, demonstrating the promise of >10Gb/s throughput at mm-wave. Transceivers presented this year leverage dual-polarization and MIMO techniques to further improve efficient use of scarce wireless spectrum, achieving >40Gb/s data rates at mm-wave. Researchers continue to focus on area and power-efficient transceiver unit-cells for scalable mm-wave arrays, particularly at 28GHz, reflecting commercial interest in 5G network deployment. Transitions from phased arrays to MIMO/Digital beamforming arrays can be seen in integrated 28GHz beamformer implementations with increased TDD/FDD/MIMO functionality. The focus on MIMO can also be seen in the first extension of integrated full-duplex techniques to MIMO transceivers.

CMOS radar technology continues to advance with demonstration of mm-wave MIMO radars with 10× higher effective transmit-receive pairs, leading to improved 3D resolution and object discrimination for automotive radar. Miniaturization of low-power radar technology opens up applications such as health monitoring, with the demonstration of sub-mW radar transceivers that measure respiration from up to 15m away.

Reported advances in ultra-low-power radio continue the drive towards pervasive and perpetual wireless communication as can be seen from Figure 10. This year, the first sub-nW wake-up radio is reported enabling practically unlimited battery lifetime for sensor nodes. Low-power operation is extended to standard-compliant transceivers with BLE radios that consume well below 1mW, enabling sensor networks that can communicate with ubiquitous mobile devices.

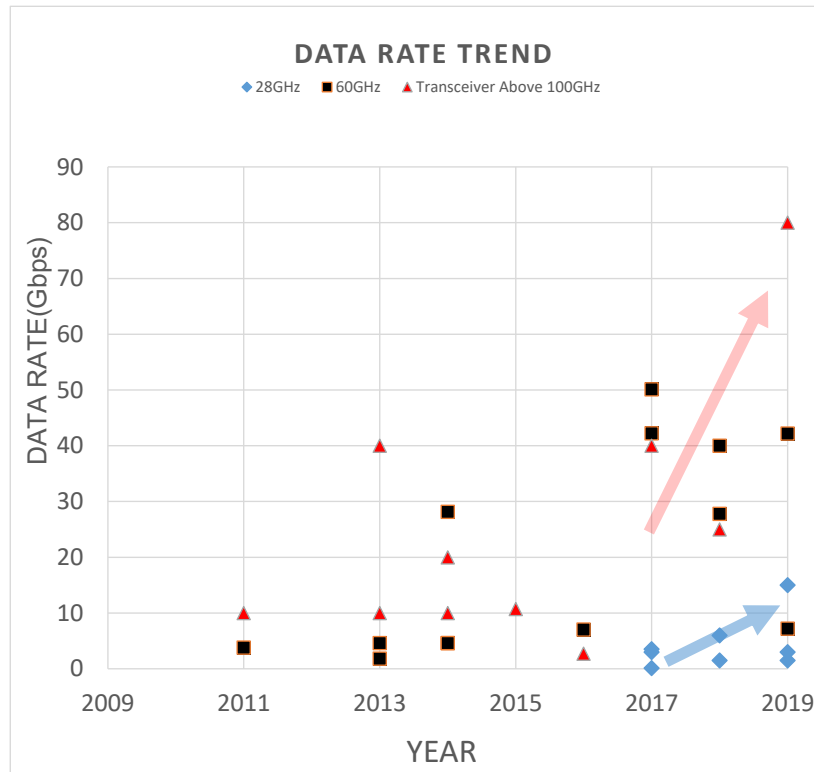


Figure 9: mm-wave Wireless Data-Rate Trends.

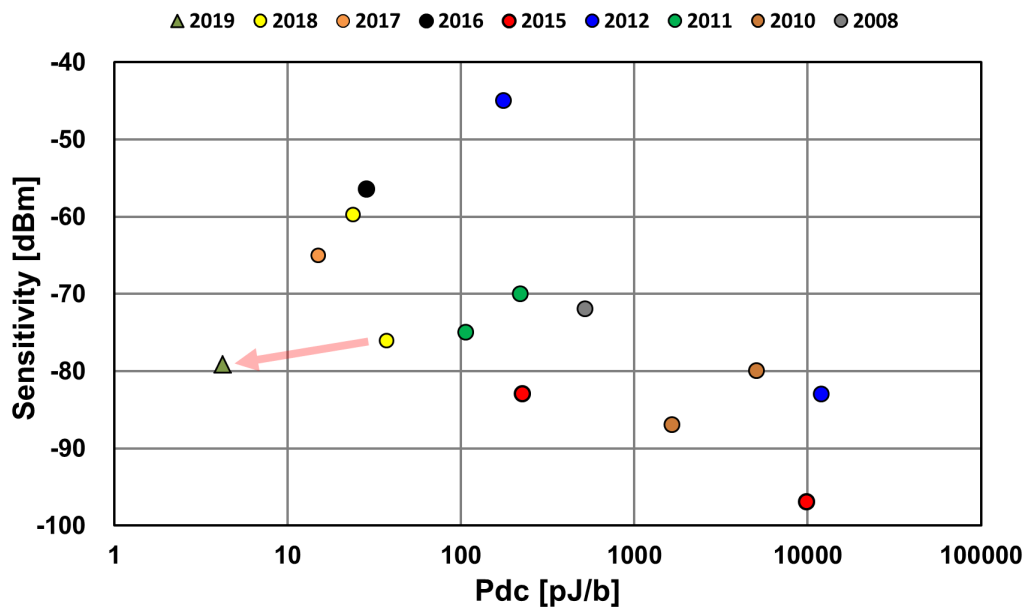


Figure 10: Wake-up Receiver Sensitivity Trends.

Wireline – 2019 Trends

Subcommittee Chair: Frank O'Mahony, Intel, Hillsboro, OR

Over the past decade, wireline I/O has been instrumental in enabling the incredible scaling of computer systems, ranging from handheld electronics to supercomputers. During this time, aggregate I/O bandwidth requirements have increased exponentially, driven by applications such as memory, graphics, chip-to-chip fabric, backplane, rack-to-rack, and LAN. In part, this demand is met by expanding the number of I/O pins per component. As a result, I/O circuitry consumes an increasing amount of area and power on today's chips. Increasing bandwidth has also been enabled by rapidly accelerating the per-pin data rate. Figure 11 shows that per-pin data rate has approximately doubled every four years across a variety of diverse I/O standards ranging from DDR, to graphics, to high-speed Ethernet. Figure 12 shows that the data rates for published transceivers have kept pace with these standards, enabled in part by process technology scaling. However, continuing along this rather amazing trend for I/O scaling will require more than just transistor scaling. Significant advances in both energy efficiency and signal integrity must be made to enable the next generation of low-power and high-performance computing systems. Although 100Gb/s standards in OIF and IEEE are still in progress, papers at ISSCC this year include the first ever 100Gb/s PAM-4 mixed-signal receiver in 14nm FinFET (Paper 6.1), the world's first 400Gb/s 4-lane PAM-4 optical transceivers in 16nm FinFET (Paper 6.5), and several power-efficient 56Gb/s ADC-based transceivers in 7nm FinFET.

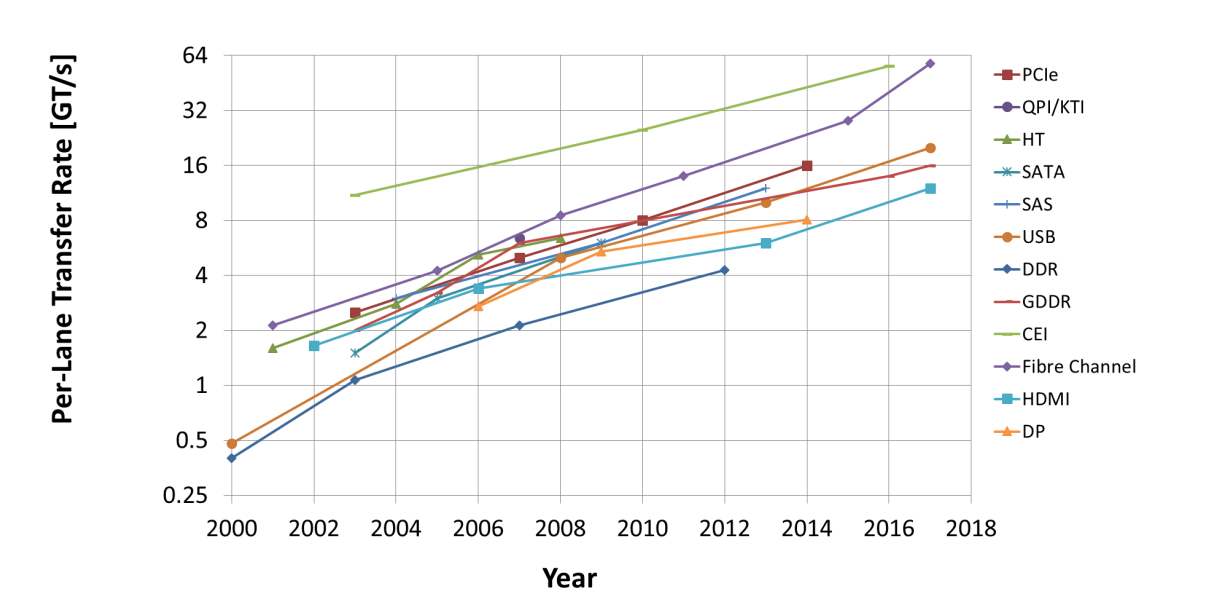


Figure 11: Per-pin data rate vs. Year for a variety of common I/O standards.

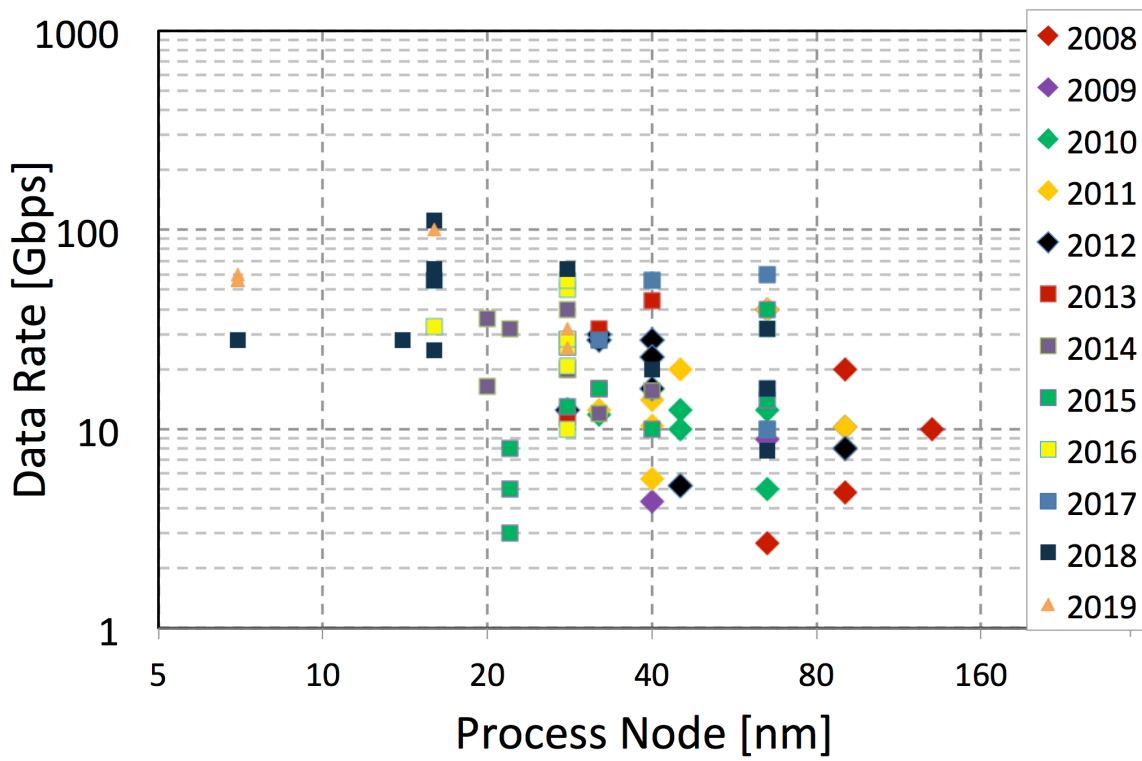


Figure 12: Data-rate vs. process node and year.

Energy Efficiency and Interconnect Density:

Power consumption of I/O circuits is a first-order design constraint for systems ranging from cell phones to servers. As the pin count and per-pin data rate for I/Os have increased, so has the percentage of total power consumed by I/Os. Technology scaling enables increased clock and data rates and offers improved energy efficiency, especially for digital components. However, simply increasing per-pin baseband data rates with existing circuit architectures and channels is not always a viable path given fixed system power limits. Many recent advances have reduced power for high-speed link components through circuit innovation, including low-power RX equalization (DFE, CTLE), CMOS and resonant clocking, low-swing voltage-mode transmitters and links with low-latency power-saving states. Medium and long reach mixed-signal solutions at data rates of 50-100Gb/s face implementation challenges even on the most advanced process nodes. But mixed-signal equalization can still be an attractive option due to its power and area efficiency and low latency. At ISSCC this year, IBM (Paper 6.1) demonstrates a 100Gb/s PAM-4 mixed-signal receiver in 14nm CMOS for medium reach channels. Its analog front-end shapes the channel response to permit an efficient implementation of a speculative DFE consuming only 1.1pJ/bit with 19dB loss at the Nyquist frequency for PAM-4.

Pushing the Channel Limits with ADC-DSP-based PAM-4 Transceivers:

There is ever-growing demand for very high data rate communication across a wide variety of channels. Some types of channels, especially those related to medium-distance electrical I/O, such as direct-attach copper cables and server backplanes, must support high data rates over high-loss channels (30-40dB at Nyquist). For these links, the key to scaling has been improvements in equalization and clock/data recovery. Particularly this year, we see that most of the advanced transceivers adopt PAM-4, as it doubles the bandwidth efficiency over legacy NRZ with ~9dB SNR penalty. In addition, with 7nm FinFET CMOS technology enabling low-power and high-performance implementation of forward error correction (FEC) and advanced digital signal processing techniques, ADC-DSP-based transceivers have become an attractive way of realizing advanced equalization and timing recovery. Figure 13 plots the energy efficiency (expressed in mW/Gb/s, which is equivalent to pJ/b) as a function of channel loss for recently reported wireline transceivers. Looking at the most aggressive designs, the data indicates that the scaling factor between link power and signaling loss is slightly less than unity. The trend line for the best reported transceivers indicates that a 30dB increase in channel loss corresponds to a roughly 10x increase in pJ/b. Recent receivers achieve data rates of 56-60Gb/s PAM-4 across channels with up to 40dB of loss at Nyquist. Papers 6.2, 6.3, and 6.4 describe 56Gb/s ADC-DSP based PAM-4 transceivers that operate over channels with 38-42dB loss with low power consumption.

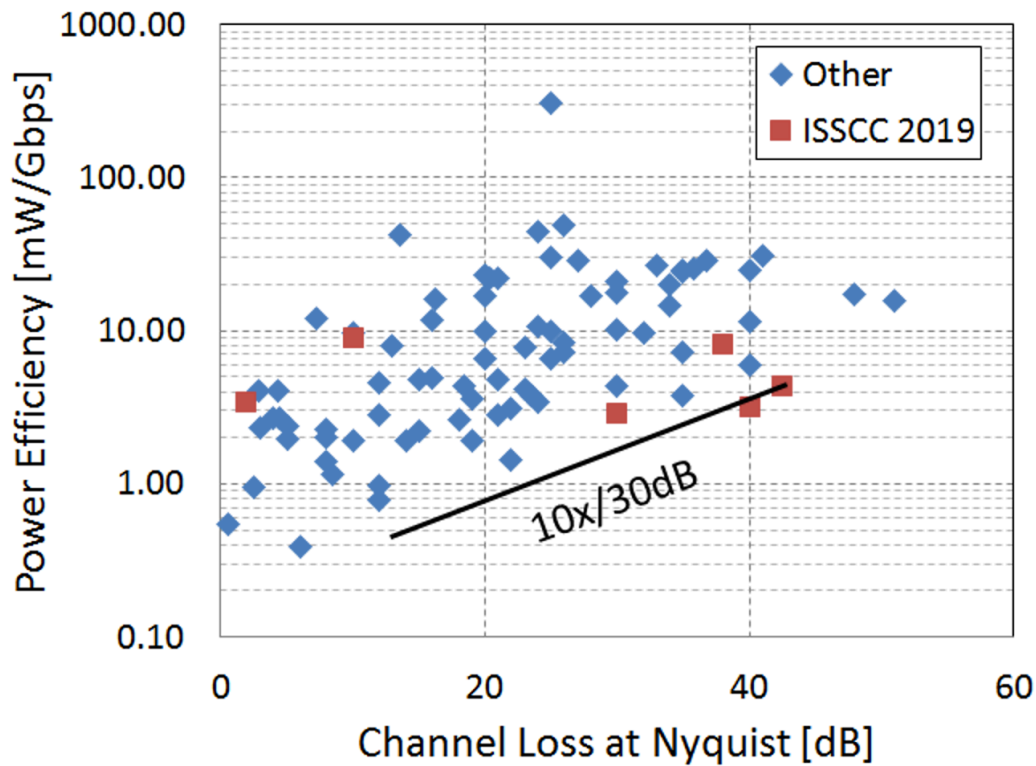


Figure 13: Transceiver power efficiency vs. channel loss.

Extending the Horizon of Wireline Transceivers:

The advent of ADC-DSP-based transceivers opens a path to more advanced modulation schemes that could not be easily realized in traditional mixed-signal implementations. Beyond PAM-4 modulation with a conventional DFE, we are starting to see transceivers that use alternative equalization and modulation schemes including sequence detection (Paper 30.4) and discrete multi-tone (DMT) modulation (Paper 30.2). The same schemes that enabled high-bandwidth communication for modems over a telephone line are now being evaluated for 56Gb/s+ wireline transmission within computer systems. Also, this DSP-based architecture can be a cross-pollination platform with other advanced fields, such as optimization and perhaps AI. For instance, Paper 30.5 showcases a 56.25Gb/s, PAM-4 receiver that adopts a genetic algorithm to address the vast search space problem of adapting its analog/mixed-signal frontend. On the other hand, optical interconnects continue to be an attractive alternative to traditional electrical wireline interconnects and Paper 6.5 reports a 400Gb/s 4-lane transceiver for optical communication in 16nm FinFET technology consuming a total of 900mW.

Concluding Remarks:

Continuing to aggressively scale I/O bandwidth is both essential for the industry and extremely challenging. Innovations that provide higher performance and lower power will continue to be made in order to sustain this trend. Advances in circuit architecture, interconnect topologies, and transistor scaling are together changing how I/O will be done over the next decade. The most exciting and most promising of these emerging technologies for wireline I/O will be highlighted at ISSCC 2019.



HISTORICAL TRENDS IN TECHNICAL THEMES

DIGITAL SYSTEMS

DIGITAL ARCHITECTURES & SYSTEMS SUBCOMMITTEE

DIGITAL CIRCUITS SUBCOMMITTEE

Digital Architectures & Systems (DAS) – 2019 Trends

Interim Subcommittee Chair: Thomas Burd, Advanced Micro Devices, Santa Clara, CA

Deep learning continues to rapidly evolve at ISSCC 2019. Historically, the computational complexity of typical deep neural networks impedes their execution on resource-scarce mobile or wearable devices. Last year, several innovative solutions were introduced to enhance throughput and improve energy efficiency, mostly focusing on the efficiency of convolutional neural networks (CNN). This year, many of the papers show universal architectures that handle CNN, FC and RNN networks. There is also a focus on multiple-bit precision to dynamically adjust to the required accuracy and throughput, rather than just lowering the precision to realize high efficiency metrics. There are significant improvements for peak throughput and energy efficiency as well.

On-device training, which is important for personal data security and personalized optimization, is one of new trends of this year. Training usually requires more performance and accurate data precision, which presents more challenges to the accelerators for power limited devices. The training has been executed on large scale servers through network transferred data. Accelerator design is evolving to handle on-device training supporting back propagation with higher data precision. Some research incorporates a neural spiking model with deep neural networks.

Figure 14 illustrates deep-learning processor efficiency and throughput improvements for CNNs/DNNs presented at ISSCC 2019, as compared to the state-of-the-art in 2018.

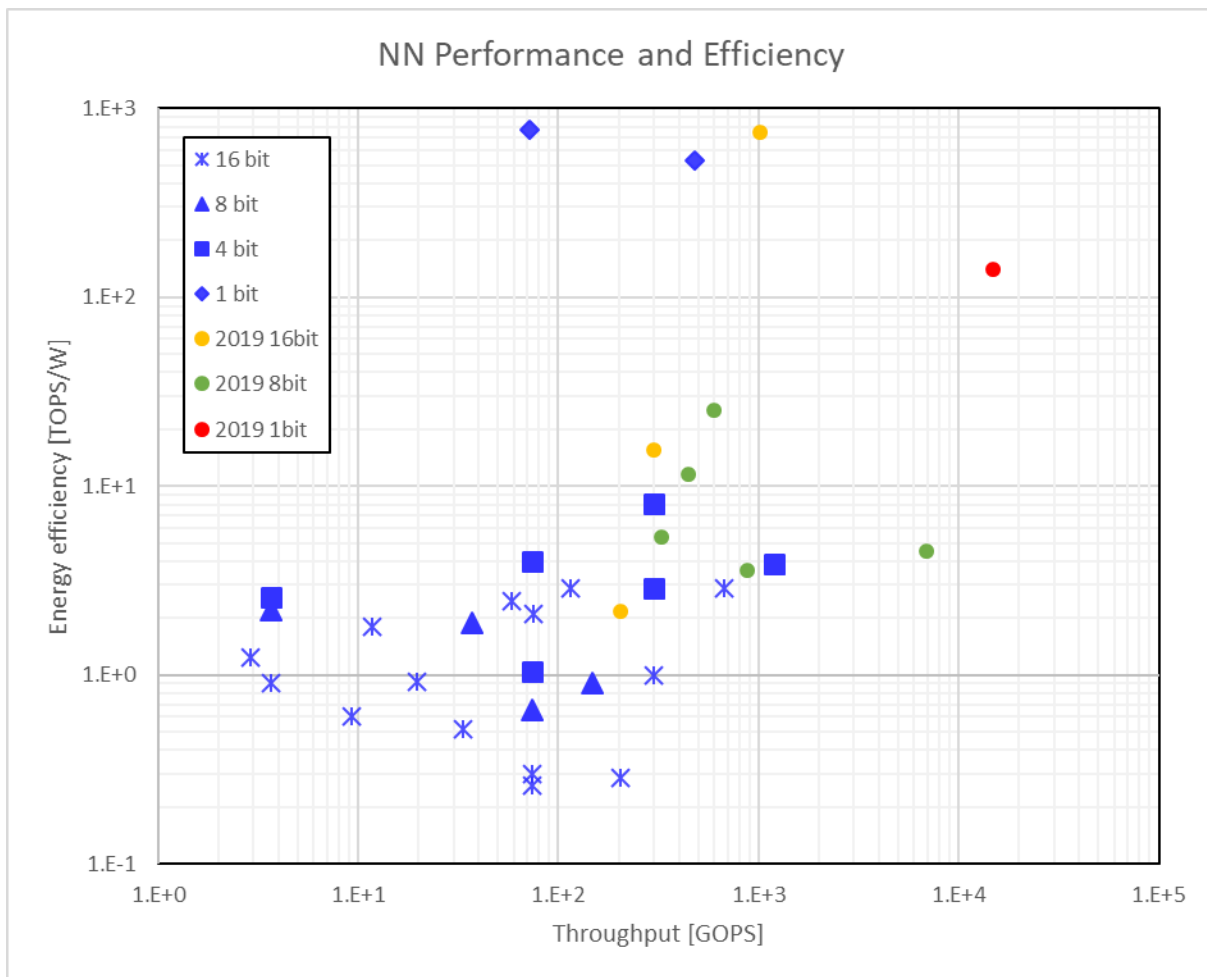


Figure 14: Deep-learning processor throughput and efficiency.

Unlike previous years, there were no flagship industry microprocessors presented at ISSCC. We do not believe this will be a continuing trend, but rather an indication of where the industry is in terms of product cycles. The notable system standout paper in ISSCC 2019 describes the Summit and Sierra supercomputers, which are an IBM, Nvidia and Mellanox collaboration to produce the world's fastest super computer capable of 200PFLOPs.

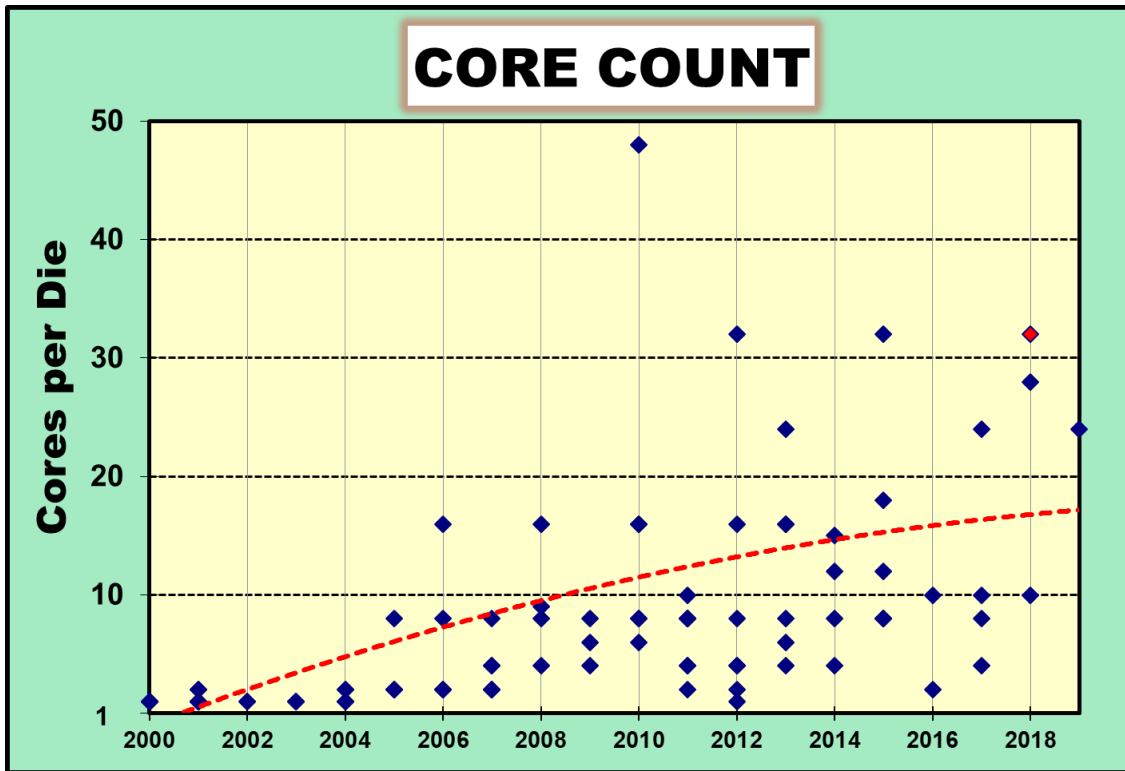


Figure 15: Core-count trends (red diamond designates multi-chip module).

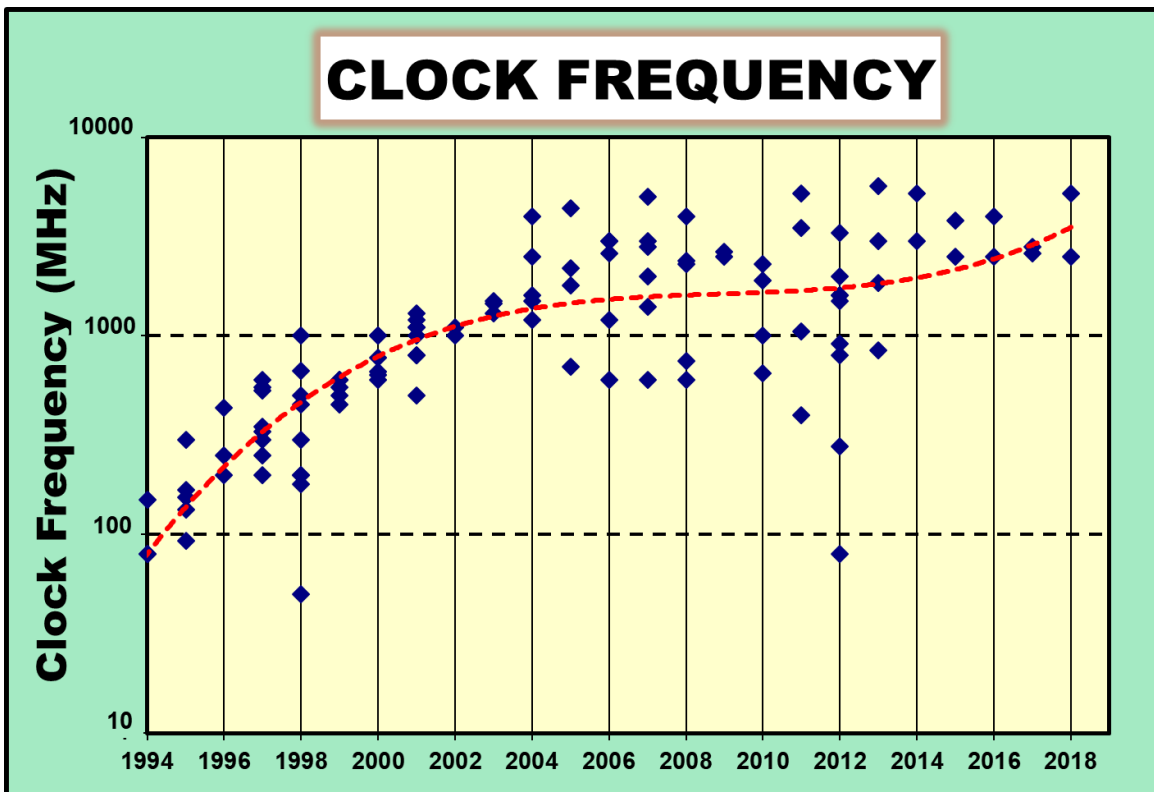


Figure 16: Clock-frequency-scaling trends.

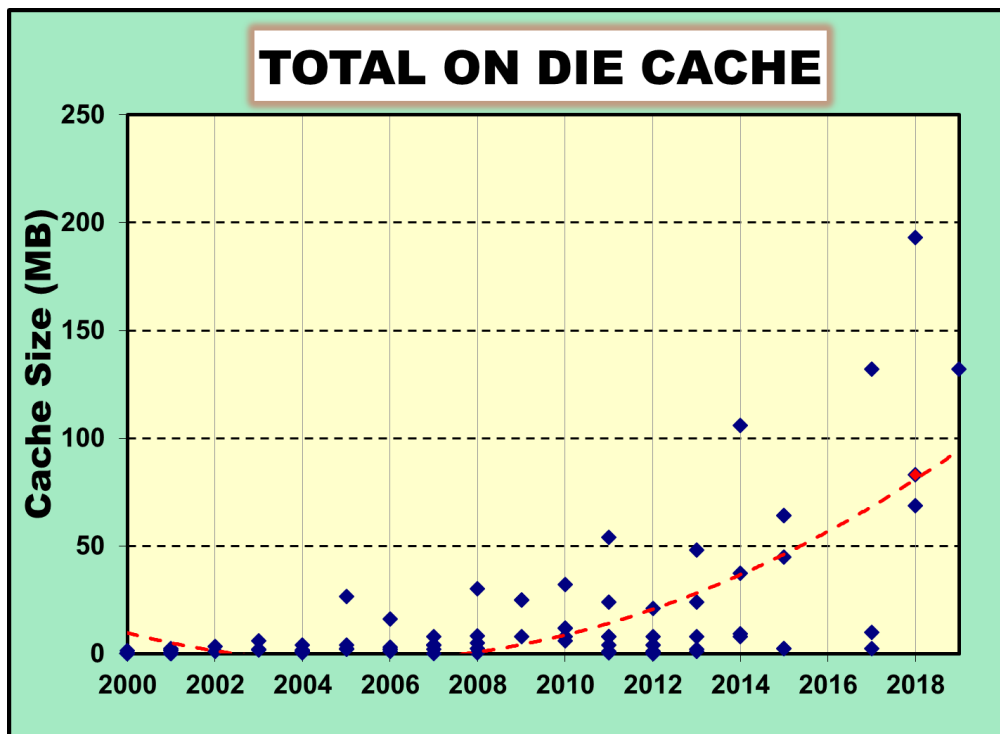


Figure 17: On-die cache-size trends (red diamond designates multi-chip module).

The computational performance of mobile AP (Application Processor) SoCs has historically grown as silicon process technology advances. AP SoCs continue to add more features, including multimedia IP cores and accelerators on-chip to enhance functionality. Programmable neural-network processors have appeared in AP SoCs to enhance machine-learning application capabilities. Dedicated neural-network accelerators execute machine-learning functions faster and with higher energy efficiency than generic CPUs and GPUs. Neural-network processor units (NPU) will be adopted in most future AP SoCs, establishing an important future direction, where an

Digital Circuits – 2019 Trends

Subcommittee Chair: Edith Beigne, Facebook, Menlo Park, CA

Demand for higher performance across ubiquitous, connected, and energy-constrained platforms ranging from Internet of Everything (IoE) to cloud data-centers continues to drive innovations in all CMOS digital-circuit building blocks, with goals of improving energy-efficient performance, lowering cost/design effort, and enhancing security. Classic technology scaling has slowed and circuit design efforts are exploiting technology features, such as body biasing and passive-device advancements, to enable circuit innovation.

Energy-Efficiency Techniques and Integrated Voltage Regulators: Energy reduction remains a top priority as power density continues to increase. Voltage regulators, while traditionally being off-chip, have increasingly been integrated on-chip to reduce cost. Low-dropout (LDO) linear regulators, switched-capacitor voltage regulators (SCVR), and now, inductor-based buck voltage regulators (LCVR) are integrated in scaled process nodes to enable faster and fine-grain dynamic voltage and frequency scaling (DVFS) of individual functional blocks. In turn, the low voltages supported in DVFS systems necessitate a move from analog-based LDOs to digital implementations. Another trend is towards hybrid LDOs that incorporate the best features of both analog and digital designs. Figure 20 shows the conversion efficiency and current density of these integrated voltage regulators, which continues to improve. Variation mitigation has also become a major trend in digital circuits in order to improve robustness and power efficiency across Process, Voltage, and Temperature (PVT). Specific all-digital sensors and adaptive techniques are currently proposed to mitigate these effects on-chip.

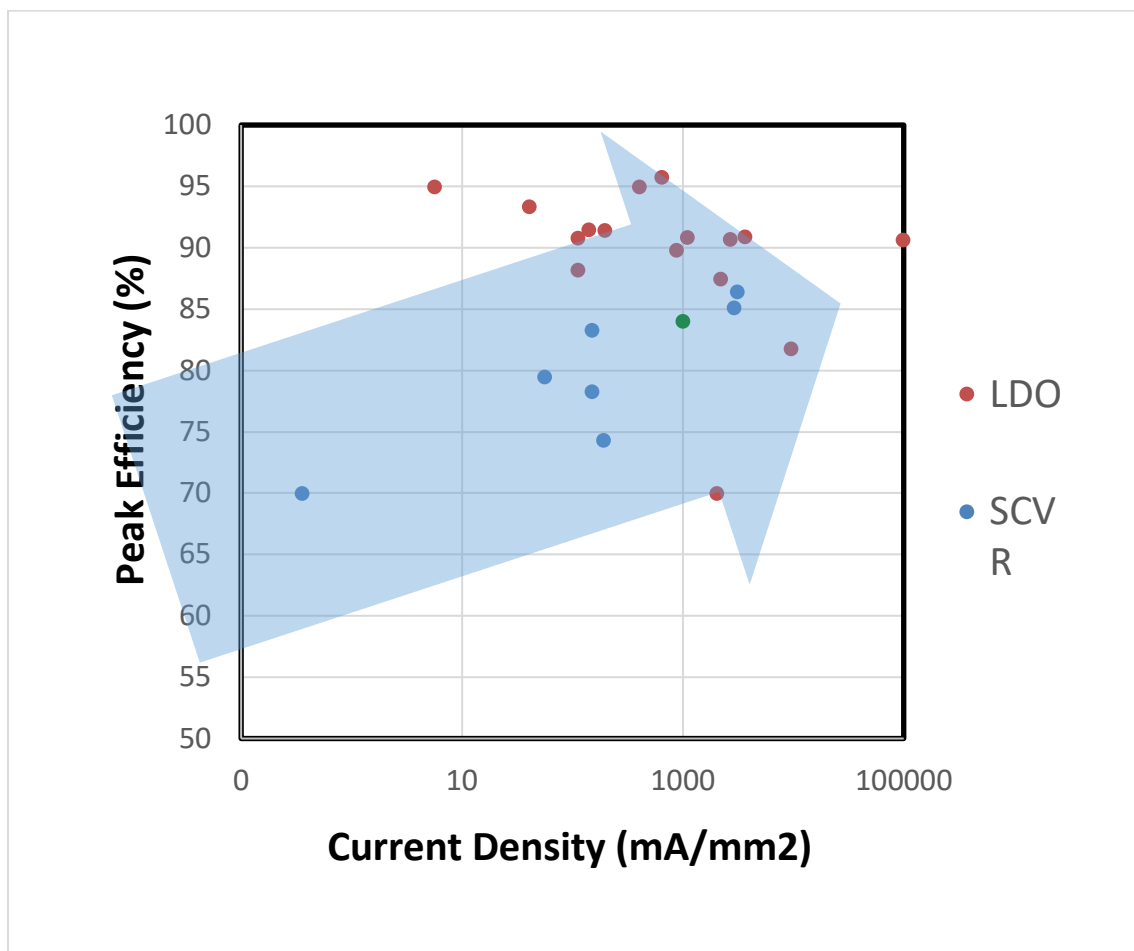


Figure 20. Integrated voltage regulators

Synthesizable Digital PLLs for Low-Jitter Applications: PLL trends include migration from analog to digital to include more functionality, cope with variability, and ease scaling to finer geometries. Demand for compact low-jitter PLLs is increasing. The use of more automated digital design flows (such as synthesis and APR) dramatically reduces development costs, but can degrade jitter, requiring new techniques to compensate. Figure 21 highlights metrics for PLLs and DPLLs published at ISSCC over the past 10+ years. The plot shows the relationship between reference (input) frequency and figure-of-merit, demonstrating the tradeoff between cost (higher reference frequency) and overall PLL performance.

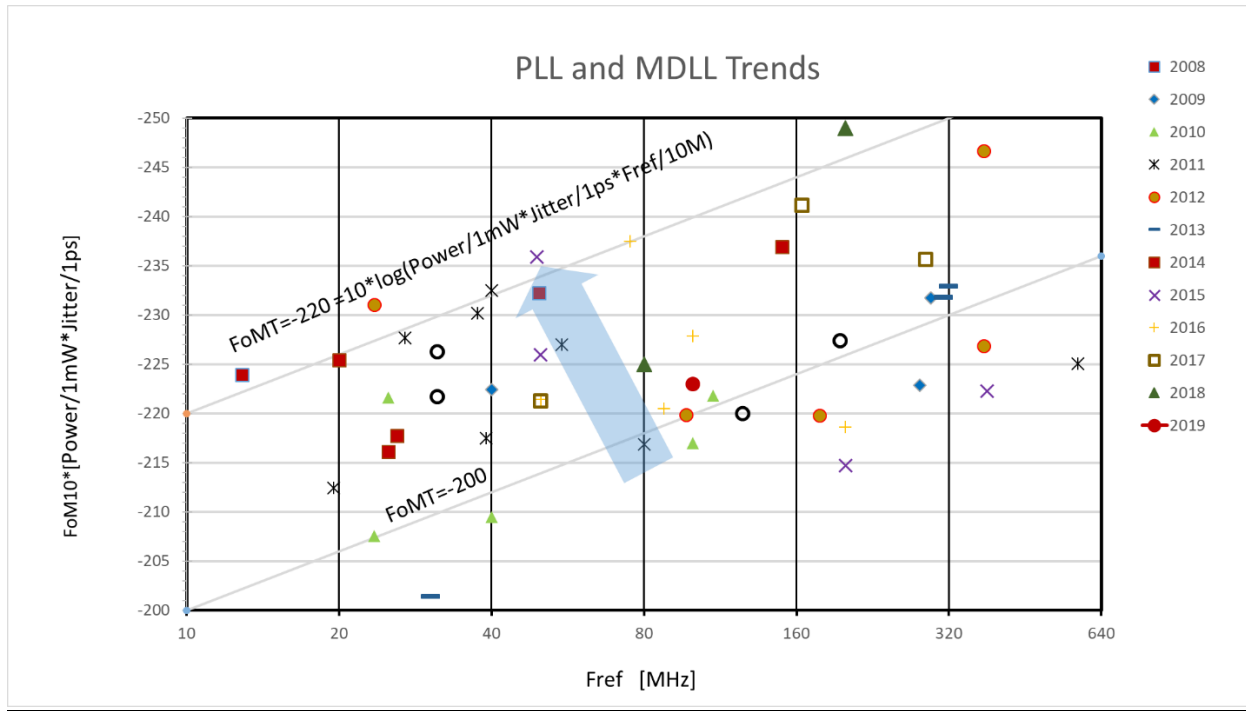


Figure 21. PLL and Multiplying Delay-Locked Loop (MDLL) trends.

Circuits for Hardware Security: With the increasing risk and cost of information theft, hardware-implemented security has become a common circuit component. Though focus on cryptographic implementation continues, cost-effective PUFs (Physically Unclonable Functions) are now a focus area, such as in smart cards and consumer devices. TRNGs (True Random-Number Generators) are also commonly leveraged to strengthen secret key generation in cryptographic applications. Figure 22 illustrates trends in area/bit scaling and bit-error rates for PUFs published recently at ISSCC.

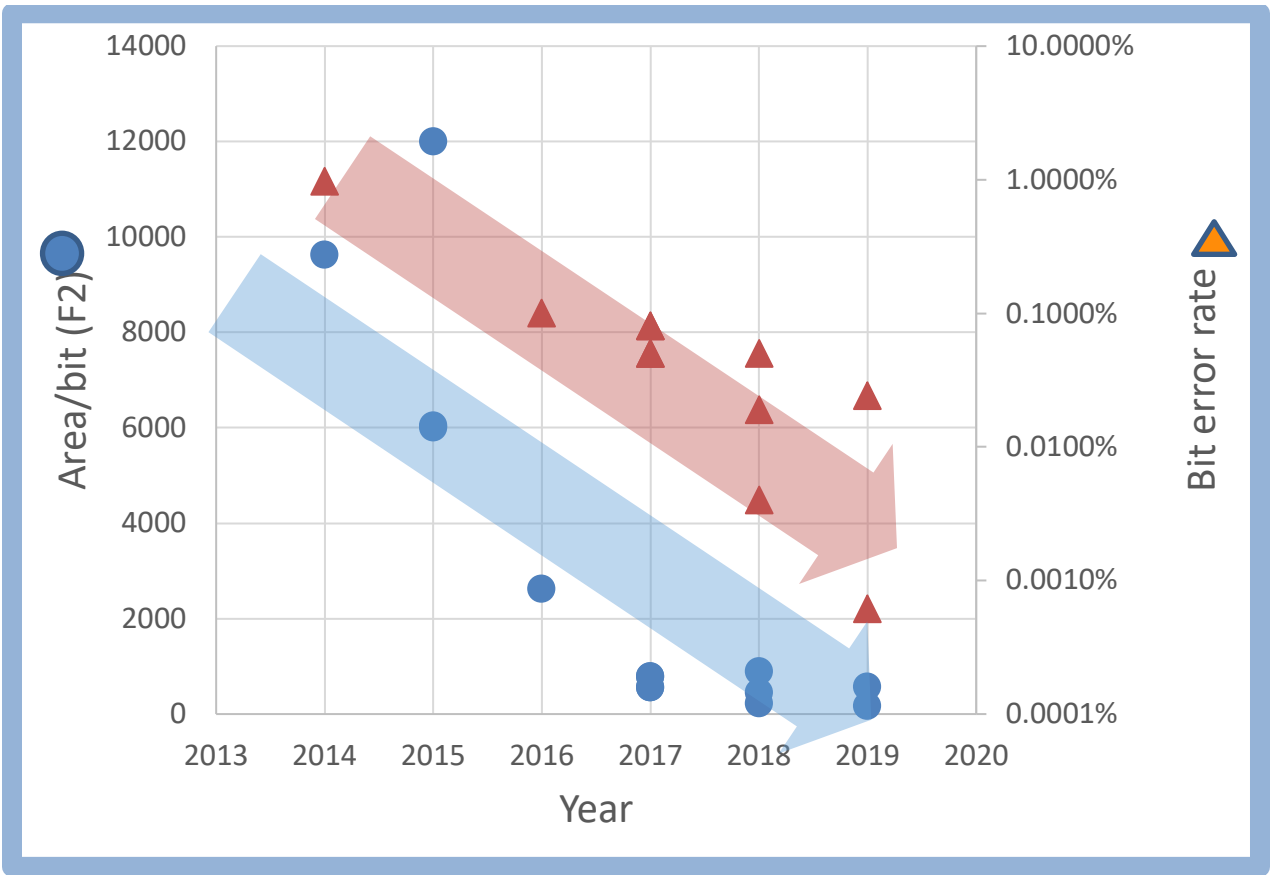


Figure 22. Area/bit and bit-error-rate trends for physically unclonable functions (PUFs).

Memory – 2019 Trends

Subcommittee Chair: Jonathan Chang, TSMC, Hsinchu, Taiwan

The demand for high density, high bandwidth, and low energy memory systems continues everywhere from High Performance Computing to SoC, Wearables and IoT. This year's conference highlights high speed embedded cache applications in cutting edge process technologies, as well as two 7nm SRAM bit cells for high-speed dual-port memories. Computation-In-Memory (CIM) improves the energy efficiency of multiplication-and-accumulation (MAC) operations in both SRAM and ReRAM. DRAM high-performance memory interface technologies are enhanced for LPDDR5 and DDR5. NAND Flash memory extended the capacity using both bit cell and number of layers in 3D structures.

Some current state-of-the-art papers from ISSCC 2019 include:

- A $0.075\mu\text{m}^2$ dual-port SRAM bit cell in 7nm which mitigates the WL-R/C and cross talk issue in the advanced technology node by process and layout co-optimization
- A 22nm FinFET process with an array density of $10.1\text{Mb}/\text{mm}^2$ with all thin gate periphery, leveraging a low voltage ReRAM technology.
- A 7.5Gbps LPDDR5 with WCK clocking, non-target ODT (NT-ODT), dynamic voltage and frequency scaling (DVFS), and a deep sleep mode (DSM).
- A 16Gb 6.4Gbps DDR5 with a phase-rotator-based DLL, write-level training, and RX/TX with enhanced DFE/FFE.
- A 1.33Tb 4bit/cell (QLC) 3D-Flash memory in a 96-Word-Line-Layer Technology with $8.5\text{Gb}/\text{mm}^2$.
- A 512Gb 3b/cell 3D-flash memory on 128-word-line-layer technology with 4 planes architecture and 132MB/s with CMOS under array architecture.

SRAM

Innovations in SRAM continue to support high speed embedded cache applications in cutting edge process technologies, as well as new areas of Computation-In-Memory. This year's conference highlights two 7nm SRAM bit cells for high-speed dual-port memories, and to support lower- V_{MIN} across PVT corners. The conference also includes multiple versions of SRAM applications where Multiply-and-Accumulate (MAC) is done in the memory arrays for optimized TOPS/W in AI and Machine Learning. Figure 23 shows SRAM bit cell area and V_{MIN} scaling trend.

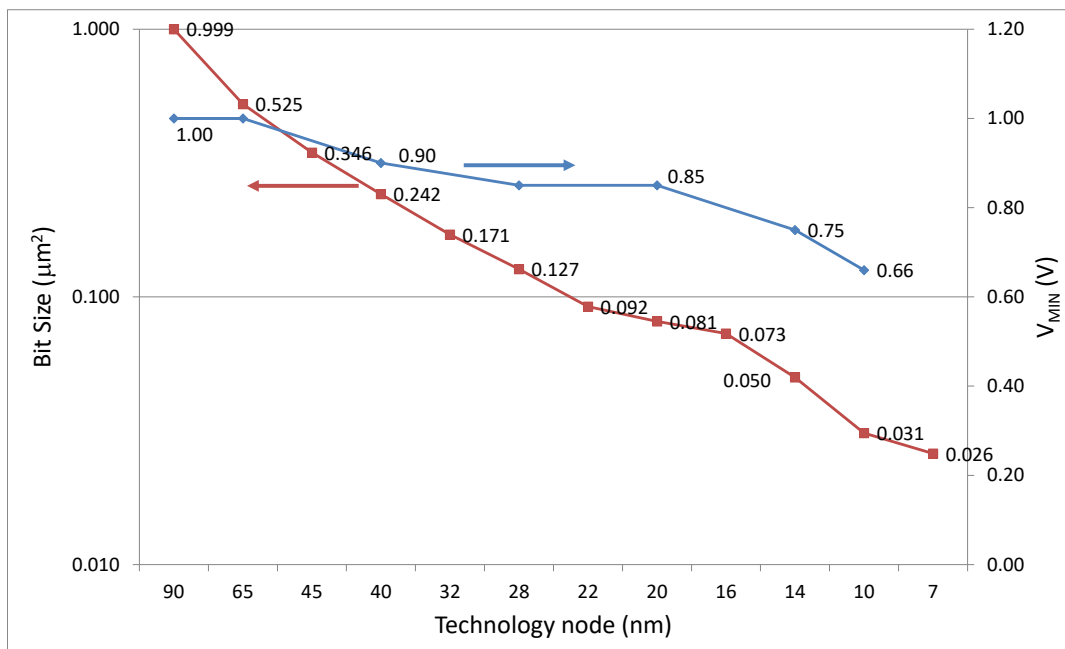


Figure 23 – Bit Cell and V_{MIN} scaling trend for SRAM

HIGH-BANDWIDTH AND LOW-POWER DRAM

In order to maintain the optimal memory hierarchy ratio with respect to storage memory, DRAM continues to scale density, form factor, and bandwidth. This year, for ISSCC 2019, benchmarks for the latest interface standards are presented, including LPDDR5 for high-speed mobile and DDR5 for server/computing memory standards. Figure 24 shows DRAM Bandwidth scaling over last decade.

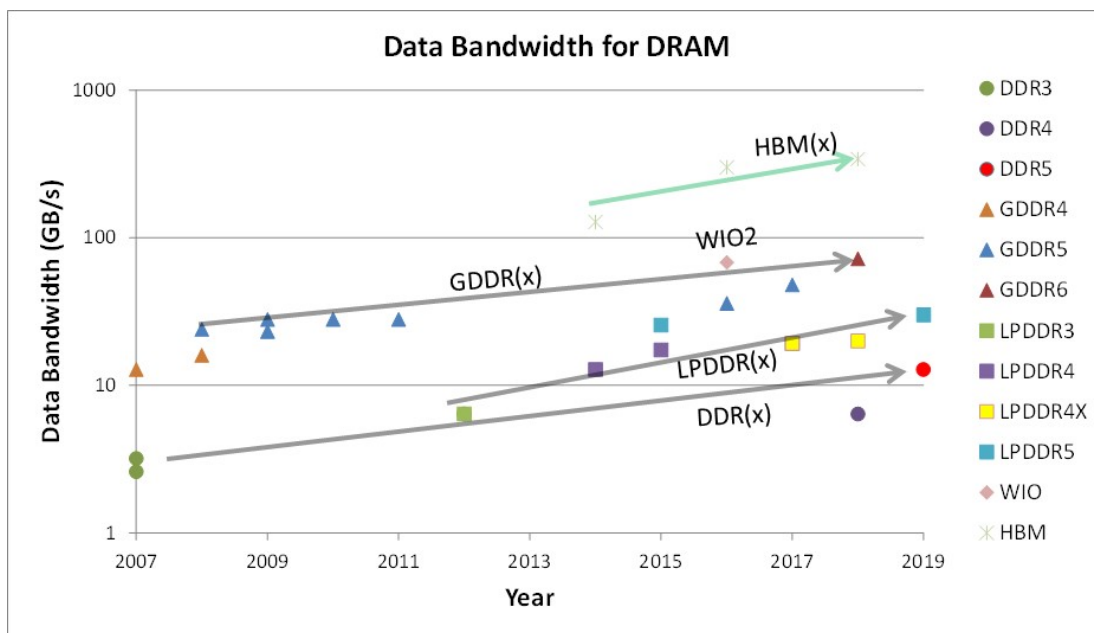


Figure 24 - DRAM data bandwidth trends

NONVOLATILE MEMORIES

In the past decade, significant investment has been put into the emerging memories field to find an alternative to floating-gate-based nonvolatile memory. The emerging NVMs, such as phase-change memory (PRAM), ferroelectric RAM (FeRAM), magnetic spin-torque-transfer (STT-MRAM), and Resistive memory (ReRAM), are showing potential to achieve high cycling capability and lower power per bit in read/write operations. Figure 25 highlights 3b/cell(TLC) NAND Flash and 4b/cell(QLC) NAND Flash write throughput. Figure 26 shows a significant increase in NAND Flash capacity from 1Tb to 1.33Tb this year. Such high areal densities are achieved through advancements in 3-dimensional vertical bit cell stacking technologies.

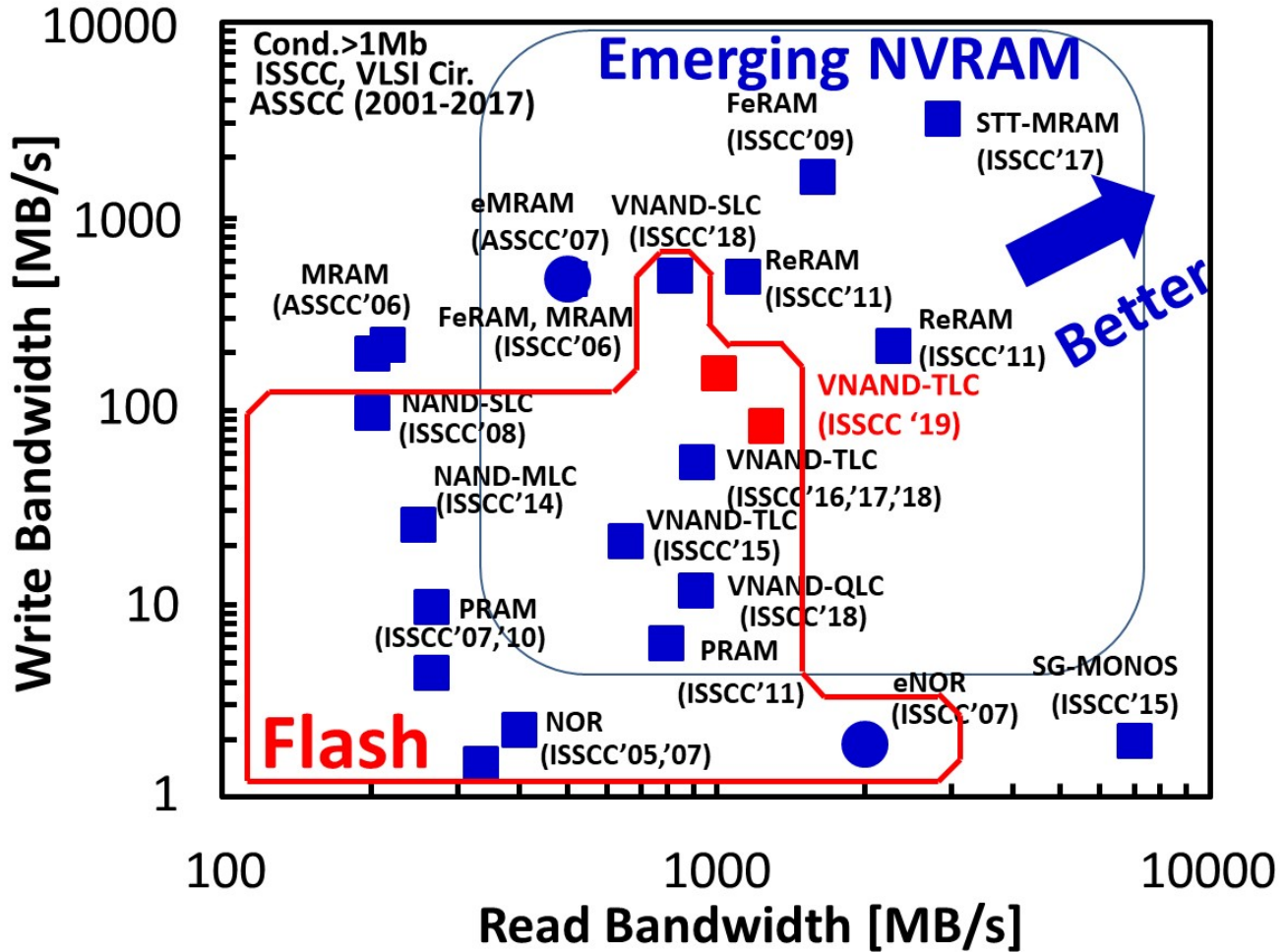


Figure 25 - Read/write bandwidth comparison of nonvolatile memories

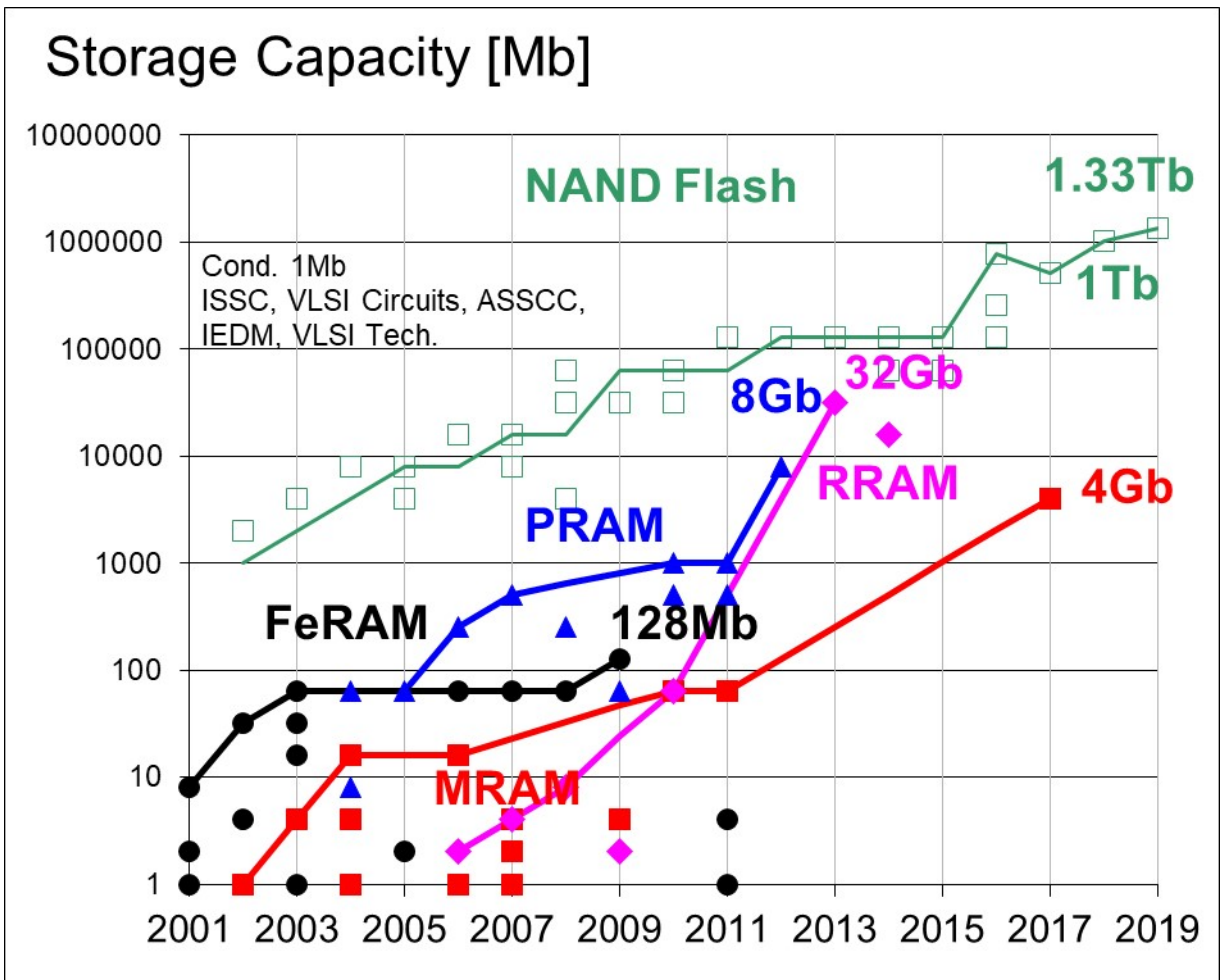


Figure 26 - Memory capacity trend of emerging nonvolatile memories

NAND FLASH MEMORY

NAND flash memory continues to advance towards higher density and lower power, resulting in low-cost storage solutions that are replacing traditional hard-disk storage with solid-state disks (SSDs). 3D memory technology has been the mainstream for NAND flash memory in mass-production of semiconductor industries. This year, a 1.33Tb 4b/cell with 96 stacked WL layers achieves 8.5Gb/mm² areal density and a 512Gb 3b/cell 3D NANDs with 128 stacked WL layers, 7.8Gb/mm² are reported, continuing the trend to satisfy the ever-growing demand for increased density requirements and lower manufacturing cost. Not only higher density, but also high performance over 82MB/s program throughput and 1.2GB/s read throughput with lower IO voltage from 1.8V to 1.2V has been reported. Figure 27 shows the observed trend in NAND Flash capacities at ISSCC over the past 15 years.

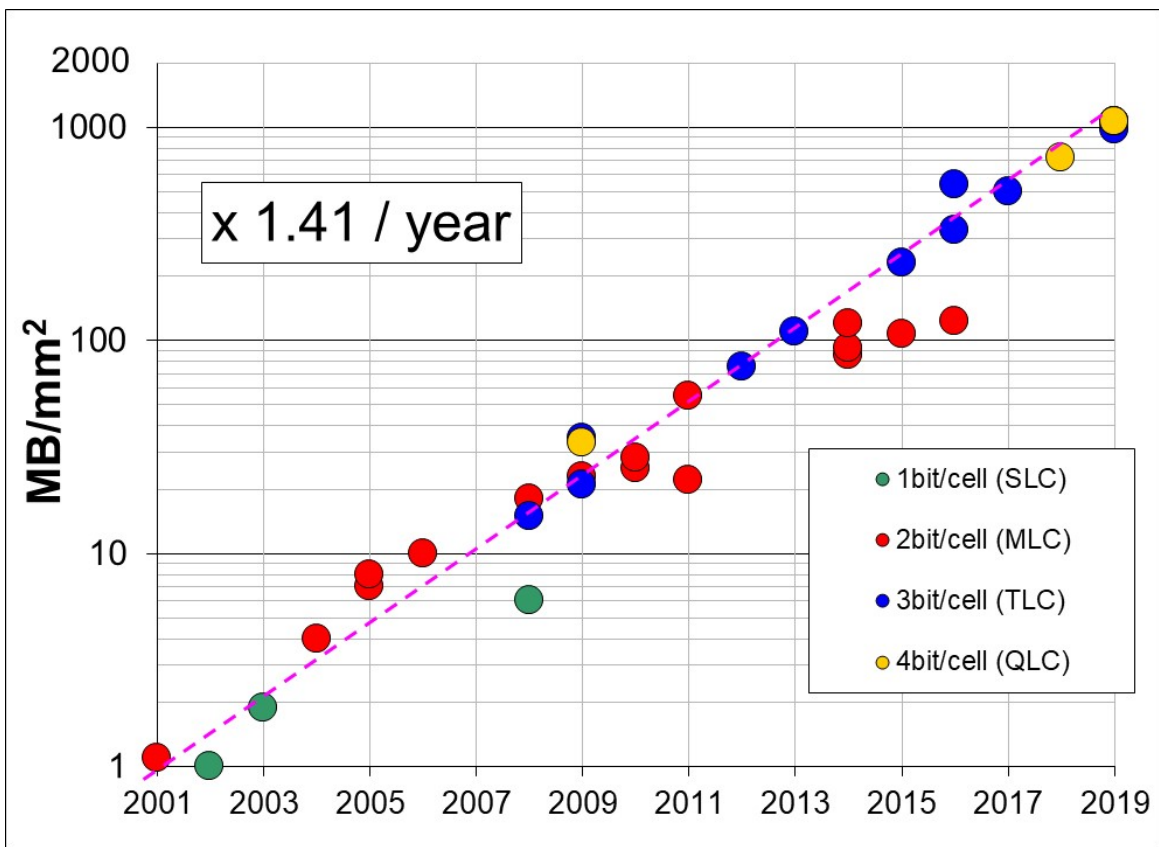


Figure 27 - NAND Flash memory trends

HISTORICAL TRENDS IN TECHNICAL THEMES

INNOVATIVE TOPICS

IMAGERS/MEMS/MEDICAL/DISPLAYS SUBCOMMITTEE

TECHNOLOGY DIRECTIONS SUBCOMMITTEE

IMMD – 2019 Trends (Medical)

Subcommittee Chair: Chris Van Hoof, IMEC, Leuven, Belgium

As illustrated at ISSCC 2019, both sensor and actuator systems for on-body wearable and in-body implantable usage continue to evolve toward more robust and energy-efficient operation, as well as closed-loop operation. Wearable and implantable SoCs record weak biopotential signals in the presence of real-life interference and under stringent power and size constraints. These new SoCs and corresponding techniques pave the way toward robust non-invasive devices that involve direct sensing, multi-sensor fusion and implantable closed-loop sensor/actuator systems. These advancements enable multimode physiological recordings from nearly every major organ system.

The state-of-the-art in biomedical integrated circuits and systems has further advanced this year at ISSCC 2019 with miniaturization, higher sensitivity, higher dynamic ranges, and interference mitigation as major trends in both implantable and in vitro diagnostic devices, while continuing to improve power efficiency. Improved sensitivity will enable applications such as cancer biomarker detection, label-free DNA hybridization detection, and in-body imaging. High-dynamic-range sensing systems (>100dB) improve tolerance to interference and motion artifacts, while new techniques are introduced to mitigate noise and large amplitude (>30V) interference. Miniaturization enables minimally invasive implants with low tissue displacement, and simultaneously miniaturized, high channel-count pixels for high throughput diagnostics. Miniaturization combined with a high level of integration enables a minimally invasive system for intracardiac echocardiography.

Multi-modal physiological monitoring and sensor fusion have the potential to offer improved monitoring and diagnosis of a number of chronic conditions. The form factor of a low cost, easy to use, wearable patch will enable continuous monitoring of multiple vital signs, allowing everyone to track and monitor their health outside of the hospital.

IMMD – 2019 Trends (Imagers)

Subcommittee Chair: Chris Van Hoof, IMEC, Leuven, Belgium

The CMOS-image-sensor business remains one of the fastest-growing segments of the semiconductor industry with double-digit CAGR. Image sensors are required components in most mobile devices, which now include multiple front- and rear-facing cameras. The other applications that continue to drive the demand for image sensors include autonomous driving, smart security, wearables, gaming, VR, AR, IoT, and biomedical. 3D-stacked image sensors continue to dominate in performance, since they enable increasing on-chip functionality without detracting from image quality.

At ISSCC 2019, three out of the eight image sensors target low-power optimized designs for always-on imaging and detection. Improvements in architecture and data conversion have continued to drive down power consumption, while providing the necessary image quality and detection for the targeted applications.

We observe continued development of depth sensors to address the emerging applications in VR, AR, and LiDAR for autonomous driving. Two of the eight image sensor papers this year at ISSCC 2019 describe depth-sensing applications. BSI and 3D wafer stacking continue to improve performance. SPADs and vertical avalanche photodiodes (VAPD) are shown to be effective devices for direct time-of-flight measurement.

High dynamic range, global shutter and computational imaging are also delivering image sensor improvements in 2019. As the pixel size reduction in image sensors starts to slow, there appears to be renewed focus in other imaging metrics.

Technology Directions – 2019 Trends

Subcommittee Chair: Makoto Nagata, Kobe University, Kobe, Japan

Technology innovations bring the promise of enabling completely new system functionalities or substantially greater efficiency of existing ones. It is significant that harnessing such innovations for the solution of real-world problems requires thinking about technologies in the context of systems. With a focus on envisioning the future, emerging trends in Technology Directions include quantum engineering, technologies for human interaction and health, and heterogeneous integration.

Quantum engineering: Quantum technologies are emerging as a major research topic touching several disciplines, including computing, sensing, telecommunications, information technology, security, etc. Common to these technologies is the need for managing quantum effects and devices by means of proper engineering. Quantum engineering deals with these requirements and aims at creating designs capable of delivering specific control signals with very challenging properties, often operating at deep-cryogenic temperatures. An example of this trend is the recent effort of developing arrays of CMOS compatible quantum bits, or qubits, the core technology of quantum computers. Qubits are fragile quantum devices that require milli-Kelvin refrigeration and continuous control by means of complex room-temperature instrumentation equipment. Very recently, it has been proposed to develop miniaturized, scalable control electronics operating at temperatures near those of the qubits that would enable not only scalable but also miniaturized systems. Leveraging over 50 years of CMOS technology development, researchers are currently engaged in the creation of cryogenic CMOS (cryo-CMOS) circuits and systems to fill this gap. Cryo-CMOS technologies will not only serve qubits but also a range of quantum devices that can be used in several quantum engineering problems. In this context, quantum engineering is expected to evolve in the future bringing significant innovation in many domains of human activity. ISSCC 2019 will feature a full session devoted to some of these topics, including a cryo-CMOS controller for superconductive qubits and an integrated system for the control and readout of a Nitrogen Vacancy (NV) center in diamond.

Technologies for human interaction and health: In the recent past, humans have had to turn away from their natural activities to interact with electronic devices. Now, we are seeing a clear shift towards electronics that more seamlessly integrate and participate in our lives and natural activities. This trend has been enabled by a confluence of emerging sensors, low-power computing and communication technologies, and efficient algorithms for perception and detection of information from embedded signals. The result is advances in form factor and integration of devices, processing of new kinds of relevant signals, and continued increase in energy efficiency. The role of electronics in health and wellness has been well recognized and represented at ISSCC. This continues especially with a focus on signals that can be acquired non-invasively and by users themselves. In the past, sensing such signals has relied on materials and technologies that are disparate from standard silicon CMOS, limiting accessibility and, therefore, the feasible applications. To enable ubiquitous access and exploitation of such signals much more broadly, we are now seeing a strong focus on leveraging sensors that can be monolithically integrated on chip. The various restrictions and limitations these introduce are being overcome by innovations in the readout architectures, fusion of multiple signal modalities, and the use of specialized algorithms. Beyond the urgent need for addressing health, systems are also emerging to make electronic devices more relevant in our lives. This is highlighted at ISSCC 2019 by human-interactive robots, but also through enabling devices for motion, voice, and tactile sensing. Real-world demonstrations of these devices will foster further innovations in algorithms, actuating a virtuous cycle of further technology refinements and advancements, as evidenced by the papers presented.

Heterogeneous integration: We are now firmly in an era of accelerated more-than-Moore innovation. In addition to opening new uses for silicon CMOS itself, this is also driving system-level innovations and advances in alternate technologies. Such technologies are enabling transformations in sensing, low-power operation, power management, and reference generation. Most notably, this is represented by innovative architectures and aggressive integration solutions that boldly enable heterogeneous integration on a large scale. Though driven by the applications of today, the reduction in cost and accompanying increase in accessibility, is clearly driving new applications. While the technologies at play are highly diverse, various alignment of challenges and design approaches are emerging, suggesting the potential for greater generalization of solutions and foundational design principles in the future. At ISSCC 2019, such efforts are highlighted by a single-chip optical phased array in a 3D integrated silicon photonics/CMOS technology, a self-healing technique for analog carbon-nanotube circuits, and a short-circuit detecting circuit implemented using IGZO thin-film transistors on top of a CMOS battery protection chip.

ISSCC 2019 will feature three sessions representing the latest technological innovations in the abovementioned trends.

INDEX

INDEX

A paper number mentioned in this section follows the convention *S.P*, where *S* is the session number and *P* is the paper number. For example 23.2 will be the second paper in the twenty-third session. You can refer back to the TECHNICAL SESSION OVERVIEWS in this Press Kit for additional details on any given paper. Some of the papers will also be available in the “not-so-technical” SESSION HIGHLIGHTS part of this Press Kit. All sessions and papers are in ascending order in both the Session Overviews and the Session Highlights sections of the Press Kit.

Technical Topics Mapped to Papers

Technical Topic	All papers in the following Sessions
Communication Systems <i>includes Wireless, RF, and Wireline Subcommittees</i>	4, 6, 9, 16, 21, 26, 28, 30
Analog Systems <i>includes Analog, Power Management and Data Converter Subcommittees</i>	3, 8, 10, 15, 18, 20, 27
Digital Systems <i>includes Memory, Digital Circuits, and Digital Architectures and Systems Subcommittees</i>	2, 7, 13, 14, 19, 23, 24, 25
Innovative Topics <i>includes Imagers/MEMS/Medical Devices/Displays and Technology Directions Subcommittees</i>	5, 11, 12, 17, 22, 29

Selected Presenting Companies/Institution Mapped to Papers

Chart 4.1

Affiliation	Paper Numbers
*now with KAIST	30.2
*now with K-Motion Interactive	5.3
ams AG	5.5
Analog Devices	8.7, 10.1, 15.4, 15.5, 16.9, 18.2, 27.1
Arizona State University	24.5, 27.5
Asahi Kasei Microdevices	3.7
Boxing Electronics	24.4
Broadcom	16.6
California Institute of Technology	11.5

Carnegie Mellon University	21.3
CEA-LETI-MINATEC	14.3
Colleges of Nanoscale Science and Engineering	29.5
Columbia University	11.5, 16.6, 28.1, 28.5, 28.6
Delft University of Technology	9.3, 10.3, 10.4, 18.3
Dialog Semiconductor	18.6
Elenion Technologies	30.6
e-peas semiconductors	19.6
EPFL	17.8, 30.2
eSilicon Italy	6.3
ETH Zürich	30.2
Fondazione Bruno Kessler	5.5
Fudan University	4.2, 26.4, 27.1, 27.3
Fujitsu America	19.2
Fujitsu Laboratories	6.8
Fujitsu Semiconductor	19.2
Georgia Institute of Technology	4.4, 4.6, 4.8, 4.9, 14.1, 19.3, 21.2, 24.5, 25.2, 25.3
Google	29.1
Hanbat National University	9.8
Heriot-Watt University	5.7
Hiroshima University	9.5
HiSilicon	8.4
Hitachi	2.6, 10.2
Hokkaido University	5.8
Holst Centre/TNO	12.3
Hong Kong University of Science and Technology	30.8
Huawei Technologies	6.2, 30.5
IBM Research	2.1, 6.1
IBM Systems and Technology	2.1
IBM T. J. Watson Research Center	6.6, 30.2
IBM Zurich Research Laboratory	30.2

IHP	4.5
imec	3.1, 3.6, 9.3, 9.4, 12.3, 22.1, 22.5, 26.1
imec - Netherlands	9.3, 22.1, 22.5
Incheon National University	23.3
Indian Institute of Technology Delhi	2.3
Indian Institute of Technology Madras	26.3
Inphi Corporation	6.5
InSilixa	11.2
Instituto Superior Tecnico/University of Lisboa	3.2, 3.5, 16.3, 16.8, 20.5, 20.7, 26.2, 27.3
Intel	2.4, 8.1, 8.5, 9.6, 9.7, 13.2, 13.3, 14.7, 19.5, 21.5, 25.3, 30.4
Intel DMCE	21.7
Johannes Kepler University	21.7
JST/ACCEL	12.1
KAIST	7.4, 7.7, 9.8, 11.1, 17.7, 22.3, 22.4
KIST	11.5
Korea University	23.3
Krembil Neuroscience Center	22.8
KU Leuven	2.2, 3.3, 12.3, 20.1, 22.1, 22.5
Kumoh National Institute of Technology	5.4
Kyushu University	29.3
Leibniz University Hannover	8.6
Massachusetts Institute of Technology	2.3, 29.2, 29.5, 29.8
MaXentric Technologies	22.2
MediaTek	6.4, 9.1, 18.1, 20.2, 20.4, 20.6, 21.4, 30.7
Microelectronic Circuits Centre Ireland	16.9
Nagoya University	29.3
Nanyang Technological University	14.3
National Cheng Kung University	22.7, 27.6
National Chiao Tung University	15.3, 27.8, 29.6

National Institute of Advanced Industrial Science and Technology	29.4
National Institute of Information and Communications Technology	9.5
National Tsing Hua University	7.5, 24.1, 24.5, 25.2
National University of Singapore	11.1, 22.6
NEC	21.1
New York University	11.2
Nokia Bell Labs	3.3
Northeastern University	7.5
Northwestern University	19.4, 19.7
NXP Semiconductors	30.1
Oregon State University	3.7, 28.6
Panasonic	5.6, 9.5
Pennsylvania State University	27.4
Photon Force	29.7
Pohang University of Science and Technology	18.8
Politecnico di Milano	16.7
Princeton University	17.3, 22.8
Qualcomm	19.3
Realtek Semiconductor	15.3, 27.8, 29.6
Renesas Electronics	2.7
Rice University	25.1
Ricoh	29.4
RIKEN	5.8
Robert Bosch	5.3
Samsung Advanced Institute of Technology	7.1
Samsung Electronics	7.1, 13.4, 15.1, 15.2, 21.6, 24.3, 27.7
Samsung Semiconductor	23.1
Semiconductor Energy Laboratory	12.2
Semtech	29.7

Seoul National University	7.6, 27.7
Shanghai Jiao Tong University	22.6
Singapore Institute for Neurotechnology	11.1
SK hynix	23.2, 23.4
Skyworks Solutions	4.4
SmartSens Technology	5.1
Sony	17.1
Sony Semiconductor Solutions	26.1
Southeast University	24.4
Stanford University	5.3, 14.3
STMicroelectronics	5.7, 29.7
Synopsys	5.5
Technische Universität Berlin	4.5
Teletx	6.7
Texas Instruments	8.6, 17.4, 18.5
Tohoku University	12.1
Tokyo Institute of Technology	16.1, 21.1, 29.4
Toronto Western Hospital	22.8
Toshiba	15.8
Toshiba Electronic Devices & Storage	7.2
Toshiba Memory	13.1, 13.5, 30.3
Tsinghua University	7.5, 24.4, 25.2
TSMC	18.7, 24.2
TU Eindhoven	9.3
Ubilinx Technology	16.5
UCLouvain	19.6
Uhnder	9.2
Ulsan National Institute of Science and Technology	16.2, 30.9
University of Texas	3.4
University College Dublin	16.9
University of Alberta	30.4

University of British Columbia	30.6
University of California	11.1, 16.4, 16.5, 16.6, 17.5, 18.4, 28.7, 28.8, 29.1, 29.5
University of California, San Diego	4.7, 8.2, 11.4, 17.6, 22.2, 26.5, 28.2
University of Colorado	8.3
University of Edinburgh	5.7, 29.7
University of Electronic Science and Technology of China	18.2, 24.5
University of Illinois	18.5
University of Macau	3.2, 3.5, 16.3, 16.8, 20.5, 20.7, 26.2, 27.3
University of Massachusetts	29.1
University of Michigan	5.2, 7.3, 14.2, 17.2, 19.2, 20.3, 27.2, 28.3
University of Minnesota	2.5
University of Southampton	28.4
University of Southern California	4.1
University of Texas	3.4, 14.4, 18.2
University of Texas at Dallas	15.6, 15.7
University of Tokyo	12.2
University of Toronto	5.5, 6.8, 22.8, 30.5
University of Ulm	20.5
University of Utah	4.3, 27.4
University of Virginia	14.6
University of Washington	14.5, 19.1, 26.4
Washington State University	8.4
Western Digital	13.1, 13.5
Xidian University	3.4
Yonsei University	5.4, 11.3
Yuan Ze University	6.7
Zhejiang University	28.8

CONTACT INFORMATION

ANALOG

Subcommittee Chair: Kofi Makinwa
Delft University of Technology
+31-15-27-86466
Email: k.a.a.makinwa@tudelft.nl

Press Designates: NA/EU: David Blaauw
FE: Man-Kay Law

DATA CONVERTERS

Subcommittee Chair: Michael Flynn
University of Michigan Ann Arbor
734-936-2966
Email: mpflynn@umich.edu

Press Designates: NA/EU: Yun Chiu
FE: Takashi Oshima

DIGITAL ARCHITECTURES & SYSTEMS

Subcommittee Chair: Byeong-Gyu Nam
Chungnam National University
+82-42-821-6858
Email: bgnam@cnu.ac.kr

Press Designates: NA/EU: Christopher Gonzalez
FE: Wookyeong Jeong

DIGITAL CIRCUITS

Subcommittee Chair: Edith Beigné
CEA-LETI
+33-4-38-78-59-36
Email: edith.beigne@cea.fr

Press Designates: NA/EU: Dennis Sylvester
FE: Koji Hirairi

IMAGERS, MEMS, MEDICAL & DISPLAYS

Subcommittee Chair: Chris Van Hoof
imec
+32-16-281815
Email: chris.vanhoof@imec.be

Press Designates: NA/EU: Rikky Muller
FE: Masayuki Miyamoto

MEMORY

Subcommittee Chair: Jonathan Chang
TSMC
+886-3-5636688 ext 7125890
Email: jon_chang@tsmc.com

Press Designates: NA/EU: Wolfgang Spirk
FE: Donguk Lee

POWER MANAGEMENT

Subcommittee Chair: Yogesh Ramadass
Texas Instruments
669-721-6737
Email: yogesh.ramadass@ti.com

Press Designates: NA/EU: Hoi Lee
FE: Yen-Hsun Hsu

RF

Subcommittee Chair: Piet Wambacq
imec
+32-16-281-218
Email: wambacq@imec.be

Press Designates: NA/EU: John Long
FE: Kohei Onizuka

Technology Directions

Subcommittee Chair: Makoto Nagata
Kobe University
+81-78-803-6569
Email: nagata@cs.kobe-u.ac.jp

Press Designates: NA/EU: Shahriar Mirabbasi
FE: Pui-In Mak

Wireless

Subcommittee Chair: Stefano Pellerano
Intel
503-712-4576
Email: stefano.pellerano@intel.com

Press Designates: NA/EU: Arun Natarajan
FE: Ken Yamamoto

Wireline

Subcommittee Chair: Frank O'Mahony
Intel
503-613-1467
Email: frank.omahony@intel.com

Press Designates: NA/EU: Bo Zhang
FE: Jaeha Kim

Program Chair, ISSCC 2019

Eugenio Cantatore
Eindhoven University of
Technology

Work Phone: +31-40-247-3388
Email: E.Cantatore@tue.nl

Program Vice-Chair, ISSCC 2019

Un-Ku Moon
Oregon State University

Work Phone: 541-737-2051
Email: moon@eecs.oregonstate.edu

Press Coordinator

Denis Daly
Omni Design Technologies

Email: denis.daly+isscc@gmail.com

Press-Relations Liaison

Kenneth C. Smith
University of Toronto

Work Phone: 416-418-3034
Email: lcfujino@aol.com



Editor-in-Chief: Denis Daly

Editor-at-Large: Kenneth C (KC) Smith

Publisher: Laura Chizuko Fujino

