INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS

ISSCC®

UNIVERSITY OF PENNSYLVANIA

2016

PRESS KIT

ISSCC Press Kit Disclaimer
The material presented here is preliminary.
As of November 5, 2015, there is not enough information to guarantee its correctness.
Thus, it must be used with some caution.

ISSCC VISION STATEMENT

The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and use to maintain technical currency, and to network with leading experts.

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1. PREAMBLE

1.1 FAQ on ISSCC

What is ISSCC?

ISSCC (International Solid-State Circuits Conference) is the **flagship** conference of the IEEE Solid-State Circuits Society. According to the SIA, the Semiconductor industry generated US$335.8 billion in sales in 2014 and ISSCC continues to be the premier technical forum for presenting advances in solid-state circuits and systems.

Who Attends ISSCC?

Attendance at ISSCC 2016 is expected to be around **3000**. Corporate attendees from the semiconductor and system industries typically represent around **60%**.

Where is ISSCC?

The **63rd ISSCC** will be held at the San Francisco Marriott Marquis on January 31st through February 4th 2016.

Are there Keynote Speakers?

After a day devoted to educational events, ISSCC 2016 begins formally on Monday, February 1, 2016 with four exciting plenary talks:

- William Holt, Executive Vice President, Intel, USA
- Sophie V. Vanderbroek, Chief Technology Officer, Xerox, USA
- Seizo Onoe, Executive Vice President, NTT DoCoMo, Japan
- Lars Reger, CTO Automotive, NXP Semiconductors, Germany

What is the Technical Coverage at ISSCC?

ISSCC covers a full spectrum of design approaches in advanced technical areas broadly categorized as: (1) Communication Systems, (2) Analog Systems, (3) Digital Systems, and (4) Innovations including micro-machines and MEMS, imagers, sensors, biomedical devices, as well as forward-looking developments that may take three or more years for commercialization.

How are ISSCC Papers Selected?

Currently around 600 submissions are received each year across the broad spectrum of specified topics. Review is by a team of over 150 scientific and industry experts from the Far-East, Europe, and North America. These experts are organized into 10 Sub-Committees that cover the 4 broad areas described earlier:

- **Communication Systems** includes Wireless, RF, and Wireline Subcommittees
- **Analog Systems** includes Analog and Data Converter Subcommittees
- **Digital Systems** includes Memory, Digital Circuits, and Digital Architectures and Systems Subcommittees
- **Innovative Topics** includes Imagers/MEMS/Medical Devices/Displays and Technology Directions Subcommittees

What Companies are Presenting this year?

Companies presenting papers at ISSCC 2016 include AMD, Broadcom, IBM, Intel, Marvell, MediaTek, Panasonic, Samsung, and Toshiba, just to name a few. A more complete list can be found in the Index.

Are there educational sessions?

ISSCC features a variety of educational events which include:

- Ten Tutorials (targeted toward participants looking to broaden their horizon)
- Six Forums (targeted toward experts in an information sharing context)
- One Short Course (targeted toward in-depth appreciation of a current hot topic)

Are There Other Events?

A more complete list of all activities at ISSCC 2016:

- Four Plenary Presentations
- One Invited Talk on System Issues
- Technical Sessions (28 distinct sessions)
- Five Evening Sessions and Panels
- Educational Sessions Featuring:
    - Ten Tutorials
    - Six Forums
    - One Short Course
- Student Research Preview (for the introduction of graduate-student research-in-progress)
- Demonstration Sessions from Academia and Industry
- Networking Social Events
- Author Interview Sessions
- Women's Networking Luncheon
- A Number of University Alumni Events
- Book Display

How Do I Use this Press Kit?

The Press Kit provides a PREAMBLE section that features this FAQ and other general information. The kit also includes TECHNICAL OVERVIEWS of all 27 technical sessions into which the 202 papers are grouped, together with brief descriptions and context for each. As well, there is an abstract for each of the Plenary talks. For your convenience, the Kit includes two structural charts in the INDEX section: (a) a list of the 4 Technical Topics and their associated Subcommittees (10) and Sessions (27); (b) a list of contributing companies and institutions with their associated papers. Thus, to located information of interest you can access chart 4.1 to identify sessions of interest, after which you might logically access its Session's Overivew or Highlight section. Alternatively, if your interest is in particular organization then Chart 4.1 will direct you immediately to papers of interest each of which is detailed in its corresponding Session Overview and possibly in the Highlights section. For anyone's interest it is useful to use Chart 4.1 to access the appropriate Trend information which provides a broad historical view of the context of your interest and often includes reference to current ISSCC 2016 papers.

Anything New This Year?

Yes! This year, for the first time in decades, we have an invited talk which will expand on the idea of system-motivated technology, and is embedded in an appropriate regular session [22.1].

1.2 OVERVIEW; ISSCC 2016 – Silicon Systems for the Internet of Everything

The way we access the Internet has changed dramatically over the past few years, transitioning from desktops to mobile tablets and smartphones, thereby greatly impacting our society and our lifestyle. Now, the Internet is expanding again — coming to all of the everyday devices found in our homes, businesses, cities, and vehicles, heralding the age of the "Internet of Everything (IoE)".

The Internet of Everything is predicted to transform the future, proliferating networks of intelligent devices driving the development of fundamental new products and services. At its heart, this transformation employs silicon sensors, silicon chips, silicon systems and communication networks which unite to convert everyday objects into intelligent and interactive devices.

1.3 PLENARY SESSION (Session 1)

The Plenary Session on the morning of Monday, February 1, 2016, will feature four renowned speakers:

- William Holt, Executive Vice President, Intel, USA, will give his insights into "Moore's Law: A Path Forward"
- Sophie V. Vanderbroek, Chief Technology Officer, Xerox, USA, will present the "Three Pillars Enabling the Internet of Everything: Smart Everyday Objects, Information-Centric Networks, and Automated Real-Time Insights.
- Seizo Onoe, Executive Vice President, NTT DoCoMo, Japan, will explore "5G Mobile Technology Evolution Towards 2020 and Beyond".
- Lars Reger, CTO Automotive, NXP Semiconductors, Germany, will discuss "The Road Ahead for Securely Connected Cars".

Highlights of these Plenary talks are provided in Section 4.

ISSCC 2016
SESSION OVERVIEWS

CONDITIONS OF PUBLICATION

PREAMBLE

The Session Overviews to follow serve to capture the context, highlights, and potential impact, of the papers to be presented in each Session at ISSCC 2016 in January in San Francisco

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FOOTNOTE

- From ISSCC's point of view, the phraseology included in the box below captures what we at ISSCC would like your readership to know about this, the 63rd appearance of ISSCC, on January 31st to February the 4th, 2016, in San Francisco.

This and other related topics will be discussed at length at ISSCC 2016, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on January 31 - February 4, 2016, at the San Francisco Marriott Marquis Hotel.

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Session 2 Overview: *RF Frequency Synthesis Techniques*

RF SUBCOMMITTEE

Session Chair: *Ahmad Mirzaei, Broadcom, CA*
Session Co-Chair: *Hyunchol Shin, Kwangwoon University, Seoul, Korea*

Subcommittee Chair: *Piet Wambacq, imec, Belgium, RF Subcommittee*

Frequency generation and synthesis circuits are ubiquitous building blocks in communication, sensing, and imaging systems. This session covers the latest advances in frequency synthesizers and VCOs in GHz and THz frequency ranges. The session begins with a CMOS frequency synthesizer operating above 0.5THz and a 28GHz coupled PLL for mm-Wave 5G applications. The session also presents two GHz-range PLLs, which include a PLL-DLL cascaded structure operating over a wide bandwidth and achieving low phase noise and a high-performance BiCMOS fractional-N synthesizer for backhaul applications. Two VCOs are presented next. The first VCO is a low-power complementary VCO with a low flicker noise corner. This is followed by a 190GHz VCO with very wide tuning range and a time-interleaved ring VCO with a low $1/f^3$ noise corner. The last two papers describe an injection-locked frequency-locked loop with a self-calibrated locking algorithm and a 2GHz 244fs-resolution digital-to-time converter.

- In Paper 2.1, UCLA, JPL and TSMC present the first integrated synthesizer realized in silicon IC operating above 0.5THz. The 65nm CMOS 0.56THz frequency synthesizer has a 21GHz locking range and -74dBc/Hz phase noise at 1MHz offset.

- In Paper 2.2, Oregon State University presents a 65nm CMOS scalable 28GHz coupled PLL with single-wire synchronization for large-scale 5G mm-Wave arrays.

- In Paper 2.3, HKUST presents a 2.1GHz PLL in 65nm CMOS employing a Type-II PLL cascaded with a time-amplified clock-skew sub-sampling DLL to achieve a 40-MHz-bandwidth and 3rd-order phase-noise rejection of VCO phase noise without degrading stability and bandwidth.

- In Paper 2.4, STMicroelectronics presents a 2-to-16GHz BiCMOS ΔΣ fractional-N PLL synthesizer with integrated VCOs and frequency doubler for wireless backhaul applications.

- In Paper 2.5, Broadcom presents a 4.7-to-5.4GHz complementary VCO with 195 dBc/Hz FoM and the flicker noise corner of 200kHz, which is suitable for ultra-low-power IoE applications.

- In Paper 2.6, University of California, Davis, describes a 190.5 GHz mode-switching VCO with a 20.7% continuous tuning-range and the maximum power of -2.1dBm in 0.13μm BiCMOS.

- In Paper 2.7, University of Macau, University of Pavia and Instituto Superior Tecnico present a 1.7-to-3.5GHz dual-mode time-interleaved ring-VCO that achieves 90-to-150kHz $1/f^3$ phase noise corner

- In Paper 2.8, Virginia Tech presents a mixed-mode injection frequency-locked loop with a self-calibration of injection locking range and phase noise in 0.13μm CMOS.

- In Paper 2.9, Intel and Technical University of Munich present a 2GHz, 244fs resolution, 1.2ps peak INL edge-interpolator-based digital-to-time converter in 28nm CMOS.

Session 3 Overview: *Ultra-High-Speed Wireline Transceivers and Energy-Efficient Links*

WIRELINE SUBCOMMITTEE

Session Chair: *Hyeon-Min Bae, KAIST, Daejeon, KOREA*
Session Co-Chair: *Ajith Amerasekera, Texas Instruments, Dallas, TX*

Subcommittee Chair: *Daniel Friedman, IBM, Yorktown Heights, NY, Wireline Subcommittee*

Smart phones and their social apps are key drivers for the growth of the internet and, more generally, of big data infrastructure. The ever-increasing demands placed on this infrastructure, in turn, spurs the insatiable need for data communication bandwidth between chips. In this context, wireline transceivers that push the limits imposed by process technology – in terms of data rate, energy efficiency, and area – are extremely critical. This session introduces 2 ADC-based receivers operating at or beyond 25Gb/s for multi-standard support. It continues with a presentation of a 25Gb/s equalizer for cable-dominated channels with up to 50dB of half-baud loss. Two papers addressing different approaches for high-data-rate, short-reach communication are presented next, including an NRZ/PAM-4 Ethernet ADC-based transceiver and a 56Gb/s per lane NRZ transceiver. Finally, the session concludes with two papers describing critical components for I/O solutions at per-lane rates at or beyond 45Gb/s, including a power-efficient 45Gb/s PAM-4 transmitter and a 64Gb/s NRZ transmitter for CDE-56-VSR/MR applications, the latter implemented in 16nm finFET.

- In Paper 3.1, IBM presents a 25Gb/s ADC-based serial line receiver in 32nm CMOS SOI. The receiver uses a ¼ rate 5b flash ADC with on-chip calibration followed by an interleaved 8-tap FFE and 8-tap DFE backend and digital CDR. The transceiver occupies 0.39mm^2 and compensates a reflective 40dB loss channel while consuming 453mW.

- In Paper 3.2, Broadcom presents a 32Gb/s 8b ADC-based PAM-4 receiver in 28nm CMOS. The ADC achieves an ENOB of 6.4 and 5.85 at DC and Nyquist, respectively. The entire receiver, occupying 0.89mm^2, features a continuous-time linear equalizer with a 7dB peaking gain, and compensates for channel loss of more than 50dB at 16GHz while consuming 320mW.

- In Paper 3.3, Hitachi presents a 25Gb/s multi-standard serial link transceiver in 28nm CMOS. The receiver, using a 20dB CTLE and a 14-tap DFE, achieves 3mV input sensitivity by using sub-mV dynamic DC-offset cancellation and DFE tap-bias control schemes. The transceiver, occupying 5.5x4.6mm^2, achieves BER < 10^{-12} over a 51dB-loss 5m AWG channel at 25Gb/s and consumes 403mW from 0.9 and 1.5V power supplies.

- In Paper 3.4, Inphi describes a 40/50/100Gb/s NRZ/PAM-4 Ethernet transceiver in 28nm CMOS. The receiver integrates two SAR ADCs with ENOB of 4.8, a DSP for calibration, and an FEC encoder. The transmitter includes a FEC decoder and supports both NRZ and PAM-4 signaling with a maximum swing of 1.4Vpp. The transceiver, which includes an internal supply voltage regulator, occupies 6.3x4.9mm^2 and achieves less than 200fs output jitter while consuming 2.4W from 0.9V and 1.2V power supplies.

- In Paper 3.5, Fujitsu presents a 56Gb/s/lane electrical NRZ transceiver in 28nm CMOS for high-data-rate applications, using baud-rate sampling to minimize the power consumption. The design features a 2-tap feed-forward equalizer and a continuous-time linear equalizer, followed by a 1-tap speculative decision-feedback equalizer. The receiver compensates for 18.4dB half-baud loss. The transceiver occupies 1.4mm^2 per two lanes and consumes 247mW/lane from a 0.96V supply.

- In Paper 3.6, researchers from the University of Pavia present a 45Gb/s PAM-4 transmitter able to deliver 1.3Vppd output swing; the design is implemented in 28nm fully-depleted SOI CMOS and is intended to address next generation CEI-56G standards for high speed links. The design occupies an area of 0.28mm^2 and consumes 120mA from a 1V supply.

- In Paper 3.7, Xilinx presents a 3-tap 64Gb/s NRZ transmitter using a quad-rate architecture for short reach electrical links implemented in a 16nm FinFET technology. The design, which is applicable to next generation standards such as CEI-56-VSR/MR, uses power efficient techniques that take into consideration the 16nm FinFET device properties. The transmitter achieves 800mVppd output swing with 150fs random jitter while consuming 225mW at 64Gb/s and occupying an area of 0.32mm^2.

Session 4 Overview: *Digital Processors*

DIGITAL ARCHITECTURES AND SYSTEMS SUBCOMMITTEE

Session Chair: *Mahesh Mehendale, Texas Instruments, Bangalore, India*
Session Co-Chair: *Luke Shin, Oracle, Santa Clara, CA*

Subcommittee Chair: *Stephen Kosonocky, Advanced Micro Devices, Fort Collins, CO; Digital Architectures and Systems*

Improved performance, battery-life and interactive user-experience continue to drive advances in digital processors for PCs, smartphones, tablets, ultra-light laptops and automobile infotainment systems, as described in the first four papers of this session. The fifth paper describes techniques to meet safety standards for automotive processing. The final two papers address ultra-low power applications, such as sensor node processing and wearables, using special-purpose acceleration hardware and non-volatile memory for zero power standby modes.

- In Paper 4.1, Intel presents its sixth-generation Core processor, a 14nm fully featured SoC, which provides comparable performance for less than 50% power versus a 22nm Ultrabook processor.

- In Paper 4.2, AMD presents a range of system techniques to manage power, thermal, voltage margin, and reliability to increase the effective performance of a 28nm x86-64 microprocessor by 15% within the same process node.

- In Paper 4.3, MediaTek presents industry's first tri-cluster, 10-core CPU, featuring three ARMv8a CPU clusters optimized for 1.4GHz, 2.0GHz, and 2.5GHz operation in a 20nm high-κ metal-gate process. Compared to dual-cluster CPUs, the addition of a third cluster provides 40% higher overall performance with 40% improved power efficiency.

- In Paper 4.4, Renesas presents a 12-channel HD-video-processing SoC, implemented in 16nm FinFET CMOS, with 197mW power consumption and 70ms video latency for automobile infotainment and driver-assistance applications.

- In Paper 4.5, Renesas presents a heterogeneous nine-core SoC complying with the ISO26262 ASIL-B standard for automobile safety, achieving a reliability rate of less than 10^{-7} random hardware failures per hour, in the same 16nm FinFET SoC as described in paper 4.4.

- In Paper 4.6, ETH Zurich presents a 6.4-to-29.2pJ/FLOP (at 0.8V supply) tightly coupled quad-core processor cluster in 65nm CMOS, with a shared-logarithmic floating-point unit for acceleration of nonlinear function kernels.

- In Paper 4.7, Tsinghua University presents the first ReRAM-enabled nonvolatile 100MHz micro-controller in a 65nm CMOS-logic-compatible process, with 20ns restore time and 0.45nJ restore energy.

Session 5 Overview: *Analog Techniques*

ANALOG SUBCOMMITTEE

Session Chair: *Marco Berkhout, NXP Semiconductors, The Netherlands*
Session Co-Chair: *Tim Piessens, ICsense, Belgium*

Subcommittee Chair: *Axel Thomsen, Cirrus Logic, Austin TX, Analog Subcommittee*

Analog technology continues to defy simple categories. This session illustrates the diversity and vigor of modern analog circuitry. The common thread among the various papers is the improvement of energy efficiency for the various applications. Sensor nodes and consumer devices can achieve more battery life and smaller form factors. Entries span the range of operational amplifiers, Class-D audio, sensor front-ends, VGAs, and oscillators. New frontiers of precision, power, and performance are established.

- In Paper 5.1, Texas Instruments presents a chopper-stabilized operational amplifier with 10MHz bandwidth and 4µs large settling up to 0.01%. The amplifier offset is below 3.5µV, with less than 0.07µV/ºC temperature drift for a 6.5nV/ √Hz noise.

- In Paper 5.2, Mediatek presents a 3.1W fully differential Class-D audio amplifier with PWM common-mode control achieving 118dB PSRR and -103.5dB THD+N. The Class-D amplifier shows 108dB peak SNR and 89.5% efficiency with a 4Ω load.

- In Paper 5.3, a 70W/4Ω Class-D audio amplifier is described by Merus Audio and Knowles Corporation. The 1.8/5V BCD device uses five-level modulation and dynamic-switching frequency reduction, achieving a 108dB dynamic range, with a 0.03% THD at 10W/1kHz/4Ω.

- In Paper 5.4, MIT describes a noise-efficient 36nV/√Hz analog front-end for sensors with a Power-Efficiency Figure of 1.5. To reduce power consumption, the input stage is supplied from a 0.2V supply, while a following 0.8V stage provides high gain and signal swing, improving linearity.

- In Paper 5.5, UCLA presents a chopper-stabilized amplifier for neural recording, with 40mV_{pp} linear input range and -74dB harmonic distortion, consuming 2µW of power. The input impedance is boosted to 300MΩ for a signal bandwidth from 1Hz to 5kHz.

- In Paper 5.6, the performance of the cross-coupled pair is investigated for discrete-time linear amplification by the University of Pavia and STMicroelectronics. A test-chip in 0.18µm CMOS provides 15-to-66dB gain over 50MHz bandwidth. A GBW up to 100GHz is demonstrated with only 420µW power dissipation.

- In Paper 5.7, a stacked-amplifier crystal oscillator in 65nm CMOS is proposed by the University of Tokyo. By stacking 4 amplifiers, the supply current is reduced by 91% for a 39.25MHz frequency with a phase noise of -139dBc/Hz at 1kHz offset, achieving an FOM of 278dB.

- In Paper 5.8, the University of Michigan presents a 3kHz, 4.7nW, 13.8 ppm/ºC wake-up timer. The ultra-low power consumption is achieved by employing a switched-resistor scheme, and a switched-capacitor-based DC-DC converter improves the stability of the output frequency while making the power consumption insensitive to temperature.

- In Paper 5.9, Texas Instruments presents a crystal oscillator with a robust fast start-up feature implemented by injecting a dithered oscillation close to the resonance frequency. The start-up time is reduced by a factor of 6 even as the injection frequency drifts over temperature.

- In Paper 5.10, the Institute of Microelectronics of Singapore and Daegu Gyeongbuk Institute of Science and Technology present a 1.4V, 10.5MHz swing-boosted differential relaxation oscillator with 162.1dBc/Hz FOM at 100kHz offset and 157.7dBc/Hz FOM at 1kHz offset. The proposed oscillator achieves 9.86ps_{rms} period jitter.

Session 6 Overview: *Image Sensors*

IMMD SUBCOMMITTEE

Session Chair: *Jun Deguchi, Toshiba, Kawasaki, Japan*
Session Co-Chair: *David Stoppa, Fondazione Bruno Kessler, Trento, Italy*

Subcommittee Chair: *Makoto Ikeda, University of Tokyo, Japan, IMMD*

The session presents advances in image sensors, covering emerging topics like 3D stacking, organic photoconductive film technologies and single-photon detectors as well as new trends in high-resolution cameras. The first two papers integrate organic photoconductive film with a CMOS image sensor to enable wide intrascene dynamic range, global shutter, multiple exposure and variable sensitivity image capture. The next two papers present high-resolution CMOS image sensors for airborne mapping applications and DSLR cameras. Single-photon avalanche photodiodes for long-range time-of-flight and low-light imaging applications are presented in the fifth and sixth papers. Finally, the last three papers report on 3D-stacked CMOS image sensors for mobile and emerging high-end applications.

- In Paper 6.1, Panasonic presents an image sensor based on organic photoconductive film. The sensor features over 120dB intrascene dynamic range, a full well capacity of 600ke^- on 3.3.V pixel power supply and a random noise of 5.4e^-.

- In Paper 6.2, Panasonic proposes a global shutter imager based on organic photoconductive film exploiting in-pixel gain switching featuring 210ke^- saturation in a 3μm-pitch pixel.

- In Paper 6.3, CMOSIS NV presents a 105×65mm^2 391Mpixel CMOS image sensor for airborne mapping applications. The sensor based on 3.9μm-pitch pixels exhibits a 3.7e^- rms noise and 78dB dynamic range.

- In Paper 6.4, Canon presents an APS-H size 250Mpixel CMOS image sensor. The sensor is fabricated with a 0.13μm CMOS technology and is based on 1.5μm-pitch pixels and single-slope column ADCs featuring 6dB wider dynamic range and 75% shorter conversion time than a conventional single-slope ADC.

- In Paper 6.5, Fondazione Bruno Kessler presents a 64×64-pixel Time-of-Flight 3D imager for spacecraft navigation and landing. The sensor achieves a precision of 0.14% up to 6km distance and a background rejection up to 100Mphotons/s/pixel.

- In Paper 6.6, Panasonic proposes a 1280×720-pixel array achieving single-photon detection capability thanks to a modified BSI pinned-photodiode device that can operate as in conventional photodiode and avalanche photodiode modes.

- In Paper 6.7, Toshiba describes a 3D-stacked image sensor for mobile applications exploiting low-noise PGA and low-power single-slope ADC to achieve a temporal noise of 1.2e^- at 20fps and 32× multiple sampling.

- In Paper 6.8, TSMC describes a 33Mpixel 3D-stacked CMOS image sensor demonstrating 82.5% array-area to chip-area ratio and featuring 82.35μV_{rms} noise at unitary gain.

- In Paper 6.9, NHK Science & Technology Research Laboratories present a 33Mpixel 3D-stacked CMOS image sensor based on 12b 3-stage pipelined ADCs featuring 3.6e^- temporal noise at 7.96Gpixel/s.

Session 7 Overview: *Nonvolatile Memory Solutions*

MEMORY SUBCOMMITTEE

Session Chair: *Sungdae Choi, SK hynix, Icheon, Korea*
Session Co-Chair: *Jin-Man Han, Samsung Electronics, Hwaseong, Korea*

Subcommittee Chair: *Leland Chang, IBM, Yorktown Heights, NY, Memory*

Market demand for higher density, higher performance but lower price nonvolatile memory is increasing. This year, NAND Flash memories answer such demand with more evolved 3D technologies such as 48-layer stacking and peripherals under the cell array while PCRAM introduces an MLC-enabling scheme to double its density. Emerging memories contribute to building higher performance and lower power systems by enabling nonvolatile memory blocks.

- In paper 7.1, Samsung introduces the 3rd generation V-NAND Flash memory with 48 stacked WL layers and 3b/cell for 256Gb density. 660us programming time leads to 53.2MB/s write throughput, and on-chip-resistor-referenced ZQ calibration enables robust IO driver strength against PV variations for 1Gb/s I/O speed.

- In paper 7.2, Toshiba presents a 4Mb STT-MRAM-based last level cache (LLC) memory. Power state control with predictive power-off and look-ahead power-on can reduce total energy by 93% compared with conventional SRAM-based LLC in combination with a read–modified–write (r–m–w) scheme.

- In paper 7.3, Macronix presents a resistance drift compensation (RDC) scheme that features an error correcting RDC pulse as a data recovery mechanism. MLC PCM fixed-threshold read raw bit error rates (RBER) are suppressed by over 100X to bring it within ECC capabilities.

- In paper 7.4, National Tsing Hua University presents a 256b-wordlength ReRAM-based nonvolatile TCAM. A 2.5T1R cell and a region-splitter sense amplifier reduce macro area, match-line (ML) parasitic load, and search energy, resulting in a 14× improvement in figure-of-merit (FoM).

- In paper 7.5, Samsung demonstrates continued 2D NAND Flash scaling. A 128Gb density 2b/cell NAND Flash memory is implemented with 14nm technology and achieves 640us programming time, which enables 50MB/s write performance. The proposed first cycle recovery of RE and DQS enables 800Mbps high speed I/O rate.

- In paper 7.6, Renesas presents a 90nm embedded 1T-MONOS flash macro with a read-disturb-free array architecture for automotive applications. The 1T-MONOS cell with adaptable slope pulse control achieves P/E endurance of over 100 million cycles and P/E energy of 0.07mJ/8KB at Tj of 175°C with low implementation cost.

- In paper 7.7, Micron achieves the highest density NAND Flash memory by placing the peripheral circuits under the array. A 768Gb density with 64KB page buffer is realized in 179.2mm^2 die area by stacking the floating-gate WLs vertically and placing the string drivers and page buffers under the array.

Session 8 Overview: *Low-Power Digital Circuits*

DIGITAL CIRCUITS SUBCOMMITTEE

Session Chair: Eric Fluhr, IBM, Austin, TX
Session Co-Chair: Bing Sheu, TSMC, Hsinchu, Taiwan

Subcommittee Chair: Stefan Rusu, TSMC, San Jose, CA, Digital Circuits Subcommittee

Energy efficiency continues to be a key driving force in digital circuits. The 8 papers in this session describe innovative low-power digital design techniques. Contributions include a 3D circuit using an asynchronous network-on-chip, two new design approaches for LDOs, and a technique for monitoring delay degradation to trigger adaptive voltage scaling. In addition, papers describe a fully integrated PMU with switched capacitor DC-DC converter, a balanced charged-recycling bus in a 16nm FinFET process, a Physically Unclonable Function (PUF) for security applications, and an iRazor error detection and correction design approach.

- In Paper 8.1, CEA-LETI describes a homogeneous 3D circuit in 65nm using a 4×4×2 asynchronous Network-on-Chip, fully scalable in a face-to-back configuration, targeting MIMO telecom applications. It uses robust self-adaptive asynchronous 3D links, which integrate ESD protection and an extendible test and fault-tolerant architecture. Compared to previous 3D-stacked circuits, it achieves the lowest energy consumption on 3D I/O power supply at 0.32pJ/b, and the highest data rate at 326Mb/s.
- In Paper 8.2, Columbia University presents a design approach to break the trade-off between electrical passive component size and efficiency of LDO design by introducing an event-driven control scheme which allows short latency at low power dissipation. Measured data shows this 400µA class event-driven LDO at typical V_{IN}=0.5V and V_{OUT}=0.45V in a 65nm node, achieving high-performance controllability with the integrated Cout of 0.4nF and providing peak current efficiency of 96.3%.
- In Paper 8.3, Samsung presents an LDO with two loops for precision output, which are a coarse loop using a current-mirror flash ADC and a fine loop using shift registers. The proposed LDO provides up to 200mA of load current and occupies an area of 0.021mm^2 in 28nm. The output voltage droop is about 120mV for load variation of 90% of the maximum supported current load.
- In Paper 8.4, Intel presents a 22nm graphics execution core that uses an in-situ Tunable Replica Circuit (TRC) to monitor delay degradation due to slow variations in temperature and aging, which triggers Adaptive Voltage Scaling (AVS) to dynamically adjust the supply voltage, as needed during run-time. Measured data shows a 35% [14%] energy reduction under worst-case temperature and aging at 0.4V [0.8V]. The TRC is also used in a dynamic power gating (DPG) scheme to lower energy overhead by 14.5% [7%] at 0.8V [0.6V] via relaxed fast-droop voltage guard-band.
- In Paper 8.5, the University of Michigan presents a fully integrated PMU with switched-capacitor DC-DC converter that converts an input voltage with a 0.9-to-3.8V range to 3 fixed output voltages: 0.6V, 1.2V, and 3.3V. It maintains ~60% efficiency over a wide input voltage and output power range from 1V to 3.8V, and from 10nW to 500µW. The converter is built in 180nm technology.
- In Paper 8.6, Nvidia presents a single-ended, balanced charge-recycling bus using stacked CMOS inverters that approaches theoretical quadratic power reduction, without requiring a voltage regulator to compensate for mismatches in data activity. Measured data shows 11.7-23.3fJ/b/mm for random data at 2.6Gb/s/wire over a repeater bus, varying in length from 6-12mm, in 16nm FinFET CMOS at 0.8V. Interleaved bidirectional wires mitigate crosstalk enabling simultaneous signaling as if every wire is shielded on both sides.
- In Paper 8.7, Samsung presents a Physically Unclonable Function (PUF) for security applications, with a unique key generation based on intrinsic properties of every chip. The design approach generates reliable PUF cryptographic keys with an error rate as low as 2E-38. This architecture is built on a PUF cell with size 3.78µm×1.4µm^2 and has been verified in a mass-production 45nm node for smart-card chips.
- In Paper 8.8, the University of Michigan presents iRazor, an error detection and correction design approach that uses a lightweight current-based detector. Only three additional transistors are needed per storage element, yielding 4.3% area overhead over a standard D-type flip-flop. iRazor is implemented in an ARM Cortex-R4 microprocessor in 40nm to demonstrate automated insertion in a large processor. At the typical corner, the proposed design achieves 1.3× throughput gain and 45% energy reduction with 13.6% area overhead relative to a baseline design.

Session 9 Overview: *High-Performance Wireless*

WIRELESS SUBCOMMITTEE

Session Chair: Ali Afsahi, Broadcom, San Diego, US
Session Co-Chair: Guang-Kaai Dehng, MediaTek, Taiwan

Subcommittee Chair: *Aarno Pärssinen, University of Oulu, Oulu, Finland, Wireless Subcommittee*

This session describes state-of-the-art wireless systems and building blocks implemented in low-cost, deep-submicron CMOS processes to support a wide range of applications. This session includes a 45nm multimode cellular base station transceiver SoC, a highly integrated 28nm WLAN/BT combo SoC, a compact 40nm WLAN digital transmitter, a high performance 28nm fractional-N sampling PLL with an FOM of -246.8dB, a 28nm 10Mb/s GMSK modulator and three advanced receiver techniques including digital beamforming with spatio-spectral-filtering, a frequency-translational quadrature-hybrid receiver, and an N-path-filter-based non-reciprocal circulator.

- In Paper 9.1, Texas Instruments presents a 45nm CMOS, 400MHz-to-4GHz, 3GPP TDD & FDD, RF-to-SerDes base-station transceiver SoC with two 100MHz BW receivers, two 200MHz BW transmitters, and an auxiliary, 200MHz BW observation receiver used for digital PA pre-distortion. At 2.7GHz, the SoC consumes 5W/6.5W in TDD/FDD modes at maximum TX/RX/FBRX bandwidths, 40Gb/s SerDes I/O rate and +12dBm TX RF P_{out}.
- In Paper 9.2, Columbia University and Oregon State University present a scalable spatio-spectral-filtering which enables digital beamforming in a 4-element multi-in-multi-out (MIMO) receiver array. A spatial notch suppression of 34dB, in-band OIP3 of +34dBm in the notch direction and an equivalent single-element NF of 2.4 to 3.4dB are achieved. A wireless imaging demo showcases the combination of the RF/analog spatial notch rejection and digital multi-beamforming capability.
- In Paper 9.3, Columbia University presents a 65nm wideband concurrent frequency-translational quadrature-hybrid receiver that achieves wideband input matching for a reflective LNTA impedance. Inter-band carrier aggregation is realized from a single antenna through RF signal-sharing and hybrid-coupler daisy-chaining. It achieves a sub-1dB minimum NF, 12MHz-to-70MHz RF bandwidth, +8dBm IIP3, -15dBm IP_{1dB} and <2.8% EVM.
- In Paper 9.4, Marvell presents a 28nm 2×2 MIMO 802.11abgn WLAN and Bluetooth combo SoC with integrated T/R and WLAN/BT SP3T switches. The WLAN transmitter uses a digital power amplifier that achieves +21.3/+20.5dBm output power with 19.5%/19% efficiency from a 2.2V supply for the 2G and 5G bands respectively. A 2× carrier frequency plan with pulling cancellation is used in the Bluetooth transmitter.
- In Paper 9.5, MediaTek presents a 40nm dual-band digital transmitter supporting WiFi 802.11 a/b/g/n using a digital-OR function to combine I and Q digital signals, which cuts the PA core size by half for the same output power. The resulting diamond-shaped profile shows smaller die area and better PA efficiency. The TX achieves an MCS7 HT40 output power of 18.6dBm/17.8dBm for 2.4GHz/5.5GHz bands with 3dB margin on the IEEE emission-mask requirement. The entire digital PA core efficiency exceeds 14% for both bands.
- In Paper 9.6, Marvell presents a 28nm 2.7-to-4.33GHz CMOS digital fractional-N sampling PLL with a 0.7ps-resolution sampling TDC. A counter-based coarse TDC helps to extend the high-resolution TDC's linear detection range. A multimodulus divider on the feedback path defines frac-N operation while a DTC on the reference path cancels quantization noise to relax the TDC's linear range requirement. It achieves 0.16ps rms jitter (10kHz to 40MHz) while consuming 8.2mW, leading to an FOM of -246.8dB for fractional-N PLLs.
- In Paper 9.7, imec and Vrije Universiteit Brussel present a 28nm two-point phase modulator that makes use of an analog, fractional-N, digital-to-time-converter-based subsampling PLL with -246.6dB FOM, that achieves -37.4 dB EVM around a 10.24GHz fractional carrier during 10Mb/s GMSK modulation. The gain errors and nonlinearities in the digital-to-modulated phase conversion are automatically background calibrated and result in 15.6dB fractional spur suppression and ≈4dB EVM improvement during modulation.
- In Paper 9.8, Columbia University presents a full-duplex (FD) receiver with an integrated magnetic-free N-path-filter-based circulator and analog baseband self-interference (SI) cancellation that (1) enables a compact FD radio with an integrated shared-antenna interface, and (2) achieves 42dB on-chip SI suppression across antenna and analog domains over a 12MHz signal BW. In conjunction with digital cancellation of SI and its IM3 distortion, nearly 80dB SI suppression is demonstrated, enabling an FD link budget of -7dBm TX average output power and -86dBm noise floor.

Session 10 Overview:
Advanced Wireline Transceivers and PLLs
WIRELINE SUBCOMMITTEE

Session Chair: *Jaeha Kim, Seoul National University, Seoul, Korea*
Session Co-Chair: *Roberto Nonis, Infineon, Austria*

Subcommittee Chair: *Daniel Friedman, IBM, Yorktown Heights, NY, Wireline*

The era of Internet of Everything and Big Data drives a never-ending evolution of high-speed interfaces towards ever-higher levels of performance. Beyond the need for speed and energy efficiency, the growing variety of deployments, such as in mobile devices and in automobiles, pose new challenges to the wireline transceiver and PLL/CDR designs, including improving immunity to noise and interference and responding quickly to user commands. This session hosts a series of transceiver and clocking techniques to address these emerging challenges. The session's first two papers present coding and modulation techniques for improving the resiliency of memory channels to noise and reflection, respectively. The third paper presents clamping and filtering circuits for tolerating over-voltage stress and suppressing EMI emissions for emerging automotive interconnect applications. The session's last five papers present advances in clock synthesis, including a new spur cancellation approach, injection-locked oscillators that can instantly turn on and off with the ability to continuously compensate PVT variations and frequency drifts, and the demonstration of an LC-oscillator-based PLL with a wide, seamless tuning range.

- In Paper 10.1, Kandou Bus presents a 25Gb/s forwarded clock CNRZ-5-coded transceiver transmitting 125Gbps over 6 wires. The transceiver, implemented in 28nm CMOS technology, achieves a power efficiency of 0.88pJ/bit across a 12mm short-reach MCM channel.
- In Paper 10.2, University of California, Los Angeles, presents a 40Gb/s 4-lane tri-band transceiver in 28nm CMOS for high-speed memory interfaces. Using PAM-4 at baseband and 16-QAM at 3 and 6GHz passbands, the transceiver achieves the aggregate data rate of 40Gb/s and link energy efficiency of 0.95pJ/bit.
- In Paper 10.3, Broadcom presents an analog front-end for 100BASE-T1-compliant automotive Ethernet in 28nm CMOS. With the focus on meeting stringent electromagnetic compatibility (EMC) requirements, the AFE supports 4.4Vppd full-duplex voltage swing without over-voltage stress and tolerates over 150mApp common-mode current injected to the I/O pins.
- In Paper 10.4, Sony presents a 12Gb/s, injection-locked-oscillator-type CDR with a capture range of -25% to +15% at a power dissipation of 11mW. The CDR is equipped with a robust phase/frequency detection algorithm that both adjusts the phase of the oscillator and also continuously calibrates its free-running frequency, all without an external reference.
- In Paper 10.5, the University of Southern California presents a 3-5GHz fractional-N digital PLL with feedforward multi-tone spur cancellation implemented in 65nm CMOS. The proposed cancellation scheme suppresses both internally and externally generated multi-tone spurs in harmonic or nonharmonic relationship to each other. The DPLL achieves a worst case fractional spur of -73.66 to -117dBc over different fractional frequency settings, and achieves external spur reduction of 15 to 35dB.
- In paper 10.6, University of Illinois presents an LC-based rapid on/off fractional-N injection-locked clock multiplier in 65nm CMOS. The proposed PLL generates an output clock in the range of 6.75 to 8.25GHz using a 125MHz reference clock and achieves the best-reported FoM in both integer-N (-255dB) and fractional-N (-247dB) modes. The power-on lock time is less than 4ns.
- In Paper 10.7, Ulsan National Institute of Science and Technology presents a PVT-robust, low-jitter ring-VCO-based injection-locked clock multiplier with a continuous frequency-tuning loop implemented using a single replica-delay cell. The design achieves RMS jitter of 185fs, with jitter degradation of less than 7% over temperatures and supply voltage.
- In Paper 10.8, IBM Research presents a hybrid fractional-N PLL in 32nm SOI CMOS. The PLL includes a pair of LC D/VCOs and enables seamless frequency sweep across their tuning ranges of 17.3 to 26.4GHz, and 12.2 to 18.4GHz, respectively. The measured phase noise is -124dBc @10MHz offset at 22.1GHz. The design includes a chirp generating state machine such that 18 to 26GHz chirps can be generated from a fixed reference clock (133MHz).

Session 11 Overview: *Sensors and Displays*

IMMD SUBCOMMITTEE

Session Chair: *Yong Ping Xu, National University of Singapore, Singapore*
Session Co-Chair: *Joseph Shor, Bar Ilan University, Tel Mond, Israel*

Subcommittee Chair: *Makoto Ikeda, The University of Tokyo, Tokyo, Japan, IMMD*

This session exhibits recent advances in the state of the art of physical sensors and displays. A novel 3D sensor features dermal and sub-dermal imaging, which makes it robust, tamper-proof, and resistant to surface contamination. This will enhance security of personal identification and mobile devices. Three sensor papers report the smallest and most accurate real-time clocks (RTC), as well as the world's smallest integrated sensor for processor monitoring. The highest-bandwidth magnetic sensor for contactless current sensing is reported, which is 10× higher in bandwidth without lowering performance. A 100-TRX-channel analog front-end (AFE) for a touch controller is featured with a 20× improvement in noise immunity and object sizes of 1 to 30nm. A load-insensitive pre-emphasis column driver for large-size and high-resolution flat-panel displays is reported. Also featured is a hybrid CMOS/Si-Photonic LIDAR (light detection and ranging) with 8μm depth precision at 5cm target distance.

- In Paper 11.1, SiTime, UCLA, and University of Texas present a dual-MEMS resonator temperature sensor that digitizes the two oscillator frequencies using a high-resolution temperature-to-digital converter. It improves the best-reported resolution FOM by 5× and achieves a resolution of 40μK over a 130Hz BW, which enables a TCXO with ±0.1ppm stability over the temperature range of -40 to 85°C.
- In Paper 11.2, the University of California at Berkeley, the University of California at Davis, and Invensense present a 3D ultrasonic fingerprint sensor consisting of a 110×56 PMUT array bonded to a CMOS chip. The sensor consumes 280μJ to record a 431×582 dpi image in 2.64ms. Its unique ability to image both the surface epidermis and sub-surface dermis fingerprint make it insensitive to perspiration and resistant to spoofing.
- In Paper 11.3, Delft University of Technology presents a hybrid magnetic field sensor that extends the state of the art in bandwidth by nearly 10× to 3MHz, without compromising offset and resolution. This technology is useful in high-voltage, high-current, contactless current sensing.
- In Paper 11.4, Delft University of Technology presents the world's smallest integrated thermal sensor utilizing Si thermal diffusivity (TD) sensing in 40nm technology. The sensors achieve an untrimmed inaccuracy of ±1.4°C(3σ) from -40 to 125°C, and to ±0.5°C after one-point trim and phase calibration, making it the most accurate compact sensor for processor hot-spot monitoring.
- In Paper 11.5, CSEM and Micro Crystal present a compact temperature-compensated real-time clock module. Consuming 4× less power than the prior art, it achieves a typical accuracy of ±1ppm at 1Hz over the industrial temperature range.
- In Paper 11.6, Seoul National University presents a 100-TRX-channel analog front-end (AFE) of a touch controller that achieves up to $20V_{pp}$ noise immunity to external noise injection with TX/RX modulation, differential sensing, and high-order noise filtering. The noise immunity is 20× higher than IEC62684 specification. This AFE provides configurable frame rate from 85 to 385Hz and supports various sizes of touch object from 1 to 30mm diameter with comparable SNR to the state of the art.
- In Paper 11.7, KAIST and Samsung Display present a load-insensitive pre-emphasis column driver for large-size and high-resolution flat-panel displays. The column driver self-calibrates a pre-emphasis factor (K) in a column-parallel fashion to achieve fast settling under panel-load RC variation. The column driver drives panel load of 3.87kΩ and 150.6pF within 1.8μs, which is a one-horizontal (1-H) time of UHD (3840×2160) display at a scan frequency of 240Hz, with 0.7% error under ±18% panel RC variation. It is the first work considering a panel-load RC variation in a pre-emphasis driving for a display column driver.
- In Paper 11.8, The University of California at Berkeley and EPFL describe a hybrid CMOS/Silicon-photonic sensor for frequency-modulated continuous-wave LIDAR system featuring a resolution of 8μm/4mm over a 50mm/1.4m range.

Session 12 Overview: *Efficient Power Conversion*

ANALOG SUBCOMMITTEE

Session Chair: Vadim Ivanov, *Texas Instruments – Tucson, AZ*
Session Co-Chair: Jaejin Park, *Samsung Electronics, Korea*

Subcommittee Chair: Axel Thomsen, *Cirrus Logic, Austin, TX*

The session on Efficient Power Conversion is about improvement of efficiency and versatility in switched-capacitor, inductor-based DC-DC converters, and LED drivers. The first two papers address switched-capacitor power conversion, dealing with loss mechanisms and limited ratios. The next two papers present innovative ideas in inductive switched-mode power supplies. This is followed by two LED driver solutions. Finally, the last paper revisits switched-capacitor power converters, achieving high efficiency with a very unusual approach.

- In Paper 12.1, the University of Michigan presents a reconfigurable switched-capacitor DC-DC converter structure with any arbitrary rational conversion ratio, with the highest normalized output conductance ever reported. By incorporating negative voltage feedback into the cascaded converter stages, it achieves a resolution higher than existing binary SC converters while maintaining the conversion efficiency of dedicated fixed-ratio SC converters.
- In Paper 12.2, KU Leuven describes a way to decrease SC converter losses from parasitic capacitances. The presented Switched-Capacitor DC-DC converter achieves a record efficiency of 94.6% and this in a baseline CMOS process without the use of high-density capacitors.
- In Paper 12.3, Toshiba presents an SC reconfigurable converter with both on- and off-chip capacitors. It offers up to 95.8% efficiencies over a wide input voltage range from 0.85V to 3.6V.
- In Paper 12.4, Reutlingen University describes a fully integrated reconfigurable SC converter from 2-to-13V input into 5V output. It uses back-to-back switch configurations, which reduces dynamic power loss.
- In Paper 12.5, the University of Texas at Dallas presents a combination of inductor-based and SC DC-DC converters doubling the supply voltage range above the process limit while decreasing losses and size of off-chip components.
- In Paper 12.6, National Cheng Kung University describes a way to calibrate inductors and load capacitor of a multiphase DC-DC converter. By using this technique, measured output voltage undershoot and settling time are reduced from 225mV and 712ns to 100mV and 133ns respectively.
- In Paper 12.7, National Chiao Tung University presents the structure of a single-inductor multiple-color LED driver, improving the cross-regulation. This driver can dim all LEDs simultaneously or each LED individually to achieve 24bits of color resolution without flicker hazard.
- In Paper 12.8, Dankook University shows how to improve current distribution in a multiple-LED dimming structure with floating current mirrors.
- In Paper 12.9, the University of California at San Diego challenges the SC-converter efficiency limits by flipping load and capacitor connections, achieving 99.8% peak efficiency and 3.2× higher power density compared to 32nm deep-trench switched-capacitor converters.

Session 13 Overview: *Wireless Systems*

WIRELESS SUBCOMMITTEE

Session Chair: *Yuu Watanabe, Denso Corporation, Tokyo, Japan*
Session Co-Chair: *Pierre Busson, ST Microelectronics, Crolles, France*

Subcommittee Chair: *Aarno Pärssinen, University of Oulu, Oulu, Finland, Wireless Subcommittee*

Wireless systems play a crucial role in the IoE, not only for data communication but also for radar. They continuously evolve to more functionality, more integration and higher performance. For example, radar capabilities are required to support car drivers and enable autonomous car driving, traffic mapping, etc. To support higher data rates, wireless circuits require very fast communication and efficient transmission systems. This session discusses recent innovations in both data communication and radar ICs, e.g. to push communication speed, realize efficient digitally-controlled transmission towards 5G and to offer improved radar resolution.

- In Paper 13.1, Seoul National University and Samsung describe an 8.9GHz, digitally-controlled frequency synthesizer PLL capable of precise triangular frequency chirping with up to 940MHz bandwidth and down to 28.8us period. By employing a phase-modulating two-point modulation and a second-order digital loop filter with polarity-alternating frequency ramp estimator, the PLL achieves the highest chirp slope of 32.63MHz/□s with a frequency error less than 1.9MHz_{rms} including the turn-around points while dissipating only 14.8mW.
- In Paper 13.2, Nangyang Technological University describes an FMCW Synthetic Aperture Radar (SAR) Transceiver chip in 65nm CMOS that is targeted for unmanned aerial vehicle SAR imaging in 11.2cm resolution. The transmitter has 13.3dBm output power, 1.1dB ripple, 1.48GHz chirp bandwidth and 0.15-to-1.25MHz/μs tunable chirp rate. The receiver RFFE attains 23.5dB gain, –33dBm IP_{1dB}, 5.6-to-6.3dB NF and 0.51dB ripple, the RX baseband achieves 0.68-to-9.8MHz programmable passband and 55dB variable gain-range, and the integrated ADC has 9.4dB ENOB. The chip consumes 260mW at 1.2 V supply.
- In Paper 13.3, Tokyo Institute of Technology and Fujitsu describe a 56Gb/s W-band 65nm CMOS Wireless Transceiver. Two wideband IF signals are up- and down-converted simultaneously with 68GHz and 102GHz carriers. The transceiver achieves 56Gb/s data rate with TX-to-RX EVM of -16.5dB within 0.1m distance between TX and RX. The transceiver consumes 260mW and 300mW from a 1V supply in TX and RX modes, respectively. This results in 10pJ/bit efficiency, which represents the state-of-the-art in high-data-rate 16-QAM mm-Wave CMOS transceivers.
- In Paper 13.4, the University of California San Diego and the University of California Santa Barbara describe an 8GHz outphasing modulator constructed from the unilateral injection locking between oscillators to map the oscillator tuning voltage to an outphasing angle without the need for a CORDIC or DSP. The modulator circuit is implemented in 45nm SOI CMOS, delivers 9.2dBm to a 50Ω external load while consuming only 36.5mW to achieve a 22.7% overall system efficiency and provide 30dB of dynamic range. Measurements demonstrate complex waveforms such as 64-QAM modulation with 2.1% EVM at 60Mb/s.
- In Paper 13.5, imec and VUB describe a 4-antenna beam-forming transceiver for 60GHz communication in 28nm CMOS. With a core supply of 0.9V, the 7.9mm^2 transceiver IC designed in 28nm CMOS consumes 670mW in TX mode and 431mW in RX mode. Frequency multiplication by means of a subharmonic injection-locked oscillator is chosen to avoid PA pulling on the 24GHz PLL. Combined with antenna arrays on PCB, a TX-to-RX EVM better than -20dB with single-carrier modulation is achieved up to 64QAM.
- In Paper 13.6, Tokyo Institute of Technology describes a 60GHz CMOS transceiver aiming for the IEEE 802.11ay standard. The transceiver achieves 42.24Gb/s data-rate in 64QAM by operating two frequency-interleaved (FI) transceivers at the same time. Each FI transceiver uses 2-channel-bonded spectrum with different carrier frequencies, which realizes a TX-to-RX EVM of -24.1dB (low band) and -23.0dB (high band), respectively. The whole transceiver consumes 544mW and 432mW from a 1.2V supply in transmitting and receiving mode, respectively.
- In Paper 13.7, imec and Vrije Universiteit Brussel describe a CMOS resistive digital transmitter with very low out-of-band noise and high SNR, leveraging the incremental-charge-based operation by directly driving a 50Ω load up to 3.5dBm (from 0.9V supply) with no PA driver. It achieves 20MHz BW and -159dBc/Hz out-of-band noise at both 900MHz and 2.4GHz, with respective EVM and ACLR performances of -36dB and 47dBc. With a core area of 0.22mm^2, this implementation achieves a state-of-the-art small footprint for the given out-of-band noise performance, while consuming 24.8mW at 7dB backoff.

Session 14 Overview: *Next-Generation Processing*

DIGITAL ARCHITECTURE AND SYSTEMS SUBCOMMITTEE

Session Chair: *Paul Liang, Mediatek, Hsinchu, Taiwan*
Session Co-Chair: *Marian Verhelst, KU Leuven, Leuven, Belgium*

Subcommittee Chair: *Stephen Kosonocky, AMD, Fort Collins, CO*

Processors targeting embedded perception and cognition have evolved tremendously in the past decade. Thanks to CMOS process scaling, the cost in terms of area and energy per operation have decreased drastically. This makes it feasible to equip next generation processing with human-like intelligence for emerging applications such as gesture detection, object recognition, and classification.

This session covers highly integrated embedded next-generation processing systems for improved accuracy of HMD/AR user interfaces, intention prediction for automotive, and path identification for micro robots. In addition, programmable accelerators for deep Convolutional Neural Networks and K-Nearest-Neighbors are presented, as building blocks for a wide range of applications, including computer vision, detection, and machine learning. The session concludes with the first integrated 8K Ultra HD video decoder.

- In Paper 14.1, KAIST presents a low-power natural UI/UX processor with an embedded deep learning engine for AR/HMD users implemented in 65nm CMOS. It achieves a 56.5% power efficiency improvement over the latest HMD processor, and ~2% higher recognition rate over the best-in-class pattern recognition processor.
- In Paper 14.2, KAIST presents a high-performance and ultra-low-power dual-mode advanced driver assistance system SoC, capable of predicting potentially risky objects in automotive systems. The chip is implemented in 65nm CMOS, achieves 520GOPS, 0.984mW, and 1.53x power efficiency compared to the state-of-the-art, and it is successfully tested in an autonomous vehicle.
- In Paper 14.3, KAIST presents an ultra-low-power AI processor (AIP) for real-time decision making in intelligent micro robots. Fabricated in 65nm CMOS, the proposed AIP supports 14K searches/s at 1.1mW and up to 470K searches/s at 1.51mW for autonomous robot navigation.
- In Paper 14.4, Intel presents a 128×128-dimensional k-nearest-neighbor accelerator with reconfigurable distance modes fabricated in 14nm tri-gate CMOS. It has an area of 0.333mm^2 and achieves 21.5M vectors/s with 3.37nJ/vector or 9.7TOPS/W measured at 750mV, 25°C.
- In Paper 14.5, MIT presents a 65nm CMOS energy-efficient deep convolutional neural network (CNN) accelerator featuring a spatial array of 168 processing elements fed by a reconfigurable on-chip network. The chip supports state-of-the-art CNNs, such as AlexNet, and is over 10× lower power and requires 4.7× fewer DRAM access per pixel than a mobile GPU.
- In Paper 14.6, KAIST presents a deep CNN processor, implemented in 65nm, for a universal in-situ recognition platform designated for IoE devices. The 1.2V 4x4mm^2 125MHz processor significantly improves energy efficiency over the state-of-the-art at 1.42TOPS/W.
- In Paper 14.7, Waseda University presents the first integrated 8K HEVC decoder chip. The decoder, implemented in 40nm CMOS, features a variable-block-size locally-synchronized pipeline, achieving a pipeline utilization of 83.3%. The chip supports 7680×4320 120fps decoding at a core power of 690mW.

Session 15 Overview: *Oversampling Data Converters*

DATA CONVERTERS SUBCOMMITTEE

Session Chair: *Venkatesh Srinivasan, Texas Instruments, Dallas, TX*
Session Co-Chair: *Tai-Cheng Lee, National Taiwan University, Taipei, Taiwan*

Subcommittee Chair: *Un-Ku Moon, Oregon State University, Corvallis, OR, Data Converters*

Improved power efficiency, wider bandwidths and higher linearity are the primary drivers in the context of data converters. In this session, a number of circuit- and system-level solutions are presented that extend the state of the art in delta-sigma modulators. The papers present a number of techniques that are used to demonstrate very wide bandwidths, low 1/f noise corners, high power efficiency, high dynamic range and linearity.

- In Paper 15.1, the University of Texas at Dallas introduces a SAR-assisted continuous-time delta-sigma modulator in 65nm CMOS that uses 2nd-order noise coupling to achieve a peak SNDR of 75.3dB SNDR in 45MHz BW.
- In Paper 15.2, NXP Semiconductors and Catena Microelectronics present a converter that uses a 1b feedback DAC with a return-to-open technique to achieve a high linearity of -102dBc/-104dBc THD/IM3 in a 25MHz bandwidth.
- In Paper 15.3, New University of Lisbon presents a 65nm CMOS 10MHz BW passive-active CT 2-1 MASH that uses RC integrators and low gain stages to achieve high power efficiency.
- In Paper 15.4, IIT Madras introduces a 1b modulator with chopping used in conjunction with a FIR feedback DAC to achieve a 1/f corner frequency of <10Hz without chopping artifacts and 98.5dB SNDR in the audio band.
- In Paper 15.5 Analog Devices describes a continuous-time 1-2 MASH ADC clocking at 8GHz in 28nm CMOS. This ADC achieves the largest signal bandwidth (465MHz) thus far reported for a CMOS delta-sigma ADC.
- In Paper number 15.6 MediaTek describes a 4th-order continuous-time delta-sigma ADC in 16nm CMOS. The ADC uses an analog ISI-reduction technique to achieve 72dB DR over 160MHz with only 40mW of power.
- In Paper 15.7 Delft University of Technology and NXP Semiconductors describe a Dynamic Zoom ADC that uses energy-efficient pseudo-differential inverter-based OTAs to achieve 107.5dB of dynamic range over the audio band with only 1.6mW of power.
- In paper 15.8, Austria Microsystems describe a 1b discrete-time modulator that uses amplifier stacking to achieve 136dB of dynamic range in a bandwidth of 1kHz with only 13mW of power consumption.

Session 16 Overview: *Innovations in Circuits and Systems Enabled by Novel Technologies*

TECHNOLOGY DIRECTIONS SUBCOMMITTEE

Session Chair: *Pirooz Parvarandeh, Roche, Sunnyvale, CA*
Session Co-Chair: *Shuichi Nagai, Panasonic, Osaka, Japan*

Subcommittee Chair: *Eugenio Cantatore, Eindhoven University of Technology, Eindhoven, The Netherlands, Technology Directions*

Innovations in technology have enabled novel circuits and systems for a wide range of applications including medical, security and power. A diverse set of technologies such as flexible electronics, embedded FeRAM, transformer integration, and nanogap sensors will be explored in this session. These technologies have feature sizes spanning the nm to µm range and voltage ratings up to 5kV.

- In Paper 16.1, University of California, San Diego and Intel describe a scalable, silicon-based DNA sequencing system for personalized medicine using high-density nanogap sensors on 32nm CMOS to dramatically reduce the cost and turnaround time. A proof-of-concept chip is demonstrated with 8,192 pixels and integrated readout circuits.
- In Paper 16.2, Massachusetts Institute of Technology and Texas Instruments describe a Keccak-based wireless authentication tag with FeRAM-based non-volatile D-flip-flops and a fully integrated energy backup unit, which also implements a pseudo-random number generator and authenticated encryption modes. The 0.13µm CMOS tag harvests inductive power from a 433MHz link via a regulating voltage multiplier that supplies 1.5V for AC input >0.55V with <1.1% line/load regulation.
- In Paper 16.3, Fondazione Bruno Kessler, University of Trento, and Telsy describe a robust quantum random number generator based on an array of 16×16 SPAD-based pixels embedding the random bit extraction algorithm at the pixel-level for robustness. The maximum 128Mb/s output is achieved with a light rejection ratio of about –74dB and a sensitivity to temperature variation of -6.7ppm/ºC.
- In Paper 16.4, Princeton University describes an EEG acquisition system using thin-film electronics integrated on a flexible substrate. It incorporates a-Si TFT low-noise 230nV/√Hz chopper-stabilized amplifiers and a-Si TFT compressive-sensing circuits. Signal reconstruction is demonstrated at 8× compression, and spectral-energy features enable a seizure detection error rate of <4%.
- In Paper 16.5, IMEC, KU Leuven, and ICSense describe an a-IGZO active pixel array for large area X-ray imaging with a high charge-to-current gain (59µA/pC) and low non-linearity. The pixel is a 3T1C topology, with a resolution of 254ppi and readout speeds of up to 50Hz at FHD. The readout IC using the proposed transimpedance conversion circuit reduces the cost per channel and the input-equivalent noise.
- In Paper 16.6, IMEC describes a 12b NFC transponder chip on flexible film using low-cost self-aligned a-IGZO thin-film transistors, which uses only 4 photo-lithography steps. The supply voltage can be as low as 0.5V and the transponder exhibits a maximum data rate of 396.5kb/s.
- In Paper 16.7, University of Catania and ST Microelectronics describe a 5kV on-chip galvanic isolation integrated system in a 0.35µm BCD technology. The chip has galvanically isolated power transfer and bidirectional data by using a single integrated coreless transformer. The 40Mb/s digital isolation system includes a current-reuse power oscillator with transformer-based power combining and a rectifier, delivering a dc output power up to 23.7mW.
- In Paper 16.8, University of Texas at Dallas and Texas Instruments describe a 10-to-30MHz GaN driver with an active BST balancing (ABB) technique to withstand 3-to-40V V_{IN} for high reliability. Using dual-edge dead-time modulation with I_o/V_{in} sensing, the efficiency is improved by 8.3% (to 90.7%) for 12V-to-5V DC/DC conversion over I_o range from 0.01 to 1.2A.

Session 17 Overview: *SRAM*

MEMORY SUBCOMMITTEE

Session Chair: *Hugh Mair, Mediatek, Austin, TX*
Session Co-Chair: *Atsushi Kawasumi, Toshiba, Kawasaki, Japan*

Subcommittee Chair: *Leland Chang, IBM, Yorktown Heights, New York, Memory*

Advanced SRAM continues to be one of the critical technology enablers for a wide range of applications – from mobile to high performance servers to the Internet of Everything. Combining the process technologies of FinFET and FD-SOI with advanced circuit techniques enables high-performance, low-voltage, and low-power applications. This session highlights 10nm FinFET technology with the smallest bitcell achieved to date for SRAM at 0.04μm^2. Area efficient 8T SRAMs are demonstrated in 14nm FinFET technology by adopting small signal sensing to enable longer bitlines. FD-SOI is utilized by researchers in applying Razor techniques to SRAM.

- In Paper 17.1, Samsung presents a 128Mb embedded SRAM fabricated in 10nm FinFET technology featuring the smallest bitcells to date with 0.040μm^2 high density and 0.049μm^2 high current offerings. Assist features are explored in detail, and the impact to Power, Performance, and Area is summarized.
- In Paper 17.2, Intel demonstrates two 1.75Mb 1R1W 8T SRAM designs in 14nm FinFET technology using small signal pseudo-differential sensing enabled by a charge sharing scheme that generates a reference voltage in one case, and asymmetric sense amplifier sizing in another. Bit density of 5.6Mb/mm^2 and Vmin of 560mV is achieved.
- In Paper 17.3, University of Michigan proposes timing error detection and correction for SRAM arrays to improve performance at low Vdd. By double sampling during reads and merging wordlines in a dual-port bitcell for writeability gains, energy efficiency at 0.6V is improved by 70%.

Session 18 Overview: High bandwidth DRAM

MEMORY SUBCOMMITTEE

Session Chair: *Chulwoo Kim, Korea University, Seoul*
Session Co-Chair: *Martin Brox, Micron, Munich*

Subcommittee Chair: *Leland Chang, IBM, Yorktown Heights, NY, Memory*

Graphics and high-performance computing systems demand high bandwidth. In graphics systems, the resolution of handheld and desktop systems keeps increasing and emerging visual reality systems will push requirements even higher. High performance computing is benefitting from GPU-acceleration as long as the bandwidth requirements of the GPU are fulfilled.

In this session, new developments in three different high-bandwidth DRAM standards will be presented. Bandwidth of GDDR5 components is improved up to 36GB/s at a data-rate of 9Gb/s/pin. Two different implementations of the TSV-based HBM2 protocol push this barrier beyond 250GB/s. The last paper presents the new Wide-IO2 interface, which is optimized for space-constrained, hand-held applications.

- In paper 18.1, Samsung describes an 8Gb GDDR5 DRAM, which uses a resonant clock-load, a dual-mode equalizing/duty-cycle correcting receiver and on-die de-emphasis to achieve a data-rate of 9Gb/s/pin. Reliability of the device is guaranteed by an on-chip NBTI-monitor circuit and stable power delivery.
- In paper 18.2, Samsung presents an 8Gb HBM2 DRAM with a bandwidth of 307GB/s in a stack of 2, 4 or 8 DRAM-dies. Testing these devices poses a major challenge and is addressed by an at-speed wafer-level test driven by an on-chip PLL. Thermal management of this device is achieved by an adaptive refresh scheme considering the temperature distribution.
- A second HBM2 DRAM in the same stack configuration reaching 256GB/s is described in paper 18.3 by SK Hynix. A new architecture is presented where command decoding and bias generation for the memory core is moved from the memory layer to the logic base-layer of the HBM-stack. Small swing signaling on the heavily loaded TSV-connection is implemented to reduce power for driving the interconnects.
- In paper 18.4, SK Hynix presents the first WIO2 DRAM at a density of 8Gb. Multiple solutions are discussed to test this micro-bumped device. An additional transistor enables inter-channel testing, and an active silicon interposer is developed to directly test the I/O circuitry.

Session 19 Overview: *Digital PLLs*

DIGITAL CIRCUITS SUBCOMMITTEE

Session Chair: *John Maneatis, True Circuits, Los Altos, CA*
Session Co-Chair: *Kathy Wilcox, AMD, Boxborough, MA*

Subcommittee Chair: *Stefan Rusu, TSMC, San Jose, CA, Digital Circuits*

The eight papers in this session highlight developments in clock generation. Digital PLL solution improvements include higher TDC linearity, reference spur reduction, higher power supply noise rejection, and reduced jitter. Other highlights include reduced area and the use of FinFET technology. In addition, a quasi-resonant clocking implementation is presented.

- In Paper 19.1, Broadcom presents a DPLL in 16nm CMOS. A dual-stage phase-acquisition-based loop filter is proposed for fast locking in 1.2μs without frequency overshoot. A nonlinear DCO achieves ±1.25% UI jitter over 0.5-9.5GHz.
- In Paper 19.2, the University of Minnesota presents a 0.2-to-1.45GHz digital sampling fractional-N MDLL occupying 0.0054 mm^2 in 65nm CMOS. It features a zero-offset latch-based aperture phase detector and an in-situ detection scheme. Test chip measurements show 2.8ps integrated RMS jitter at 1.4175GHz with 8mW power dissipation.
- In Paper 19.3, Samsung Electronics presents a digital MDLL with a double reference injection scheme. By adjusting rising and falling edge times of the reference, it achieves a reference spur of -51.4dBc and integrated RMS jitter of 699.2fs. It generates a 2.4GHz clock, while dissipating only 1.5mW in 28nm CMOS.
- In Paper 19.4, Intel presents a modular PLL architecture fabricated in 14nm CMOS. A new reference current generation circuit provides adaptive current to the charge pump and self-maintains the PLL bandwidth and stability providing 15dB of supply noise rejection. The PLL achieves 1.26ps integrated RMS jitter at 2.6mW at 4GHz and meets PCIe Gen2/Gen3 clocking specifications.
- In Paper 19.5, National Taiwan University presents a 0.0216mm^2 DPLL with background supply noise cancellation fabricated in 40nm CMOS. At 3.2GHz, consuming 2.9mW, it produces only 3.85ps integrated RMS jitter, and 31.17ps P-P jitter, when subjected to 50mV P-P 100KHz sinusoidal supply noise.
- In Paper 19.6, the University of Washington presents a frequency-independent resonant clocking architecture enabling efficient wide-range DVFS. A 65nm CMOS prototype test-chip achieves a 33-to-47% clock power reduction over a 0.7-to-1.2V supply range.
- In Paper 19.7, Toshiba presents an ADPLL with a single-slope (SS) ADC-based TDC, in which the SS-ADC leverages the PLL's feedback counter to realize a TDC that is DCO-period detection-free and low-power. The prototype fabricated in 65nm CMOS achieves 1.6ps (0.27LSB) INL and 8.9ps (5.5ENOB) resolution at 2.24GHz with power consumption of 360μW.
- In Paper 19.8, the University of Illinois presents a PLL that combines the advantages of analog and digital PLLs using a time-based integral path. Fabricated in 65nm CMOS, the PLL occupies only 0.0021mm^2 and operates over 0.6-1.2V at 0.4-to-2.6GHz output. At 2.2GHz and a 1V supply, it consumes 1.82mW power and achieves 3.73ps integrated RMS jitter.

Session 20 Overview: *RF-to-THz Transceiver Techniques*

RF SUBCOMMITTEE

Session Chair: *Harish Krishnaswamy, Columbia University, New York, NY*
Session Co-Chair: *Jussi Ryynänen, Aalto University, Espoo, Finland*

Subcommittee Chair: *Piet Wambacq, imec, Belgium, RF Subcommittee*

The ever-increasing demand for high-speed data-rates as well as emerging sensing applications have driven designers to employ novel circuits that explore the entire spectrum from RF to THz more efficiently. This session describes transceiver concepts that improve data-rates and efficiency while supporting complex modulations. The session also features techniques for signal generation at terahertz frequencies as well as various key building blocks for RF and mm-Wave transceivers.

- In Paper 20.1, Hiroshima University, NICT and Panasonic describe a 300GHz transmitter (TX) in 40nm CMOS that adopts a new PA-less QAM-capable architecture employing a cubic mixer, thereby enabling QAM transmission and massive power combining without undue layout complication. 17.5Gb/s/ch 32-QAM transmission is demonstrated over 6 channels.
- In Paper 20.2, Princeton University presents a frequency-agile mm-Wave power amplifier based on asymmetrical non-isolated power combining where the interaction of amplifiers is exploited to synthesize the optimal load-pull impedance at each frequency. The 0.13□m SiGe PA is capable of generating Psat>22dBm between 40 and 65 GHz while maintaining PAE>25%.
- In Paper 20.3, HKUST and Southeast University describe an 86-to-94.3GHz 65nm-CMOS transmitter that integrates a spur-canceling PLL and a single-stage injection-locked PAs with power combining and automatic phase-tuning. The transmitter output power is 15.3dBm and it achieves 9.6% efficiency with the phase noise of -89.5dBc/Hz at 1MHz.
- In Paper 20.4, Tel Aviv University presents a wirelessly-locked 2×3 radiating source array at 0.3THz in 65nm CMOS. By using back-side partial dicing of the die, a record total radiated power of +5.4dBm and EIRP of +22dBm were achieved resulting in 5.1% DC-to-THz efficiency.In Paper 20.5, University of Texas, Dallas, presents a 1.4THz passive frequency multiply-by-10 chain using accumulation-mode MOS varactors in a 65-nm CMOS process. The chain reaches a peak EIRP of -13dBm at 1.33THz with a test-setup-limited output frequency range of 1.3-to-1.47THz.
- In Paper 20.6, Texas A&M University and Qualcomm describe a 28nm CMOS power amplifier (PA) for 28GHz 5G mobile phased arrays. The PA achieves 9% PAE at Pout of +4.2dBm for a 64-QAM OFDM signal having PAPR of 9.6dB at -25dBc EVM using a 1V supply. The PA also achieves 35.5%/10% PAE at saturation/9.6dB back-off.
- In Paper 20.7, Samsung presents a 0.13μm CMOS hybrid supply modulator that achieves a 50MHz envelope-tracking (ET) bandwidth, 83% efficiency, and a receive-band noise level of -136dBm/Hz. An ET-PA achieves 42% power-added efficiency while delivering 26.5dBm power with -41dBc ACLR.
- In Paper 20.8, imec demonstrates a dual-frequency balanced duplexer in 0.18um SOI CMOS. A distributed filtering concept is introduced that enables semi-independent and simultaneous tuning of distinctively different impedances at the TX and RX frequencies. The balanced duplexer covers all LTE bands in the 0.7-to-1GHz range.
- In paper 20.9, University of Toronto describes a 0.13μm CMOS filtering transimpedance amplifier (TIA) for use with RF passive mixers. The TIA demonstrates an in-band high-pass noise and distortion shaping and an adaptive transfer function. A TIA prototype, reconfigurable between 2.8MHz and 12MHz, shows an out-of-band SFDR of 85dB with 1.92mW power dissipation.
- In paper 20.10, KU Leuven presents a 28nm bulk CMOS LNA for E-Band applications that employs transformer-based 4th-order inter-stage matching networks to achieve a 29.6dB gain over 28.3GHz 3dB bandwidth. The measured minimum in-band noise figure is 6.4dB and ICP1dB is -28.1dBm.

Session 21 Overview: *Harvesting and Wireless Power*

ANALOG SUBCOMMITTEE

Session Chair: *Anton Bakker, Arctic Sand, San Jose*
Session Co-Chair: *Yuan Gao, IME A*STAR, Singapore*

Subcommittee Chair: *Axel Thomsen, Cirrus Logic, Austin TX, Analog Subcommittee*

The first four papers in this session focus on wireless sensing applications. They can be powered by harvesting energy from RF, piezoelectric, photovoltaic and thermoelectric energy sources. Many innovations focus on optimization of cold-start conditions in no-battery or dead-battery situations. Several techniques are used to minimize the number and size of external components such as inductors and capacitors. Maximum-Power-Point Tracking (MPPT) remains an important feature that needs optimization. The last four papers in the session focus on the fast-growing market of wireless charging for cell phones and wearables. The emphasis here is to comply with all the available standards (A4WP, Qi and PMA) with a single solution.

- In Paper 21.1, Texas A&M University describes a reconfigurable charge-pump energy harvester with hysteretic regulation and single-cycle MPPT to eliminate the storage capacitor at its output. This is the first charge-pump energy harvester achieving 72% efficiency while simultaneously tackling the startup, self-sustaining, MPPT, and output regulation challenges.
- In Paper 21.2, the University of Freiburg presents a 4μW-to-1mW autonomous piezoelectric energy harvesting system in 0.35μm CMOS. Regular operation is possible with input voltages as low as 670mV. It extracts up to 6.81 times more power compared to an ideal full-bridge rectifier.
- In Paper 21.3, Analog Devices presents a multi-input and -output converter using a single inductor for energy harvesting with two-stage charging to reduce the cold start time by 77%. The other advantages are wide input range (30mV to 3.6V), ultra-low quiescent current (200nA) due to the wide use of the native NMOS and sample/hold scheme, as well as low cold-start voltage (0.3V) and power (5.4uW).
- In Paper 21.4, the University of Michigan presents a fully-integrated light harvester that maintains >78% end-to-end efficiency from 100lux to 100klux when charging a 1.5V-to-2.5V battery. This harvester improves the minimum and maximum harvesting efficiency by 23% and 9%, respectively, compared to the previous fully-integrated harvesters with MPPT circuit.
- In Paper 21.5, the University of Michigan presents a current-mode wireless power receiver with optimal resonant cycle tracking for implantable systems. Minimum harvestable power is 600nW (3.9× lower than prior art) and power efficiency is 61.2% at 2.8μW.
- In Paper 21.6, Oregon State University presents an area-efficient rectifier-antenna co-design approach that leverages high-Q, electrically-small antennas and rectifier circuits to enable a self-oscillation phase. Two 65nm CMOS designs achieve -34.5dBm sensitivity for 1.6V across a 2MΩ load and -24dBm sensitivity for 2.5V across 100kΩ load.
- In Paper 21.7, the Hong Kong University of Science and Technology presents a 3-level reconfigurable resonant regulating (R^3) rectifier for a wireless power receiver. The receiver regulates the output voltage at 5V and delivers a maximum power of 6W. It was designed in a standard 0.35μm CMOS process with a die area of 4.77mm^2, and the measured peak efficiency reaches 92.2%.
- In Paper 21.8, Mixed Analog Power Solution presents a 0.18um BCDMOS 2.5W fully integrated wireless battery charger IC that covers Qi, PMA and A4WP standards for wearable applications. The chip efficiency is 84% when the IC delivers 2W to a load at 6.78MHz. The TX-to- RX efficiencies at Qi, PMA and A4WP at 2.5W are 63%, 62% and 54% respectively.

Session 22 Overview: *Systems and Instruments for Human-Machine Interfaces*

TECHNOLOGY DIRECTIONS & IMMD SUBCOMMITTEES

Session Chair: *Long Yan, Samsung Electronics, Korea*
Session Co-Chair: *Refet Firat Yazicioglu, GlaxoSmithKline, UK*

Subcommittee Chairs:
Eugenio Cantatore, Eindhoven University of Technology, The Netherlands, Technology Directions
Makoto Ikeda, University of Tokyo, Japan, IMMD

Advanced bioelectronics systems, that bridge modern electronics and biology, offer devices and tools ranging from continuous extraction of physiological parameters and diagnostics to implementing therapeutic schemes through electrical stimulation. These research tools enable neuroscientists to design novel experiments and help them in understanding the fundamentals of the human body. New devices and systems not only implement therapeutic functions for healing motor disorders and chronic diseases, but also enable early diagnosis outside of traditional clinical settings.

This session presents recent advances in human-machine implantable interfaces for monitoring and stimulation of neurons to enable prosthetics that recover motor function and for therapeutic purposes. It also includes SoCs and novel wearable systems for enabling continuous monitoring of vital signs that can provide immediate and long term diagnostic care, and for biological audio sensing.

- Paper 22.1 from Stanford University, an invited system talk, discusses brain machine interfaces for converting neural signals from the brain into control signals used by prosthetic limbs and/or other machines. Various solutions for higher neural recording density, efficient signal acquisition/processing/transmission, system integration, and robust system operation are explored.
- Paper 22.2 from UCLA presents a 0.7g, 0.5cm^3 wireless implant for motor function recovery after spinal cord injury. It performs 160-channel current-mode stimulation, 16-channel physiological signal recording, 48-channel bio-impedance characterization and 2Mb/s quasi full-duplex data telemetry with 18mW power.
- In Paper 22.3 from KAIST, an ultra-low-power sensor SoC on OLED/OPD substrate for enabling a SpO_2/ExG monitoring sticker is presented. The sticker features small area (2.5cm×5.5cm), light weight (2g including batteries) and the lowest reported power consumption (141μW).
- Paper 22.4 from IMEC describes a 172μW compressive sampling photoplethysmographic readout chip. By directly extracting heart-rate and variability from compressively sampled data, it reduces power consumption by up to 30× without significantly compromising other important performance metrics.
- Paper 22.5, ETH Zurich presents a 0.5V 55μW 64×2-channel binaural silicon cochlea for event-driven stereo-audio sensing. An event cochleagram corresponding to natural speech input is demonstrated. The cochlea-inspired chip is 18× more power-efficient than the best reported implementation to date and exhibits a 1.3-to-39 Q-tuning range, while achieving appropriate matching between the two ears.
- In Paper 22.6, IMTEK presents a 22V compliant CMOS active charge balancer for safe chronic electrical stimulation. The system consumes only 56μW and features a 36% mismatch correction in stimuli amplitude as well as an autonomous 100% charge removal at maximum compensation amplitude of 500μA.
- Paper 22.7 from IMEC introduces a 966-electrode neural probe with 384 configurable channels in 0.13μm SOI CMOS. Compared to prior art, it has double the number of active electrodes and 7× higher number of integrated recording channels on the same substrate, while ensuring low crosstalk.
- Paper 22.8 from ETH Zurich presents the highest density electrode array reported to date for in-depth neuroscientific studies on subcelluar-resolution details or large complex networks. It discusses a switch-matrix-based multi-functional monolithic micro-electrode system that has 59,760 electrodes with 13.5μm pitch.

Session 23 Overview:
Electrical and Optical Link Innovations
WIRELINE SUBCOMMITTEE

Session Chair: *Frank O'Mahony, Intel, Hillsboro, OR*
Session Co-Chair: *Simone Erba, STMicroelectronics, Pavia, Italy*

Subcommittee Chair: *Daniel Friedman, IBM, Yorktown Heights, NY, Wireline*

Continued data bandwidth scaling is essential in all segments of electronics, from low-power mobile to high-speed data centers. Each of these segments is faced with different constraints to bandwidth scaling, including power, process technology, and form factor. This session highlights how design and technology are keeping pace with bandwidth demands with innovations in both electrical and optical data links. It starts with a transceiver that combines an integrated regulator and rapid wake-up to scale data rate by 500× while keeping energy-per-bit within a factor of 2×. The next paper describes a proximity communication link with 32Gb/s total bandwidth over four parallel capacitively coupled channels across a 1mm air gap. This is followed by a paper that implements a 5-tap DFE in a 4 x 6Gb/s display interface while overcoming the f_t limits of 0.18µm CMOS. Two papers then introduce a 56Gb/s MZM-based TX and 2x64Gb/s optical TIA, respectively, demonstrating the next-generation path for optical bandwidth scaling. The session concludes with two high-speed wireline receivers that demonstrate <1pJ/bit energy efficiency at 30-40Gb/s and one that demonstrates fast DFE-IIR equalization adaptation.

- In Paper 23.1, the University of Illinois at Urbana-Champaign presents a source-synchronous transceiver that combines dynamic voltage and frequency scaling with rapid on-off techniques to maintain energy efficiency of 5.9-14.1pJ/b across a 500× effective data-rate range. A DC-to-DC converter with 94% efficiency supports fast changes in voltage and load current. Link wake-up time is only 14ns; the design includes a wide-range MDLL that settles in only two reference clock cycles.
- In Paper 23.2, Intel describes a 4-channel bi-directional proximity interface with 32Gb/s total bandwidth that consumes 4pJ/b in 14nm CMOS. The capacitive couplers use an alternating, rectangular pattern to suppress crosstalk without keep-out areas between channels. Transmitter slew-rate control, along with receiver filtering and a 1-tap DFE, equalize the resonant channel to reduce power.
- In Paper 23.3, Samsung Semiconductor presents a 4x6Gb/s display interface for next-generation 8K TVs. The receiver implements a 5-tap partial-response DFE in 0.18µm CMOS. To overcome the f_t limits of this process, it uses body bias to set the weight of the loop-unrolled tap and reduces the number of sequential logic elements in the feedback path.
- In Paper 23.4, STMicroelectronics and the University of Pavia describe a complete 56Gb/s electro-optical transmitter, operating at a 1310nm wavelength, dissipating 300mW and achieving a >2.5dB extinction ratio. The combination of a traveling-wave Mach-Zender Modulator in a silicon photonic technology and an electronic driver in 55nm BiCMOS realizes the proposed transmitter. Integrated transmission line bandwidth limitations are compensated by applying passive boost, shunt peaking in the pre-driver stage, and passive peaking in the load.
- In Paper 23.5, IHP describes a 64Gbaud linear transimpedance amplifier for long-haul coherent receivers. Implemented in 130nm BiCMOS, it achieves a 3dB bandwidth of 53GHz while consuming 277mW. The dual TIA chip provides an aggregate data rate of 128Gb/s using QPSK modulation.
- In Paper 23.6, IBM Zurich Research Laboratory presents a 14nm SOI CMOS 30Gb/s receiver data path. It achieves 0.8pJ/b energy-efficiency at maximum data rate. The CTLE exhibits 9.5dB gain boost tunable at Nyquist frequency without passive inductors. In the 1-tap DFE a single regenerative stage per slice discriminates after selection of analog speculated paths.
- In Paper 23.7, University of Toronto presents a 16Gb/s 28nm FD-SOI CMOS receiver. Based on 1 IIR + 1 discrete DFE tap and including integrated clock recovery and adaptation, it equalizes a 28dB-loss channel. An edge-based algorithm adapts both IIR and DT equalizer coefficients using the same high-speed circuitry required for clock recovery.
- In Paper 23.8, the University of California, Los Angeles, presents a 40Gb/s NRZ receiver in 45nm CMOS. It consists of a one-stage CTLE, a half-rate CDR circuit, a half-rate/quarter-rate DFE, a discrete-time linear equalizer, and a deserializer. The receiver, which dissipates only 14mW, achieves a BER < 10^-12 with a recovered clock jitter of 1.3ps-rms and a jitter tolerance of 0.45UI at 5MHz when operating over a channel with loss of 18.6dB at Nyquist.

Session 24 Overview: *Ultra-Efficient Computing: Application-Inspired and Analog-Assisted Digital*

TECHNOLOGY DIRECTIONS SUBCOMMITTEE

Session Chair: *Antoine Dupret, CEA-LIST-Leti, Saclay, France*
Session Co-Chair: *Subhasish Mitra, Stanford University, Stanford, CA*

Subcommittee Chair: *Eugenio Cantatore, Eindhoven University of Technology, Eindhoven, The Netherlands, Technology Directions*

The next wave of pervasive computing imposes stringent energy and performance constraints that cannot be met by today's approaches. The circuits in this session use a broad spectrum of design techniques to overcome this challenge. They span a wide range of application domains, from vision assists to machine learning and data analytics. For such applications, new analog-assisted digital techniques enable compact kernel implementations that trade output accuracy for high efficiency.

- In Paper 24.1, MIT presents an energy-efficient 3D vision processor that post-processes time-of-flight camera data. It forms the core of a navigation device for the visually impaired, and successfully detects safe areas and obstacles at 30fps. By co-optimizing its hardware architecture and vision algorithms, it consumes 8mW from a 0.6V supply and achieves 1,500× higher energy efficiency than Cortex-A9.
- In Paper 24.2, Stanford University, presents a switched-capacitor matrix multiplier with co-designed local memory targeting machine-learning applications. It demonstrates accelerators for stochastic gradient descent optimization solvers and the compression-classification layer of convolutional neural networks. Compared to a previous analog-assisted digital design presented at ISSCC 2015, it achieves approximately 2 orders of magnitude better TeraOps/W and 125,000× faster execution time.
- In Paper 24.3, Isocline and University of Michigan Ann Arbor present a GPS acquisition accelerator. It combines analog computations and digital storage for high-energy efficiency and performance. Designed in a 65nm LP CMOS process, it achieves 2b operations at 36.8TeraOps/W through a differential current-steering circuit topology.

Session 25 Overview: *mm-Wave and THz Sensing*

RF SUBCOMMITTEE

Session Chair: *Brian Ginsburg, Texas Instruments, Dallas, TX*
Session Co-Chair: *Minoru Fujishima, Hiroshima University, Hiroshima, Japan*

Subcommittee Chair: *Piet Wambacq, imec, Leuven, Belgium, RF Subcommittee*

The continuing advancement of silicon electronics enables a wide range of sensing applications in mm-Wave and terahertz frequency ranges. Integrated electromagnetic interfaces support frequency-to-spatial mapping, highly confined evanescent fields, and artificial magnetic conductors to expand operating bandwidths of antennas-on-silicon. Quadrature processing and heterodyne down-conversion, both well-known from microwave communication, have been applied to passive and active imaging, respectively, to achieve record sensitivity. The session papers demonstrate advancements in imaging, spectroscopy, and near-field measurements.

- In Paper 25.1, University of Wuppertal and IHP describe a 0.55THz near-field sensor in a 0.13µm SiGe BiCMOS. It uses a magnetically-coupled differential split-ring resonator with high surface-field confinement to achieve a lateral resolution down to 8µm, 1/71 of the wavelength, and maintains a 20dB SNR.
- In Paper 25.2, University of Texas, Dallas, describes a wideband receiver front-end for rotational spectroscopy. Using an artificial magnetic conductor-backed antenna, an NMOS anti-parallel-diode-pair mixer with floating body, and a hybrid-based broadband signal-isolation structure, the receiver achieves 13.9-19dB noise figure across its 210-305GHz RF bandwidth.
- In Paper 25.3, Princeton University presents a THz spectroscope-on-chip operating from 40 to 330GHz. Electromagnetic scattering of the incident signal across an on-chip radiator provides for spectral estimation with 10MHz accuracy without any frequency synthesis, RF amplification, or mixing.
- In Paper 25.4, University of California, Davis, and the Jet Propulsion Laboratory present a 100GHz radiometer in 65nm CMOS without a Dicke switch. Using quadrature signaling and by monitoring the antenna and a calibration resistor simultaneously, the cancelation of the multiplicative noise in a back-end DSP achieves a 0.43K noise equivalent temperature difference.
- In Paper 25.5, Cornell University, Massachusetts Institute of Technology and STMicroelectronics present a coherent imager in a 0.13µm SiGe BiCMOS. At 320GHz, a phase-locked high-power transmitter and an 8-cell subharmonic mixer use coherent heterodyne detection to achieve 70.1pW sensitivity.

Session 26 Overview: *Wireless for IoE*

WIRELESS SUBCOMMITTEE

Session Chair: *Kenichi Okada, Tokyo Institute of Technology, Tokyo, Japan*
Session Co-Chair: *Jan van Sinderen, NXP Semiconductors, Eindhoven, The Netherlands*

Subcommittee Chair: *Aarno Pärssinen, University of Oulu, Oulu, Finland, Wireless Subcommittee*

This session features numerous low-power wireless techniques and systems to address the challenges of IoE. Presented are an ADPLL-based hybrid-loop BLE receiver, an ultra-low-power receiver using transmitted reference modulation, a fully digital IEEE 802.11ah-compliant polar transmitter, an ETSI Class-1-compliant IoE transceiver, a GNSS receiver aimed at IoE applications, a Filtering-by-Aliasing receiver, a syringe-implantable radio system on glass substrate including antenna, a BLE-compliant wake-up radio and an N-path switched-capacitor-based transceiver.

- In Paper 26.1, Toshiba presents a hybrid-loop RX based on an ADPLL architecture for Bluetooth Low Energy. A novel single-channel receiving method is adopted to reduce the power consumption. The 65nm CMOS prototype achieves a sensitivity of -90dBm with an adjacent-channel-rejection performance of -2/24/29dB at offset frequencies of 1/2/3MHz respectively, while consuming 5.5mW.
- In Paper 26.2, the University of Twente presents a 915MHz ultra-low-power receiver with 10kb/s data-rate for wireless sensor networks. An in-band SIR of -50dB is achieved by Transmitted-Reference modulation and Shifted-Limiter, while consuming only 135 to 175μW.
- In Paper 26.3, imec presents a 1.3nJ/b IEEE 802.11ah TX for IoE applications by a 40nm CMOS. A fully digital polar architecture consisting of an ADPLL-based frequency modulator and an AM-retimed ΔΣ switched-capacitor PA achieves more than 10× power reduction with 4.4% EVM and >4.8dB spectral mask margin.
- In Paper 26.4, Analog Devices presents a Wireless SoC Transceiver targeted at Smart-Metering and IoE in bands 160 to 960MHz, compliant to the ETSI Class-1 specification. GFSK/MSK/OOK modulation is supported at data-rates from 0.1 to 400kb/s, achieving 100dB blocker rejection at +/-10MHz and 70dB ACR at +/-12.5kHz.
- In Paper 26.5, Sony presents a 0.72mm^2 GNSS receiver aimed at IoE applications. The receiver achieves a 2.5dB NF while consuming 2.3mW from a 0.7V supply. Noise and gain are achieved under low voltage using an LNA with DC bias feedback and baseband OTAs that employ positive feedback.
- In Paper 26.6, UCLA and Silvus Technologies present a receiver front-end that employs Filtering-by-Aliasing (FA) to implement a sharp bandpass function. By incorporating an integrator-based baseband that avoids voltage gain at RF, the receiver achieves very high tolerance of closely spaced interferers as well as in-band impedance matching.
- In Paper 26.7, the University of Michigan presents a syringe-implantable radio system, including a magnetic antenna realized within a 1×10mm^2 dimension on glass substrate. This radio system achieves a link distance up to 50cm (sensor TX) and 20cm (sensor RX) through organic tissue. The transmitter consumes 43.5μw average power at 2kb/s, while the receiver power consumption is 36μW with -54dbm sensitivity at 100kb/s.
- In Paper 26.8, PsiKick presents a 236nW BLE-compliant wakeup receiver with -56.5dBm sensitivity, capable of energy harvesting. Back-channel communication is presented to allow BLE-compliancy.
- In Paper 26.9, the University of Macau and Instituto Superior Tecnico present a 0.038mm^2 SAW-less multi-band transceiver with zero inductors and external matching components for both TX and RX modes, fabricated in 65nm CMOS. It features both an N-Path Switched- Capacitor (SC) Gain Loop and an LO-defined high-Q bandpass (de)modulator, rejecting the OB noises in TX mode or OB blockers in RX mode.

Session 27 Overview: *Hybrid and Nyquist Data Converters*

DATA CONVERTER SUBCOMMITTEE

Session Chair: *Stéphane Le Tual, STMicroelectronics, Grenoble, France*
Session Co-Chair: *Kostas Doris, NXP Semiconductors, Eindhoven, The Netherlands*

Subcommittee Chair: *Un-Ku Moon, Oregon State University, Corvallis, OR, Data Converters*

The traditional boundaries between classical data converter architectures are being dissolved. Hybrid combinations that optimally exploit CMOS technology strengths have emerged. This session demonstrates multiple innovative hybrid and Nyquist-rate data converters ranging from 1 kHz to 4 GHz bandwidths and SNR levels exceeding 100dB. Papers in this session demonstrate hierarchical time interleaving, capacitor and opamp-sharing, and time interleaving skew calibration. SAR ADCs utilizing charge-injection DACs, embedded mismatch and noise shaping, and sub-ADCs using Delta-Sigma or digital slope techniques are disclosed. A noise-cancellation technique combined with amplitude and timing error pre-distortion demonstrates improved IM3 performance in a current-steering DAC.

- In Paper 27.1, University of Southern California describes a 12b 2GS/s current-steering segmented DAC with an oversampled LSB segment and MSB pre-distortion. Built in 65nm technology, the converter achieves SFDR of 74 to 96dBc and IM3 of -80 to -101dBc over the Nyquist band.
- In Paper 27.2, MediaTek introduces a DAC mismatch error-shaping technique. The 55nm CMOS prototype consumes 15.7μW and exhibits 96.1dB peak SNDR over 4kHz BW with a Schreier FoM of 180dB.
- In Paper 27.3, University of Michigan presents a charge-injection DAC based SAR ADC to improve the DAC linearity, compactness, and speed. Fabricated in 40nm CMOS, this 6b 1GS/s ADC consumes 1.26mW from 1V power supply and occupies an area of only 0.00058mm^2.
- In Paper 27.4, MediaTek combines a fine digital slope ADC with a coarse SAR ADC. At 100MS/s, the 28nm CMOS ADC achieves an SNDR of 64.4dB and an SFDR of 75.4dB at Nyquist input frequency, while consuming only 0.35mW from a 0.9V supply and occupying an area of 66×71μm^2.
- In Paper 27.5, Maxim presents a hierarchically time-interleaved ADC for wide-bandwidth communication applications. This 65nm 4GS/s RF ADC digitizes input frequencies up to 4GHz with an aperture jitter of 50fs rms, while consuming 2.2W. The ADC achieves 56.1dB SNR and 64dBc linearity at 1.842GHz input frequency.
- In Paper 27.6, Broadcom presents a pipelined converter using capacitor and amplifier sharing. Implemented in 16nm FinFET, the 13b 4GS/s ADC occupies 0.34mm^2 and consumes 300mW. It achieves 75dB peak SFDR, 68dB SFDR at Nyquist, -66dBFS noise level and 56dB SNDR at Nyquist.
- In Paper 27.7, National Taiwan University introduces a time-interleaved skew-correction technique based on signal-slope estimation. The 40nm CMOS 10b 2.6GS/s SAR ADC employing the technique achieves a 50.6dB SNDR at Nyquist rate while dissipating 18.4mW from a 1.1V power supply.
- In Paper 27.8, Marvell enables significant power and area reduction by combining SAR and incremental Delta-Sigma ADCs. The 12b 28nm 600MS/s 4× time-interleaved ADC with an on-chip buffer achieves an SNDR of 60.7dB at low input frequency and 58.0dB at high frequency, while consuming 26.5mW and occupying 0.076mm^2.

Session 28 Overview: *Biological Sensors for Point of Care*

IMMD SUBCOMMITTEE

Session Chair: *Peter (Chung-Yu) Wu, National Chiao Tung University, Hsinchu, Taiwan*
Session Co-Chair: *Jan Genoe, imec, Leuven, Belgium*

Subcommittee Chair: *Makoto Ikeda, University of Tokyo, Japan. IMMD*

Point-of-care (PoC) medical services aim to deliver care at the convenient proximity of patients using dedicated PoC testing tools. Thus, they inevitably require various integrated and miniaturized biological sensors. The sensor systems discussed in this session comprise the technologies and designs for several key modalities, including: NMR (Nuclear Magnetic Resonance), ESR (Electron spin resonance), dielectric spectroscopy of water comprising biomolecules, ECG (Electrocardiogram), BIOZ (bio-impedance), PPG (Photoplethysmogram), and GSR (Galvanic Skin Response), measurements of vital signals, and airborne particle matter.

- In Paper 28.1, the University of Macau, together with the University of Glasgow, the University of Pavia and the Instituto Superior Técnico present the first micro-NMR CMOS system for multi-type biological and chemical assays. The implementation, supported by a vertical Hall sensor and a thermal-controlled coil, reaches a detection limit of 50pM.
- In Paper 28.2, the University of Ulm presents a 14GHz, battery-operated, point-of-care ESR spectrometer. The portable system, containing a 0.5T permanent magnet, the 15mW ESR detector ASIC, and signal processing PCBs, consumes 4W from a battery, which allows truly autonomous operation.
- In Paper 28.3, Sharp, Kyoto University, and Hiroshima University propose a biosensor utilizing 60GHz and 120GHz LC oscillator arrays to detect target biological molecules in 2 dimensions by using biological water as a label.
- In Paper 28.4, imec, the Holst Centre, and Samsung Electronics present the most complete and versatile sensor read-out system. It is the first design that supports ECG, BIOZ, PPG, and GSR. Power consumption is usually between ~300 and 1000μW, depending on the application.
- In Paper 28.5, imec, the Holst Centre, and the KU Leuven describe a time-based ECG readout front-end in 40nm CMOS. It improves dynamic range by >5× at 0.6V supply while consuming only 3.3μW and occupying 0.015mm^2.
- In Paper 28.6, the University of California at Los Angeles and Silicon Laboratories propose a front-end achieving a linear input-range of ±50mV, which is a 10× improvement with respect to the range of previous designs. The SFDR is 79dB, which is 20dB higher than existing designs.
- In Paper 28.7, Politecnico di Milano presents an airborne-particle-matter detector that has been integrated in CMOS technology for the first time. It implements 32 channels operating in parallel with a capacitance resolution of 65zF, 2× better than previous single-channel CMOS capacitance detectors.

ISSCC 2016
SESSION HIGHLIGHTS

CONDITIONS OF PUBLICATION

PREAMBLE

The Session Highlights to follow serve to capture the context, highlights, and potential impact, of the papers to be presented in each Session at ISSCC 2016 in January in San Francisco

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- From ISSCC's point of view, the phraseology included in the box below captures what we at ISSCC would like your readership to know about this, the 63rd appearance of ISSCC, on January 31st to February the 4th, 2016, in San Francisco.

This and other related topics will be discussed at length at ISSCC 2016, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on January 31 - February 4, 2016, at the San Francisco Marriott Marquis Hotel.

ISSCC Press Kit Disclaimer
The material presented here is preliminary.
As of November 5, 2015, there is not enough information to guarantee its correctness.
Thus, it must be used with some caution.

Session 2 Highlights: RF Frequency Synthesis Techniques

[2.1] An Integrated 0.56THz Frequency Synthesizer with 21GHz Locking Range and -74dBc/Hz Phase Noise at 1MHz Offset in 65nm CMOS

Paper 2.1 Authors: Y. Zhao, Z.Z. Chen, G. Virbila, Y. Xu, R.A. Hadi, Y. Kim, A. Tang, T. Reck, H. N. Chen, C. Jou, F.L. Hsueh, M.C.F. Chang
Paper 2.1 Affiliation: University of California, Los Angeles, CA, Jet Propulsion Laboratory, Pasadena, CA, TSMC Limited, Hsinchu, Taiwan

Subcommittee Chair: Piet Wambacq, imec, Belgium, RF Subcommittee

CONTEXT AND STATE OF THE ART

- A 320GHz phase-locked loop has been reported in ISSCC 2015, achieving -79dBc/Hz phase noise at 1MHz offset.
- For some applications such as planetary science, astrophysics and radio-astronomy, operation frequency needs to be increased to 0.5-to-0.6THz range.

TECHNICAL HIGHLIGHTS

A 0.54-to-0.56THz synthesizer in a standard 65nm CMOS technology is reported.

- Paper 2.1 presents the first integrated CMOS frequency synthesizer operating at record-breaking 0.56THz with 21GHz locking range and -74dBc/Hz phase noise at 1MHz offset.

APPLICATIONS AND ECONOMIC IMPACT

- Compared with III/V MMIC synthesizers used in existing THz instruments, the proposed CMOS frequency synthesizer promises to increase the level of integration and considerably reduce weight, volume and power.

Session 3 Highlights: Wireline

[3.5] A 56Gb/s NRZ-Electrical 247mW/lane Serial-Link Transceiver in 28nm CMOS

[3.7] A 40-to-64Gb/s NRZ Transmitter with Supply-Regulated Front-End in 16nm FinFET

Paper 3.5 Authors: Takayuki Shibasaki, Takumi Danjo, Yuuki Ogata, Yasufumi Sakai, Hiroki Miyaoka, Futoshi Terasawa, Masahiro Kudo, Hideki Kano, Atsushi Matsuda, Shigeaki Kawai, Tomoyuki Arai, Hirohito Higashi, Naoaki Naka, Hisakatsu Yamaguchi, Toshihiko Mori, Yoichi Koyanagi, Hirotaka Tamura,
Paper 3.5 Affiliation: *Fujitsu Laboratories Ltd., Kamiodanaka, Nakaharaku, Kawasaki, Japan*
Paper 3.7 Authors: Yohan Frans, Scott McLeod, Hiva Hedayati, Mohamed Elzeftawi, Jin Namkoong, Winson Lin, Jay Im, Parag Upadhyaya, Ken Chang
Paper 3.7 Affiliation: *Xilinx Inc, San Jose, CA*
Subcommittee Chair: *Daniel Friedman, IBM, Yorktown Heights, NY, Wireline*

CONTEXT AND STATE OF THE ART

- The demand for bandwidth between chips and sub-systems continues to skyrocket, driving the need for ever faster and more efficient transceivers. To meet this demand, this session reports for the first time a number of transceivers supporting 25Gb/s and up to 64Gb/s.
- Process technology scaling continues to drive the need for substantial innovation in wireline circuits to deal with the ever-changing properties of the devices. In particular, FinFET transistors exhibit several favorable analog characteristics, but also introduce a number of limitations, particularly in terms of device sizing and capacitive parasitics.

TECHNICAL HIGHLIGHTS

- **Lowest-power CMOS 56Gb/s NRZ transceivers over a VSR channel**
  In paper 3.5, Fujitsu Laboratories describes a 56Gb/s/lane NRZ-electrical transceiver in 28-nm CMOS. The receiver uses a baud-rate sampling to minimize the power consumption. A 2-tap feed-forward equalizer formed by source-series-terminated driver stages in the transmitter and a continuous-time linear equalizer followed by a 1-tap speculative decision-feedback equalizer in the receiver compensate for an 18.4dB loss. The transceiver consumes 247mW/lane from a 0.96V supply.

- **40-64Gb/s PAM4 Transmitters in 16nm FinFets**
  In Paper 3.7, a 3-tap 64Gb/s NRZ transmitter using a quad-rate architecture is demonstrated in a 16nm FinFET technology. A 4:1 MUX consisting of static CMOS pulse generators and a tailless CML multiplexing stage is used at the final stage of serialization. An on-chip regulator provides power to the pulse generators and CMOS clock buffers. A phase error correction circuit corrects the phase errors of the four-phase clocks generated by an LC-PLL. The transmitter achieves 800mVppd with150fs RJ while consuming 225mW at 64Gb/s.

APPLICATIONS AND ECONOMIC IMPACT

- The demonstration of complete transceivers operating at data rates of 56Gb/s and beyond is critical to extending the high-speed signaling roadmap that supports and enables Big Data infrastructure.
- The realization of NRZ transmitters in 16nm FinFet demonstrates circuit techniques to realize 64Gb/s operations

Session 4 Highlights: Digital Processors

[4.1] 14nm 6th-Generation Core Processor SoC with Low Power Consumption and Improved Performance
[4.3] A 20nm 2.5GHz Ultra-Low-Power Tri-Cluster CPU Subsystem with Adaptive Power Allocation for Optimal Mobile SoC Performance
[4.4] A 197mW 70ms-Latency Full-HD 12-Channel Video-Processing SoC for Car Information Systems

Paper [4.1] Authors: *Eyal Fayneh, Marcelo Yuffe, Ernest Knoll, Michael Zelikson, Muhammad Abozaed, Yair Talker, Ziv Shmuely, Saher Abu Rahme*
Paper [4.1] Affiliation: *Intel, Haifa, Israel*
Paper [4.3] Authors: *Hugh Mair[1], Gordon Gammie[1], Alice Wang[2], Rolf Lagerquist[1], CJ Chung[1], Sumanth Gururajarao[1], Ping Kao[2], Anand Rajagopalan[1], Anirban Saha[3], Amit Jain[4], Ericbill Wang[2], Shichin Ouyang[5], Huajun Wen[1], Achuta Thippana[1], HsinChen Chen[1], Syed Rahman[1], Minh Chau[1], Anshul Varma[1], Brian Flachs[1], Mark Peng[2], Alfred Tsai[2], Vincent Lin[2], Ue Fu[2], Wuan Kuo[2], Lee-Kee Yong[2], Clavin Peng[2], Leo Shieh[2], Jengding Wu[2], Uming Ko[2]*
Paper [4.3] Affiliation: *MediaTek, Austin, TX; MediaTek, Hsinchu, Taiwan; MediaTek, Singapore; MediaTek, Bangalore,India; MediaTek, San Jose, CA*
Paper [4.4] Authors: *Seiji Mochizuki[1], Katsushige Matsubara[1], Keisuke Matsumoto[1], Chi Nguyen[2], Tetsuya Shibayama[1], Kenichi Iwata[1], Katsuya Mizumoto[1], Takahiro Irita[3], Hirotaka Hara[3], Toshihiro Hattori[1]*
Paper [4.4] Affiliation: *[1]Renesas System Design, Tokyo, Japan; [2]Renesas Design Vietnam, Ho Chi Minh City, Vietnam; [3]Renesas Electronics, Tokyo, Japan*
Subcommittee Chair: *Stephen Kosonocky, Advanced Micro Devices, Fort Collins, CO; Digital Architectures and Systems*

CONTEXT AND STATE OF THE ART

- Today's handheld devices demand ever increasing performance, necessitating the use of multiple heterogeneous cores and graphics engines in most advanced technology nodes.
- To achieve higher performance and energy efficiency within power and thermal limits of mobile processors, innovative architectural and circuit-level techniques are required.
- Computing is increasingly used in today's Integrated Automobile Cockpit Systems for vehicle safety and infotainment.

TECHNICAL HIGHLIGHTS

- **Intel introduces its sixth generation Core processor.**

- In Paper 4.1, Intel presents its sixth-generation Core processor, a 14nm fully featured SoC, which provides comparable performance for less than 50% power versus a 22nm Ultrabook processor.

- **MediaTek incorporates three processor variants on a single die having different performance/power trade-offs.**

- In Paper 4.3, MediaTek presents industry's first tri-cluster, 10-core CPU, featuring three ARMv8a CPU clusters optimized for 1.4GHz, 2.0GHz, and 2.5GHz operation in a 20nm high-κ metal-gate process. Compared to dual-cluster CPUs, the addition of a third cluster provides 40% higher overall performance with 40% improved power efficiency.

- **Renesas presents an SoC integrating 17 video processors (of 6 different types) for automobile applications.**

- In Paper 4.4, Renesas presents a 12-channel HD-video-processing SoC, implemented in 16nm FinFET CMOS, with 197mW power consumption and 70ms video latency for automobile infotainment and driver-assistance applications.

APPLICATIONS AND ECONOMIC IMPACT

- These processors represent a new level of performance and integration, as well as innovative circuit techniques to deliver significantly increasing performance and energy efficiency. These efficient engines will enable mobile devices to meet the needs for the world's growing mobile computing ecosystem.

- The use of the 14nm technology node provides increased performance and higher levels of integration by combining an ever-expanding list of features onto a single die. This enables a new generation of energy-efficient, lower cost computing systems.

- Heterogeneous multi-core CPUs have expanded from their use in desktops and laptops into smart phones and tablets, and 64b mobile processors are now available.

- The market for mobile SoCs is predicted to be 5× larger than the traditional PC market by 2017, according to 2013 IDC Worldwide Smart Connected Device Tracker forecast data. These SoCs must satisfy mobile market needs for high performance and low power, and consumer desires for long battery life.

- Competition is fierce in the global smartphone market, estimated to be $400 billion in 2015.

- As the demand for safe driving grows, advanced driver-assistance systems need higher detection rates for obstacles in a vehicle's path. High-performance and low-power video processing chips for advanced driver-assistance systems have the potential to reduce accident rates and save lives.

- Today's Car Information Systems (CISs) provide automobile infotainment, including navigation systems and AV playing/recording. This automobile semiconductor market is projected to be $30 billion in 2015.

Session 5 Highlights: Analog Techniques

[5.2] A 118dB PSRR, 0.00067% (-103.5dB) THD+N and 3.1W Fully-Differential Class-D Audio Amplifier with PWM Common-Mode Control

W. Wang, Y. Lin
MediaTek, Hsinchu, Taiwan

Subcommittee Chair: Axel Thomsen, *Cirrus Logic, Austin, Analog Subcommittee*

CONTEXT AND STATE OF THE ART

- Class-D amplifiers are the most power-efficient audio amplifiers. The challenge for these amplifiers is to achieve the linearity and noise performance of less power-efficient architectures such as Class-AB. Additionally, they tend to be sensitive to variations in the power supply.

TECHNICAL HIGHLIGHTS

- **Highest PSRR and excellent linearity in Class-D audio amplifier**
- In Paper 5.2, the Class-D audio amplifier adopts PWM common-mode control to enhance PSRR and linearity performance. 118dB PSRR and 0.00067%(-103.5dB) THD+N are achieved.

APPLICATIONS AND ECONOMIC IMPACT

- High linearity, high PSRR, and low noise allow to build portable and compact audio devices with excellent hifi performance.

Session 5 Highlights: Analog Techniques

[5.7] A 39.25MHz 278dB FOM 19µW LDO-Free Stacked-Amplifier Crystal Oscillator (SAXO) Operating at I/O Voltage

S. Iguchi, T. Sakurai, and M. Takamiya
University of Tokyo, Tokyo, Japan

Subcommittee Chair: Axel Thomsen, *Cirrus Logic, Austin, Analog Subcommittee*

CONTEXT AND STATE OF THE ART

- Crystal oscillators are key building blocks for communication devices. For example, their power consumption is an important part of the power budget for wireless sensor nodes. It is difficult to reduce their power consumption while maintaining reliable oscillation.

TECHNICAL HIGHLIGHTS

- **Press Headline for Paper 5.7 – Best power efficiency for a crystal oscillator**
- By stacking 4 amplifiers, the proposed 3.3V, 39.25MHz, 19µW LDO-free stacked-amplifier crystal oscillator (SAXO) in 65nm CMOS consumes the lowest supply current of 5.8µA and the highest FOM of 278dB in the previously published crystal oscillators.

APPLICATIONS AND ECONOMIC IMPACT

- Power reduction in wireless sensor nodes is important to increase battery life and enable power independence through energy harvesting.

Session 6 Highlights: Image Sensors

[6.9] 1.1μm 33Mpixel 240fps 3D-Stacked CMOS Image Sensor with 3-Stage Cyclic-Based Analog-Digital Converters
[6.1] An Over 120dB Purely Simultaneous Wide-Dynamic-Range and 1.6e⁻ Ultra-Low-Reset-Noise Organic Photoconductive Film CMOS Image Sensor

Paper 6.1 Authors: *Masashi Murakami, Yoshihiro Sato, Junji Hirase, Ryota Sakaida, Masaaki Yanagida, Tokuhiko Tamaki, Masayuki Takase, Hidenori Kanehara, Masashi Murakami, Yasunori Inoue*
Paper 6.1 Affiliation: *Panasonic, Osaka, Japan*
Paper 6.9 Authors: *Toshiki Arai[1], Toshio Yasue[1], Hiroshi Shimamoto[1], Tomohiko Kosugi[3], Sungwook Jun[3], Satoshi Aoyama[3], Ming-Chieh Hsu[3], Yuichiro Yamashita[3], Hirofumi Sumi[3], Shoji Kawahito[4]*
Paper 6.9 Affiliation: *[1]NHK Science & Technology Research Laboratories, Tokyo, Japan, [2]Brookman Technology, Hamamatsu, Japan, [3]TSMC, Hsinchu, Taiwan, [4]Shizuoka University, Hamamatsu, Japan*

Subcommittee Chair: *Makoto Ikeda, University of Tokyo, Tokyo, Japan, IMMD*

CONTEXT AND STATE OF THE ART

- The trend towards 3D wafer-level stacking for integration of the sensor substrate with an independent CMOS substrate is continuing to enable designs with large pixel array area to base chip area ratio, high pixel count, high frame rate and reduced power and noise.
- Integration of CMOS with organic film is demonstrating increased intrascene wide dynamic range and global shutter capabilities.

TECHNICAL HIGHLIGHTS

- **NHK Science & Technology Lab reports a 3D Stacked CMOS Image Sensor for UHDTV that will enable even more realistic user experiences**

  In Paper 6.9, NHK Science & Technology Lab presents a 33Mpixel 240fps CMOS image sensor operating at 3W with 12b 3-stage pipelined ADCs at 4.4μm pitch using hybrid-stacking technology and pixel size of 1.1μm.

- **Panasonic introduces a high-dynamic-range high-fill-factor organic photoconductive film image sensor**

  In Paper 6.1, Panasonic presents an organic photoconductive film CMOS image sensor with 1.6e⁻ reset noise. A dual-sensitivity pixel with capacitive-coupled feedback noise cancellation is implemented to achieve 123.8dB intrascene wide dynamic range.

APPLICATIONS AND ECONOMIC IMPACT

- NHK Science & Technology Research Lab is developing high-resolution, high-speed, compact image sensors for cameras that will enable the migration to 8K UHDTV. Businesses and R&D related to UHDTV will stimulate growth in imaging, data transmission and display to provide highly realistic and sensational video contents to the home.
- The organic photoconductive film CMOS image sensor by Panasonic extends dynamic range by improving both the low-light sensitivity and full-well capacity for applications in automotive, autonomous transportation systems, machine vision, and security and surveillance.

Session 7 Highlights: Nonvolatile Memory Solutions

[7.1] 256Gb 3b/cell V-NAND Flash Memory with 48 Stacked WL Layers
[7.7] A 768Gb 3b/cell 3D-Floating-Gate NAND Flash Memory

Paper 7.1 Authors: *Dongku Kang et al.*
Paper 7.1 Affiliation: *Samsung Electronics, Hwaseong, Korea*
Paper 7.7 Authors: *Tomoharu Tanaka[1], Mark Helm[2], Tommaso Vali[3], Ramin Ghodsi[2], Koichi Kawai[1], Jae-Kwan Park[2], Shigekazu Yamada[1],Feng Pan[2], Yuichi Einaga[1], Ali Ghalam[2], Toru Tanzawa[1], Jason Guo[2], Takaaki Ichikawa[1], Erwin Yu[2], Satoru Tamada[1],Tetsuji Manabe[1], Jiro Kishimoto[1], Yoko Oikawa[1], Yasuhiro Takashima[1], Hidehiko Kuge[1], Midori Morooka[1], Ali, Mohammadzadeh[2], Jong Kang[2], Jeff Tsai[2], Emanuele Sirizotti[3], Eric Lee[2], Luyen Vu[2], Yuxing Liu[2], Hoon Choi[2], KwonsuCheon[2], Daesik Song[2], Daniel Shin[2], Jung Hee Yun[2], Michele Piccardi[2], Kim-Fung Chan[2], Yogesh Luthra[2], DheerajSrinivasan[2], Srinivasarao Deshmukh[2], Kalyan Kavalipurapu[2], Dan Nguyen[2], Girolamo Gallo[3], Sumant Ramprasad[2],Michelle Luo[2], Qiang Tang[2], Michele Incarnati[3], Agostino Macerola[3], Luigi Pilolli[3], Luca De Santis[3], Massimo Rossini[3],Violante Moschiano[3], Giovanni Santin[3], Bernardino Tronca[3], Hyunseok Lee[2], Vipul Patel[2], Ted Pekny[2], Aaron Yip[2],Naveen Prabhu[4], Purval Sule[4], Trupti Bemalkhedkar[4], Kiranmayee Upadhyayula[4], Camila Jaramillo[4]*
Paper 7.7 Affiliation: *[1] Micron, Tokyo, Japan, [2]Micron, San Jose, CA, [3]Micron, Avezzano, Italy, [4]Intel, Folsom, CA*
Subcommittee Chair: *Leland Chang, IBM, Yorktown Heights, New York, Memory*

CONTEXT AND STATE OF THE ART

- The new cell type and architecture of 3D NAND Flash memory technology builds upon the introduction of Samsung's 2nd generation 3D V-NAND Flash memory presented at ISSCC last year.
- 3b/cell technology becomes mainstream for 3D NAND Flash to continue solid cost per bit reduction.

TECHNICAL HIGHLIGHTS

- **3b/cell 256Gb 3D NAND Flash**
    - [7.1] Samsung's 3rd generation 3D NAND Flash memory of 48 stacked wordline layers with a conventional 2-plane architecture
    - [7.1] 53.2MB/s programming throughput and 1Gb/s I/O bandwidth.

- **3b/cell 768Gb 3D NAND Flash**
    - [7.7] Highest-density 768Gb 3D NAND Flash memory based on a floating gate memory cell technology achieving 4.29Gb/mm^2
    - [7.7] 4-plane architecture with X-decoders and page buffers all placed underneath the memory cell array

APPLICATIONS AND ECONOMIC IMPACT

- With the introduction of monolithic 3D NAND Flash with densities of 256Gb or more, NAND Flash will continue to be the major player in storage media.
- High-density 3D NAND Flash memory will contribute to the growth of the SSD market, which is expected to be well over $20 billion USD in 2016.

Session 8 Highlights: Low-Power Digital Circuits

[8.1] A 4×4×2 Homogeneous Scalable 3D Network-on-Chip Circuit with 326MFlit/s 0.66pJ/b Robust and Fault-Tolerant Asynchronous 3D Links
[8.3] A 200mA Digital Low-Drop-out Regulator with Coarse-Fine Dual Loop in Mobile Application Processors
[8.8] iRazor: 3-Transistor Current-Based Error Detection and Correction in an ARM Cortex-R4 Processor

Paper 8.1 Authors: *P. Vivet[1], Y. Thonnart[1], R. Lemaire[1], E. Beigné[1], C. Bernard[1], F. Darve[1], D. Lattard[1], I. Miro Panades[1], C. Santos[1], F.Clermidy[1], S. Cheramy[1], F. Pétrot[2], E. Flamand[3], J. Michailos[3]*
Paper 8.1 Affiliation: *[1]CEA-LETI, Grenoble, France, [2]TIMA, Grenoble, France, [3]STMicroelectronics, Grenoble, France*
Paper 8.3 Authors: *M.Y. Lee[1], M. Jung[2], S. Singh[1], T.H. Kong[1], D.Y. Kim[1], K.H. Kim[1], S.H. Kim[1], J.J. Park[1], H.J. Park[1], G.H. Cho, KAIST[2]*
Paper 8.3 Affiliation: *[1]Samsung Electronics, [2]KAIST, Korea*
Paper 8.8 Authors: *Y. Zhang[1], M. Khayatzadeh[1], K. Yang[1], M. Saligane[1], M. Alioto[2], D. Blaauw[1], D. Sylvester[1]*
Paper 8.8 Affiliation: *[1]University of Michigan, Ann Arbor, MI, [2]National University of Singapore, Singapore*

Subcommittee Chair: Stefan Rusu, TSMC, San Jose, CA, Digital Circuits

CONTEXT AND STATE OF THE ART

- To realize smaller form factor and higher computational density, 3D integration using through-silicon vias (TSVs) is considered as promising due to shortened communication distances. Reliable links have to be provided with fault tolerance mechanisms.
- Intelligent power management is applied to reduce energy consumption and is realized by integrating the power management unit on the same die. Large power fluctuations require fast response time of on-die power delivery circuits.
- Owing to reduced supply voltage margins caused by process variation, temperature and aging, some adaptive techniques, as well as error-correcting architectures in microprocessors are investigated. Key requirements to integrate more complex systems are smaller area overhead to minimize cost and higher scalability.

TECHNICAL HIGHLIGHTS

CEA-LETI demonstrates the first 3D homogeneous NoC, providing the fastest 3D link performance with the lowest energy consumption.

- In Paper 8.1, CEA-LETI describes a homogeneous 3D circuit in 65nm using a 4×4×2 asynchronous Network-on-Chip, fully scalable in a face-to-back configuration, targeting MIMO telecom applications. It uses robust self-adaptive asynchronous 3D links, which integrate ESD protection and an extendible test and fault-tolerant architecture. Compared to previous 3D-stacked circuits, it achieves the lowest energy consumption on 3D I/O power supply at 0.32pJ/b, and the highest data rate at 326Mb/s.

Samsung develops an LDO suitable for large load current variation for mobile processors.

- In Paper 8.3, Samsung presents an LDO with two loops for precision output, which are a coarse loop using a current-mirror flash ADC and a fine loop using shift registers. The proposed LDO provides up to 200mA of load current and occupies an area of 0.021mm^2 in 28nm. The output voltage droop is about 120mV for load variation of 90% of the maximum supported current load.

The University of Michigan demonstrates a 40nm ARM Cortex-R4 microprocessor with a small area overhead Razor-FF, named iRazor.

- In Paper 8.8, the University of Michigan presents iRazor, an error detection and correction design approach that uses a lightweight current-based detector. Only three additional transistors are needed per storage element, yielding 4.3% area overhead over a standard D-type flip-flop. iRazor is implemented in an ARM Cortex-R4 microprocessor in 40nm to demonstrate automated insertion in a large processor. At the typical corner, the proposed design achieves 1.3× throughput gain and 45% energy reduction with 13.6% area overhead relative to a baseline design.

APPLICATIONS AND ECONOMIC IMPACT

- For coming IoE era, intelligent sensors, smart cards and medical equipment will greatly impact our quality of life and the overall market for such devices is expected to grow. These devices require even lower power with smaller form factors, necessitating intelligent power management.
- General homogenous 3D NoCs are expected to bring lower power consumption and higher density computation. Integrated LDOs for mobile processors will lower the cost of mobile phones. Low-area-overhead Razor techniques can lower the supply voltage of microprocessors and reduce the PVT and aging margins drastically with modest cost overhead.

Session 9 Highlights: High-Performance Wireless

[9.1] A 45nm CMOS RF-to-Bits LTE/WCDMA FDD/TDD 2×2 MIMO Base-Station Transceiver SoC with 200MHz RF Bandwidth
[9.2] A Scalable 0.1-to-1.7GHz Spatio-Spectral-Filtering 4-Element MIMO Receiver Array with Spatial Notch Suppression Enabling Digital Beamforming

Paper 9.1 Authors: Nikolaus Klemmer, Siraj Akhtar, Venkatesh Srinivasan, Petteri Litmanen, Himanshu Arora, Satish Uppathil, Amneh Akour, Vicky Wang, Mounir Fares, Fikret Dulger, Aaron Frank, Diptendu Ghosh, Srinadh Madhavapeddi, Hamid Safiri, Jaimin Mehta, Atul Jain, Srinivas Aluri, Hunsoo Choo, Eric Zhang, Chan Fernando, Shankar Ramakrishnan, Rajagopal K.A., Vasudev Sinari, Vijay Baireddy, Madhu Rao and Saikrishna Joginipally
Paper 9.1 Affiliation: Texas Instruments, Dallas, TX

Paper 9.2 Authors: Linxiao Zhang[1], Arun Natarajan[2] and Harish Krishnaswamy[1]
Paper 9.2 Affiliation: [1]Columbia University, New York, NY, [2]Oregon State University, Corvallis, Oregon

Subcommittee Chair: *Aarno Pärssinen, University of Oulu, Oulu, Finland; Wireless Subcommittee*

CONTEXT AND STATE OF THE ART

- Highly integrated cellular transceivers for mobile applications have been available for some years but the need for densely populated low-cost base stations brings high-level integration to that domain with significantly more stringent performance requirements than in mobile applications.
- MIMO arrays have been classically designed to enhance data-rate and range but as radio networks are becoming denser special emphasis must be paid to interference suppression.

TECHNICAL HIGHLIGHTS

- **The first cellular CMOS base-station 3G/4G transceiver for small-cell densely populated networks.**
  - **The RF Transceiver in Paper 9.1 meets very stringent performance requirements of modern cellular small-cell base stations and adapts sophisticated calibration techniques to achieve a clean transmission mask with very high adjacent-channel rejection**
- **A 4-element receiver array shows a maximum of 32dB rejection in a steerable notch direction to reduce susceptibility to radio interference**
  - **In Paper 9.2 specific techniques to implement spatial notches are presented.**

APPLICATIONS AND ECONOMIC IMPACT

- Higher cellular integration leads to lower bill-of-material and smaller footprint allowing dense base-station deployment.
- Digital beamforming is enabled to enhance data-rate and link reliability by using MIMO receivers.

Session 10 Highlights: Advanced Wireline Transceivers and PLLs

[*10.6*] *A 6.75-to-8.25GHz, 250fs$_{rms}$ Integrated-Jitter 3.25mW Rapid On/Off PVT-Insensitive Fractional-N Injection-Locked Clock Multiplier in 65nm CMOS*

Paper 10.6 Authors: Ahmed Elkholy, Ahmed Elmallah, Mohamed Elzeftawi, Ken Chang, Pavan Hanumolu
Paper 10.6 Affiliation: University of Illinois, Urbana-Champaign and Xilinx, Inc.

Subcommittee Chair: *Daniel Friedman, IBM, Yorktown Heights, NY, USA, Wireline*

CONTEXT AND STATE OF THE ART

- Frequency multipliers that generate low-noise, high-frequency clocks are key building blocks in all high performance wireline transceivers.
- Among all the different clock multiplier architectures, injection-locked clock multipliers (ILCMs), especially LC-oscillator-based ILCMs, achieve the lowest phase noise as well as fast locking time.
- However, LC-oscillator-based ILCMs to date have been limited only to integer-N operation. In other words, these ILCMs are not capable of generating output frequencies that are non-integer multiples of the reference frequency.

TECHNICAL HIGHLIGHTS

- This paper presents an LC oscillator based ILCM capable of fractional-N frequency multiplication.
- The ILCM can achieve fast frequency/phase locking, which enables turning off the ILCM to save power when not in use.
- The ILCM achieves the best figure-of-merit in both integer-N (-255dB) and fractional-N (-247dB) modes.

APPLICATIONS AND ECONOMIC IMPACT

- The proposed technique extends the use of LC-oscillator-based ILCMs to applications requiring fractional-N frequency multiplication.
- With this ILCM, one can easily synthesize multiple frequencies from a single clock source, saving cost and power consumption.
- Rapid on/off capability can extend battery life of a variety of mobile devices.

Session 11 Highlights: Sensors and Displays

[11.2] 3D Ultrasonic Fingerprint Sensor-on-a-Chip

Paper Authors: Hao-Yen Tang[1], Yipeng Lu[3], Fari Assaderaghi[2], Mike Daneman[2], Xiaoyue Jiang[1], Martin Lim[2], Xi Li[1], Eldwin Ng[2], Utkarsh Singhal[1], Julius M.Tsai[2], David A. Horsley[3], Bernhard E. Boser[1]
Paper Affiliation: [1]University of California, Berkeley, CA, [2]InvenSense, San Jose, CA, [3]University of California, Davis, CA
Subcommittee Chair: *Makoto Ikeda, University of Tokyo, Tokyo, Japan, IMMD*

CONTEXT AND STATE OF THE ART

- Increasing popularity of mobile devices such as smartphones in applications including smart payments and personal health sets a pressing need for improved security without compromising ease of use.
- Fingerprint recognition has emerged as a particularly attractive option. Unfortunately, present capacitive solutions suffer from poor accuracy in the presence of contamination such as perspiration, and are easily compromised, e.g., with fingerprints recovered from the device surface. Optical solutions are more robust but add substantial costs.

TECHNICAL HIGHLIGHTS

- **A 3D fingerprint sensor for dermal and sub-dermal imaging with robust performance, tamper-free operation, and perspiration resistance**

  The 3D ultrasonic fingerprint sensor consists of a 110×56 PMUT array bonded to a CMOS chip. The sensor consumes only 280μJ to record a 431×582 dpi image in 2.64ms. Its unique ability to image both the surface epidermis and sub-surface dermis fingerprint make it insensitive to perspiration and resistant to spoofing. This enables highly robust, low-cost personal ID sensing.

APPLICATIONS AND ECONOMIC IMPACT

- The availability of 3D ultrasonic fingerprint imaging will lead to new levels of security in mobile devices by enabling low-cost personal identification.

Session 12 Highlights: Efficient Power Conversion

[12.2] A 94.6%-Efficiency Fully Integrated Switched-Capacitor DC-DC Converter in Baseline 40nm CMOS Using Scalable Parasitic Charge Redistribution

Nicolas Butzen, Michiel Steyaert,
KU Leuven, Leuven, Belgium

Subcommittee Chair: Axel Thomsen, *Cirrus Logic, Austin, TX, Analog Subcommittee*

CONTEXT AND STATE OF THE ART

- Switched-capacitor DC-DC converters offer the promise of very compact power converters, but they suffer from several loss mechanisms that limit their efficiency below what is achievable with inductive power converters. It is important to address the efficiency issues to make this technology compelling.

TECHNICAL HIGHLIGHTS

- **New switching technique substantially reduces main loss mechanism in integrated switched-capacitor DC-DC converters**
- In Paper 12.2, KU Leuven presents a way to diminish parasitic capacitor impact on efficiency in multistage reconfigurable switched-capacitor DC-DC converters, reaching best-in-class efficiency results.

APPLICATIONS AND ECONOMIC IMPACT

- Switched-capacitor DC-DC converters are becoming a viable alternative to inductor-based counterparts for efficient power conversion, reducing the number of off-chip components and decreasing the system cost. Efficiencies approach those of inductive converters. This results in further miniaturization of power supplies.

Session 12 Highlights: Efficient Power Conversion

[12.5] A 2MHz 12-to-100V 90%-Efficiency Self-Balancing ZVS Three-Level DC-DC Regulator with Constant-Frequency AOT V2 Control and 5ns ZVS Turn-On Delay

Jing Xue, Hoi Lee,
University of Texas at Dallas, TX

Subcommittee Chair: Axel Thomsen, *Cirrus Logic, Austin, TX, Analog Subcommittee*

CONTEXT AND STATE OF THE ART

- Increased efficiency and reduced size are the never ending goals in switched-mode power-supply designs.

TECHNICAL HIGHLIGHTS

- **Tri-level architecture with floating capacitor allows very compact DC-DC converter.**
- In Paper 12.5, the Technical University of Texas, Dallas, shows how to employ the tri-level architecture to use low voltage devices in a high-voltage DC-DC converter. This allows high switching speeds and small inductors without affecting the efficiency.

APPLICATIONS AND ECONOMIC IMPACT

- The physical volume of power supplies is an important factor in the size of electronic products. Higher efficiencies allow the use of smaller batteries. These are the key elements for more attractive, more capable and more lightweight portable devices.

Session 13 Highlights: Wireless Systems

[13.3] A 56Gb/s W-Band CMOS Wireless Transceiver

Paper 13.3 Authors: *K. Tokgoz[1], S. Maki[1], S. Kawai[1], N. Nagashima[1], J. Emmei[1], M. Dome[1], H. Kato[1], Y. Kawano[2], T. Suzuki[2], T. Iwai[2], Y. Seo[1], K. Lim[1], S. Sato[1], L. Ning[1], K. Nakata[1], K. Okada[1], A. Matsuzawa[1]*
Paper 13.3 Affiliation: *Tokyo Institute of Technology[1], Fujitsu Laboratory[2]*

Subcommittee Chair: *Aarno Pärssinen, University of Oulu, Oulu, Finland, Wireless Subcommittee*

CONTEXT AND STATE OF THE ART

- [13.3] Data communication speed has grown to Gb/s and will reach to several tens of Gb/s. Movies/Picture data transfer and back-haul communication will require much higher data-rates. The frequency band for this requirement is extended to higher than 60GHz.

TECHNICAL HIGHLIGHTS

- **Record breaking data-rate of 56Gb/s achieved at millimeter-Wave frequencies in CMOS**
- In Paper[13.3] the first single-chip transceiver achieving 56Gb/s using two frequency interleaved IF wideband signals in 65nm CMOS is demonstrated. This results in record 10pJ/bit efficiency in high-data-rate 16-QAM mm-Wave CMOS transceivers.

APPLICATIONS AND ECONOMIC IMPACT

- Extremely high-data-rate communication between devices over short distances will enable new applications.

Session 14 Highlights: Next-Generation Processing

[14.1] A 126.1mW Real-time Natural UI/UX Processor with Embedded Deep-Learning Core for Low-Power Smart Glasses
[14.5] Eyeriss: An Energy-Efficient Reconfigurable Accelerator for Deep Convolutional Neural Networks

Paper 14.1 Authors: *S. Park, S. Choi, J. Lee, M. Kim, J. Park, and H. Yoo*
Paper 14.1 Affiliation: *KAIST, Daejeon, Korea*
Paper 14.5 Authors: *Y. Chen[1], T. Krishna[1], J. Emer[1,2], V. Sze[1]*
Paper 14.5 Affiliation: *[1]Massachusetts Institute of Technology, Cambridge, MA; [2]Nvidia, Westford, MA*

Subcommittee Chair: *Stephen Kosonocky, AMD, Fort Collins, CO, Digital Architectures and Systems*

CONTEXT AND STATE OF THE ART

- Deep learning has recently demonstrated state-of-the-art accuracy on many computer vision tasks, such as object detection, recognition, and segmentation. However, real-time embedded evaluation of state-of-the-art deep learning networks requires the efficient execution of millions of convolution operations and memory accesses per second.
- Current state-of-the-art deep learning processors are inefficient or limited to small networks, unable to map the state-of-the-art deep learning networks necessary for next-generation user interfaces or autonomous vehicles.

TECHNICAL HIGHLIGHTS

Best-in-class accuracy in an audio-visual interface for smart glasses achieved by KAIST through integration of a multi-core deep learning processor.

- In Paper 14.1, KAIST presents a low-power natural UI/UX processor with an embedded deep learning engine for AR/HMD users implemented in 65nm CMOS. It achieves a 56.5% power efficiency improvement over the latest HMD processor, and ~2% higher recognition rate over the best-in-class pattern recognition processor.

First reported efficient deep-learning processor is proposed by MIT capable of flexibly mapping state-of-the-art deep neural networks.

- In Paper 14.5, MIT presents a 65nm CMOS energy-efficient deep convolutional neural network (CNN) accelerator featuring a spatial array of 168 processing elements fed by a reconfigurable on-chip network. The chip supports state-of-the-art CNNs, such as AlexNet, and is over 10× lower power and requires 4.7× fewer DRAM access per pixel than a mobile GPU.

APPLICATIONS AND ECONOMIC IMPACT

- The ability to perform highly accurate object detection, recognition and tracking is the key enabler towards different emerging application domains such as autonomous vehicles, natural human-machine interaction and augmented reality.
- Upcoming augmented reality devices, like smart glasses and displays are forecast to become a $120 billion business by 2020 according to Digi-Capital. The market for autonomous vehicles is also predicted to skyrocket. By 2025, a market size of $42 billion is estimated by Boston Consulting Group for autonomous cars, while BI Intelligence predicts a market of $13 billion for drones.

Session 15 Highlights: Oversampling Data Converters

[15.5] A 930mW 69dB-DR 465MHz-BW CT 1-2 MASH ADC in 28nm CMOS
[15.6] A 160MHz-BW 72dB-DR 40mW Continuous-Time ΔΣ Modulator in 16nm CMOS with Analog ISI-Reduction Technique

Paper 15.5 Authors: Y. Dong, J. Zhao, W. Yang, T. Caldwell, H. Shibata, R. Schreier, Q. Meng, J. Silva, D. Paterson and J. Gealow
Paper 15.5 Affiliation: *Analog Devices, Wilmington, MA, USA*
Paper 15.6 Authors: S-H. Wu, T-K. Kao, Z-M. Lee, P. Chen, J-Y. Tsai
Paper 15.6 Affiliation: *MediaTek, Hsinchu, Taiwan*

Subcommittee Chair: *Un-Ku Moon, Oregon State University, Corvallis, OR, Data Converters*

CONTEXT AND STATE OF THE ART

- Continuous-Time Delta-Sigma Modulators are well-suited for wireless receive chains due to their power efficiency and inherent anti-aliasing property. Looking to the future requirements for evolving wireless standards, these ADCs must digitize bandwidths in excess of 100MHz with high dynamic range and power efficiency.

TECHNICAL HIGHLIGHTS

- **Analog Devices demonstrates a 465MHz Bandwidth 69dB Dynamic Range Delta-Sigma ADC in 28nm CMOS**
- In paper number 15.5 Analog Devices describes a 28nm continuous-time 1-2 MASH ADC clocking at 8GHz. This ADC achieves the largest signal bandwidth (465MHz) thus far reported for a CMOS Delta-Sigma ADC.

- **MediaTek reports a 160MHz Bandwidth 72dB Dynamic Range Delta-Sigma ADC in 16nm CMOS while consuming only 40mW of power**
- In paper number 15.6 MediaTek describes a 4th-order continuous-time delta-sigma ADC in 16nm CMOS. The ADC uses an analog ISI-reduction technique in the feedback DAC to achieve 72dB DR with very good power efficiency.

APPLICATIONS AND ECONOMIC IMPACT

- The papers represent increasing bandwidths and improving power efficiency in continuous-time delta-sigma modulators. These enable the continued integration of continuous-time delta-sigma modulators in wideband wireless receive chains that are needed to address the demands of increasing cellular data throughput.

Session 16 Highlights: Innovations in Circuits and Systems Enabled by Novel Technologies

[16.1] A Nanogap Transducer Array on 32nm CMOS for Electrochemical DNA Sequencing

Paper 16.1 Authors: Drew Hall[1,2], Jonathan Daniels[1], Bibiche Geuskens[1], Noureddine Tayebi[1], Grace Credo[1], David Liu[1], Handong Li[1], Kai Wu[1], Xing Su[1], Madoo Varma[1], Oguz Elibol[1]

Paper 16.1 Affiliation: [1]Intel, Santa Clara, California, United States, [2]University of California, San Diego, California, United States

Subcommittee Chair: *Eugenio Cantatore, Eindhoven University of Technology, Eindhoven, The Netherlands, Technology Directions*

CONTEXT AND STATE OF THE ART

- Existing solutions for DNA sequencing either employ optical sensing techniques that are difficult to scale or molecular sensing methods that have low SNR.

TECHNICAL HIGHLIGHTS

A large and high-density scalable *Faradaic* electrochemical biosensing technique for DNA sequencing leveraging CMOS scaling while achieving high SNR

- Paper 16.1 presents an elegant implementation of nanogap transducers fabricated on top of CMOS.
- The 8,192 pixel nanogap transducer array is integrated with its microelectronic readout circuitry implemented in 32nm CMOS.

APPLICATIONS AND ECONOMIC IMPACT

- The proposed methodology paves the way towards smaller, lower cost DNA sequencing that can be integrated with electronics.

Session 16 Highlights: Innovations in Circuits and Systems Enabled by Novel Technologies

[16.2] A Keccak-Based Wireless Authentication Tag with per-Query Key Update and Power-Glitch Attack Countermeasures

Paper 16.2 Authors: Chiraag S. Juvekar[1], Hyung-Min Lee[1], Joyce Kwong[2], Anantha P. Chandrakasan[1]
Paper 16.2 Affiliation: *[1]Massachusetts Institute of Technology, Cambridge, MA, [2]Texas Instruments, Dallas, TX*
Subcommittee Chair: *Eugenio Cantatore, Eindhoven University of Technology, Eindhoven, The Netherlands, Technology Directions*

CONTEXT AND STATE OF THE ART

- Power glitch attacks (e.g., by malicious readers) form a major concern for wireless authentication tags as they could lead to breaches in security.

TECHNICAL HIGHLIGHTS

Secure operation is maintained by adding FeRAM based non-volatile flip-flops to the critical registers, preventing state losses and guaranteeing the necessary key updates.

- The implementation overhead of integrating the non-volatile flip-flops in the ASIC is 40% smaller than using conventional approaches.

APPLICATIONS AND ECONOMIC IMPACT

- The availability of such a low-cost and secure authentication methodology in the supply chain, which is robust to fault-injections and side channel attacks, will reduce counterfeiting and the associated economic losses.

Session 16 Highlights: Innovations in Circuits and Systems Enabled by Novel Technologies

[16.4] A Flexible EEG Acquisition and Biomarker Extraction System Based on Thin-film Electronics

[16.5] A Flexible Thin-Film Pixel Array with a Charge-to-Current Gain of 59μA/pC and 0.33% Non-Linearity and a Cost Effective Readout Circuit for Large-Area X-ray Imaging

Paper 16.4 Authors: Tiffany Moy, Liechao Huang, Warren Rieutort-Louis, Sigurd Wagner, James C. Sturm, and Naveen Verma
Paper 16.4 Affiliation: Princeton University, Princeton, NJ
Paper 16.5 Authors: Florian De Roose[1,2], Kris Myny[2], Soeren Steudel[2], Myriam Willigems[2], Steve Smout[2], Tim Piessens[3], Jan Genoe[1,2], Wim Dehaene[1,2]
Paper 16.5 Affiliation: [1]KULeuven, Leuven, Belgium, [2]imec, Leuven, Belgium, [3]ICsense, Leuven, Belgium
Subcommittee Chair: *Eugenio Cantatore, Eindhoven University of Technology, Eindhoven, The Netherlands, Technology Directions*

CONTEXT AND STATE OF THE ART

- The signals of flexible sensors on large-area foils degrade because of the long interconnects between the sensor array and the electronics.
- Amorphous silicon and IGZO TFT technologies are promising candidates to realize low-noise amplifiers on foil close to the sensors, preserving signal quality.

TECHNICAL HIGHLIGHTS

- **An EEG acquisition and classification system based on amorphous-silicon (a-Si) flexible thin-film electronics**
- The system consists of a-Si TFT low-noise chopper-stabilized amplifiers with a noise PSD of 230nV/√Hz and a-Si TFT compressive-sensing scanning circuits. Spectral-energy features are extracted from the compressed signals, and seizure detection from the extracted features is demonstrated with error rate of <4%.

- **A flexible and large-area self-aligned amorphous-IGZO (a-IGZO) TFT active pixel array for X-ray imaging**
- The designed active pixel achieves a 137x higher charge-to-current gain and 2.9x better linearity compared to the state-of-the-art. A resolution of 254ppi with 50Hz frame rate is demonstrated.

APPLICATIONS AND ECONOMIC IMPACT

- The a-Si chopper-stabilized amplifier enables EEG systems on flexible foils, which are low-cost and comfortable.

- The a-IGZO readout circuit enables compact and low-cost X-ray imagers for medical and security applications.

Session 17 Highlights: SRAM

[17.1] A 10nm FinFET 128Mb SRAM with Assist Adjustment System for Power, Performance, and Area Optimization

Paper 17.1 Authors: *Taejoong Song, Woojin Rim, Sunghyun Park, Yongho Kim, Jonghoon Jung, Giyong Yang, Sanghoon Baek, Jaeseung Choi, Bongjae Kwon, Yunwoo Lee, Sungbong Kim, Gyuhong Kim, Hyo-Sig WonJa-Hum Ku, Sunhom Paak, ES Jung, Steve Park*

Paper 17.1 Affiliation: *Samsung Electronics, Hwaseung-Si, Korea*

Subcommittee Chair: *Leland Chang, IBM, Yorktown Heights, New York, Memory*

CONTEXT AND STATE OF THE ART

- SRAM remains a critical challenge to technology scaling.
- Since the demonstration of 22nm FinFET, a 2-year cadence of technology scaling has been maintained.
- This year, Samsung demonstrates the smallest SRAM bit cell to date in a leading edge 10nm FinFET technology.

TECHNICAL HIGHLIGHTS

- **Samsung demonstrates a 10nm SRAM with the smallest bit cell reported to date**
- In Paper 17.1, Samsung presents a 128Mb SRAM fabricated in 10nm FinFET technology featuring the smallest bit cells to date with 0.040μm^2 high density (HD) and 0.049μm^2 high current (HC) offerings. Integrated assist circuitry improves Vmin for the HD and HC bitcells by 130mV and 80mV, respectively.

APPLICATIONS AND ECONOMIC IMPACT

- Demonstrates FinFET transistor scaling to the 10nm node with extremely aggressive bitcell density.
- This technology and innovative circuit techniques enable low-voltage operation to power the Internet of Everything.

Session 17 Highlights: SRAM

[17.2] 5.6Mb/mm² 1R1W 8T SRAM Arrays Operating down to 560mV Utilizing Small-Signal Sensing with Charge Shared Bitline and Asymmetric Sense Amplifier in 14nm FinFET CMOS Technology

Paper 17.2 Authors: *John Keane, Jaydeep Kulkarni, Satyanand Nalam,* Zheng Guo, Eric Karl, Kevin Zhang

Paper 17.2 Affiliation: *Intel, Hillsboro, OR*

Subcommittee Chair: *Leland Chang, IBM, Yorktown Heights, New York, Memory*

CONTEXT AND STATE OF THE ART

- 8T SRAM bitcells have historically been used in applications where performance requirements supersede density requirements.
- This year, Intel improves the density of 8T SRAM arrays in their leading edge 14nm FinFET technology by utilizing small signal sense techniques, making 8T arrays compelling in both performance and area.

TECHNICAL HIGHLIGHTS

- **Intel demonstrates high density 8T SRAM in 14nm for low-voltage operation**
- In Paper 17.2, Intel presents a 5.6Mb/mm² embedded 8T SRAM in 14nm FinFET technology for low-voltage operation. The introduction of advanced sense amplifier techniques enables the use of 256-bit bitlines, which maximizes the array efficiency of the 0.106µm² cell. An operation Vmin of 560mV is demonstrated.

APPLICATIONS AND ECONOMIC IMPACT

- Extends the process entitlement of 14nm FinFET technology through improvements in circuit design.

Session 18 Highlights: High Bandwidth DRAM

[18.1] A 20nm 9Gb/s/pin 8Gb GDDR5 DRAM with an NBTI Monitor and Jitter Reduction Techniques with Improved Power Distribution

Paper 18.1 Authors: *Hye-Yoon Joo, Seung-Jun Bae, Young-Soo Sohn, Young-Sik Kim, Kyung-Soo Ha, Min-Su Ahn, Young-Ju Kim, Yong-Jun Kim, Young-Ju Kim, Ju-Hwan Kim, Won-Jun Choi, Chang-Ho Shin, Soo Hwan Kim, Byeong-Cheol Kim, Seung-Bum Ko, Kwang-Il Park, Seong-Jin Jang, Gyo-Young Jin,*

Paper 18.1 Affiliation: *Samsung Electronics, Hwaseong, Korea*

Subcommittee Chair: *Leland Chang, IBM, Yorktown Heights, New York, Memory*

CONTEXT AND STATE OF THE ART

- High-bandwidth DRAMs are strongly demanded in graphics and high-performance computing.
- Since the demonstration of 40nm 7Gb/s/pin GDDR5 products at ISSCC in 2011, higher bandwidth GDDR5 products are now being developed.
- This year, Samsung demonstrates 9Gb/s/pin GDDR5 using advanced 20nm technology.

TECHNICAL HIGHLIGHTS

- **Samsung demonstrates the highest bandwidth (9Gb/s/pin) GDDR5 to date.**
- Dual-mode equalizing/duty-cycle correcting receiver and on-die de-emphasis is utilized to enhance the bandwidth
- Reliability is guaranteed by an on-chip NBTI monitoring.

APPLICATIONS AND ECONOMIC IMPACT

- Enables higher resolution and smoother motion display in graphic applications such as gaming and emerging visual reality systems.

Session 18 Highlights: High Bandwidth DRAM

[18.2] A 1.2V 20nm 307GB/s HBM DRAM with At-Speed Wafer-Level IO Test Scheme and Adaptive Refresh Considering Temperature Distribution

Paper 18.2 Authors: Kyomin Sohn , *Reum Oh, Chi-Sung Oh, Seong-Young Seo, Min-Sang Park, Dong-Hak Shin, Won-Chang Jung, Sang-Hoon Shin, Je-Min Ryu, Hye-Seung Yu, Jae-Hun Jung, Kyung-Woo Nam, Seouk-Kyu Choi, Jae-Wook Lee, Uksong Kang, Young-Soo Sohn, Jung-Hwan Choi, Chi-Wook Kim, Seong-Jin Jang, Gyo-Young Jin,*

Paper 18.2 Affiliation: *Samsung Electronics, Hwaseong, Korea*

Subcommittee Chair: *Leland Chang, IBM, Yorktown Heights, New York, Memory*

CONTEXT AND STATE OF THE ART

- HBM is a leading candidate as main memory for power hungry applications
- A 128GB/s bandwidth HBM was demonstrated at ISSCC in 2014.
- This year, Samsung demonstrates the HBM2 standard with 307GB/s bandwidth in 20nm technology.

TECHNICAL HIGHLIGHTS

- **Samsung introduces HBM2 for high-performance computing and graphics.**
- In paper 18.1, Samsung presents 2H/4H/8H stack HBM2 in 20nm technology with the highest bandwidth of 307GB/s/stack.
- An at-speed wafer level μbump IO test scheme and temperature-aware refresh scheme are implemented.

APPLICATIONS AND ECONOMIC IMPACT

- This technology and the innovative circuit techniques enable high performance computing, accelerators and small form factor graphics cards.

Session 19 Highlights: Digital PLLs

[19.1] A 0.5-to-9.5GHz 1.2μs-Lock-Time Fractional-N DPLL with ±1.25% UI Period Jitter in 16nm CMOS for Dynamic Frequency and Core-Count Scaling in SoC

[19.4] A 0.17-to-3.5mW 0.15-to-5GHz SoC PLL with 15dB Built-In Supply Noise Rejection and Self-Bandwidth Control in 14nm CMOS

Paper 19.1 Authors: *Fazil Ahmad, Greg Unruh, Amruthalyer, Pin-En Su, SherifAbdalla, Bo Shen, Mark Chambers, Ichiro Fujimori*
Paper 19.1 Affiliation: *Broadcom Corporation, Irvine, CA*

Paper 19.4 Authors: *Kuan-Yueh She, Syed Feruz Syed Farooq, Yongping Fan, Khoa Minh Nguyen, Qi Wang, Amr Elshazly, Nasser Kurd, Intel*
Paper 19.4 Affiliation: *Intel, Hillsboro, OR*
Subcommittee Chair: *Stefan Rusu, TSMC, San Jose, CA, Digital Circuits*

CONTEXT AND STATE OF THE ART

- Today's multicore processors and complex SoCs incorporate power management techniques such as Dynamic Frequency Scaling (DFS) requiring wide-range and low jitter clock generation across many cores.
- The emergence of digital PLLs (DPLLs) is driving cost reduction in modern processors as they eliminate custom steps and components.
- To support wide-range DFS, a PLL needs to support rapid frequency change and fast locking, both without frequency overshoot, so that SoCs can continue operation. Such PLLs are also required to have a wide output frequency range, low period jitter and low power to improve the global energy efficiency.

TECHNICAL HIGHLIGHTS

Broadcom proposes a DPLL enabling dynamic frequency and core-count scaling.

- In Paper 19.1, Broadcom presents a DPLL in 16nm CMOS. A dual-stage phase-acquisition-based loop filter is proposed for fast locking in 1.2μs without frequency overshoot. A nonlinear DCO achieves ±1.25% UI jitter over 0.5-9.5GHz.

Intel presents a modular PLL architecture with flexibility for varied SoC applications.

- In Paper 19.4, Intel presents a modular PLL architecture fabricated in 14nm CMOS. A new reference current generation circuit provides adaptive current to the charge pump and self-maintains the PLL bandwidth and stability providing 15dB of supply noise rejection. The PLL achieves 1.26ps integrated RMS jitter at 2.6mW at 4GHz and meets PCIe Gen2/Gen3 clocking specifications.

APPLICATIONS AND ECONOMIC IMPACT

- Advanced process node (14/16nm) demonstrations of digital PLLs (DPLLs) leverage cost savings of technology scaling.
- DPLLs are preferred in SoCs due to faster turnaround times, lower design costs, and improved technology portability.

Session 20 Highlights: RF-to-THz Transceiver Techniques

[20.1] A 300GHz 40nm CMOS Transmitter with 32-QAM 17.5Gb/s/ch Capability over 6 Channels

Paper Authors: Kosuke Katayama, Kyoya Takano, Shuhei Amakawa, Shinsuke Hara, Akifumi Kasamatsu, Koichi Mizuno, Kazuaki Takahashi, Takeshi Yoshida, and Minoru Fujishima.
Paper Affiliation: *Hiroshima University, Hiroshima, Japan; NICT, Koganei, Japan; Panasonic, Yokohama, Japan*

Subcommittee Chair: *Piet Wambacq, imec, Belgium, RF Subcommittee*

CONTEXT AND STATE OF THE ART

- Sub-mm-Wave and terahertz frequencies offer extremely wide bandwidths that enable very-high data-rate communications.
- Transmitters operating beyond f_{max} employ architectures that cannot support QAM and other complex modulation schemes.

TECHNICAL HIGHLIGHTS

- World's first 300GHz transmitter supporting complex modulation
- Paper 20.1 presents a new PA-less architecture that employs a cubic mixer, thereby enabling QAM transmission, and massive power combining. A 40nm CMOS 300GHz transmitter based on this architecture demonstrates a 17.5Gb/s/ch 32-QAM data transmission over 6 channels.

APPLICATIONS AND ECONOMIC IMPACT

- This transceiver architecture potentially enables short-range very-high data-rate applications, such as chip-to-chip and data-center communications.
- The use of channel bonding potentially enables data-rates approach 100Gbps.

Session 21 Highlights: Harvesting and Wireless Power

[21.4] A >78%-Efficient Light Harvester over 100-to-100klux with Reconfigurable PV-Cell Network and MPPT Circuit

Paper Authors: Inhee Lee, Wootaek Lim, Alan Teran, Jamie Phillips, Dennis Sylvester, David Blaauw
Paper Affiliation: University of Michigan, Ann Arbor, MI

Subcommittee Chair: Axel Thomsen, Cirrus Logic, Austin, TX, Analog

CONTEXT AND STATE OF THE ART

- Energy harvesting is an enabling technology to realize energy-autonomous Internet-of-Everything (IoE) nodes, and ambient light is a common energy source.
- Conventional inductor-based and switched-capacitor DC-DC converters cannot achieve high efficiency over a wide range of light intensity.

TECHNICAL HIGHLIGHTS

- **Light harvester with lowest standby power and highest energy efficiency**
- In Paper 21.4, a light harvester operating over 100-to-100klux with reconfigurable 7.8mm^2 photovoltaic-cell network is described. Instead of using a DC-DC converter, photovoltaic (PV) cells are reconfigured depending on the light intensity, thereby achieving more than 78% efficiency from 100lux to 100klux when charging a 1.5V-to-2.5V battery with a 7.8mm^2 PV-cell network.

APPLICATIONS AND ECONOMIC IMPACT

- Harvesting from light as presented here is one of the most promising energy sources. Increased efficiency from harvesters, together with nano-power design is the key to enabling energy-autonomous tiny IoE nodes.

Session 21 Highlights: Harvesting and Wireless Power

[21.8] An All-in-One (Qi, PMA and A4WP) 2.5W Fully Integrated Wireless Battery Charger IC for Wearable Applications

Paper Authors: Jong Tae Hwang, Dong Su Lee, Jong Hoon Lee, Sung Min Park, Ki Woong Jin, Min Jung Ko, Hyun Ick Shin, Sang Oh Jeon, Dae Ho Kim, Joon Rhee
Paper Affiliation: MAPS Inc., Yongin, Korea

Subcommittee Chair: Axel Thomsen, Cirrus Logic, Austin, TX, Analog

CONTEXT AND STATE OF THE ART

- For wearable applications, a contactless power transfer solution is one of the required features since exposed metal contacts for battery charging could be easily corroded by moisture and sweat. There are 3 standards for the wireless power transfer: Qi, PMA and A4WP.
- Conventional approaches integrating the 3 standards degrade the efficiency due to the interference from the different standards.

TECHNICAL HIGHLIGHTS

- **First All-In-One Fully Integrated Wireless Charger IC**
- In Paper 21.8, an All-in-One (Qi, PMA and A4WP) 2.5W Fully Integrated Wireless Battery Charger IC is described. The chip efficiency is 84% when the IC delivers 2W to a load at a 6.78MHz carrier frequency. The TX-to-RX efficiencies at Qi, PMA and A4WP at 2.5W are 63%, 62% and 54%, respectively.

APPLICATIONS AND ECONOMIC IMPACT

- Designs as presented here allow one receiver to work with all prevalent transmitters from 3 different standards. The presence of many wireless charging standards has made interoperability an important key for widespread adoption. Once these challenges are solved, wireless charging will make the charging of portable devices, wearables, and IoE sensor nodes much more convenient.

Session 22 Highlights: Systems and Instruments for Human-Machine Interfaces

[22.1] Implanted Integrated Circuit Requirements for Brain-Machine Interfaces

Paper 22.1 Authors: *C. Pandarinath, P. Nuyujukian, J. Henderson, K. Shenoy*
Paper 22.1 Affiliation: *Stanford University, Stanford, CA*

Subcommittee Chair: *Eugenio Cantatore, Eindhoven University of Technology, Eindhoven, The Netherlands*

CONTEXT AND STATE OF THE ART

- Brain-machine interfaces (BMIs) require implantable integrated circuits (ICs) to convert neural signals from the brain into control signals to be used by prosthetic limbs and/or other machines.
- To make BMIs suitable for widespread use, further progress in the following critical aspects of the system/circuit must be achieved: high performance, robustness, and integration/packaging.

TECHNICAL HIGHLIGHTS

For the first time in decades, ISSCC has an invited system talk part of a regular session:
Paper 22.1, which will focus on translating the biomedical requirements of BMI systems into IC design specifications.

- Based on recent advances in pre-clinical research with animals and preliminary human research participants, system and circuit specifications for widespread adoption of BMI systems are discussed.
- Various solutions for higher neural recording density, efficient signal acquisition/processing/transmission, system integration, and robust system operation are explored.

APPLICATIONS AND ECONOMIC IMPACT

- The continuous developments in BMIs are paving the way to help people with paralysis to restore their lost motor and/or communication functions.

Session 22 Highlights: Systems and Instruments for Human-Machine Interfaces

[22.3] A 141μW Sensor SoC on OLED/OPD Substrate for SpO_2/ExG Monitoring Sticker

Paper 22.3 Authors: Y. Lee[1], H. Lee, J. Jang, J. Lee, M. Kim, J. Lee, H. Kim, K. Lee, H. Cho, S. Yoo, H.-J. Yoo
Paper 22.3 Affiliation: KAIST, Daejeon, Korea

Subcommittee Chair: *Eugenio Cantatore, Eindhoven University of Technology, Eindhoven, The Netherlands, Technology Directions*

CONTEXT AND STATE OF THE ART

- High-autonomy wearable biomedical acquisition systems for vital sign monitoring are highly desirable for 24/7 health monitoring, and eventually migrate the point of care onto the body itself.
- Integrated specific solutions dedicated to either EEG, EMG, ECG (ExG) or PPG measurements have been demonstrated, however, efficient implementation of distributed systems that can measure both ExG and PPG and communicate via body in a cooperative way have not been shown until now.

TECHNICAL HIGHLIGHTS

- An on-body sticker-type ExG/SpO_2 distributed sensory platform co-integrates: red/green OLEDs and OPD for photo-plethysmography, electrodes for ExG measurements, CMOS SoCs and battery on a flexible patch-like PET substrate. The chips embed multi-modal AFE, body channel communication (BCC) transceivers and control functions.
- The biomedical hub and sensor nodes operate at 2.8 and 0.4mW, respectively, while communicating through a 100/500kb/s down/uplink BCC TRX to achieve the cooperation of several sensors. A COTS Bluetooth module assembled on the hub node ensures seamless wireless connection to the cloud via a smartphone/tablet.

APPLICATIONS AND ECONOMIC IMPACT

- Disposable wearable physiological signals acquisition and monitoring systems capable of measuring cooperatively oxygen saturation level (SpO_2) and electro-cardio/myo/encephalo-gram (ExG) have a large market opportunity.
- This device increases the patient's autonomy and reduces the healthcare costs significantly by facilitating cloud-based remote patient monitoring.

Session 23 Highlights:
Electrical and Optical Link Innovations

[23.2] A 32Gb/s Bidirectional 4-Channel 4pJ/b Capacitively Coupled Link in 14nm CMOS for Proximity Communication
[23.4] 56Gb/s 300mW Silicon-Photonics Transmitter in 3D-Integrated PIC25G and 55nm BiCMOS Technologies

Paper 23.2 Authors: *Chintan Thakkar, Shreyas Sen, James Jaussi, Bryan Casper*
Paper 23.2 Affiliation: *Intel, Hillsboro, OR*
Paper 23.4 Authors: *G. Minoia[1], E. Temporiti[1], M. Repossi[1], D. Baldi[1], A. Ghilioni[2], F. Svelto[2]*
Paper 23.4 Affiliation: *[1]STMicroelectronics, Pavia, Italy, [2]University of Pavia, Pavia, Italy*
Subcommittee Chair: *Daniel Friedman, IBM, Yorktown Heights, NY, Wireline Subcommittee*

CONTEXT AND STATE OF THE ART

- High-speed proximity links allow connector-less communication between components when conventional connectors are not practical, such as in low-profile modular handsets. The challenge for these links is to achieve high aggregate bandwidth over a practical (~1mm) distance with very low power. In ISSCC 2015, a coupled transmission-line interconnect demonstrated 6Gb/s, but was limited to a single channel. This year, a capacitively coupled, 4-channel 32Gb/s proximity link is reported with 0.8mm separation distance with 33% lower energy per bit.

- Next generation optical interfaces will adopt 50GBaud signaling, and minimizing optical transmitter power consumption is a key to enabling small form-factor optical modules for electro-optical conversion. In 2015, a state-of-the-art directly modulated laser (DML) transmitter was demonstrated at ~800mW power dissipation, while current best-in-class silicon photonics implementations allow savings of more than 350mW. This work shows ~30% further power saving.

TECHNICAL HIGHLIGHTS

- **Lowest-power and highest-bandwidth proximity interface for 0.8mm air gap**
- In Paper 23.2, Intel describes a 4-channel bi-directional proximity interface with 32Gb/s total bandwidth that consumes 4pJ/b in 14nm CMOS. The capacitive couplers use an alternating rectangular pattern to suppress crosstalk without keep-out areas between channels. Transmitter slew-rate control, along with receiver filtering and a 1-tap DFE, equalize the resonant channel to reduce power.

- **Lowest power 56Gb/s 1310nm wavelength electro-optical transmitter**
- In Paper 23.4, STMicroelectronics and the University of Pavia describe a complete 56Gb/s electro-optical transmitter, operating at a 1310nm wavelength, dissipating 300mW and achieving a >2.5dB extinction ratio. The combination of a traveling-wave Mach-Zender modulator in a silicon photonic technology and an electronic driver in 55nm BiCMOS realizes the proposed transmitter. Integrated transmission line bandwidth limitations are compensated by applying passive boost, shunt peaking in the pre-driver stage, and passive peaking in the load.

APPLICATIONS AND ECONOMIC IMPACT

- High-bandwidth proximity interconnect is an enabling technology for low-profile, reconfigurable mobile devices and other applications where traditional connectors are not practical.
- The ever-increasing need for data center IP traffic will only be satisfied by keeping optical transmitter power consumption sufficiently low to make small form factor optical modules feasible..

Session 24 Highlights: Ultra-Efficient Computing: Application-Inspired and Analog-Assisted Digital

[24.1] A 0.6V, 8mW 3D Vision Processor for a Navigation Device for the Visually Impaired

[24.3] A 36.8 2b-TOPS/W Self-Calibrating GPS Accelerator Implemented Using Analog Calculation in 65nm LP CMOS

Paper 24.1 Authors: Dongsuk Jeon, Nathan Ickes, Priyanka Raina, Hsueh-Cheng Wang, and Anantha Chandrakasan.
Paper 24.1 Affiliation: Massachusetts Institute of Technology, Cambridge, Massachusetts, United States
Paper 24.3 Authors: S. Skrzyniarz[1,2], L. Fick[2], J. Shah[2], Y. Kim[2], D. Sylvester[2], D. Blaauw[2], D. Fick[1], and M. B. Henry[1].
Paper 24.3 Affiliation: [1]Isocline, Austin, Texas, United States, [2]University of Michigan, Ann Arbor, Michigan, United States.

Subcommittee Chair: *Eugenio Cantatore, Eindhoven University of Technology, Eindhoven, The Netherlands, Technology Directions*

CONTEXT AND STATE OF THE ART

- The next wave of pervasive computing imposes stringent energy and performance constraints that cannot be met by today's approaches.
- The circuits in this session use a broad spectrum of application-aware design techniques to overcome these challenges.
- New analog-assisted digital techniques also enable compact kernel implementations that trade output accuracy for high efficiency.

TECHNICAL HIGHLIGHTS

- **Energy-efficient 3D vision processor that post-processes time-of-flight camera data forms the core of a navigation device for visually impaired individuals.**
- By co-optimizing its hardware architecture and vision algorithms, it achieves power consumption of 8mw at 0.6V and 1,500× times higher energy-efficiency than Cortex-A9. The processor can successfully detect safe areas and obstacles at 30fps.

- **GPS acquisition accelerator that combines analog computations and digital storage for high-energy efficiency and performance**
- Designed in a 65nm LP CMOS process, it achieves 2b operations at 36.8TeraOps/W through a differential current-steering circuit topology.

APPLICATIONS AND ECONOMIC IMPACT

- Energy-stringent pervasive computing spans a wide range of IoE applications, from vision assists to machine learning and data analytics.

- Orders of magnitude energy efficiency improvement explored by these papers will have a huge economic impact, through the realization of sensor nodes with much smaller size, lower cost, longer lifetime and much smarter functionality. The presented circuit design techniques are key enablers for highly energy-efficient embedded computation that is an essential ingredient of IoE and pervasive biomedical systems.

Session 25 Highlights: mm-Wave and THz Sensing

[25.1] A Fully Integrated 0.55THz Near-Field Sensor with a Lateral Resolution down to 8μm in 0.13μm SiGe BiCMOS
[25.3] A 40-to-330GHz Synthesizer-Free THz Spectroscope-on-Chip Exploiting Electromagnetic Scattering
[25.5] A 320GHz Subharmonic-Mixing Coherent Imager in 0.13μm SiGe BiCMOS

Paper 25.1 Authors: *J. Grzyb[1], B. Heinemann[2], and U. Pfeiffer[1]*
Paper 25.1 Affiliation: *[1]University of Wuppertal, Wuppertal, Germany; [2]IHP, Frankfurt, Germany*
Paper 25.3 Authors: *X. Wu and K. Sengupta*
Paper 25.3 Affiliation: *Princeton University, Princeton, NJ*
Paper 25.5 Authors: *C. Jiang[3], A. Mostajeran[3], R. Han[4], H. Sherry[5], A. Cathelin[5], and E. Afshari[3]*
Paper 25.5 Affiliation: *[3]Cornell University, Ithaca, NY; [4]Massachusetts Institute of Technology, Cambridge, MA; [5]STMicroelectronics, Crolles, France*

Subcommittee Chair: Piet Wambacq, imec, Belgium, RF Subcommittee

CONTEXT AND STATE OF THE ART

- Advances in silicon electronics have enabled multiple sensing applications at terahertz frequencies. While these applications are normally dominated by waveguide integrated compound semiconductors and optical techniques, silicon-based solutions promise to dramatically reduce volume and power dissipation while increasing sensing speed and levels of integration for applications ranging from near- and far-field imaging to spectroscopy.

TECHNICAL HIGHLIGHTS

- **World's first fully-integrated near-field THz sensor with 8μm lateral resolution**
- Paper 25.1 by University of Wuppertal describes a 0.55THz near-field sensor in 0.13μm SiGe BiCMOS. It uses a magnetically-coupled differential split-ring resonator with high surface-field confinement to achieve a lateral resolution down to 8μm, a 1/71 of the wavelength, and maintains a 20dB SNR.

- **A 330GHz synthesizerless spectroscope-on-chip with 10MHz frequency estimation accuracy**
- Paper 25.3 by Princeton University presents a sub-THz spectroscope-on-chip operating from 40GHz to 330GHz. Electromagnetic scattering of the incident signal across an on-chip radiator provides a spectral estimation with 10MHz accuracy without any frequency synthesis, RF amplification, or mixing.

- **THz coherent imager improves sensitivity by 10× compared to current state-of-the-art**
- Paper 25.5 by Cornell University presents a coherent imager in 0.13μm SiGe BiCMOS. At 320GHz, a phase-locked high-power transmitter and an 8-cell subharmonic mixer use coherent heterodyne detection to achieve 70.1pW sensitivity, 10× lower than that of previous terahertz imagers.

APPLICATIONS AND ECONOMIC IMPACT

- Terahertz near-field imaging can replace scanning near-field optical microscope with dramatic reductions in cost and increase in scanning speed with multiple pixel readout.
- Terahertz spectroscopy and imaging have multiple uses in security and chemical and biomedical sensing of gaseous and solid materials.
- Silicon alternatives to the existing optical and III-V-based imaging and spectroscopy systems can reduce cost, size, and power dissipation by orders of magnitude.

Session 26 Highlights: Wireless for IoE

[26.2] An Ultra-Low-Power Receiver Using Transmitted-Reference and Shifted Limiters for In-Band Interference Resilience

[26.5] A 0.7V 1.5-to-2.3mW GNSS Receiver with 2.5-to-3.8dB NF in 28nm FD-SOI

Paper 26.2 Authors: *Dawei Ye, Ronan van der Zee, Bram Nauta*
Paper 26.2 Affiliation: *University of Twente, Enschede, The Netherlands*

Paper 26.5 Authors: *Ken Yamamoto[1], Kenichi Nakano[1], Yuya Kondo[1], Hitoshi Tomiyama[1], Hideyuki Takano[1], Fumitaka Kondo[1], Yusuke Shinohe[1], Hidenori Takeuchi[1], Nobuhisa Ozawa[1], Shingo Harada[2], Shinichiro Eto[2], Mari Kishikawa[2], Daisuke Ide[2], Hiroyasu Tagami[2], Masayuki Katakura[2], Norio Shoji[1]*
Paper 26.5 Affiliation: *[1]Sony, [2]Sony LSI Design, Atsugi, Japan*

Subcommittee Chair: *Aarno Pärssinen, University of Oulu, Oulu, Finland, Wireless Subcommittee*

CONTEXT AND STATE OF THE ART

- [26.2] Blocker handling capability has been improved in low-power applications due to more stringent interference scenarios. However, it is extremely challenging to achieve using circuits that operate at as low as 100μW receiver power, targeted for wireless sensor nodes.
- [26.5] Global navigation satellite receiver systems face new requirements when they need to operate in very small sensor nodes for IoE. This can be achieved by very carefully reviewing system requirements and developing new design techniques that can operate at very low power.

TECHNICAL HIGHLIGHTS

- **Novel techniques to manage interference with very low power consumption**
- The receiver in Paper [26.2] realizes both ultra-low 135-to-175μW power consumption and 10kb/s data reception in the presence of an in-band interferer that is 50dB stronger than the wanted signal.
-
- **A 2.5dB NF GNSS receiver is presented that only consumes 2.3mW from a supply voltage as low as 0.7V**
- The GNSS receiver in Paper [26.5] is capable of receiving signals from two different global-positioning satellite systems simultaneously.

APPLICATIONS AND ECONOMIC IMPACT

- [26.2] Enables deployment of ultra-low-power IoE nodes in interference-unfriendly environments
- [26.5] Enables global positioning for ultra-low-power IoE nodes

Session 27 Highlights: Hybrid & Nyquist Data Converters

[27.2] An Oversampling SAR ADC with DAC Mismatch Error Shaping Achieving 105dB SFDR and 101dB SNDR over 1kHz BW in 55nm CMOS
[27.8] A 0.076mm² 12b 26.5mW 600MS/s 4×-Interleaved Subranging SAR-ΔΣ ADC with On-Chip Buffer in 28nm CMOS

Paper 27.2 Authors: Yun-Shiang Shu, Liang-Ting Kuo, and Tien-Yu Lo
Paper 27.2 Affiliation: *MediaTek, Hsinchu, Taiwan*
Paper 27.8 Authors: Claudio Nani, Alessandro Venca, Nicola Ghittori, Alessandro Bosi
Paper 27.8 Affiliation: *Marvell, Pavia, Italy*

Subcommittee Chair: *Un-Ku Moon, Oregon State University, Corvallis, OR, Data Converters*

CONTEXT AND STATE OF THE ART

- Low-power data converters, specifically SAR ADCs, are key building blocks for modern electronics.
- Although SAR ADCs benefit from CMOS technology scaling, they remain limited at high resolutions by comparator noise, power consumption and DAC inaccuracy.
- Combining classical SAR and Delta-Sigma data converter architectures into hybrid converters, enabled by the evolution of CMOS technology, breaks the traditional limitations between resolution, noise, area, and power consumption.

TECHNICAL HIGHLIGHTS

- **MediaTek achieves a Schreier FoM of 180dB in 4kHz bandwidth with a new oversampling SAR ADC.**
  MediaTek introduces a new DAC mismatch error-shaping technique. The 55nm CMOS prototype consumes 15.7μW and exhibits 96.1dB peak SNDR over 4kHz BW with a Schreier FoM of 180dB.

- **Marvell demonstrates a 12b 600MS/s ADC with 26mW power consumption occupying only 0.076mm² in 28nm CMOS**
  Marvell enables significant power and area reduction by combining SAR and incremental Delta-Sigma ADCs. The 12b 600MS/s 4-way time-interleaved ADC with on-chip buffer achieves an SNDR of 60.7dB while consuming 26mW and occupying 0.076mm² in 28nm CMOS.

APPLICATIONS AND ECONOMIC IMPACT

- Hybrid data converter architectures enable new breakthroughs in resolution, speed, area and power efficiency.
- The oversampling SAR ADC enables emerging IoE sensor applications due to the combination of very high dynamic range and power efficiency. The combination of time-interleaving, sub-ranging SAR and Delta-Sigma techniques offers a key differentiator in complex communication SoCs through very low area and power consumption.

Session 28 Highlights: Biological Sensors for Point of Care

[28.1] A Handheld 50pM-Sensitivity Micro-NMR CMOS Platform with B-field Stabilization for Multi-Type Biological/Chemical Assays
[28.4] A Battery-Powered Efficient Multi-Sensor Acquisition System with Simultaneous ECG, BIO-Z, GSR, and PPG

Paper 28.1 Authors: *K-M. Lei[1], H. Heidari[2,3], P.-I. Mak[1], M.-K. Law[1], F. Maloberti[2] and R. Martins[1,4]*
Paper 28.1 Affiliation: *[1]University of Macau, China, [2]University of Glasgow, United Kingdom, [3]University of Pavia, Italy, [4]Instituto Superior Técnico, Lisbao, Portugal*

Paper 28.4 Authors: Mario Konijnenburg[1], Stefano Stanzione[1], Long Yan[2], Dong-Woo Jee[2], Julia Pettine 1, Roland van Wegberg1, Hyejung Kim2, Chris van Liempd1, Ram Fish3, James Schuessler3, Harmke de Groot1, Chris Van Hoof1,2, Refet Firat Yazicioglu2, Nick Van Helleputte2
Paper 28.4 Affiliation: [1]imec-Holst Centre, Eindhoven, the Netherlands; [2]imec, Leuven, Belgium; [3]Samsung Electronics, USA

Subcommittee Chair: *Makoto Ikeda, University of Tokyo, Tokyo, Japan, IMMD*

CONTEXT AND STATE OF THE ART

- Screening by micro-NMR is repeatable, versatile and low-cost, but existing NMR solutions are bulky and expensive
- The most versatile sensor read-out system with more than state-of-the-art performance.

TECHNICAL HIGHLIGHTS

- **A compact and handheld micro-NMR system with 50pM sensitivity and Magnetic and Thermal stabilization.**
  The first micro-NMR CMOS system for multi-type biological and chemical assays is presented, which, supported by a vertical Hall sensor and a thermal-controlled coil, reaches a detection limit of 50pM.

- **The most versatile bio-sensor read-out system**
  The first design that supports ECG, BIOZ (Bio-impedance), PPG (Photoplethysmogram), and GSR (Galvanic Skin Response) on a single chip. Low power: usually between ~300μW and 1000μW, depending on the application.

APPLICATIONS AND ECONOMIC IMPACT

- The compact and handheld micro-NMR platform is suitable for healthcare, the food industry and colloidal applications. It outperforms existing commercial products in terms of compactness, weight and cost by significant amounts.
- The presented complete and versatile sensor read-out system has many applications in biological and healthcare fields with high industrial value.

ISSCC 2016

Plenary Session - Invited Papers

Plenary Session — Invited Papers

Chair: ***Anantha Chandrakasan,*** Massachusetts Institute of Technology, Cambridge, MA
ISSCC Conference Chair

Associate Chair: ***Kevin Zhang***, Intel, Hillsboro, OR

1.1 Moore's Law: A Path Forward

William M. Holt, *Executive Vice-President and General Manager, Technology and Manufacturing Group, Intel Corporation, Hillsboro, Oregon*

Moore's Law has served as the guiding principle for the semiconductor industry for 50 years. But now there are growing concerns and doubts over the vitality of Moore's Law going forward, given the scaling challenges we face. This talk will directly address those concerns and explore future opportunities for the industry. We will present the scaling benefits for power, performance, and cost using specific product and design examples based on state-of-the-art 14nm CMOS technology, for applications ranging from high-performance computing down to ultra-low-power mobile applications. In additional to the scaling path of CMOS technology beyond 14nm, this talk will also discuss some leading technology options on the horizon beyond CMOS and their potential design benefits in advancing Moore's Law well into the future. Novel 3D heterogeneous integration schemes and new memory technologies will be discussed for their potential in optimizing the memory hierarchy and
addressing bandwidth challenges in processor performance and power.

1.2 Three Pillars Enabling the Internet of Everything: Smart Everyday Objects, Information-Centric Networks, and Automated Real-Time Insights

Sophie V. Vandebroek, *Chief Technology Officer, Xerox Corporation, Norwalk, CT*

When smart everyday objects, information-centric networks, and automated real-time insights work in concert a "perfect storm" of functionality emerges, one which will disrupt entire industries: Gartner predicts that the global economic value of the Internet of Everything (IoE) will be $1.7T in 2020. But, even more important will be the inevitable improvements to human society that IoE enables: personalized healthcare and education, agile urban mobility, efficient energy usage, and much more.

This talk will provide examples of how each of the three pillars of IoE relies on electronics: (1) printed hybrid logic and sensor circuits using organic inks and inks embedding microchips to create smart 2D labels and to manufacture 3D personalized Internet-connected objects; (2) information-centric network protocols and hardware (for example, CCNx®) to increase the Internet's versatility, reduce its traffic congestion, improve security, and simplify application development; and (3) machine-intelligence software and deep-learning chips to create real-time insights and automate processes at the "edge" of the IoE network.

The three pillars of IoE will be illustrated through examples from healthcare and transportation. A number of unique challenges and opportunities for general-purpose and custom chip designs will be highlighted.

1.3 The Evolution of 5G Mobile Technology Toward 2020 and Beyond

Seizo Onoe, *Executive Vice President and CTO, NTT DOCOMO, Tokyo, Japan*

Recently, LTE has become the mainstream of mobile technologies; correspondingly, global expectations for 5G are rapidly growing toward 2020 and beyond. Up to the generation of 4G, a representative technology for each generation emerged immediately after the commercial launch of the previous one; However, today, while everyone talks about 5G, there is no single technology representing it. Although researchers see some saturation in the evolution of radio, combinations of existing technologies will continue to create new possibilities and solutions. Thus, through such combinations, developments that are considered impossible today will be achieved in the 5G era. For example, cellular systems will provide cost-effective solutions with wide coverage at even higher frequencies with broader bandwidth. In this talk, the history of mobile-system evolution up to 5G will be reviewed. Then discussion will turn to 5G definition, its requirements, its technologies, and their coverage for variable use cases and spectrum bands. Finally, DOCOMO's recent R&D activities targeting a 5G commercial launch in 2020 will be described.

1.4 The Road Ahead for Securely Connected Cars

Lars Reger, *CTO Automotive, NXP Semiconductors, Hamburg, Germany*

The car is evolving: It is transforming from simply a mode of transport to a mobile personalized-information hub! Cars are enabling consumers to seamlessly integrate their mobile and wearable devices, and soon they will be able to operate autonomously.

The technologies that make autonomous driving a reality are clearly on the rise; they include secure vehicle-to-everything (V2X) communications, affordable compact radar detection, and Ethernet for high-bandwidth in-car data transfer.

As well, self-driving cars will integrate a variety of wireless interfaces for exchanging data with other vehicles and the surrounding intelligent traffic infrastructure – all aimed at understanding the world around to optimize the traffic flow, reduce CO2 emissions, and avoid accidents. While providing an essential element of autonomous driving, this connectivity also exposes cars to vulnerabilities such as hackers and viruses.

Powerful reliable wireless technologies combined with the highest-level privacy and system security are critical. This talk will discuss what it takes to realize the secure connected car of the future.

ISSCC 2016 TRENDS

CONDITIONS OF PUBLICATION

PREAMBLE

The Trends to follow serve to capture the context, highlights, and potential impact, of the papers to be presented in each Session at ISSCC 2016 in January in San Francisco

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FOOTNOTE

- From ISSCC's point of view, the phraseology included in the box below captures what we at ISSCC would like your readership to know about this, the 63rd appearance of ISSCC, on January 31st to February the 4th, 2016, in San Francisco.

This and other related topics will be discussed at length at ISSCC 2016, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on January 31 - February 4, 2016, at the San Francisco Marriott Marquis Hotel.

ISSCC Press Kit Disclaimer
The material presented here is preliminary.
As of November 5, 2015, there is not enough information to guarantee its correctness.
Thus, it must be used with some caution.

INDICATORS – HISTORICAL TRENDS IN TECHNICAL THEMES

Analog Systems

Analog Subcommittee
Data Converters Subcommittee

Analog – 2016 Trends

Subcommittee Chair: *Axel Thomsen, Cirrus Logic, Austin, TX*

The efficient control, storage, and distribution of energy are worldwide challenges, and are increasingly important areas of analog circuit research. While the manipulation and storage of information is efficiently performed digitally, the conversion and storage of energy is fundamentally performed with analog systems. Therefore, the key technologies for power management are predominantly analog. For example, there is much interest in wireless power transmission for battery charging applications, ranging from mobile handsets to medical implants: increased performance in wireless power transmission is enabling more efficient power delivery over longer distances. There is also an explosion of technologies that allow energy to be collected from the environment via photovoltaic, piezoelectric, or thermoelectric transducers, with a trend toward the use of multiple sources at the same time. A significant focus here is on analog circuits that are able to harvest sub-microwatt power levels from multiple energy sources at tens of millivolts, to provide autonomy for IoE devices, or to supplement conventional battery supplies in portable devices. To achieve this, the attendant analog circuits have to consume extremely low power, so that some energy is left over to charge a battery or super-capacitor. This trend is captured by movement towards the top-left in the plot shown in Fig. 1.

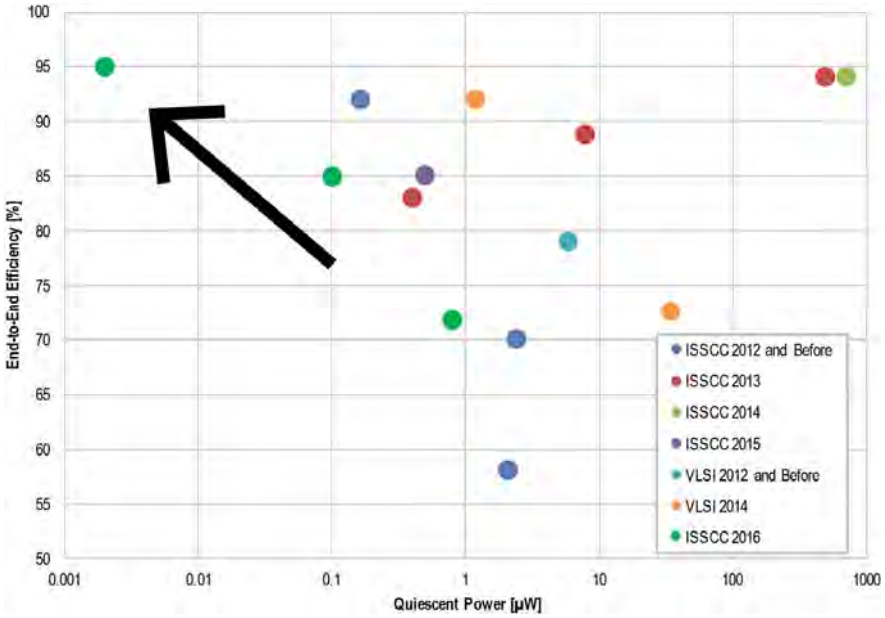


Fig. 1 – Comparison of Integrated Energy Harvesting Systems showing End-to-End Efficiency vs Quiescent Power

Similarly, the power consumption of analog instrumentation amplifiers, oscillators, and audio power amplifiers is being scaled down to meet the demands of these low-power systems. This trend is captured by movement towards the bottom-right in the plot shown in Fig. 2. Fast power-up and -down is also desired from these circuits to permit high energy-efficiency during intermittent operation. Together, these technologies will lead to devices powered indefinitely from sustainable sources, opening the door to internet of things, ubiquitous sensing, environmental monitoring, and medical applications.

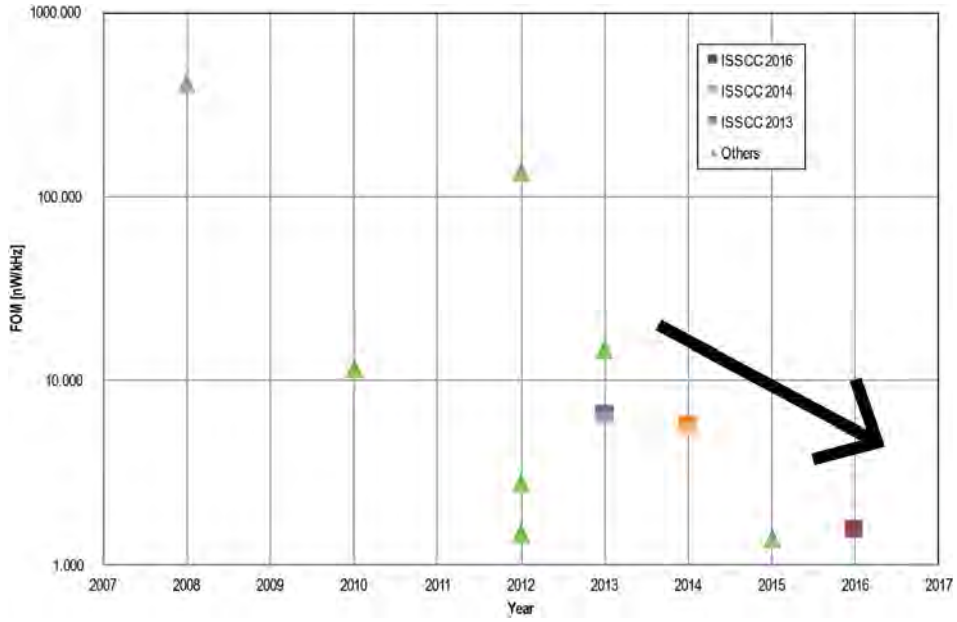


Fig. 2 – Comparison of Integrated 3-to-100kHz Oscillators showing Power Normalized to Frequency vs Year

Analog circuits also serve as bridges between the digital world and the analog real world. Just like actual bridges, analog circuits are often bottlenecks and their design is critical to overall performance, efficiency, and robustness. Nevertheless, since digital circuits, such as microprocessors, drive the market, semiconductor technology has been optimized relentlessly over the past 40 years to reduce their size, cost, and power consumption. Analog circuitry has proven increasingly difficult to implement using these modern IC technologies. For example, as the size of transistors has decreased, the range of analog voltages they can handle as well as their analog performance have decreased, while the variation observed in the analog parameters has increased.

These aspects of semiconductor technology explain two key divergent trends in analog circuits. One trend is to forgo the latest digital IC manufacturing technologies, instead fabricating analog circuits in older technologies, which may be augmented to accommodate the high voltages demanded by increasing markets in medical, automotive, industrial, and high-efficiency lighting applications. Other applications dictate full integration of analog and digital circuits together in the most modern digital semiconductor processes. For example, microprocessors with multiple cores can reduce their overall power consumption by dynamically scaling operating voltage and frequency in response to time-varying computational demands. For this purpose, DC-DC voltage converters can be embedded alongside the digital circuitry, driving research into the delivery of locally-regulated power supplies with increasing efficiency, decreasing die area, and increasing output power. These trends are captured by movement towards the top-right in the plot shown in Fig. 3.

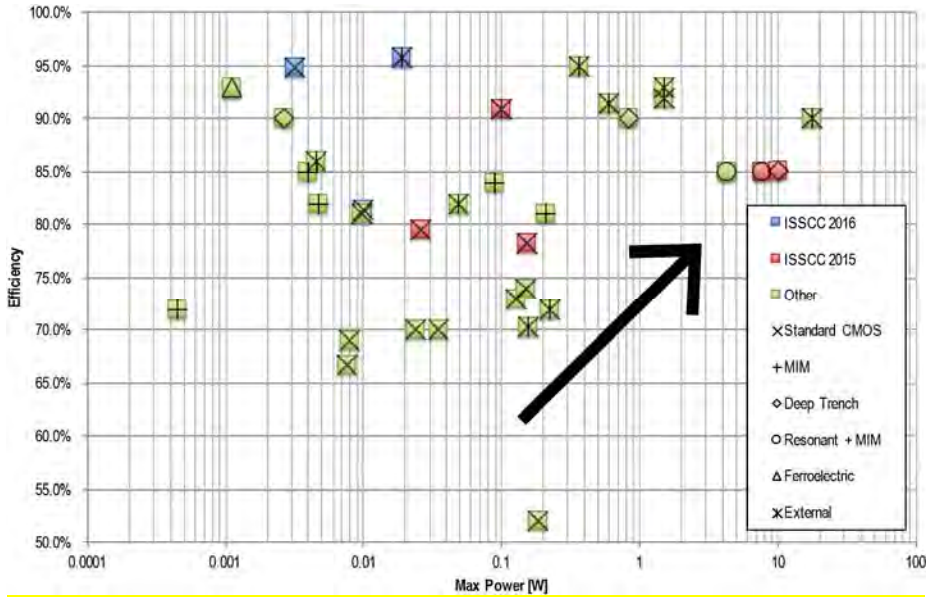


Fig. 3 – Comparison of Integrated Switched-Capacitor Power Converters showing Peak Efficiency vs Maximum Output Power

Data Converters – 2016 Trends

Subcommittee Chair: *Un-Ku Moon, Oregon State University, Corvallis OR*

Data converters continue to provide the critical link between the analog physical world and the realm of digital computing, and are key components to enable the "Internet of Everything". Increases in computational throughput and algorithmic complexity of modern electronic systems continue to pressure data converters to deliver more bandwidth and linearity with greater power efficiency. ISSCC 2016 brings the juxtaposition of successive-approximation (SAR) and oversampling ($\Delta\Sigma$) techniques to enable a new breed of "hybrid" converters that set new metrics in energy efficiency and signal fidelity.

The figures below represent three traditional metrics to capture innovative progress in data converters. The first figure plots power dissipated relative to the effective Nyquist rate (P/f_{snyq}), and as a function of signal-to-noise and distortion ratio (SNDR) to give a measure of ADC power efficiency. For low-to-medium-resolution converters, energy is primarily expended to quantize the signal; thus the overall efficiency of this operation is typically measured by the energy consumed per conversion and quantization step. The dashed trend-line represents a benchmark of 5fJ/conversion-step. Circuit noise becomes significant as with higher-resolution converters, necessitating a different benchmark proportional to the square of signal-to-noise ratio, represented by the solid line. ADCs embodying various architectures and design criteria continue to push the limits of energy efficiency. (Note that a lower P/f_{snyq} metric represents a more efficient circuit on this chart.) Contributions at ISSCC 2016 are depicted by the colored legends representing various converter architectures, including the abovementioned "hybrid" architecture distinguished by diamonds; historical contributions are shown using smaller markers.

The second figure plots signal fidelity vs. the Nyquist sampling rate normalized to power consumption. Applications such as next-generation wireless demand wide bandwidth and accuracy. Higher speeds of operation present additional challenges in maintaining accuracy in an energy-efficient manner. Nevertheless, advances in circuit innovations embodied in leading-edge technologies have resulted in new benchmarks in energy efficiency across the entire spectrum of conversion rates.

The final figure plots achieved bandwidth as a function of SNDR. Sampling jitter or aperture errors coupled with increased noise bandwidth make achieving both high resolution and high bandwidth a particularly difficult task. Nonetheless, in 2016, we see many examples achieving excellent results in this metric across a wide range of SNDR and bandwidths utilizing several different converter architectures.

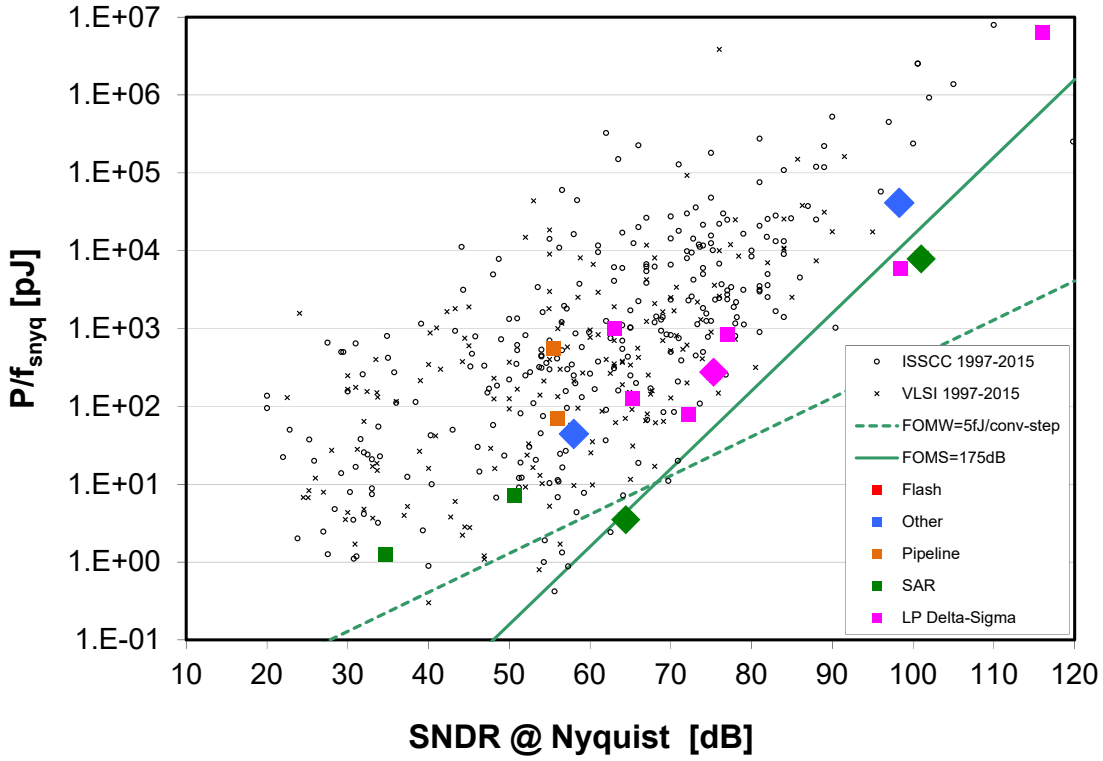


Figure 1: ADC power efficiency (P/f_{snyq}) as a function of SNDR

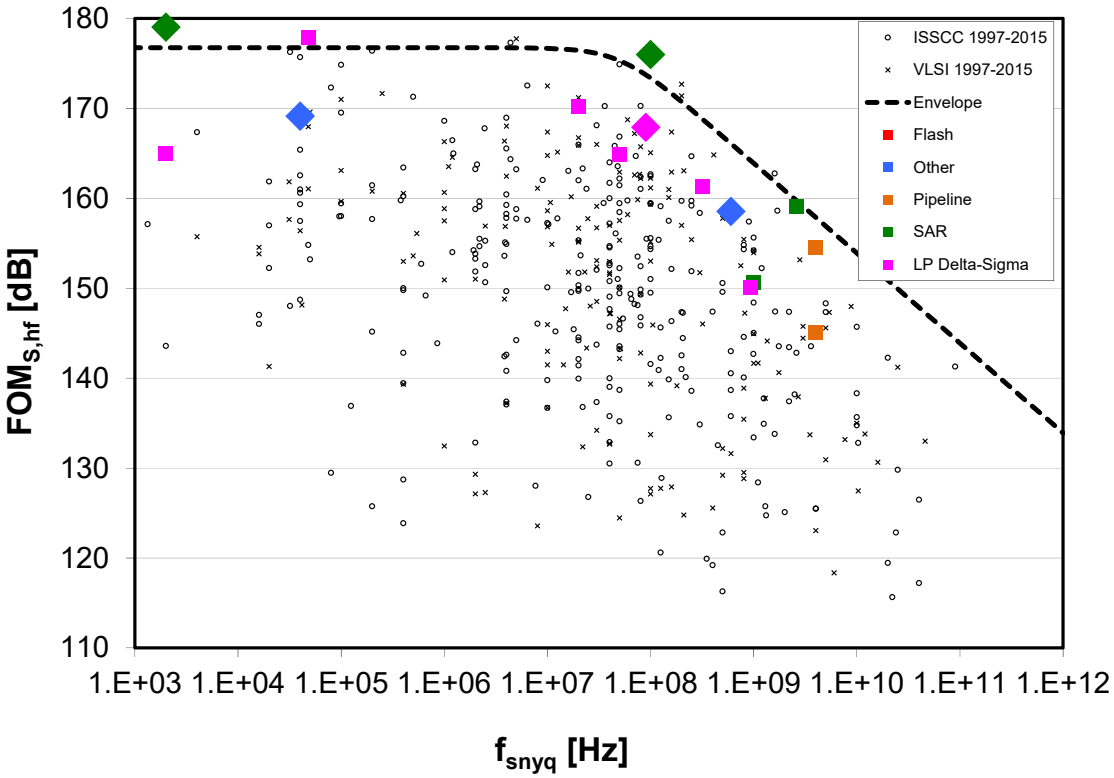


Figure 2: Power normalized noise and distortion vs. the Nyquist sampling rate

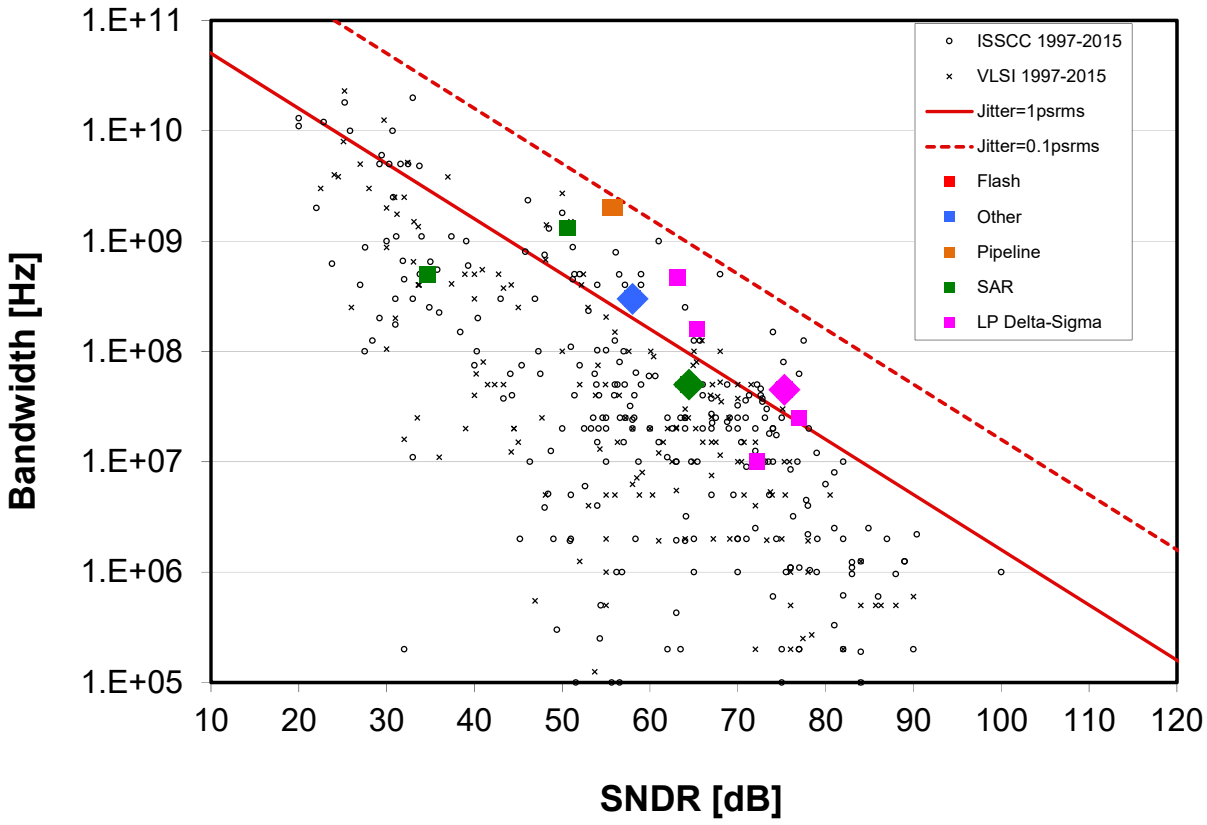


Figure 3: Bandwidth vs. SNDR

INDICATORS – HISTORICAL TRENDS IN TECHNICAL THEMES

Communication Systems

RF Subcommittee - Wireless Subcommittee Wireline Subcommittee

RF Subcommittee – 2016 Trends

Subcommittee Chair: Piet Wambacq, imec, Belgium

Introduction

This year shows increasing integration and technical maturity across the radio frequency (RF) bands from below 1GHz to beyond 1THz. The trend of innovation is continuing at circuit and system levels. This includes demonstrations of mm-Wave and THz systems as well as advances in voltage controlled oscillators, frequency synthesizers, and RF transceiver building blocks towards higher performance, lower power, and wider bandwidth. This document highlights such emerging trends, which will be presented at the 2016 ISSCC conference. Papers showcase some of the recent advances in frequency generation circuits, with an ongoing drive towards higher output frequency range, lower noise. RF transceivers demonstrate increased data-rates, efficiency, and sensitivity and support complex modulation schemes at mm-Wave/THz frequencies.

mm-Wave and THz Sensing: There is an increasing presence of silicon electronics developed for a wide range of mm-Wave and terahertz sensing and imagining applications. The trend observed in this emerging field is to improve resolution and sensitivity. Two imaging systems are proposed. A 0.55THz near-field sensor achieves the resolution of 1/71 of the wavelength and 20dB signal-to-noise ratio. A 320GHz coherent imager with 70.1pW sensitivity demonstrates a 10× improvement over prior art. A wide-band direct-down-conversion receiver for mm-Wave spectroscopy is developed to operate between 210 and 305 GHz. In addition, a frequency-synthesizer-less spectral estimator operating across a 40-330GHz frequency range with a 10MHz resolution is demonstrated. Aided by digital signal processing techniques, a 100GHz radiometer requiring no Dicke switch is shown to achieve a 0.43K noise equivalent temperature.

RF Frequency Generation: The latest advances in frequency generation range from low-GHz to THz for communication, sensing, and imaging systems. This year, innovations range from a first silicon frequency synthesizer operating above 0.5THz to a 28GHz coupled PLL, which supports phased-array element synchronization over a single-wire for 5G communications. In addition a 2.1GHz PLL-DLL with a 40MHz loop bandwidth for low-noise ring-oscillators and a 2-to-16-GHz fractional-N PLL for wireless backhaul applications are demonstrated. Three VCOs will be presented: a 4.7-5.4GHz CMOS LC-VCO for low-power Internet-of-Everything (IoE) with 196dB Figure-of-Merit (FOM), a 190GHz BiCMOS VCO with 20.7% tuning range and -2.1dBm output power, and a ring VCO with time-interleaving for low flicker noise. Circuits enabling fast locking time and fine resolutions are also demonstrated. These include a 30GHz injection-locked oscillator with envelope-detection-based FLL with a state-of-the-art 300ns locking time and a high-speed 2GHz 244fs-resolution digital-to-time converter for PLLs. The general trends for frequency generation, as illustrated in Figures 1 and 2, remain.

RF-to-THz Transceiver Techniques: Novel transceiver circuits and architectures have increased data-rate and efficiency that support complex modulations and open up the possibilities of new applications such as ultra-high-speed short-range communication and THz imaging and spectroscopy. A 65nm CMOS 1.4THz multiplier chain is demonstrated to reach a peak EIRP of -13dBm. A 32-QAM 6-channel 40nm CMOS 300GHz wireless transmitter supporting 17.5 Gb/s/ch is presented. The trend of improving efficiency of silicon THz sources continues. For example, a 65nm CMOS radiating source array at 300GHz achieves a record total radiated power of +5.4dBm and an EIRP of +22dBm with 5.1% DC-to-THz efficiency. For mm-Wave transmitters, asymmetrical power combining techniques and injection-locked PAs are proposed to enhance the power-added efficiency above 25% and up to a 60GHz frequency range. The trend to simultaneously optimize power and efficiency is indicated in Figure 3 for mm-Wave PAs. For cellular applications, an 83% efficiency low-noise envelope-tracking supply modulator is measured together with a power amplifier for 40MHz LTE. The trend of replacing external SAW filters by silicon-based solutions is continued as evidenced by a dual-frequency balanced duplexer in 0.18µm SOI CMOS covers all LTE bands in the 0.7-1GHz range.

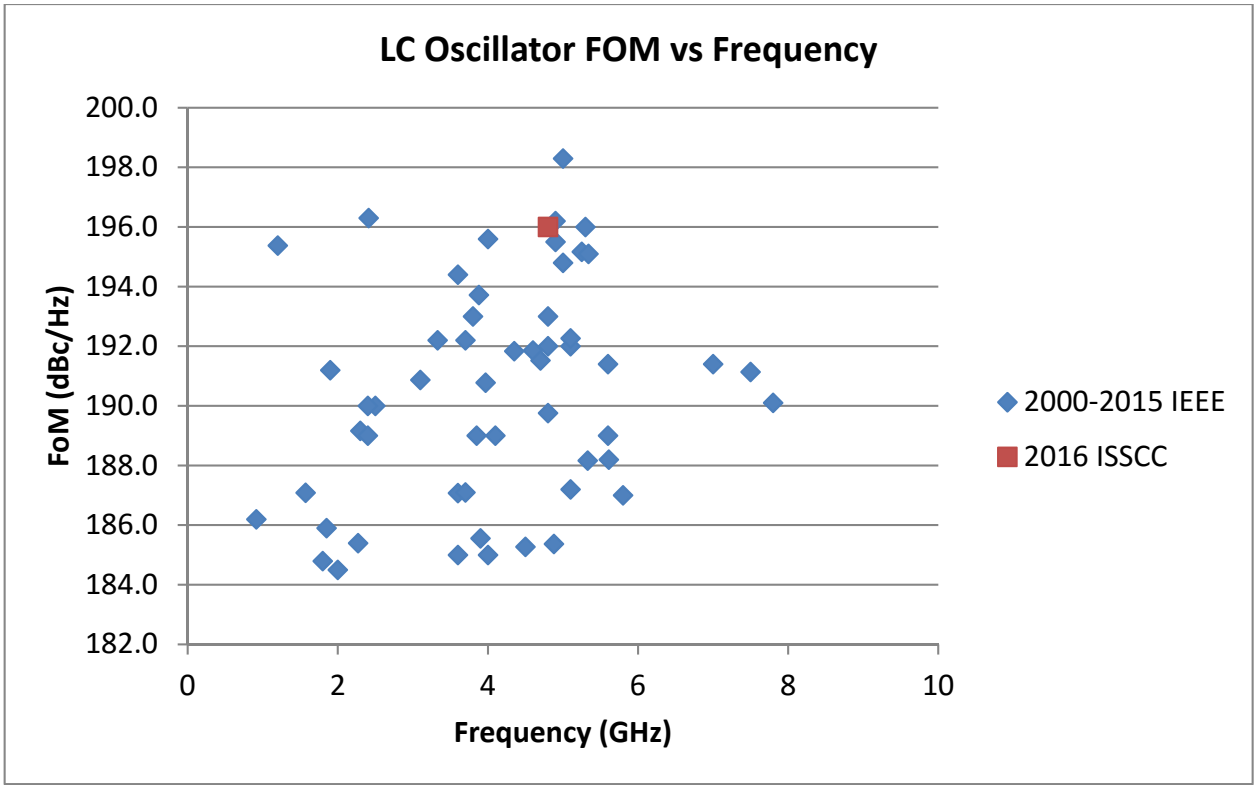


Figure 1: LC Oscillator FoM versus frequency (1-10GHz)

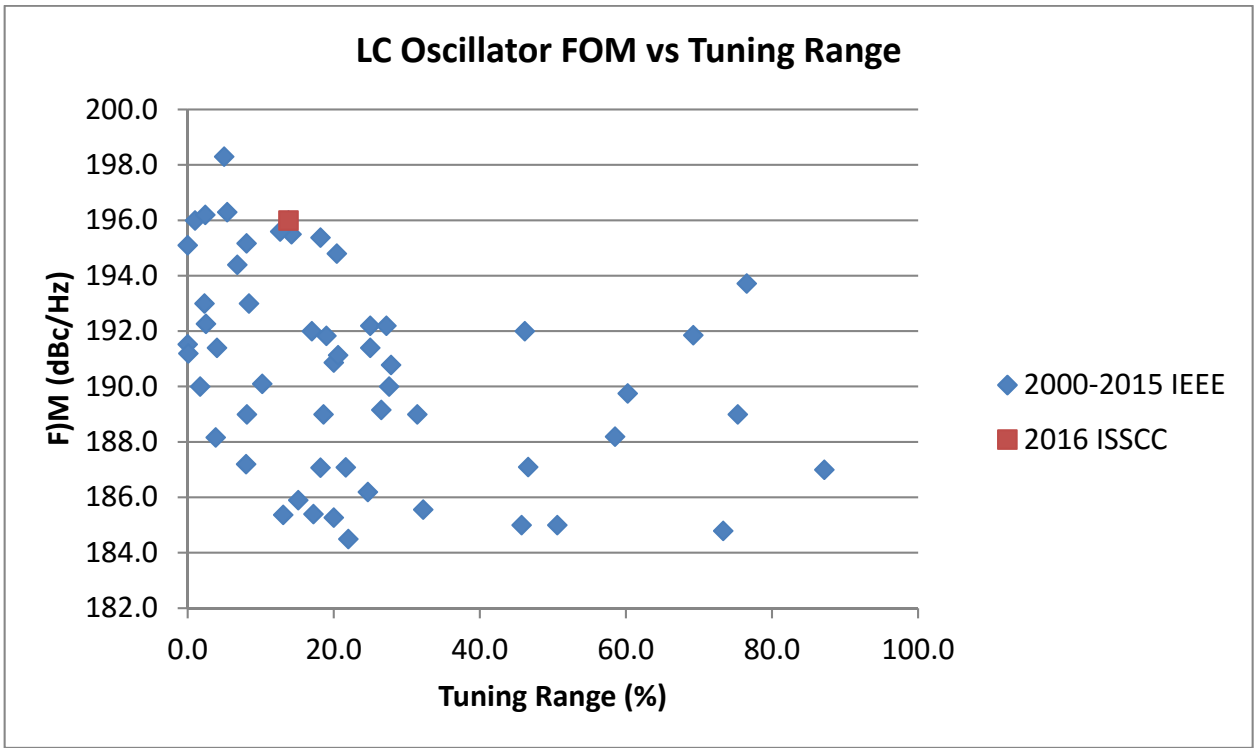


Figure 2: LC Oscillator FOM versus tuning range (1-10GHz)

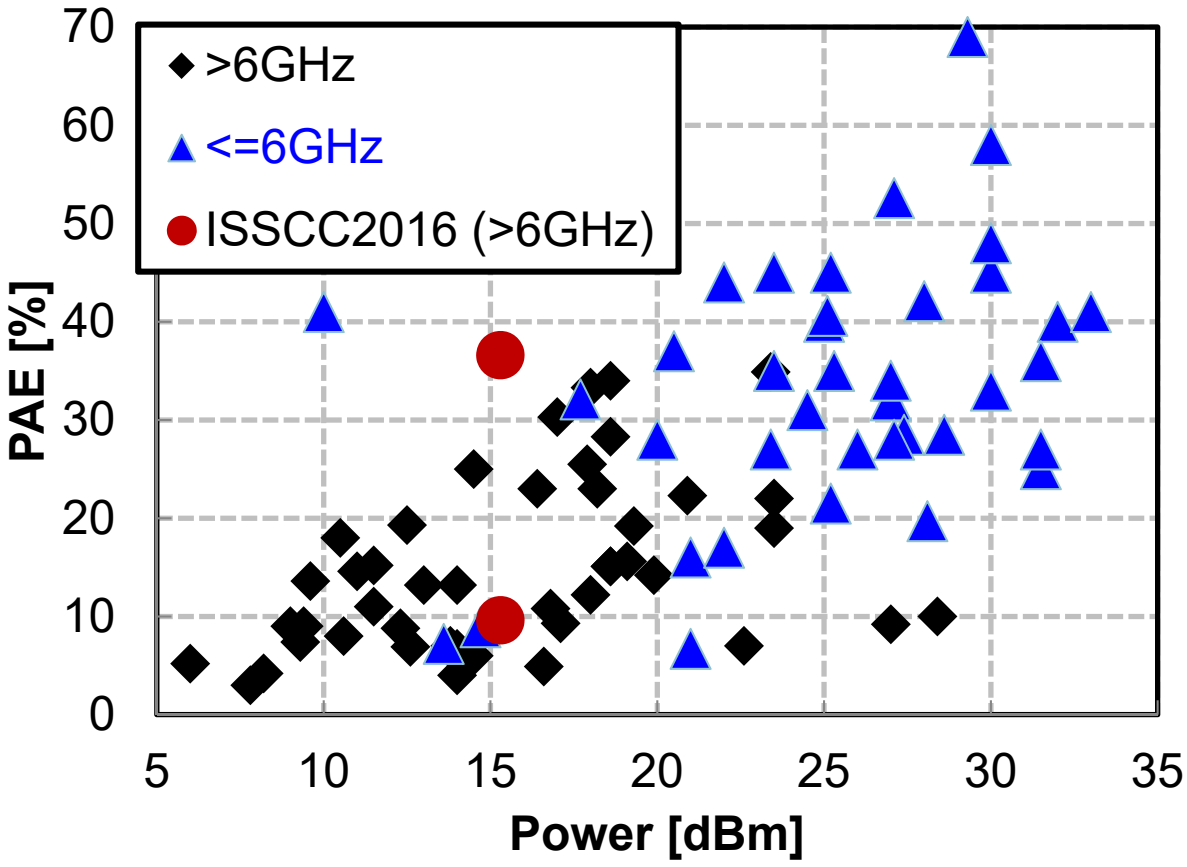


Figure 3: PAE (%) vs. output power for recent submicron CMOS PAs

Wireless – 2016 Trends

Subcommittee Chair: *Aarno Pärssinen, University of Oulu, Oulu, Finland*

The insatiable need for big data communication calls for transceivers with high throughput, achieved through carrier aggregation or frequency interleaving, MIMO with beamforming, and interference detection and cancellation. A variety of new techniques have been developed, such as digital beamforming with spatio-spectral-filtering, frequency-translational quadrature-hybrid receivers, and N-path-filter-based non-reciprocal circulators, to help push to even higher data-rates.

Complex sampling schemes applied to transmitters, receivers, and fractional-N PLL's allow RF to scale with digital in more advanced process nodes. Digital PAs replace the area-hungry inductors/transformers with high-speed digital processing circuits running at lower supply voltage. For the first time, a digital PA integrated in a complete SOC for a commercial product (WLAN) has been reported, paving the way for a lower cost, miniaturized module. Fractional-N PLL FOM continues to improve to enable higher SNR, higher data-rate, and ultimately better spectral efficiency.

In IoE space, lower-power and highly integrated system solutions have emerged in varies fields, including health care and wearable devices. A 1x1x10mm^3 syringe-Implantable near-field radio that fits inside a 14 gauge syringe needle including antenna and chip-on-glass substrate is reported. A 236nW BLE-compliant wake-up receiver and a 1.5mW GNSS receiver have been reported, facilitating the proliferation of the wearable applications.

Figure 1 shows Ultra-Low-Power 2.4GHz and MICS-band Wireless Transmit-Efficiency trends, while Figure 2 shows Ultra-Low-Power 2.4GHz and MICS-band Wireless Receiver Sensitivity Trends. Because many different techniques are used to design the circuits, there is significant scatter in the graphs. However, in both cases, the arrows show the desired trend directions.

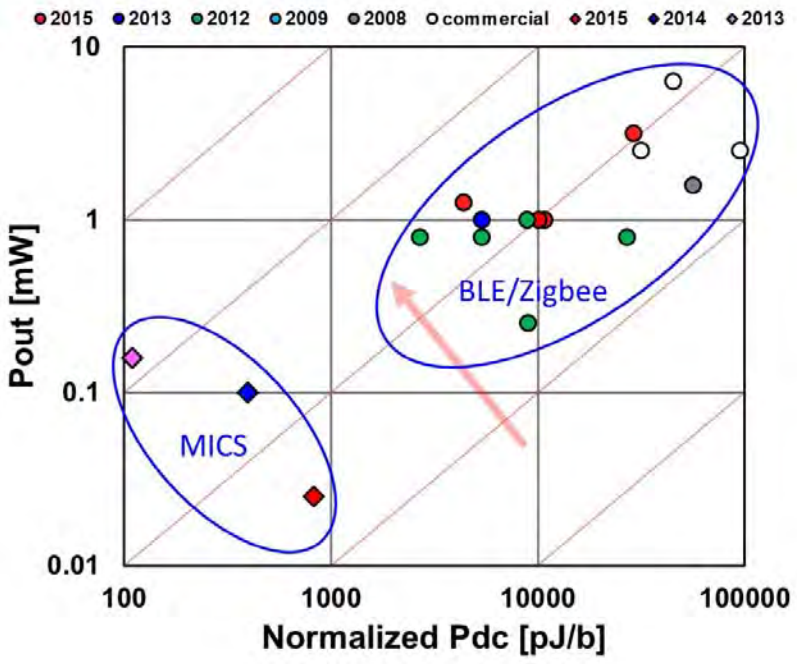


Figure 1: Ultra-Low-Power 2.4GHz and MICS-band Wireless Transmit-Efficiency Trends.

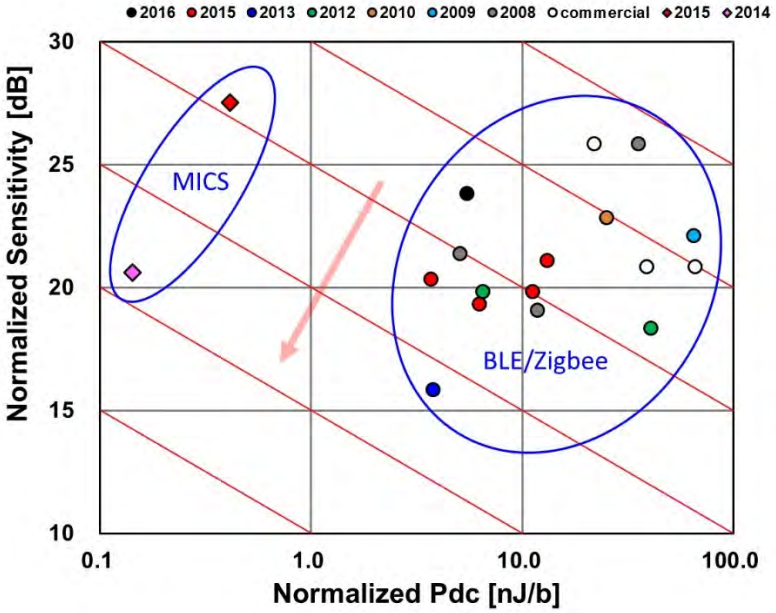


Figure 2: Ultra-Low-Power 2.4GHz and MICS-band Wireless Receiver Sensitivity Trends.

Wireline – 2016 Trends

Subcommittee Chair: *Daniel Friedman, IBM T. J. Watson Research, Yorktown Heights, NY*

Over the past decade, wireline I/O has been instrumental in enabling the incredible scaling of computer systems, ranging from handheld electronics to supercomputers. During this time, aggregate I/O bandwidth requirements have increased at a rate of approximately 2 to 3× every 2 years. Demand for bandwidth is driven by applications such as memory, graphics, chip-to-chip fabric, backplane, rack-to-rack, and LAN. In part, this demand is met by expanding the number of I/O pins per component. As a result, I/O circuitry consumes an increasing amount of area and power in today's chips. Increasing bandwidth has also been enabled by rapidly accelerating the per-pin data rate. Figure 1 shows that per-pin data rate has approximately doubled every four years across a variety of diverse I/O standards ranging from DDR to graphics to high-speed Ethernet. Figure 2 shows that the data rates for published transceivers have kept pace with these standards, enabled in part by process technology scaling. However, continuing along this rather amazing trend for I/O scaling will require more than just transistor scaling. Significant advances in both energy efficiency and signal integrity must be made to enable the next generation of low-power and high-performance computing systems. Papers at ISSCC this year include a 56Gb/s transceiver, a 4x8Gb/s transceiver with 4pJ/bit energy efficiency for contact-less board-to-board communication, and a complete ADC-based 28GBd PAM-4 transceiver.

Energy Efficiency and Interconnect Density:
Power consumption of I/O circuits is a first-order design constraint for systems ranging from cell phones to servers. As the pin count and per-pin data rate for I/Os have increased, so has the percentage of total power consumed by I/Os. Technology scaling enables increased clock and data rates and offers some energy efficiency improvement, especially for digital components. Many recent advances have reduced power for high-speed link components through circuit innovation, including low-power RX equalization (DFE, CTLE), CMOS and resonant clocking, low-swing voltage-mode transmitters and links with low-latency power-saving states. In this year's ISSCC, a combined DVFS and fast 14ns on/off link demonstrates power savings by dynamically scaling the supply voltage and gating the transceiver [23.1].

Simply increasing per-pin baseband data rates with existing circuit architectures and channels is not always a viable path given fixed system power limits. Figure 3 plots the energy efficiency (expressed in mW/Gb/s, which is equivalent to pJ/b) as a function of channel loss for recently reported transceivers. Looking at the most aggressive designs, the data indicates that the scaling factor between link power and signaling loss is slightly less than unity—in particular, that 30dB channel loss corresponds to a roughly 10× increase in pJ/b. This year's ISSCC includes paper 3.3 that describes a 25Gb/s transceiver that compensates 50dB loss at an energy efficiency of 16 pJ/bit. Additionally, the need to operate with legacy channels has resulted in degraded energy efficiency at data rates beyond 20Gb/s. Increasing channel loss also has impacted the choice of clocking schemes used in high performance I/Os. In particular, forwarded clocking that was commonly used at data rates below 20Gb/s is being replaced by embedded clocking due to jitter amplification caused by the lossy channel (see Fig. 4).

Electrical Interconnect:
There is ever growing demand for very high data rate communication across a wide variety of channels. Some types of channels, especially those related to medium-distance electrical I/O like server backplanes, must support high data rates over high-loss channels. For these links, the key to scaling has been improvements in equalization and clock/data recovery. Recent high-speed transceivers use a combination of fully adaptive equalization methods, including TX FIR, RX CTLE, DFE, as well as RX FIR and/or IIR FFEs. As a result, recent receivers achieve data rates above 28Gb/s with channels that have 30dB or more loss. Papers 3.1 and 3.2 present advanced ADC-DSP based equalization to overcome more than 40dB loss beyond 25Gb/s data rates, while paper 3.7 presents a 64Gb/s transmitter with a 3-tap FFE for short-range communication.

Optical Interconnect:
As the bandwidth demand has accelerated and as electrical channel impairments become increasingly severe as per-lane data rates rise, optical interconnects have become an increasingly attractive alternative to traditional electrical wireline interconnects. Optical communication has clear benefits for high-speed and long-distance interconnects because it offers lower channel loss. Circuit design and packaging techniques that have traditionally been used for electrical wireline are being adapted to enable integrated optical links with extremely low power. This has resulted in rapid progress in optical ICs for Ethernet, backplane and chip-to-chip optical communication. At ISSCC this year, a 56Gb/s silicon photonics transmitter and a 64Gbaud transimpedance amplifier for coherent optical receiver applications are presented.

Concluding Remarks:
Continuing to aggressively scale I/O bandwidth is both essential for the industry and extremely challenging. Innovations that provide higher performance and lower power will continue to be made in order to sustain this trend. Advances in circuit architecture, interconnect topologies, and transistor scaling are together changing how I/O will be done over the next decade. The most exciting and most promising of these emerging technologies for wireline I/O will be highlighted at ISSCC 2016.

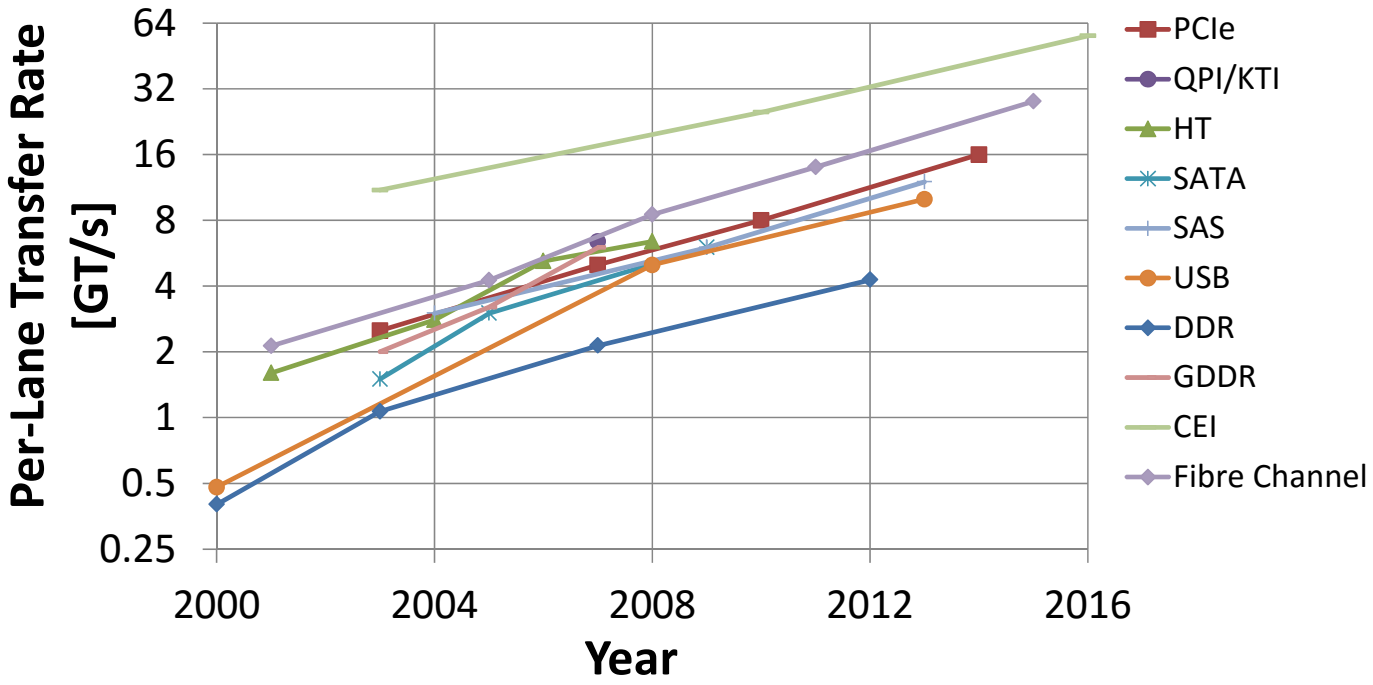


Figure 1: Per-pin data rate vs. Year for a variety of common I/O standards.

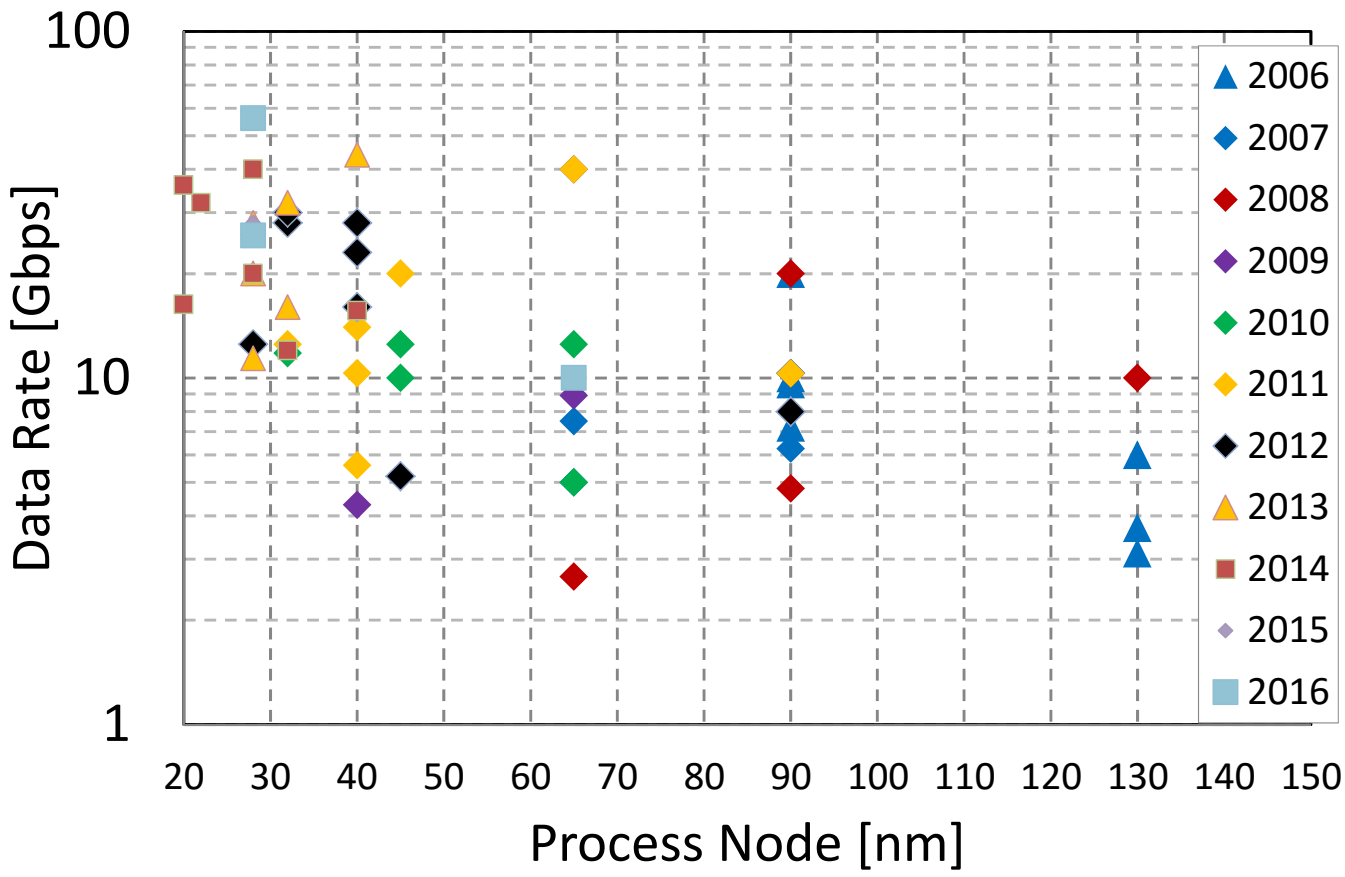


Figure 2: Data-rate vs. process node and year.

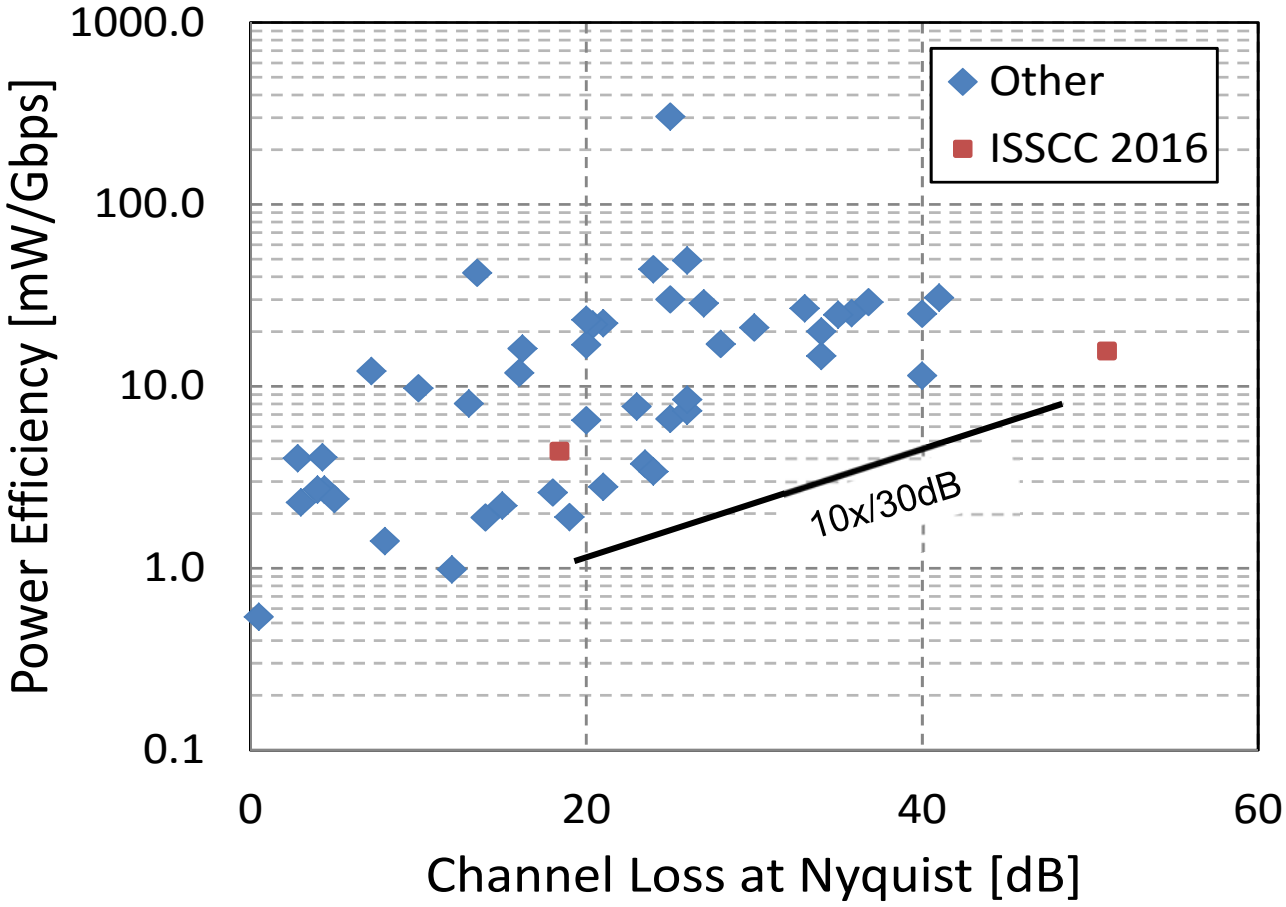


Figure 3: Transceiver power efficiency vs. channel loss.

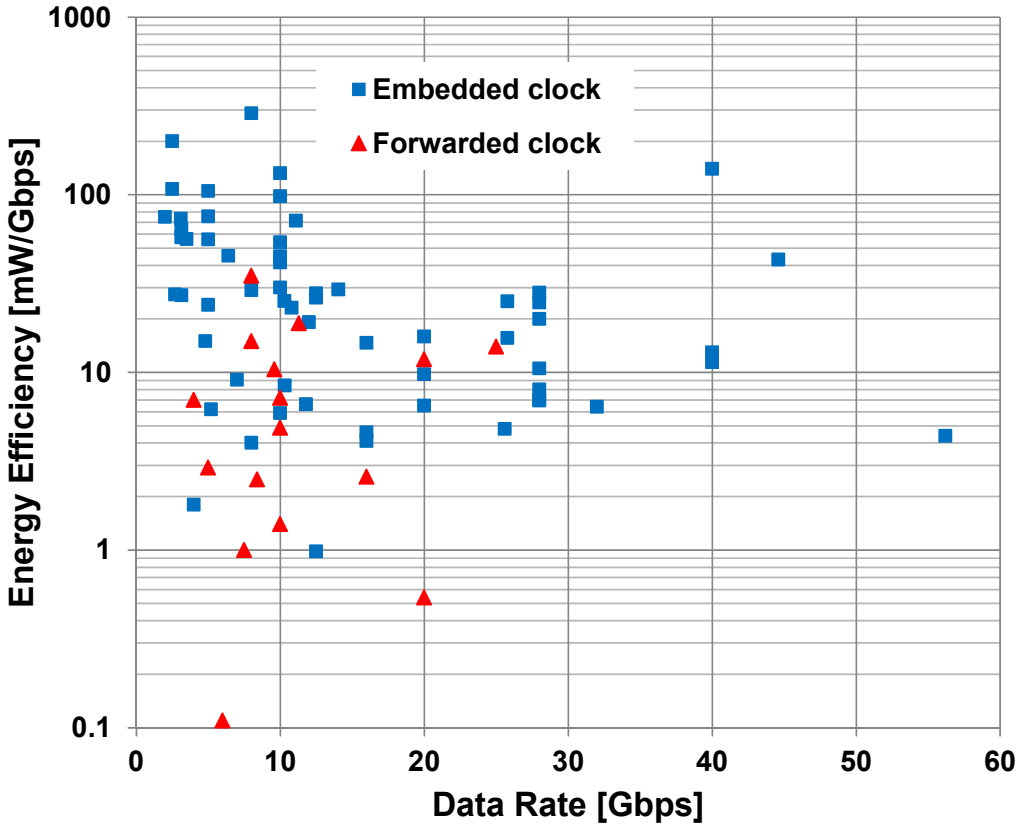


Figure 4: Energy efficiency vs. data rate.

HISTORICAL TRENDS IN TECHNICAL THEMES

DIGITAL SYSTEMS

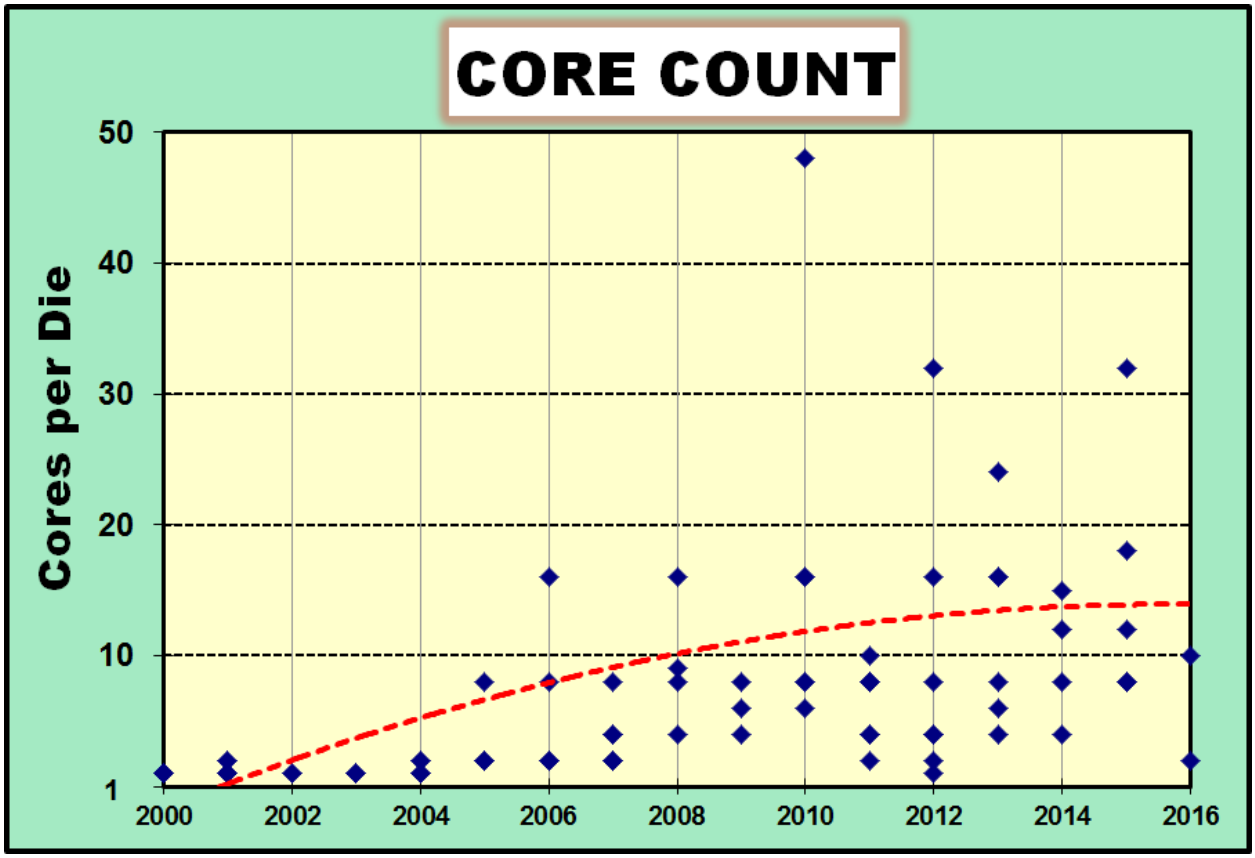
(DIGITAL ARCHITECTURES & SYSTEMS SUBCOMMITTEE
DIGITAL CIRCUITS SUBCOMMITTEE
MEMORY SUBCOMMITTEE)

Digital Architectures & Systems (DAS) – 2016 Trends

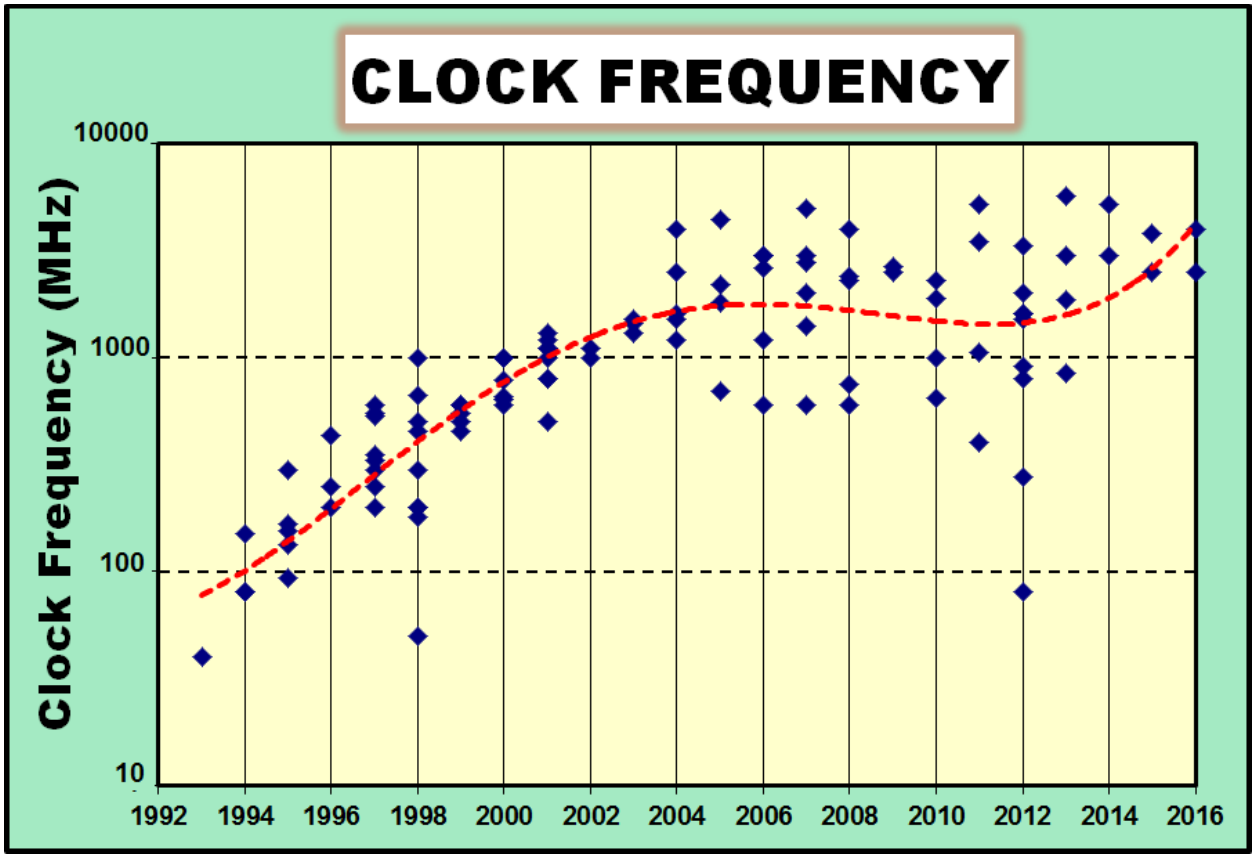
Author: Stephen Kosonocky, Advanced Micro Devices, Fort Collins, CO, Digital Architectures & Systems Sub-Committee Chair

The relentless march of process technology enables the integration of more and more transistors, and hence complex systems on a single chip. This brings advantages in terms of cost, power efficiency and computational capabilities. These trends open up new opportunities in all areas of the compute spectrum, ranging from SoCs for energy-scarce remote sensing applications, powerful yet efficient mobile SoCs, to high-end mainframe and server systems.

Compute power is increased in an energy efficient way, by parallelization and the use of custom accelerators. This permits operation at reduced clock speed, while at the same delivering additional compute performance to meet increasing consumer demands. The graphs below illustrate this clearly: While the number of cores per die is growing steadily, the maximum core clock frequency seems to have saturated in the range of 4-5GHz, primarily limited by thermal considerations. The nominal operating frequency of the power-limited processors this year is around 4GHz. Broader penetration of task-specific accelerators enables higher energy-efficiency.



Core counts on processors published at ISSCC.

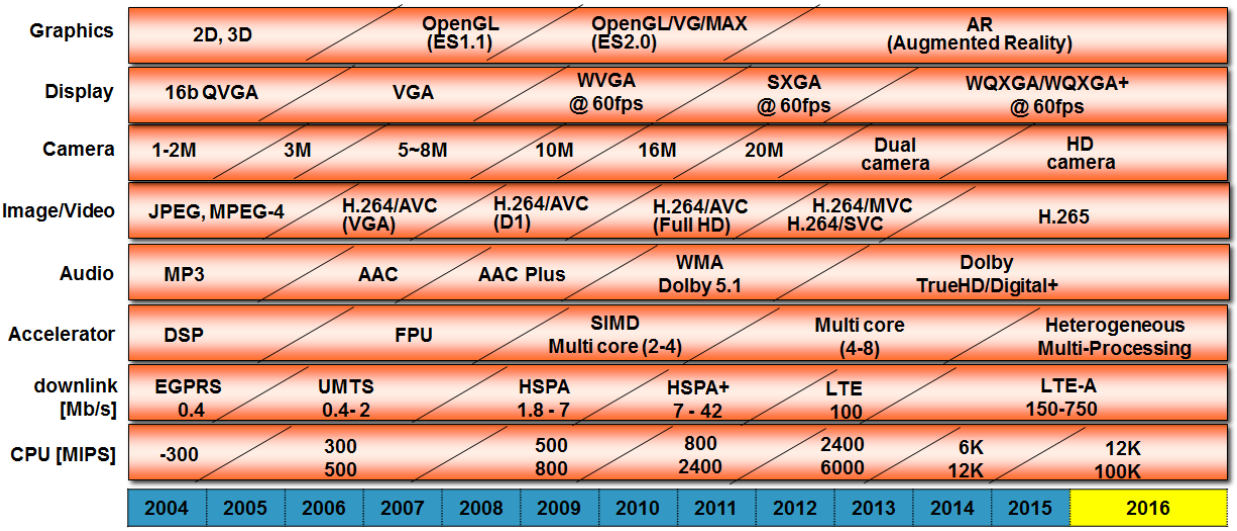


Clock frequency scaling trends.

Using Increased Integration Density to Improve Application Energy Efficiency

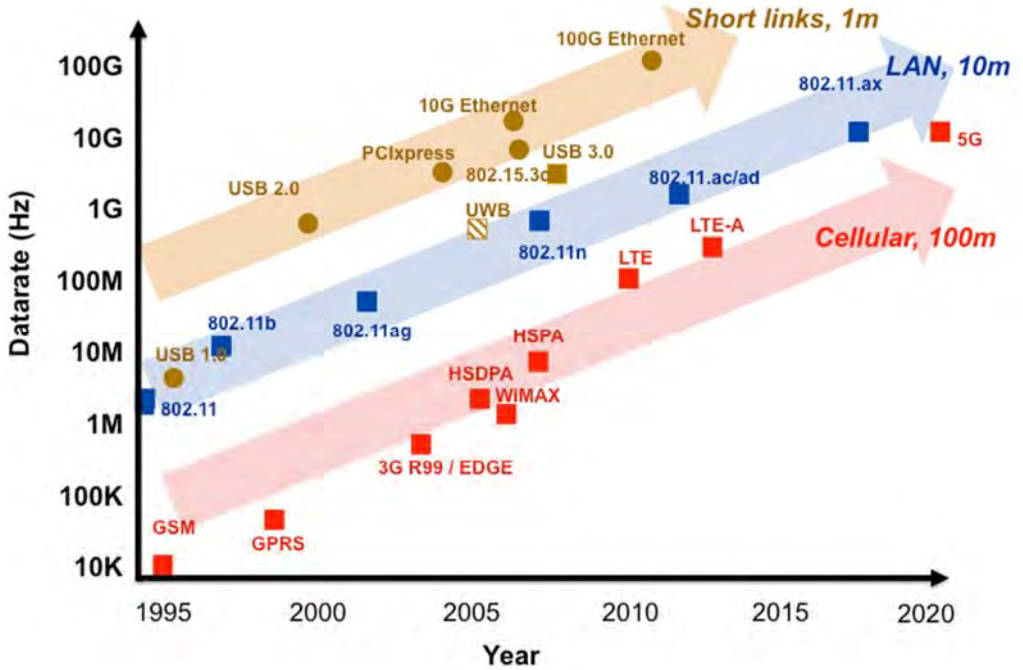
Beyond the class of general-purpose processors, increasing transistor integration density also allows application-specific SoCs to improve energy efficiency. The concept of dark silicon is exploited through the implementation of SoCs with a heterogeneous mixture of programmable and fixed-function IP blocks, which are smartly activated accorded application requirements.

This is especially apparent in the area of application processors for smart phones, illustrated in the figure below. In the late 1990s, a GSM phone contained a simple RISC processor running at 26MHz, supporting a primitive user interface. After a steady increase in clock frequency to roughly 300MHz in the early 2000s, there was a sudden sprint towards 1GHz and beyond. Moreover, following trends in laptops and desktops, processor architectures have become much more advanced, and smart phones incorporate ten-core 64b processors, now running up to 2.5GHz. Heterogeneity was recently adopted to further improve power efficiency, and a recent processor includes cores of three sizes, with different power/performance trade-offs, activated according to application demands. Overall, energy efficiency has become the main challenge in designing application processors, graphics processors, media processors (video, image, audio), and modems (cellular, WLAN, GPS, Bluetooth) for mobile platforms. For video and image processing, the trend has been towards dedicated, optimized hardware solutions. Some examples of new areas where dedicated processors are particularly needed include gesture-based user interfaces, recognition processors, augmented reality and automotive driving assistance.



Application processor trends in smart phones.

Another important class of application-specific SoCs benefiting from the increasing integration density are the baseband SoCs for wired and wireless links. As shown in the chart below, cellular links, wireless LAN, as well as short links show a consistent 10× increase in data rate every five years, with no sign of abating. With essentially constant power and thermal budgets, energy efficiency has become a central theme when designing digital circuits for mobile baseband processing. With benefits from pure CMOS scaling flattening, alternative approaches to improve energy efficiency and system throughputs are being deployed, such as new standards, power efficient algorithms, energy-efficient digital signal processors, application-optimized accelerators, optimized hardware-software partitioning, advanced power management techniques, as well as inter-system aggregation and heterogeneous networks.



Datarate trends in wired, wireless and celluar.

The power consumption of application processors has been increasing (figure below) due to the evolving workloads for advanced graphics and high-resolution images and their associated functional blocks. Power management techniques such as power gating and adaptive supply and body biasing have been widely adopted to suppress the leakage current in standby mode and extend battery life.

Application processor power trends.

Highlights ISSCC 2016

ISSCC 2016 features KAIST's deep learning processors adopted for a variety of application domains, such as natural UI/UX for AR/HMD users, automotive driving assistance, and autonomous navigation of micro-robots. A low-power natural UI/UX processor with an embedded deep learning engine is implemented in 65nm CMOS. It achieves 56.5% higher power efficiency over the latest HMD processor and ~2% higher recognition rate over the best-in-class pattern recognition processor. MIT also proposed an energy-efficient deep convolutional neural network (CNN) accelerator implemented in a 65nm CMOS process. The test chip features a spatial array of 168 processing elements fed by a reconfigurable on-chip network that handles many shapes and minimizes data movement by exploiting data reuse.

Digital Circuits – 2016 Trends

Subcommittee Chair: *Stefan Rusu, TSMC, San Jose, CA*

Demand for higher performance across ubiquitous, connected and energy-constrained platforms ranging from Internet-of-Everything (IoE) to cloud datacenters continues to drive innovations across all CMOS digital circuit building blocks to enable more energy-efficient performance, better scalability, lower cost and enhanced security. Technology scaling continues to be exploited to deliver designs capable of operating at lower voltages, resulting in reduced energy per operation, as well as shrinking the area required to implement specific functions.

Energy Efficiency Techniques and Integrated Voltage Regulators

Low-power silicon technology with reduced supply and feature sizes cuts active energy consumption. At the circuit level, the pursuit of energy efficiency drives innovation in adaptive and near-threshold operation, enabling further supply voltage reduction. All key IP blocks are enhanced with advanced integrated power management and variation mitigation. Special-purpose accelerators are selectively powered up to improve the efficiency of important compute kernels and cryptographic functions. The latest state-of-the-art focuses on dynamic scalability and efficient always-on peripherals, such as real-time clocks and wake-up sensors, enabling nano-Watt operation from integrated energy harvesters for edge devices in the IoE.

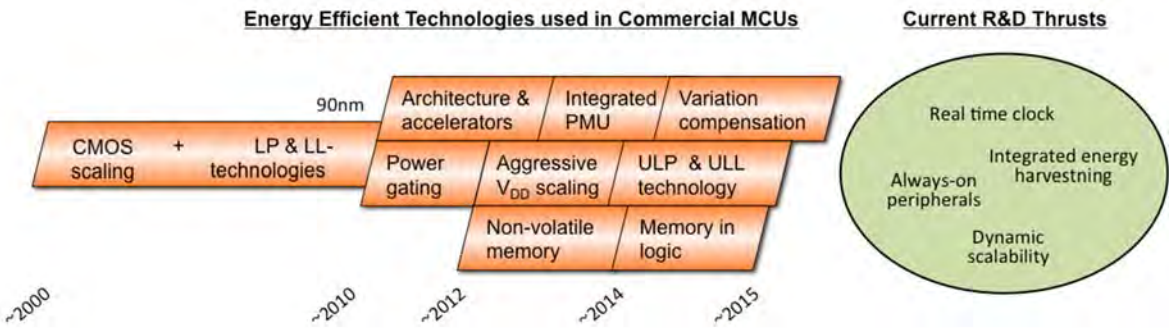


Fig. 1 Energy-efficiency techniques

Voltage regulators, while traditionally being off-chip, have increasingly been integrated on-chip to reduce cost. Low dropout (LDO) linear regulators and switched capacitor voltage regulators (SCVR) are integrated into SoC designs in scaled process nodes to enable faster and fine-grain DVFS of individual functional blocks, without major impacts on process cost and complexity. The conversion efficiency and current density of these integrated voltage regulators has been improving.

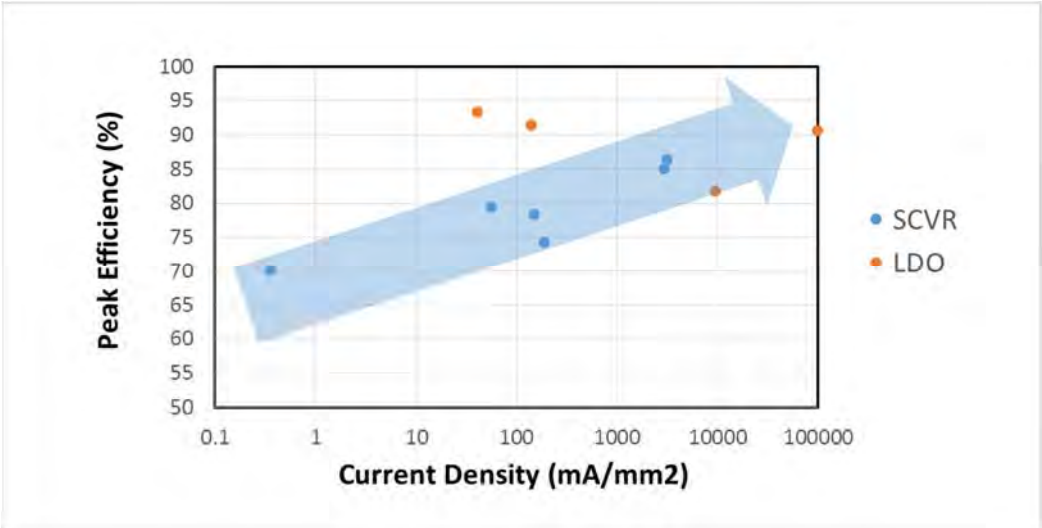


Fig. 2 Integrated voltage regulators

Scalable Digital PLL and MDLL and Special-Purpose Circuits

We observe that traditionally analog building blocks such as PLLs, MDLLs, integrated voltage regulators and sensor/monitor circuits

are being implemented using digital techniques to cope with variability and ease scaling to finer geometries. Recent developments in ISSCC 2016 include the capability for continued operation while PLL output frequencies are adjusted.

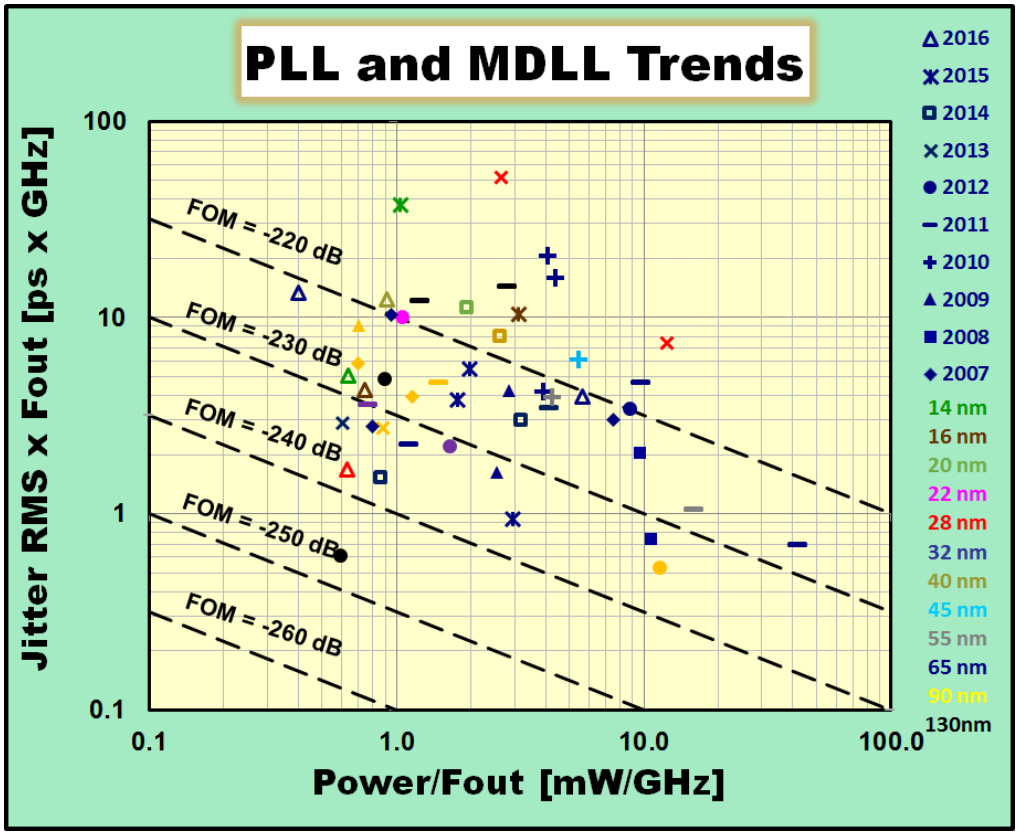


Fig. 3 PLL and MDLL trends.

Circuits for Hardware Security

Hardware security modules have become one of the essential building blocks in an IoE device. PUFs (Physically Unclonable Functions) have become commonplace for IC fingerprinting and anti-counterfeiting. TRNGs (True Random Number Generators) are leveraged for secret key generation in cryptographic applications. The figure below shows how energy/bit has scaled for such structures in recent ISSCCs, to satisfy both low-energy and stable operation at the same time.

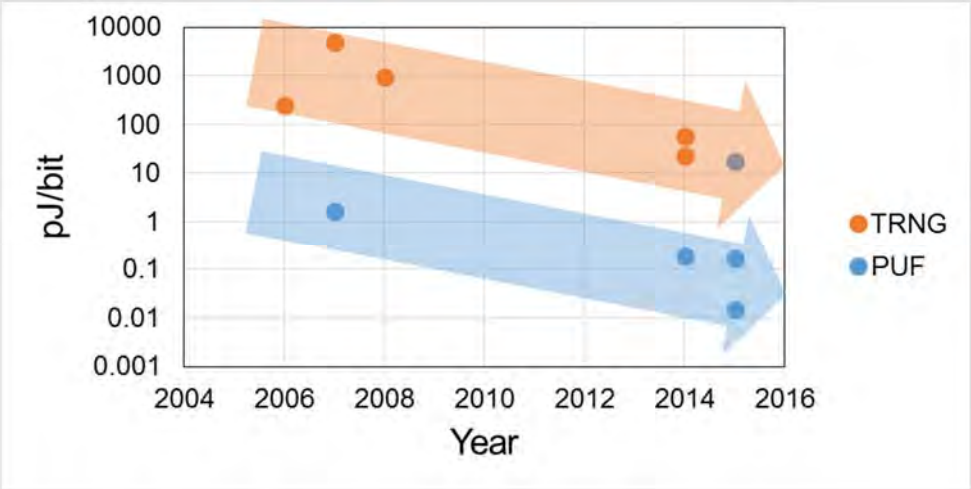


Fig. 4 Energy-efficiency evolution in security circuits.

Memory – 2016 Trends

Subcommittee Chair: *Leland Chang, IBM, Yorktown Heights, NY, Memory*

Memory systems continue to demand high density, high bandwidth, and low energy for IoE/wearables, uutomotive, high-performance computing and Mobile applications. High-performance memory interface technologies are developed for discrete (GDDR5), 2.5D (HBM2) and 3D (WIO2) packaging targeting high-performance and mobile applications. 3b/cell 3D NAND started becoming standard for high-density storage with further area reduction through hiding logic under the memory array. Embedded Flash continues to serve very low energy, high-reliability nonvolatile memory (NVM) for automotive applications. STT-MRAM and RRAM are emerging embedded NVM where PCM is a candidate for high performance Storage Memory.
Some current state-of-the-art papers from ISSCC 2016 include:

- Two 10nm SRAM bitcells, 0.040μm^2 high Density (HD) and 0.049μm^2 High Current (HC), with circuit techniques showing as high as 130mV Vmin improvement.
- A 307GB/s HBM2 in 20nm technology operating at 1.2V for 2.5D packaging with options of 2, 4 and 8 memory die stacking.
- A 68GB/s 8Gb WIO2 for 3D stacking for low-power data transfer in mobile applications.
- 9Gb/s/pin 8Gb GDDR5 in 20nm process serving discrete high-bandwidth graphics and HPC applications.
- A 48-Layer WL stacked 256Gb 3D NAND achieving 53.2MB/s write throughput
- A 179mm^2 3b/cell 768Gb 3D floating gate NAND Flash with page buffers hidden under array.
- A 90nm embedded 1T-MONOS Flash with 0.07mJ/8KB rewrite energy and 100M endurance targeting very low power automotive applications.

SRAM

For embedded high-speed applications, SRAM continues to be the memory of choice – from mobile to high performance servers to Internet of Everything. This year's conference highlights 10nm FinFET technology with the smallest bitcell achieved to date for SRAM – at 0.040µm2 for High Density and 0.049um2 for High Current. Area efficient 8T SRAMs are demonstrated in 14nm FinFET by adopting small signal sensing to enable longer bitlines to achieve 5.6Mb/mm2 bit density and 560mV Vmin. FD-SOI is utilized by researchers in applying Razor techniques to SRAM. By double sampling during reads and merging wordlines in a dual-port bitcell for writeability gains, energy efficiency at 0.6V is improved by 70% compared to reference design. Fig.1 shows SRAM bit cell area and Vmin scaling trend.

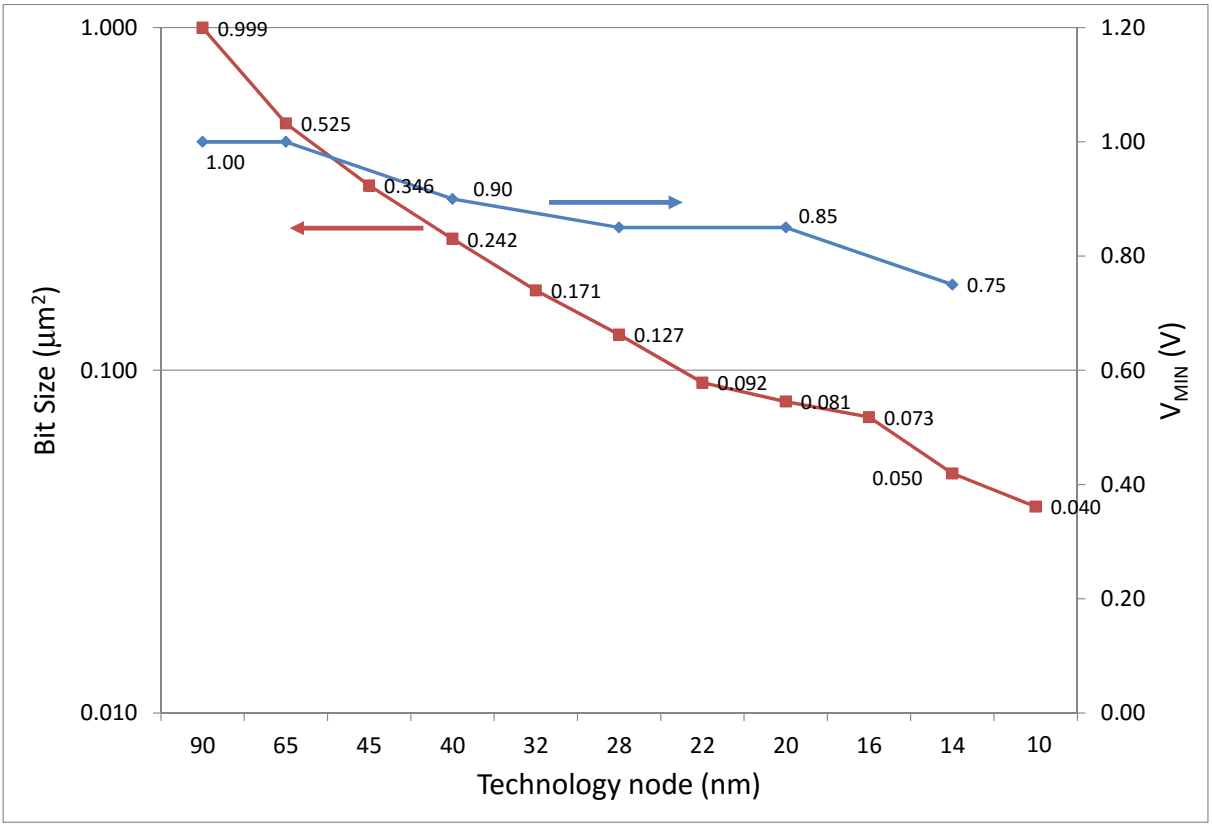


Figure 1 – Bit Cell and V_{min} scaling trend of SRAM

HIGH-BANDWIDTH DRAM

In order to maintain the optimal memory hierarchy ratio with respect to storage memory, DRAM continues to scale density, form factor, and bandwidth. GDDR5 delivers 9Gb/s/pin in 20nm technology to serve high-end discrete memory needs. A 128GB/s first generation HBM was shown before with 1Gb/s/pin in-package memory. This year two versions of 2nd generation HBM are shown that can scale from 2 to 8 stacked memory dies for various density needs while achieving doubled bandwidth of 256GB/s. Finally, a much improved 2nd generation WIO DRAM is demonstrated for 3D Stacking in 8Gb, 68GB/s bandwidth. Fig. 2 shows DRAM Bandwidth scaling over last decade.

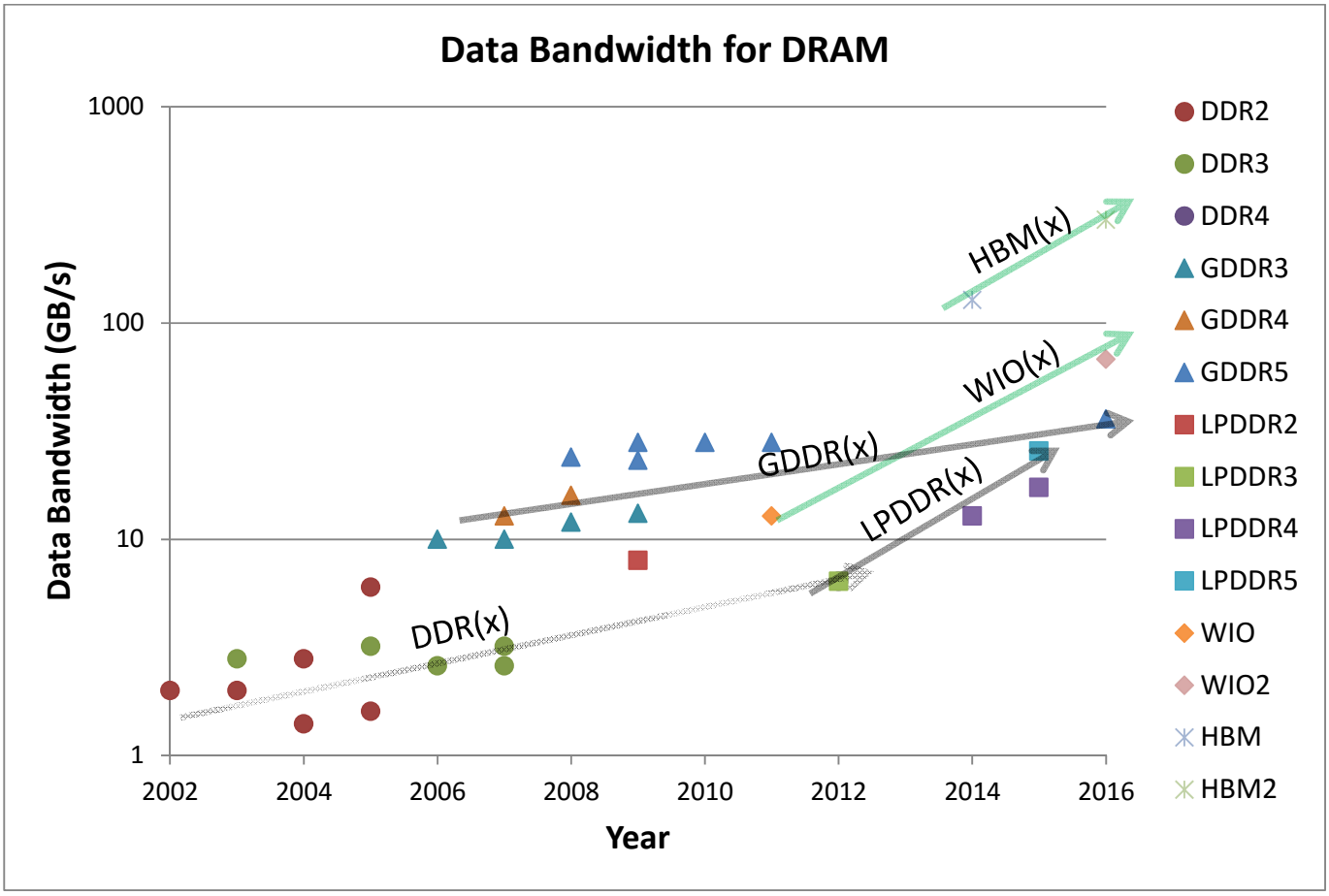


Figure 2 - DRAM Data Bandwidth Trends

NONVOLATILE MEMORIES

In the past decade, significant investment has been put into the emerging memories field to find an alternative to floating-gate-based nonvolatile memory. The emerging NVMs, such as phase-change memory (PRAM), ferroelectric RAM (FeRAM), magnetic spin-torque-transfer (STT-MRAM), and Resistive memory (ReRAM), are showing potential to achieve high cycling capability and lower power per bit in read/write operations. Figure 3 highlights how 3b/cell (TLC) NAND Flash write throughput continues to improve. Figure 4 shows significant increase in NAND Flash capacity from 128Gb to 256Gb and 768Gb this year. Such high capacities are achieved through advancements in 3-dimensional vertical bit cell stacking technologies.

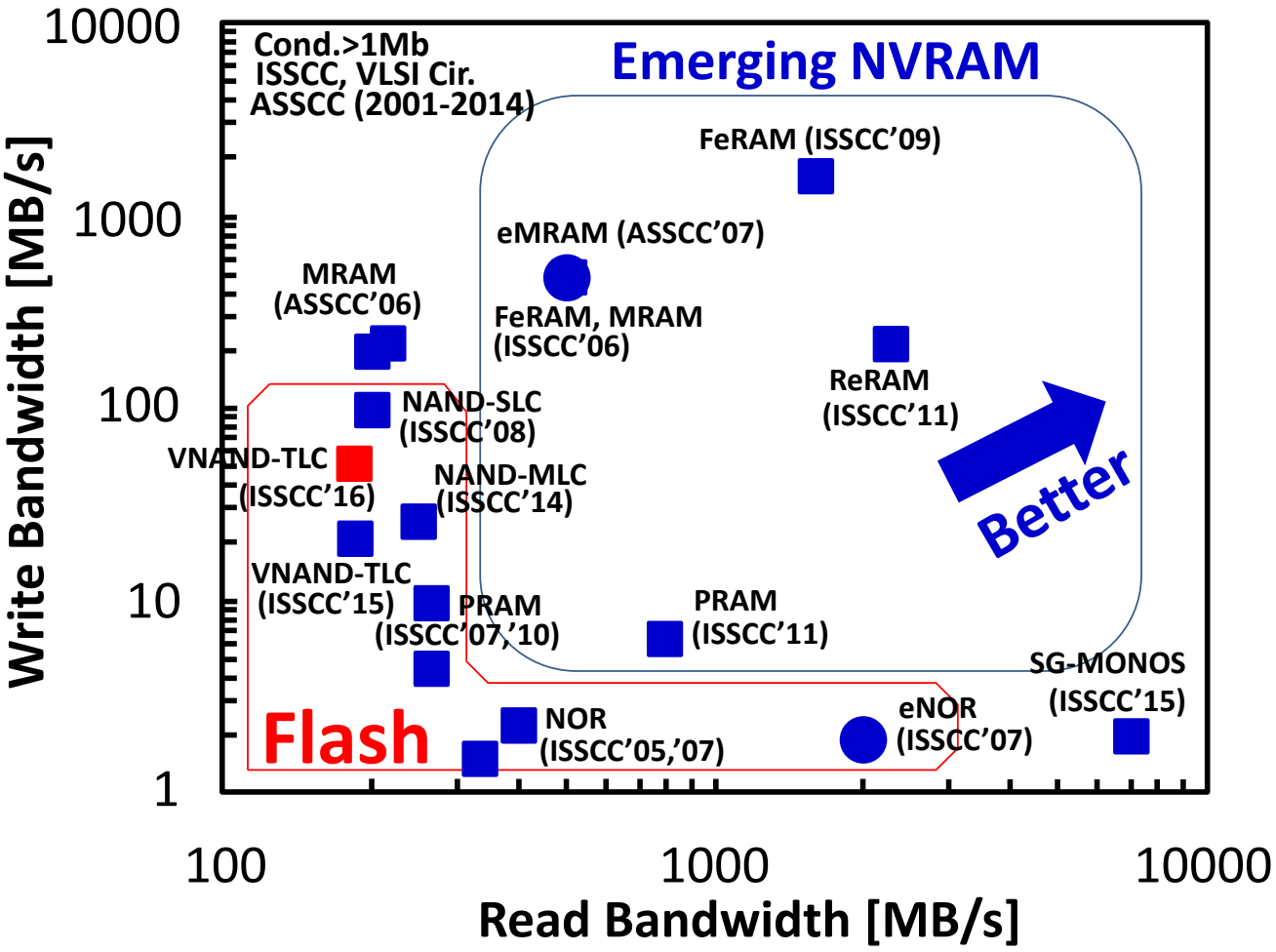


Figure 3 - Read/Write Bandwidth Comparison of Nonvolatile Memories

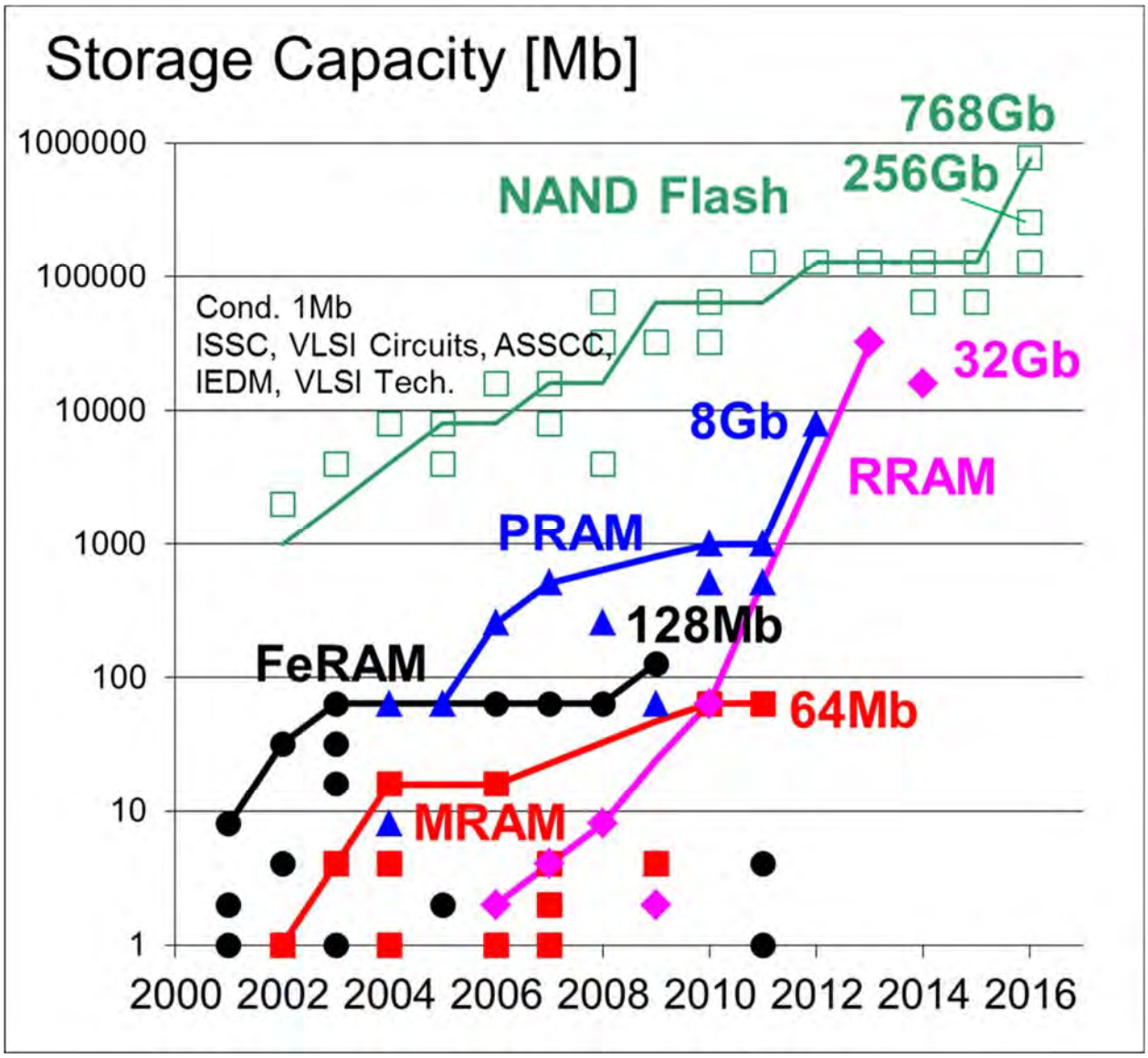


Figure 4 - Memory Capacity Trend of Emerging Nonvolatile Memories

NAND FLASH MEMORY

NAND Flash memory continues to advance towards higher density and lower power, resulting in low-cost storage solutions that are replacing traditional hard-disk storage with solid-state disks (SSDs). SSDs with typical storage density of 240GB have become the mainstream. Despite the growing difficulties to further scale down planar cell technology, the latest 2D NAND Flash technology is scaled down to 14nm, achieving 128Gb device occupying only 130mm^2. It would be very interesting to see how far planar NANDs go down the scaling path. This year, two types of 3b/cell 3D NANDs with 256 and 768Gb densities are reported, continuing the trend to satisfy the ever-growing demand for increased density requirements and lower manufacturing cost. The 256Gb device is based on the 3D NAND technology extending the number of stacked layers from 32 to 48. On the other hand, the 768Gb device is based on the floating gate technology. Figure 5 shows the observed trend in NAND Flash capacities presented at ISSCC over the past 20 years.

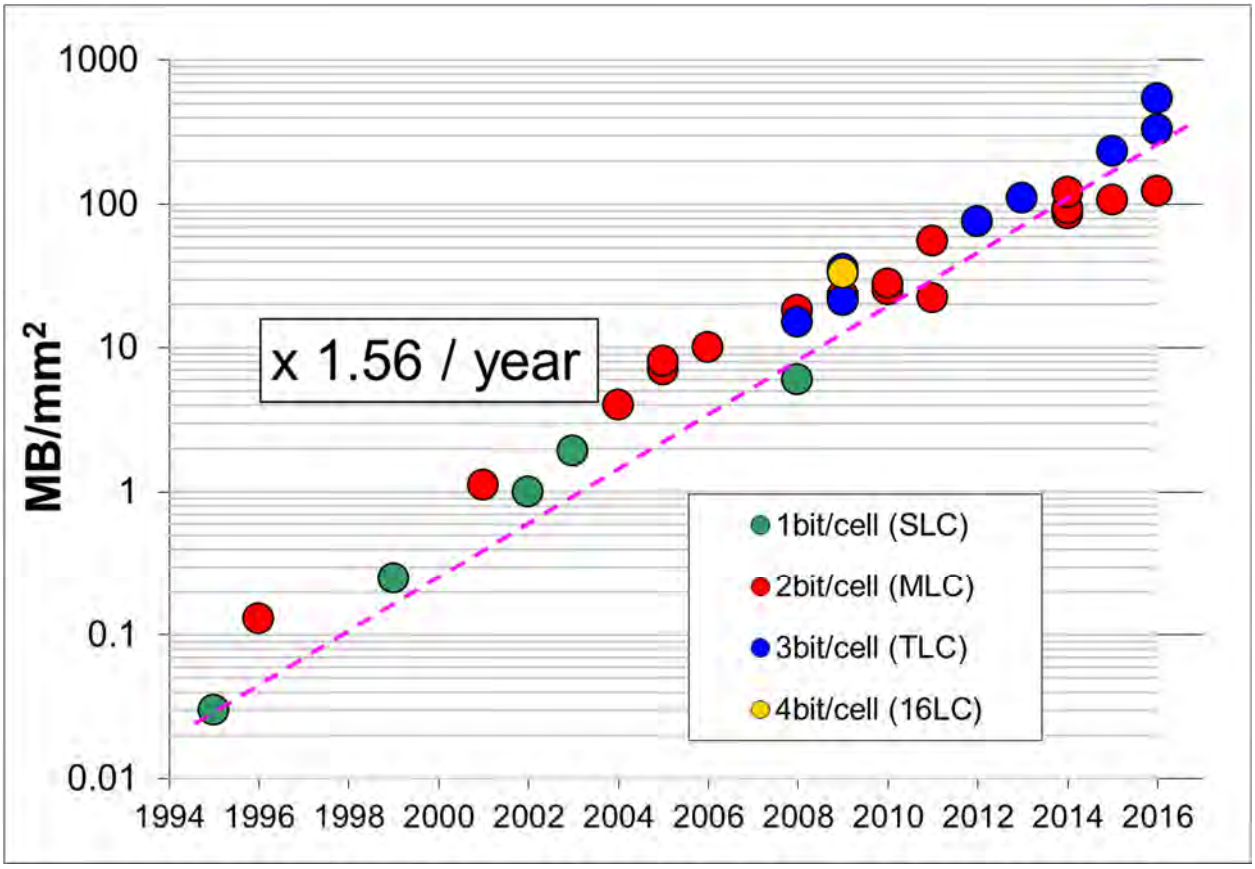


Figure 5 - NAND Flash Memory Trends

HISTORICAL TRENDS IN TECHNICAL THEMES

INNOVATIVE TOPICS

(IMAGERS/MEMS/MEDICAL/DISPLAYS SUBCOMMITTEE
TECHNOLOGY DIRECTIONS SUBCOMMITTEE)

IMMD – 2016 Trends (Sensors, MEMS & Displays)

Subcommittee Chair: *Makoto Ikeda, University of Tokyo, Tokyo, Japan*

Sensors are a key building block for the Internet of Everything. They collect the data and are an important part of the value chains that are enabling new services and fueling the need for more internet bandwidth. Increasingly, multiple sensors and their associated interface circuits are being combined on a single chip, or in a single package, allowing multi-parameter sensing and compensation for cross-sensitivity. Digital-centric implementations of sensor interfaces enable these improvements to be maintained in more advanced processes.

MEMS inertial sensors (accelerometer and gyroscopes) are key components used in a wide variety of consumer products, where low power consumption is a key requirement. For automotive applications, reduced vibration sensitivity and drift, but also high precision and reliability are additional requirements. In addition to consumer applications, with continuing improvements in accuracy, stability and cost, MEMS inertial sensors have emerged as strong contenders for high-performance navigation and positioning related applications.

Making use of the superior mechanical properties of silicon, MEMS are also expanding in many other sensing areas beyond motion sensing. Pressure sensors and ultrasonic transducers are getting smaller and more versatile. Integration of transducer arrays with CMOS circuits enables applications like ultrasonic fingerprint sensing.

CMOS temperature sensors continue to improve, with new circuit techniques increasing accuracy, supporting wider applications. While other new sensor principles for remote temperature sensing using the spectral thermal information of radiation are productizing, the change of resonance frequency with temperature of a MEMS oscillator circuits creates highly precise temperature references.

Another clear trend can be seen in the implementations of monitors in digital CMOS processes enabling spatially resolved chip temperature monitoring in large digital circuits. This is an increasingly important application case today, where other sensor parameters like small sensor area and a good variability are key performance features. While conventional BJT-based sensors continue to be applicable, thermal diffusivity is emerging as a new sensing concept that benefits from technology scaling.

Both direct and indirect current sensors are becoming more integrated and precise. Indirect current-sensing devices detect the magnetic field around a wire or trace carrying a current, and are used for instance in electrical motor drives, solar power, and battery-charging applications. Fluxgate technology arises as a third alternative to Hall- and GMR-effect based sensors while these become faster, now sensing current (or magnetic field) with a bandwidth up to 3MHz.

LCD panels with integrated touch sensing are both growing in size and becoming thinner at lower-cost. Robust circuit technology that is immune to display-driver noise is a now becoming a key design factor. For reliable touch sensing, sufficient attenuation of the noise interference injected through a touch object becomes important. As panel size and resolution of flat-panel displays grow, the challenge for a column driver to program the correct data voltage into a pixel (the one-horizontal (1-H) time) is reduced. It is becoming a main bottleneck of realizing high-resolution display.

IMMD – 2016 Trends (Medical)

Subcommittee Chair: Makoto Ikeda, University of Tokyo, Tokyo, Japan

There is an ever-increasing demand for higher-throughput life-science tools, e.g., cellular and molecular assays, coming from the field of precision and personalized medicine. Electronic platforms for genomics, proteomics, and cellular assays bring improved accuracy and throughput. For example, increased sensitivity has been successfully exploited for detection of chemical reactions through physical means, e.g., pH, charge, or impedance changes, in DNA sequencing.

Sensors used for monitoring human body parameters like electrocardiogram (ECG), electroencephalogram (EEG), bio-impedance or photoplethysmogram (PPG) are becoming more portable and lightweight so that they are easier to wear. While in the past, driving designs to even lower energy consumption to keep or even increase sensor lifetime was key, this year the resolution of the individual sensors and the amount of different sensing modalities in one device is increasing.

Both sensor and actuator systems for in-body implantable usage are maturing. New circuit concepts preventing charge accumulation at the electrode to neuron interface while doing faster and higher signal neuron activation are emerging. The ultimate goal of those developments is a closed-loop control of the neuron interface. This will allow therapy to be applied directly, for instance to suppress seizures or arrhythmias or to recover from motor function loss after spinal cord injury.

Medical imaging is an important field with a growing number of applications. For improved capability and quality, medical ultrasound is moving toward 3D imaging with large arrays. As the number of transducer elements in arrays increases, the number of connections to the front-end circuitry is becoming a bottleneck. The same trend is obvious for the amount of signal processing needed. To resolve these congestions, MEMS transducers and CMOS technology increasingly allow transducer arrays and their signal processors to be mounted together. Also the resolution and the pixel number of imagers for monitoring electrical activity of neurons is growing. Newest developments integrated more than 50,000 electrodes per imager.

IMMD – 2016 Trends (Imagers)

Subcommittee Chair: Makoto Ikeda, University of Tokyo, Tokyo, Japan

The CMOS-image-sensor business continues to be a significant part of the semiconductor industry. Key applications still include cellphone cameras, digital still cameras, camcorders, security cameras, automotive cameras, digital-video cameras, wearable devices, and gaming. However, new applications are also emerging that are calling for high sensitivity, large pixel size, or large pixel format. Even unconventional uses for imagers have emerged, including free-space optical communications.

The resolution and miniaturization races are ongoing but slowing down, and while the performance requirements stay constant, pixel size continues to scale down (see Figure 1). Images of over 250Mpixels and sensors for large TV format (8K) have been reported for high-end still and video cameras, respectively. A column-parallel approach based on pipelined and multiple-sampling implementations has become standard for low-power, high-speed, low-noise camera and video applications. Backside illumination is now a mainstream technology for mobile imaging and has been applied to image sensors with a 35mm full-size optical format. Wafer stacking of the image array on a CMOS image signal processor is becoming more common in mobile applications.

The importance of digital signal processing technology in cameras continues to grow in order to mitigate sensor imperfections and noise, and to compensate for optical limitations. The level of sensor computation is increasing to thousands of operations-per-pixel, requiring high-performance and low-power digital signal processing solutions.

High Dynamic Range (HDR) is now well established in low-cost consumer imaging. While HDR combines multiple distinct images, new work is progressing with specialized architectures to extend the dynamic range in single exposures, and thus avoid movement artifacts. Image sensors employing organic photoconductive film have been reported to enable improved low-light sensitivity, increased dynamic range, global shutter, multiple exposure and variable sensitivity image capture.

As well, global shutters are being introduced to avoid movement artifacts. Global-shutter pixels have been employed in digital broadcasting cameras. For precision scientific, medical applications, and consumer products, we now employ single-photon avalanche diode (SPAD) imager arrays. Deep-submicron CMOS SPADs will meet the requirements for high resolution, high accuracy time-to-digital converters (TDCs), and small-pitch imagers with better fill factor. Hybrid pixel structure of the conventional photodiode and SPAD has been reported. Wafer stacking of the SPAD array on a CMOS image signal processor is an emerging trend.

The market share of CCD imagers continues to shrink and they are now relegated to minor applications. Top-end broadcast and top-end digital cameras have moved from CCD to CMOS sensors (see Figure 1).

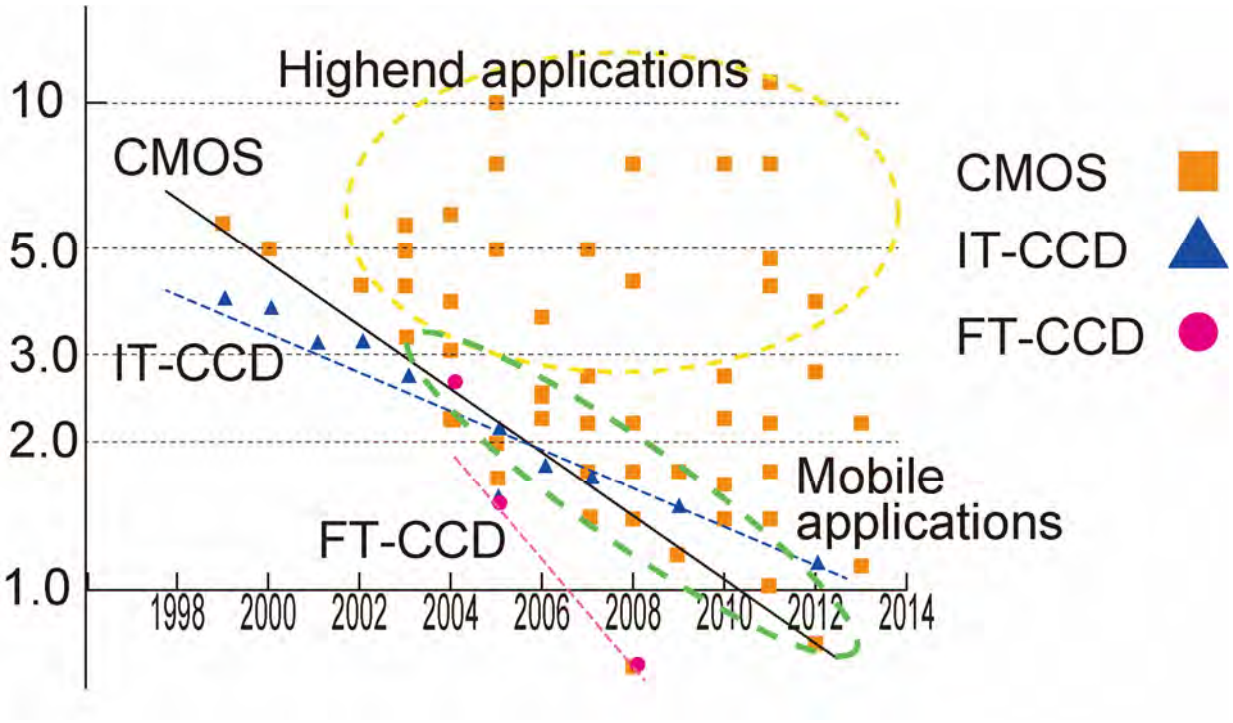


Figure 1: Pixel size trends

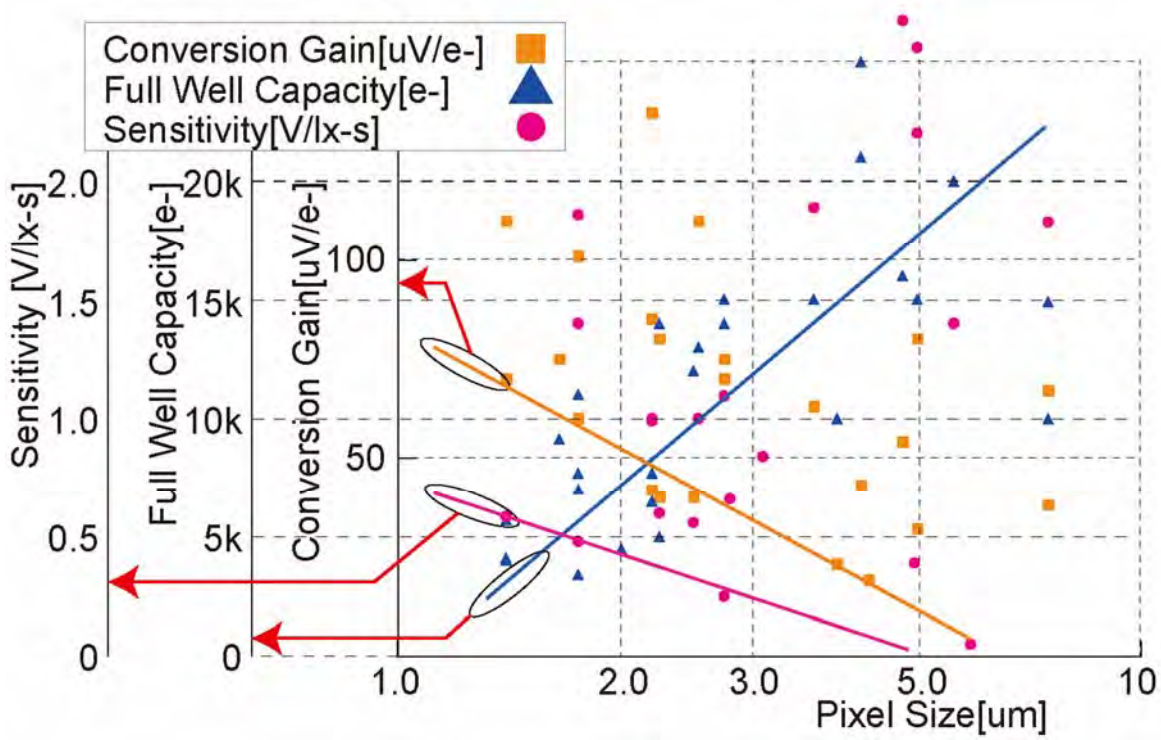


Figure 2: Image sensor performance trends: sensitivity, full-well capacity and conversion gain vs. pixel size.

Technology Directions – 2016 Trends
"Innovative Biomedical Systems"

Subcommittee Chair: *Eugenio Cantatore, Eindhoven University of Technology, Eindhoven, The Netherlands*

Architectural considerations are extremely important for building today's biomedical systems. Ten years ago, biomedical electronics research focused on developing devices for high-quality medical sensing. Recently, focus has shifted towards developing highly integrated systems, requiring biomedical system designers to understand and optimize a multitude of aspects including power delivery, wireless communication, sensor signal quality, and SNR. Such systems will enable improvements of the quality of life, such as self-health checks, remote medical examination, and constant monitoring for acute diseases by bringing the point-of-care to the patient.

Key enablers of biomedical systems include:

(1) High-accuracy and multi-modal monitoring devices for superior QoS,
(2) Small footprint devices
(3) Ultra-low-power processor and wireless communication systems.

Biomedical systems need to have high-accuracy sensing. Traditional medical applications employ high-quality monitoring devices with the desired accuracy, however, at a high cost. To enable using cost-efficient sensors, innovative methodologies to efficiently compensate for artifacts are being developed. One such example is motion artifacts correction that minimizes the adverse effects of subject movements on the acquisition of weak vital signals such as electrocardiogram (ECG) and electroencephalogram (EEG). Furthermore, state-of-the-art biomedical SoCs are capable of multi-modal monitoring by sensing a variety of bio-signals and processing them in a single SoC to further expand the diagnosis capability and quality of the system.

One critical requirement of a biomedical system is to have a small footprint in order to be highly portable and minimally or non-invasive to the patients. To develop devices with a small footprint, research has been done on highly integrated biomedical SoCs that include embedded sensors, power delivery, signal processing and wireless communication functionalities. Also, advancements in MEMS technologies in the development of 3D-integrated electrodes and sensors have contributed to reduce the footprint of the sensors.

In biomedical systems, often the battery determines the footprint, thus requiring very good power efficiency. To improve the power efficiency, SoC blocks are being optimized across the entire system. For example, the power efficiency of the biomedical frontends has been improved substantially, with typical Noise Efficiency Factors (NEFs) now below 2. A dedicated processor is included to run diagnostic algorithms locally to reduce the data which are transmitted wirelessly from the patient to the doctor. Furthermore, innovative communication standards such as body channel communication (BCC) are being developed. BCC takes advantage of the body environment to enable ultra-low power communication, as compared to the relatively power-hungry wireless communication schemes. Implementing all circuits to run at ultra-low voltage (<0.5V) can make possible extremely low power dissipation, to the level where power delivery can be performed from an energy-harvesting technology.

Another trend in biomedical systems is the move towards Lab-on-Chips, which are semiconductor systems for diagnosis and disease screening. These portable silicon-based solutions can quickly and inexpensively: (1) diagnose illness from simple blood tests, (2) perform medical imaging and spectroscopy. Emerging technologies such as MEMS or CMOS-CNT (carbon nanotube) arrays are being developed to make it possible to bring traditionally expensive diagnosis technologies to rural and remote areas where medical expertise is typically scarce.

In line with these historical trends, ISSCC 2016 Session 22 features 8 papers representing the latest technological innovations in biomedical systems.

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Analog Systems includes Analog and Data Converter Subcommittees	**5, 12, 15, 21, 27**
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