2011

PRESS KIT

ISSCC PRESS KIT DISCLAIMER

The material presented here is preliminary.
As of November 1, 2010, there is not enough information to guarantee its correctness.
Thus, it must be used with some caution.

ISSCC VISION STATEMENT

The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and use to maintain technical currency, and to network with leading experts.

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ISSCC 2011

Conference Overview

CONFERENCE THEME

ELECTRONICS FOR HEALTHY LIVING

The ISSCC 2011 Conference theme is:

"Electronics for Healthy Living"

Electronics play a significant role in enabling a healthier lifestyle. Technology in the hospital enables doctors to diagnose and treat illnesses that might have gone undetected just a few years ago. External monitors provide us with a good assessment of our health risk and vital-sign status. Those with chronic diseases can live a more normal life with internal and external electronic devices. In the future, Body Area Networks could be connected to a monitoring program running on our mobile phone. Those with disabilities also benefit from electronics that improve their lifestyle. Contributions to ISSCC are encouraged in support of this theme.

EVENTS

TUTORIALS (SUNDAY, FEBRUARY 20, 2011)

- **9** 90-minute Tutorials, each taught twice, by circuit experts from the International Technical Program Committee, serve to meet attendees` needs for introductory material in circuit specialties.

FORUMS (SUNDAY & THURSDAY, FEBRUARY 20 & 24, 2011)

- Circuit experts exchange information on their current research in an all-day informal environment.

SPECIAL-TOPIC EVENING SESSIONS (SUNDAY – TUESDAY, FEBRUARY 20-22, 2011)

- **6** Special-topic presentations, in which experts provide insight and background on a subject of current importance.
- **Student Research Preview** – short student presentations of work-in-progress at Universities around the world.

EVENING PANELS (MONDAY – TUESDAY, FEBRUARY 21-22, 2011)

- **2** Panels in which industrial and academic experts debate a selected topic and field audience questions in a semi-formal atmosphere.

TECHNICAL SESSIONS (MONDAY – WEDNESDAY, FEBRUARY 21-23, 2011)

- **3 invited talks, and 1 distinguished panel** presented in the Plenary Session.
- **211 technical papers** presented in **28** Regular Sessions, highlighting the latest circuit developments.

SOCIAL HOURS (MONDAY – TUESDAY, FEBRUARY 21-22, 2011)

- Network with experts in a wide range of circuit specialties; meet colleagues in an informal exchange; browse the technical-book exhibits!

SHORT COURSE (THURSDAY, FEBRUARY 24, 2011)

- Intensive all-day course on a single topic, taught by world-class instructors, can serve to “jump start” a change in an engineer’s circuit specialty.

PAPER STATISTICS

OVERALL:

- **3** papers invited
- **669** papers submitted to ISSCC 2011
- **211** papers accepted
  - **80** papers from North America, including
    - **36** Industry papers
    - **43** University papers
    - **1** Institution/Lab papers
  - **69** papers from the Far East, including
    - **30** Industry papers
    - **38** University papers
    - **1** Institution/Lab papers
  - **62** papers from Europe, including
    - **22** Industry papers
    - **19** University papers
    - **21** Institution/Lab papers
- **28** Sessions, over 3 days

INTERNATIONAL SCOPE:

	2011	2010	2009	2008
Americas:	38 %	41 %	38 %	43 %
Far East:	33 %	31 %	35 %	28 %
Europe:	29 %	28 %	27 %	29%

WIDE COVERAGE:

	2011	2010	2009	2008
Analog:	10 %	9 %	11 %	9 %
Data Converters:	8 %	7 %	7 %	10 %
Energy-Efficient Digital:	6 %	6 %	6 %	5 %
High-Performance Digital:	7 %	10 %	4 %	7 %
Imagers, MEMs, Medical, and Displays:	14 %	12 %	12 %	11 %
Memory:	10 %	11 %	9 %	12 %
PLL:	--	6 %	--	--
RF:	12 %	8 %	11 %	11%
Technology Directions:	10 %	12 %	13 %	12%
Wireless:	11 %	11 %	13 %	11%
Wireline:	11 %	8 %	14 %	11%

PLENARY SESSION

Paper 1.1:
New Interfaces to the Body Through Implantable System Integration
Steve Oesterle, *Senior Vice President, Medtronic, Minneapolis, MN*

This presentation will discuss:

- For the last 40 years, Moore's law has driven the semiconductor industry, enabling new interfaces to the world.
- This engine has provided enhanced sensing, processing, actuating, and communicating with the environment.
- A particular beneficiary has been, is, and will be healthcare.
- The first marked success was the implantable electronic pacemaker.
- Then cellular modulation schemes were developed to ameliorate neurological disorders.
- But, future developments must include a systems approach in the design of both implantable devices and the entire healthcare pathway.
- Implantable designs must heed three abstractions: device interface, information flow, and energy management.
- As Moore's law slows for simple planar scaling, packaging and other techniques introduce "More than Moore".
- In spite of obvious dramatic developments, much remains to be done: system-focused thinking is needed for individual device development, and for a more global approach to easing clinical burden with improved patient outcomes.

Paper 1.2:
Game-Changing Innovation for Wireless Personal Healthcare and Lifestyle: Magical, Revolutionary and Low-Cost Product Opportunities
Jo De Boeck, *Senior Vice President, imec, Leuven, Belgium*

This presentation will discuss:

- Healthcare is increasingly reliant on silicon for disease-centric care, patient-centric decision making and therapy, proactive personalized ubiquitous diagnosis and treatment.
- Personalized predictive preventive participatory healthcare implies massive measurement, myriad data, and convenient ICT infrastructure.
- Future data will be gathered "on the move" in residential and desolate settings by minimally-trained individuals.

- Currently, self-reported data is key to clinical trials, diagnosis, treatment progress, and assessment of quality of life. But, it is not reliable!
- In the future, connected devices which provide such data in acceptable unobtrusive ways, with guaranteed quality, privacy, and identity, will make all the difference.
- Such monitoring can potentially capture high-yield micro-events that predict upcoming problematic situations.
- Currently, wireless ECG patches are starting to impact care efficiency; in the future, multi-sensory smart patches will be a game changer.
- Such patches will connect to healthcare infrastructure will likely smell, listen, and feel.
- But, change in interaction between the medical and electronics communities is necessary, as illustrated by current world-wide trials of wireless sensors and body-area networks.
- Body-area networks are likely to foster and strengthen the individual in their search for better quality of life.

Paper 1.3:
Eco-Friendly Semiconductor Technologies for Healthy Living
Oh-Hyun Kwon, *President, Samsung Electronics, Giheung, Korea*

This presentation will discuss:

- Pollution has negatively affected the positive contributions of technological development.
- All industries must commit themselves to rescuing us from this peril!
- A dominant source of pollution is energy consumption.
- Semiconductor manufacturers can contribute directly and indirectly in several ways: reduce energy required in their basic manufacturing processes; reduce energy required by all products; encourage low-energy replacement by electronics of high-energy mechanisms.
- Semiconductor efficiency can be achieved by improved design including architecture, design methodology, process technology, and packaging.
- Pollution reduction can be achieved also by improved interaction with other industries: software developers and end-users for overall product efficiency, power-equipment manufacturing, generation, and distribution companies.
- To reduce power consumption of the semiconductor manufacturing industry itself, a strong cooperation with fabrication-equipment manufacturers is necessary.
- Recent examples of all of these many approaches include power-efficient multi-core processors, green memory solutions, 3D packaging, low-voltage low-leakage process technologies, low-power design methodologies, and implementing technology for smart-grid power systems.
- For an eco-friendly future, the IC manufacturing industry has lots of work ahead!

1.4 Technology Roundtable:

Beyond the Horizon: The Next 10x Reduction in Power – Challenges and Solutions

In this inaugural Plenary Technology Roundtable, experts will discuss opportunities for achieving the next order-of-magnitude reduction in energy consumption across various domains, including analog, digital, RF, and memory. The role of process-technology innovation and CAD tools will also be discussed.

Three domain experts will challenge the six distinguished panelists to suggest directions for the future, and help create a roadmap for next-generation energy-efficient electronics.

Moderator: **Jan Rabaey**, Professor, University of California, Berkeley, Berkeley, CA

Panelists: **Jack Sun**, CTO, TSMC, Hsin-Chu, Taiwan
Dan Dobberpuhl, Consultant, Monterey, CA
Kiyoo Itoh, Fellow, Hitachi, Tokyo, Japan
Philippe Magarshack, Group Vice President, STMicroelectronics, Crolles, France
Asad Abidi, Professor, University of California, Los Angeles, Los Angeles, CA
Hermann Eul, Executive Vice President, Infineon, Neubiberg, Germany

Domain Experts: **Hugo De Man**, Professor Emeritus, imec, Leuven, Belgium
Mark Horowitz, Professor, Stanford University, Stanford, CA
Takayasu Sakurai, Professor, University of Tokyo, Tokyo, Japan

TECHNICAL HIGHLIGHTS

Analog:

- A digital PLL incorporates a new technique to remove the effects of power-supply noise that have plagued prior PLLs when integrated in system-on-chip ICs. Toshiba uses a digital calibration signal to facilitate cancellation of the deleterious effects of power-supply disturbances. **[5.6]**
- Highly efficient LED lamps can now be driven directly from the wall! A new BiCMOS chip designed by Fairchild Semiconductor connects to 110 and 220 VAC, and delivers a power factor of 0.98 and 0.92 respectively into a 5W LED. **[13.1]**
- Extraordinary DC performance is now combined with very low noise in a chopper operational amplifier. Analog Devices has established a new world record of 5.9nV/√Hz achieved with a maximum of only 0.78μV of input offset. **[13.4]**
- Advanced microprocessors can now contain their own power regulators: an extremely efficient DC-DC converter has been implemented by Arizona State University and JPL in an advanced CMOS digital technology; this technology is optimized for digital application, and previously thought incapable of supporting such analog functionality; the design exploits its dense and power-efficient digital capabilities to implement digital control algorithms. **[22.2]**

Data Converters:

- Unprecedented level of performance in an ADC! NXP describes a hierarchical interleaving of large numbers of Successive-Approximation- Register (SAR) ADCs which enable 10-bit operation at 2.6GS/s, while achieving more than 7 ENOB with less than 0.5W power dissipation. **[10.1]**
- Unprecedented combination of ENOB, bandwidth and power-efficiency in an ADC. Broadcom presents a 12b 800MS/s Nyquist-rate ADC with less than 105mW of power dissipation, by combining a dual-residue topology with simple and fast background offset calibration. **[10.3]**
- Highest DAC sampling rate ever reported! Ciena presents a 56GS/s 6-bit DAC in 65nm standard CMOS. **[10.8]**
- Never before reported bandwidth! NXP and Delft University of Technology present a 125MHz continuous-time delta-sigma modulator in 45nm CMOS which achieves a dynamic range of 70dB. **[27.1]**
- Record low supply voltage operation of a Delta-Sigma modulator! The K.U. Leuven design achieves 61dB of SNDR, using only 7.5uW of power from a 250mV supply while operating at a bandwidth of 10kHz. **[27.4]**

Energy-Efficient Digital:

- A never before seen level of 3D multimedia experience is demonstrated. A chip from National Taiwan University shows a record high resolution of 4096 x 2160 pixels with free view point at a previously unseen frame rate of 216 frames per second. **[7.1]**
- The first 28 nm digital signal processor is presented by Texas Instruments and MIT. Low-voltage operation at 0.6 V is demonstrated. **[7.5]**
- The lowest energy-per-operation for a wireless sensor-node processer is demonstrated by the imec and NXP. The energy efficiency is as low as 10 pJ per clock cycle. **[19.1]**
- Pioneering work is presented for ultra-low-voltage standard cells. The corresponding chip from the University of Freiburg and HSG-IMIT, shows digital-logic gates operating with a supply voltage as low as 62mV. **[19.5]**

High-Performance Digital:

- Highest frequency in microprocessor history! The IBM zEnterprise 196 server chip runs at 5.2GHz in 45nm CMOS with four processing cores and 30MB of cache memory using 1.4 billion transistors. **[4.1]**
- Highest x86 server processor core count! The Intel Bangalore Westmere-EX packs 10 dual-threaded cores on a single die, together with the L3 cache and ring interconnect in a 32nm CMOS process. **[4.3]**
- Highest energy efficiency in a processor! The Godson-3B processor from the Chinese Academy of Sciences is an 8-core design implemented on 65nm CMOS. Its peak performance is 128GFlops for double-precision with 40W power, thereby delivering an astonishing energy efficiency of 3.2GFlops/Watt. **[4.4]**
- Highest transistor count and most complex microprocessor ever developed! The Intel 32nm "Poulson" processor contains 3.1 billion transistors integrated onto a single 544mm^2 silicon die size. Eight processor cores and a total of 54MB of on-chip cache are linked by an on-chip ring-like interconnect bus. **[4.8]**.
- Two contenders for highest level of integration including graphics processing units (GPUs) on a single silicon die with multiple CPU cores. The 32nm Intel "Sandy Bridge" processor integrates four high performance x86 cores, an optimized GPU, dual-channel DDR3 memory controller, and a 20-lane PCIe interface **[15.1]**. The 40nm AMD "Zacate" processor integrates two x86 "Bobcat" cores (each with a 512KB L2 cache) with a dedicated Radeon HD5000 series graphics and multimedia engine, DDR3 memory controller, client northbridge, and a 4X PCIe link **[15.4]**.

Imagers, MEMS, Medical and Displays (IMMD):

- New concepts in energy harvesting for autonomous systems! Several academic and industrial organizations report devices that utilize energy harvesting from photovoltaic, and mechanical (piezoelectric) processes, with one design even integrating the energy harvesting circuitry into the pixel structure itself. **[6.7, 6.8, 6.9]**
- First fully-implantable laser-based fluorescence detector. Stanford University's solution fits within a 1 cm^3 form factor weighing just 0.7g while achieving a 5x improvement in dynamic range, and a 10dB reduction in noise over conventional sample-and-hold-based solutions. **[17.5]**
- First bidirectional microdisplay enables eye-tracking on a head-mounted display. The Fraunhofer Institute for Photonic Microsystems integrates a 320x240 monochrome AMOLED display with a 160x120 image sensor in 0.35µm CMOS. **[17.8]**
- Fastest frame rate ever reported for an image sensor! An academic and industrial consortium around DALSA deliver an image sensor with a capture speed of 16Mframes/s. High light sensitivity is essential given the extremely high capture rate so the sensor incorporates state-of-the-art design techniques to optimize light sensitivity, including Backside Illumination (BSI) and Charge-Carrier Multiplication (CCM) for low-noise readout. **[23.4]**
- World's largest and most light-sensitive monolithic image sensor! Canon's new image sensor contains 1.6Mpixels with a 160µm pitch, and occupies an entire 12" (300mm) CMOS wafer. The huge pixel size, combined with a built-in 0 to 24dB programmable gain, enable an ultra-high light sensitivity of 25Melectrons/lux/sec. **[23.5]**

Memory:

- The smallest die size reported for a 64Gb MLC 2bit/cell NAND device at 151mm^2. Toshiba and Sandisk provide new programming algorithms which improve the Data-Write throughput of the device by 5%. **[11.1]**
- First 32nm HKMG SOI SRAM employing bitline regulation and write-assist techniques. This IBM device enables low voltage operation down to 0.7V. **[14.1]**
- Smallest 28nm SRAM with a 0.12µm^2 bitcell. This design from MIT and TI enables high density embedded SRAM down to 0.6V for System-on-Chip Applications. **[14.4]**

- Highest data rate of 12.8GB/s in mobile wide-I/O DRAM. Using 512 bit I/O, 2-stacked 2Gb mobile I/O with micro-bumps and TSV technology, Samsung achieves 90% I/O-power reduction. **[28.5]**
- Highest density of 2Gb GDDR5 Graphics DRAM achieved using 40nm CMOS. Samsung achieves data rates of 7Gb/s/pin using a channel-crosstalk-equalization scheme. **[28.6]**

Radio Frequency (RF):

- New AD-PLL techniques remove impunity to interference in radio front ends enabling highly programmable radio front ends used in high-density environments. **[3.1, 3.2]**
- Radio receiver architecture has come full circle! Broadcom and UCLA will demonstrate the re-emergence of the old-school super-heterodyne receiver in 65nm with fully-integrated high-Q IF filters, and UCLA will demonstrate that the similarly-aged super-regenerative receiver can be put to good use in a very compact 186GHz low-power imaging application also in 65nm CMOS. **[3.5, 16.10]**
- Revolutionary advancements in fundamental millimeter-wave technology blocks. A variety of industrial and academic researchers deliver innovative techniques that yield revolutionary millimeter-wave building blocks capable of operating at frequencies up to 300GHz. **[16.2, 16.3, 16.5, 16.6, 16.7]**
- New AD-PLL techniques dramatically enhance range and velocity resolutions of FMCW radars. An FMCW synthesizer radar by Toshiba achieves range and velocity resolutions of 10cm and 1.4km/h respectively thanks to a 2x wider bandwidth and 6x longer modulation period than previously reported solutions. **[16.8]**
- First demonstrations of linear PAs in CMOS. Intel and Samsung will deliver CMOS-only linear PA solutions addressing the WLAN and EDGE/GSM markets respectively. **[24.2, 24.4]**
- Demonstration of switched-capacitor techniques being applied to high-power signal processing. The University of Washington will demonstrate a 2GHz power amplifier delivering 25dBm, using purely switched-capacitor techniques for signal modulation. **[24.3]**
- Record-low power levels for a 60GHz PA in 65nm CMOS. UC Berkeley will demonstrate 18.6dBm saturation power using only 0.28mm² of silicon area! **[24.5]**

Technology Directions (TD):

- A transceiver with ultra low energy (0.24nJ/b) and high sensitivity (250μV) for body-communication-channel-based Body Area Network. A design by KAIST has the potential to revolutionize wearable and continuous healthcare monitoring. **[2.1]**
- A 15-patch ultra-lightweight (400mg) low-power wearable sensor network. A design by KAIST, consuming less than 450μW, makes sleep-apnea monitoring and detection a true therapeutic solution! **[2.2]**
- Technology and architectural choices enable critical building blocks for Terahertz (300GHz to 3THz) based imaging. CEA-LETI-MINATEC and Universite Montpellier use a pixel embodying a single CMOS transmitter integrated with a bowtie antenna and low-noise amplifier; University of Wuppertal and IHP will present an 820GHz SiGe based chipset for THz active imaging. **[2.5, 12.5]**
- A low start-up voltage scavenging converter and a stand-alone self-powered electrical outlet energy monitor will accelerate the remote-sensor market. The University of Tokyo and STARC will present a voltage converter requiring only 95mV for start-up, with 72% system efficiency; NEC will present a realtime non-contact power-line-current sensor for home energy management. **[12.1, 12.3]**
- The world's first flexible organic substrate microprocessor! imec, et. al. will present an 8-bit processor running 6 instructions per second which foreshadows the future "Internet of things". **[18.1]**

Wireless:

- First fully-integrated CMOS 60GHz transceivers reported, that address the new Wireless-HD and WiGig standards. Researchers from CEA-LETI-MINATEC and STMicroelectronics will deliver an industrially-packaged Wireless-HD solution capable of 3.8Gb/s operation, using an HTCC substrate, including glass antennas. SiBeam describes a 65nm chipset that supports the maximum Wireless-HD and WiGig data rates, using 32 transmitter and 32 reciever antennas. **[9.2, 9.3]**
- First 3-stream 3x3 MIMO WLAN SoC to improve throughput, range, and link robustness. A chip designed by National Taiwan University integrates three dual band WLAN transceivers and is backward-compatible with legacy IEEE 802.11 a/b/g networks. **[9.6]**
- First-reported single transceiver showing diversity-performance gains of 50-120%. A consortium including ST-Ericsson, Ericsson, and Lund University will deliver the smallest reported WCDMA/EDGE diversity receiver with a DigiRF interface. **[21.2]**
- Highest level of integration reported for a cellular chipset. Qualcomm will deliver a fully-integrated solution containing an embedded EDGE/UMTS RF section, digital baseband processor, memories, and audio processor, all on a single SoC. In addition, a novel DPLL architecture ensures very-low peak transmitter-battery current for GSM low-band operation. **[21.3]**
- First-reported all-digital multi-mode transmitter meeting the stringent 3GPP RX-band noise requirements. A collaboration between Infineon Technologies and DICE will deliver a low-power polar architecture with lowest-reported power consumption. **[21.7]**
- New RFID sensor with the widest frequency range ever reported. Collaboration between Graz University and Infineon yields an ultra-low-power sensor node, employing innovative design techniques to support a frequency range of 13MHz to 2.45GHz, while minimizing power dissipation by an additional 70% over the current state-of-the-art. **[26.1]**
- First self-correlation-based RFID reader is demonstrated. Researches from KAIST and PHYCHIPS will demonstrate an RFID reader which isolates small back-scattered sensor signals from self-leakage in the transmitter, eliminating the need for large off-chip isolators. **[26.2]**

Wireline:

- The best equalization capability ever demonstrated by a receiver! Researchers from Fujitsu Laboratories will describe the first reported receiver that is able to accurately reconstruct an incoming signal while receiving less than 1% of the transmitted data energy! **[20.1]**
- New low-cost plastic materials are being developed to carry data signals. A co-operative venture between Sony and Caltech combines a new technology, plastic channel waveguides, and full-duplex transceiver technology to create a low-cost 25Gb/s interconnect. **[8.5]**
- The world's first CMOS 100Gb/s Ethernet gearbox has been developed! Engineers from Hitachi will present a 10:4 CMOS MUX/DEMUX gearbox for 100Gb/s Ethernet operation. **[8.4]**
- A new record for the "greenest" interface for display panels has been set! Researchers from Seoul National University will present a new video interface in 130nm CMOS that has both lower power and smaller area than the existing state-of-the-art. **[25.8]**
- The most sophisticated CMOS transceivers ever demonstrated. Engineers from LSI and Texas Instruments, along with Arda Technologies, have independently developed the first generation of transceivers with 10 or more taps of DFE correction and an operating rate of over 14Gb/s. **[20.2, 20.3]**

EDUCATIONAL EVENTS

TUTORIALS

T1: Integrated LC Oscillators
Pietro Andreani (Lund University)

T2: Embedded Memories for SoC
Harold Pilo (IBM)

T3: Ultra-Low Power and Low Voltage in Digital Design
Jos Huisken (imec)

T4: Layout — The Other Half of Nanometer Analog Design
Jed Hurwitz (Gigle Networks)

T5: DPLL-Based Clock and Data Recovery
John T. Stonick (Synopsys)

T6: Practical Power-Delay Design Trade-Offs
Tim Fischer (AMD)

T7: Distortion in Cellular Receivers
Sven Mattisson (Ericsson)

T8: Noise Analysis in Switched-Capacitor Circuits
Boris Murmann (Stanford University)

T9: Interfacing Silicon with the Human Body
Tim Denison (Medtronic)

SHORT COURSE

SC1: Cellular and Wireless LAN Transceivers: From Systems to Circuit Design
Hooman Darabi (Broadcom), Frank Op't Eynde (Audax Technologies),
Behzad Razavi (University of California Los Angeles), Bogdan Staszewski (TU Delft)

FORUMS

F1: Advanced Transmitters for Wireless Infrastructure

Earl McCune (RF Communications Consulting), Renato Negra (RWTH Aachen University), Klaas Bult (Broadcom Netherlands BV), Ian Galton (University of California San Diego), Olivier Charlon (Scintera Networks Inc.), Martin Clara (Lantiq A GmbH), Bumman Kim (Pohang University of Science and Technology)

F2: Ultra-Low Voltage VLSIs for Energy-Efficient Systems

Ticky Thakkar (Intel), Philip K.T. Mok (Hong Kong University of Science and Technology), Frederic Boeuf (ST Microelectronics), Takayasu Sakurai (University of Tokyo), Kaushik Roy (Purdue University), Guido De Sandre (ST Microelectronics), Baher Haroun (Texas Instruments), Peter Kinget (Columbia University), Akira Matsuzawa (Tokyo Institute of Technology)

F3: Towards Personalized Medicine and Monitoring for Healthy Living

Carlotta Guiducci (EPFL), Ken Shepard (Columbia University), Yogesh Gianchandani (University of Michigan), Jerald Yoo (Masdar Institute of Science and Technology), Shey-shi Lu (National Taiwan University) Wentai Liu (University of California Santa Cruz), Stefan Launer (Phonak/Sonova), Rahul Sarpeshkar (MIT), Chris Toumazou (Imperial College)

F4: Design of "Green" High-Performance Processor Circuits

Matthias Knoth (MIPS), William Dally (NVIDIA), Anthony Hill (Texas Instruments), David Flynn (ARM), Masafumi Takahashi (Toshiba Corporation), Ronald Preston (Intel Corporation), David Blaauw (University of Michigan), Sung Bae Park (Samsung Electronics)

F5: Image Sensors for 3D Capture

Ian Underwood (University of Edinburgh), Peter Seitz (CSEM), Pierre Magnan (ISAE), Cyrus Bamji (Canesta), Bernhard Buettgen (MESA Imaging), Edoardo Charbon (TU Delft), Shingo Mandai (University of Tokyo), Ralph Etienne-Cummings (Johns Hopkins University), Keith Fife (Ubixum)

F6: High-Speed Transceivers: Standards, Challenges, and Future

Jared Zerbe (Rambus), Thomas Toifl (IBM Research GmbH), Marcus van Ierssel (Snowbush IP), Takeshi Horie (Fujitsu Laboratories), Daniel Weinlader (Synopsys), Fulvio Spagna (Intel), Anthony Fraser Sanders (Lantiq Deutschland)

EVENING SESSIONS

SPECIAL TOPICS

ES0: Student Research Preview

Organizers: Jan Van der Spiegel (University of Pennsylvania), SeongHwan Cho (KAIST)

ES1: Data-Converter Breakthroughs in Retrospect

Hae-Seung Lee (MIT), Stephen Lewis (UC Davis), Doug Mercer (Analog Devices), Bruce Wooley (Stanford University)

ES2: Wireless Sensor Systems: Solutions & Technology

Masayoshi Esashi (Tohoku University), Kris Pister (Dust Networks), Raphaël Salot (CEA-LITEN), Dennis Sylvester (University Of Michigan), Ruud Vullers (IMEC)

ES3: Future System and Memory Architectures: Transformations by Technology and Applications

Jim Kahle (IBM), Stephen Pawlowski (Intel), Tomofumi Shimada (Toshiba), Raj Talluri (Qualcomm)

ES4: Body Area Networks (BAN): Technology, Solutions, and Standardization

Arthur Astrin (Astrin Radio), David Davenport (GE Global Research), Okundu Omeni (Toumaz UK), Huang-Bang Li (NICT), Anuj Batra (Texas Instruments), Seong-Jun Song (Samsung)

ES5: Gb/s+ Portable Wireless Communications

Jeff Gilbert (SiBEAM), Jri Lee (National Taiwan University), Ali S. Sadri (Intel), Rolf De Vegt (Qualcomm)

ES6: Technologies for Smart Grid and Smart Meter

Keith Findlater (Gigle Networks), Sang-Gug Lee (KAIST), Martin Manniche (GreenWave Reality), Mick Mueck (Analog Devices)

PANELS

EP1: Good, Bad, Ugly - 20 Years of Broadband Evolution: What's Next?

David Borison (Ralink), Larry DeVito (Analog Devices), Sven Mattisson (Ericsson), Stephen Palm (Broadcom), Michiel Steyaert (KU Leuven), Eric Yeh (MediaTek)

EP2: 20/22nm Technology Options and Design Implications

Mark Bohr (Intel), Min Cao (TSMC), Koichiro Ishibashi (Renesas), Bill Liu (GlobalFoundries), Ghavam Shahidi (IBM)

SUBCOMMITTEE CONTRIBUTIONS

SUBCOMMITTEE	SESSIONS	EVENING SESSIONS	EVENING PANELS	TUTORIALS	FORUMS	SHORT COURSES	PRESS COPY PAGE #'S
ANALOG	5, 13, 22	ES6		T1	F3, F6		141, 153, 164
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ENERGY-EFFICIENT DIGITAL	7,19	ES2		T5	F4		143, 144, 161
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RF	3, 16, 24		EP1	T7	F1, F3	SC1	157, 165
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ANALOG
SUBCOMMITTEE

ISSCC 2011 – ANALOG

Subcommittee Chair: *Bill Redman-White, NXP/Southhampton University, UK*
Press Designate: *Ian Galton, University of California San Diego, San Diego, CA*

OVERVIEW

CONTEXT AND PRESENT STATE OF THE ART

- Despite the trend toward digital, analog circuits are not only still required in modern communication and computing systems, but their required performance is higher than ever.
- Digital circuits such as microprocessors drive the market, so the evolution of integrated circuit (IC) technology (as described by Moore's Law), has sacrificed traditional analog circuit performance in favor of digital circuitry.
- At each new IC technology node, analog-circuit designers are faced with increasingly challenging specifications, and traditional circuit-design techniques are increasingly ineffective. One of the few options open to analog-circuit designers to solve this problem is to incorporate digital signal processing techniques to overcome analog-circuit limitations.

MOST-SIGNIFICANT PAPERS

- A digital PLL incorporates a new technique to avoid an error source that has plagued prior digital PLLs. Politecnico di Milano use a 10-bit controllable delay element to cancel delta-sigma quantization noise. This, in turn, makes it possible to use a bang-bang phase detector in place of a noisy time-to-digital converter. **[5.1]**
- A digital PLL incorporates a new technique to remove the effects of power-supply noise that have plagued prior PLLs when integrated in system-on-chip ICs. Toshiba uses a digital calibration signal to facilitate cancellation of the deleterious effects of power-supply disturbances. **[5.6]**
- Highly efficient LED lamps can now be driven directly from the wall! A new BiCMOS chip designed by Fairchild Semiconductor connects to 110 and 220 VAC, and delivers a power factor of 0.98 and 0.92, respectively into a 5W LED. **[13.1]**
- Extraordinary DC performance is now combined with very low noise in a chopper operational amplifier. Analog Devices has established a new world record of 5.9nV/√Hz achieved with a maximum of only 0.78μV of input offset. **[13.4]**
- Advanced microprocessors can now contain their own power regulators: an extremely efficient DC-DC converter has been implemented by Arizona State University and JPL in an advanced CMOS digital technology; this technology is optimized for digital application, and previously thought incapable of supporting such analog functionality; the design exploits its dense and power-efficient digital capabilities to implement digital control algorithms. **[22.2]**

APPLICATIONS AND ECONOMIC IMPACT

- PLLs get quiet, even in a noisy environment, enabling higher-levels of integration and cost reduction. **[5.1, 5.6]**
- Sensing the impossible! High performance amplifiers designed for sensor applications make it possible to resolve smaller signals than ever thought possible, thereby enabling new sensor applications. **[13.4, 13.6, 13.8]**
- Power conversion goes digital – advanced DSP techniques make complex embedded power-management systems feasible with low external-component count, even in nanometer technologies, enabling higher system integration and reduced system costs. **[13.1, 22.2, 22.3, 22.4]**

SURVIVAL OF ANALOG TECHNIQUES!

With the increasing excitement over the digital world, people often forget that the real world is actually analog. Even though most of our technologies process information via computers and digital circuitry, the signals themselves originate and end up in analog form, such as sound and radio waves. Furthermore, all electronic circuits, whether analog or digital, must be supplied with power, and the power supply circuits are inherently analog. Nevertheless, digital circuits such as microprocessors, drive the market; so, integrated circuit (IC) technology (used in the factories that make integrated circuits) have been optimized relentlessly over the last 40 years to reduce the size, cost, and power consumption of digital circuits. This trend has made analog circuitry increasingly difficult to implement, yet the number of essential analog interface circuits and their performance requirements have increased.

Interestingly, analog designers have turned the curse of this trend away from "analog-friendly" IC technology into a cure. Rather than struggle to overcome the problem with traditional, time-tested analog circuit tricks, they have turned toward the utilization of digital signal-processing circuits, embedded within the analog-circuit blocks, to overcome analog-circuit limitations. This new approach blurs the distinction between analog and digital circuit design, but yields continued advances in the analog state-of-the-art. Increasingly, these techniques have enabled performance that matches, and now even exceeds, what was possible in traditional high-performance analog IC technology.

DATA CONVERTERS
SUBCOMMITTEE

ISSCC 2011 – DATA CONVERTERS

Subcommittee Chair: *Venu Gopinathan, Texas Instruments, Bangalore, India*
Press Designate: *Klaas Bult, Broadcom, Bunnik, The Netherlands*

OVERVIEW

CONTEXT AND PRESENT STATE OF THE ART

- Digital Calibration to enhance data-converter performance is becoming common-place. **[10.1, 10.2, 10.3, 10.5, 10.7, 27.2]**
- Current state-of-the-art in CMOS DACs is 12GS/s. **[10.8]**
- The highest bandwidth in CMOS Delta-Sigma converters is several tens of MHz. **[27.1]**

MOST-SIGNIFICANT PAPERS

- Unprecedented level of performance in an ADC! NXP describes a hierarchical interleaving of large numbers of Successive-Approximation- Register (SAR) ADCs which enable 10-bit operation at 2.6GS/s, while achieving more than 7 ENOB with less than 0.5W power dissipation. **[10.1]**
- Unprecedented combination of ENOB, bandwidth and power-efficiency in an ADC. Broadcom presents a 12b 800MS/s Nyquist-rate ADC with less than 105mW of power dissipation, by combining a dual-residue topology with simple and fast background offset calibration. **[10.3]**
- Highest DAC sampling rate ever reported! Ciena presents a 56GS/s 6-bit DAC in 65nm standard CMOS. **[10.8]**
- Never before reported bandwidth! NXP and Delft University of Technology present a 125MHz continuous-time delta-sigma modulator in 45nm CMOS which achieves a dynamic range of 70dB. **[27.1]**
- Now, digital correction technique improves the DAC performance of a high-speed Delta-Sigma ADC. This technique by Ulm University delivers 63dB SNDR at 10MHz bandwidth, and boosts the SFDR to an unprecedented 81dB. **[27.2]**
- Record low supply voltage operation of a Delta-Sigma modulator! The K.U. Leuven design achieves 61dB of SNDR, using only 7.5uW of power from a 250mV supply while operating at a bandwidth of 10kHz. **[27.4]**

APPLICATIONS AND ECONOMIC IMPACT

- A 2.6GS/s highly interleaved SAR ADC enables digitizing the entire TV-band which allows integration of multiple receivers on a single die, reducing system cost. **[10.1]**
- High-speed, low-power ADCs provide the technological building blocks which will enable 10G-ethernet applications for high-speed LAN, creating new and exciting opportunities for businesses and consumers alike. A side benefit of the

introduction of 10G solutions will be the continued commoditization of 1G solutions which will make existing high-speed LAN technologies even more economical. **[10.3]**

- A 56GS/s 65nm CMOS DAC allows integration with existing100Gb/s optical-link designs, reducing system cost. **[10.8]**
- Continued improvements in Delta-Sigma converter design propagates to the numerous applications in which they are used today such as GSM base stations and HD video systems. Ultimately this delivers higher quality solutions at better price points, resulting in improved feature sets and reduced costs for today's consumers. **[27.1, 27.2]**
- Driving Delta-Sigma data converter power consumption levels down into the µ-power range opens up exciting new application spaces where energy harvesting can be used to create truly autonomous systems such as portable or implantable medical sensors and diagnostic tools! **[27.4]**

ENERGY-EFFICIENT DIGITAL

Subcommittee

ISSCC 2011 – ENERGY-EFFICIENT DIGITAL

Subcommittee Chair: *Tzi-Dar Chiueh, National Taiwan University, Taipei, Taiwan*
Press Designate: *Alice Wang, Texas Instruments, Dallas, TX*

OVERVIEW

CONTEXT AND PRESENT STATE OF THE ART

- Existing TV sets and set-top boxes have limited 3D capability and require shuttered glasses to look at interleaved frames **[7.1, 7.3]**
- Industry is still pursuing technology scaling to provide ultra-low-power devices. **[7.5]**
- Current mobile devices (such as, smart phones) have internet connectivity, but are still in need of more multimedia functionality with minimal power dissipation **[7.6, 7.7, 7.8, 19.6]**
- Deployment of wireless sensor networks is limited by the energy efficiency of the internal processors. The inability to operate at sub-threshold supply voltages prevents exploitation of the huge potential of wireless sensor networks in biomedical and other monitoring applications. **[19.1, 19.2, 19.5]**

MOST-SIGNIFICANT PAPERS

- A never before seen level of 3D multimedia experience is demonstrated. A chip from National Taiwan University shows a record high resolution of 4096x2160 pixels with free view point at a previously unseen frame rate of 216 frames per second. **[7.1]**
- The first 28nm digital signal processor is presented by Texas Instruments and MIT. Low-voltage operation at 0.6V is demonstrated. **[7.5]**
- The lowest energy-per-operation for a wireless sensor-node processer is demonstrated by the imec and NXP. The energy efficiency is as low as 10pJ per clock cycle. **[19.1]**
- Pioneering work is presented for ultra-low-voltage standard cells. The corresponding chip from the University of Freiburg and HSG-IMIT, shows digital-logic gates operating with a supply voltage as low as 62mV. **[19.5]**
- An unprecedented combination of increased energy efficiency and high performance for Fourier-transform block is demonstrated. The University of Michigan and Arizona State University will present a chip that consumes only 17.7nJ per transform with a record performance of 30MHz at a 0.27V supply voltage **[19.6]**

APPLICATIONS AND ECONOMIC IMPACT

- The electronic entertainment market is a financial juggernaut. An immersive unencumbered 3D experience will further boost this market to unprecedented heights and help make 3D television a standard in every household. **[7.1, 7.3]**
- Enhanced multimedia functions and high-data-rate connectivity make it possible to watch movies or television on every smart phone. This will further enhance the economic potential of the mobile market. **[7.2, 7.3, 7.4]**
- Ultra-high-efficiency electronic systems are essential to support applications that enhance human comfort and health. This is especially important for society's aging population. **[19.2, 19.2, 19.5, 19.6]**

HIGH-PERFORMANCE DIGITAL

Subcommittee

ISSCC 2011 – HIGH-PERFORMANCE DIGITAL

Subcommittee Chair: *Stefan Rusu, Intel, Santa Clara, CA*
Press Designate: *Sonia Leon, Intel, Santa Clara, CA*

OVERVIEW

CONTEXT AND PRESENT STATE OF THE ART

- This year's ISSCC processor lineup contains several record breaking processors enabled by engineering innovations in state-of-the-art 32nm manufacturing processes. Both general purpose and specialized SoC processors for graphics and multimedia are being integrated on a single silicon die to reduce system power and cost.
- Enterprise processors **[Session 4]** feature the fastest clock frequencies, the highest x86 core counts, the highest energy efficiencies, and the highest transistor counts ever achieved in commercial microprocessors.
- Integration rules! High performance SoC processors **[Session 15]** are integrating other chips and components from the system onto the processor die. This not only enables better use of the available silicon area, it also improves communication, reduces system complexity and cost, and lowers overall system power.

MOST-SIGNIFICANT PAPERS

- Highest frequency in microprocessor history! The IBM zEnterprise 196 server chip runs at 5.2GHz in 45nm CMOS with four processing cores and 30MB of cache memory using 1.4 billion transistors. **[4.1]**
- Highest x86 server processor core count! The Intel Bangalore Westmere-EX packs 10 dual-threaded cores on a single die, together with the L3 cache and ring interconnect in a 32nm CMOS process. **[4.3]**
- Highest energy efficiency in a processor! The Godson-3B processor from the Chinese Academy of Sciences is an 8-core design implemented on 65nm CMOS. Its peak performance is 128GFlops for double-precision with 40W power, thereby delivering an astonishing energy efficiency of 3.2GFlops/Watt. **[4.4]**
- Highest transistor count and most complex microprocessor ever developed! The Intel 32nm "Poulson" processor contains 3.1 billion transistors integrated onto a single 544mm^2 silicon die size. Eight processor cores and a total of 54MB of on-chip cache are linked by an on-chip ring-like interconnect bus. **[4.8]**.
- Two contenders for highest level of integration including graphics processing units (GPUs) on a single silicon die with multiple CPU cores. The 32nm Intel "Sandy Bridge" processor integrates four high performance x86 cores, an optimized GPU, dual-channel DDR3 memory controller, and a 20-lane PCIe interface **[15.1]**. The 40nm AMD "Zacate" processor integrates two x86 "Bobcat" cores (each with a 512KB L2 cache) with a dedicated Radeon HD5000 series graphics and multimedia engine, DDR3 memory controller, client northbridge, and a 4X PCIe link **[15.4]**.

APPLICATIONS AND ECONOMIC IMPACT

- The drive to integrate dozens of cores and billions of transistors on a single die is required to feed today's insatiable demand for computation. The exploding core counts and heterogeneous integration enabled by billion plus transistor designs has required fast-paced architectural and circuit innovations in on-chip networks since integrated components need to transfer data at a pace that matches their computational ability. These innovations are enabling significant advances in energy-efficiency and application throughput on systems with a large number of cores. **[4.1, 4.3]**
- Innovative enterprise processors and design components achieve new heights of performance, integration, and energy efficiency. By continuing to deliver exponentially increasing performance and capability, these efficient engines will enable computers to analyze the world's most challenging scientific problems, and manage the corresponding increasing demands of the ever-expanding global IT infrastructure. **[Session 4]**
- Processors are integrating other chips and components from the system onto the processor die**.** This trend not only enables better use of the available silicon area, it also improves communication, reduces system complexity, and lowers overall system power. More importantly, the higher levels of integration also enable lower overall system cost. This means one overwhelming thing for the consumer: more bang for the buck! **[Session 15]**

TRENDS IN PROCESSORS PRESENTED AT ISSCC

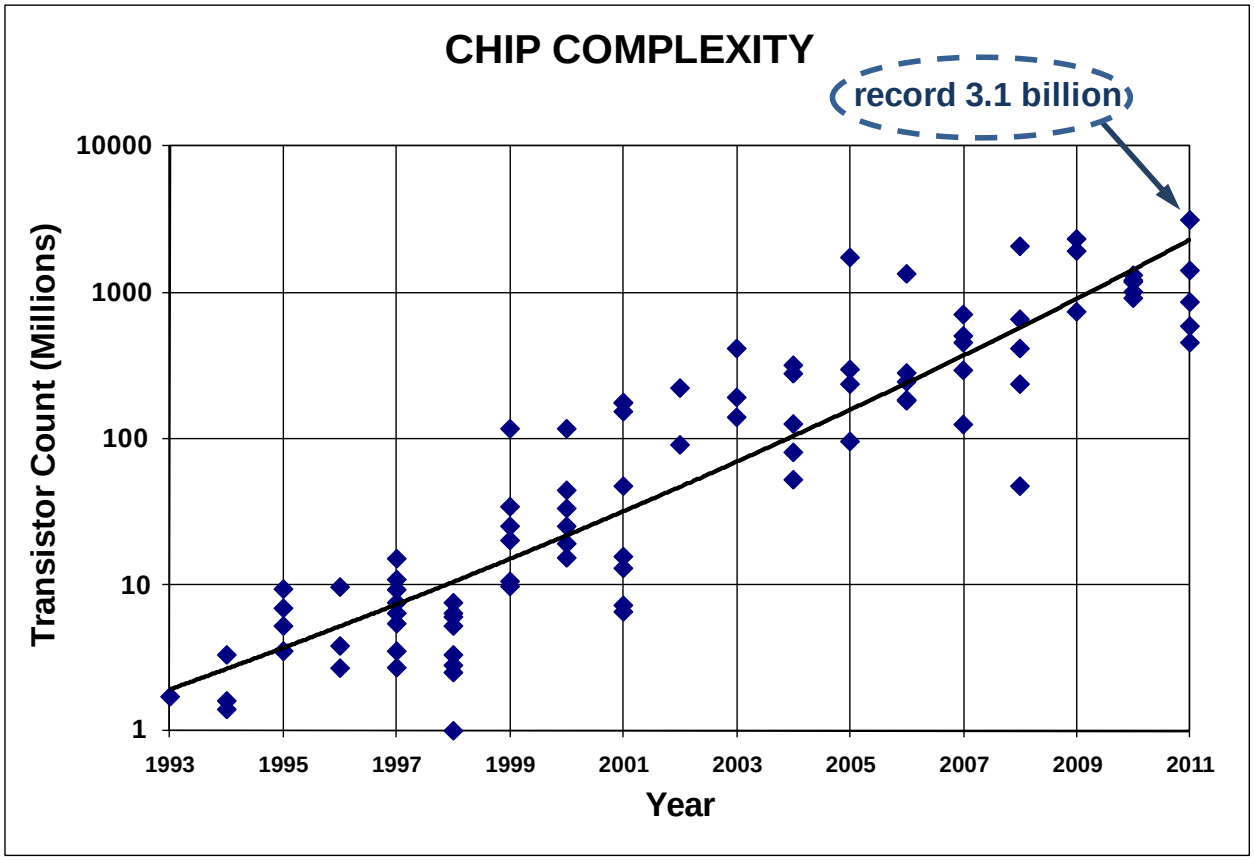
While process technology continues its onward advancement, enabling integration on massive scales, this year's processors come from wide technological backgrounds. New ground is broken in key areas of transistor integration, performance per unit power, and functional integration. This is accomplished across a wide range of process technologies – 65nm, 45nm, 40nm, and 32nm bulk and SOI CMOS technologies.

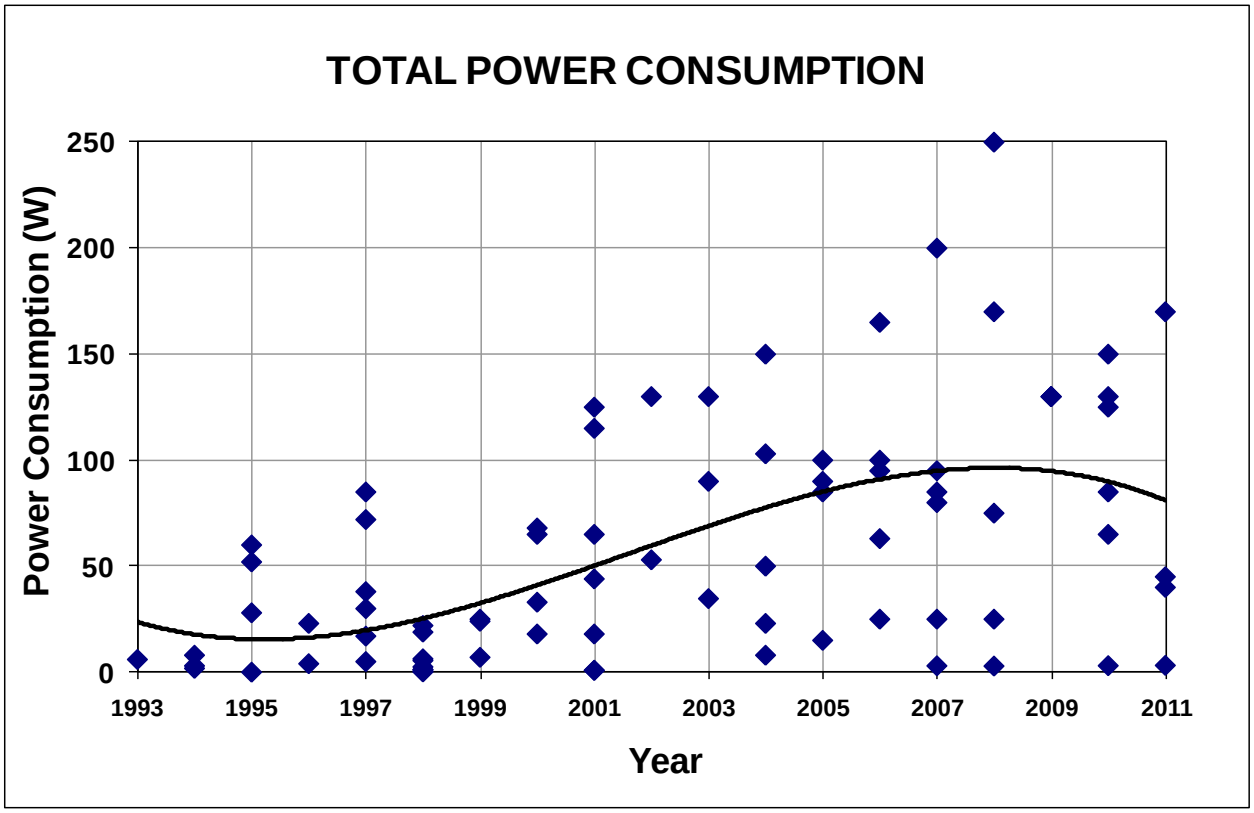
The chip-complexity chart below shows the trend in integrating transistors on a single chip over the past two decades. While the 1 billion limit was passed some 5 years ago, this year marks the first commercial product exceeding 3 billion transistors on a single die with the 32nm Intel Itanium Processor. The massive integration continues to drive the inclusion of large caches on-die as we see with 30MB on IBM's zEnterprise, and 54MB on the 32nm Intel Itanium.

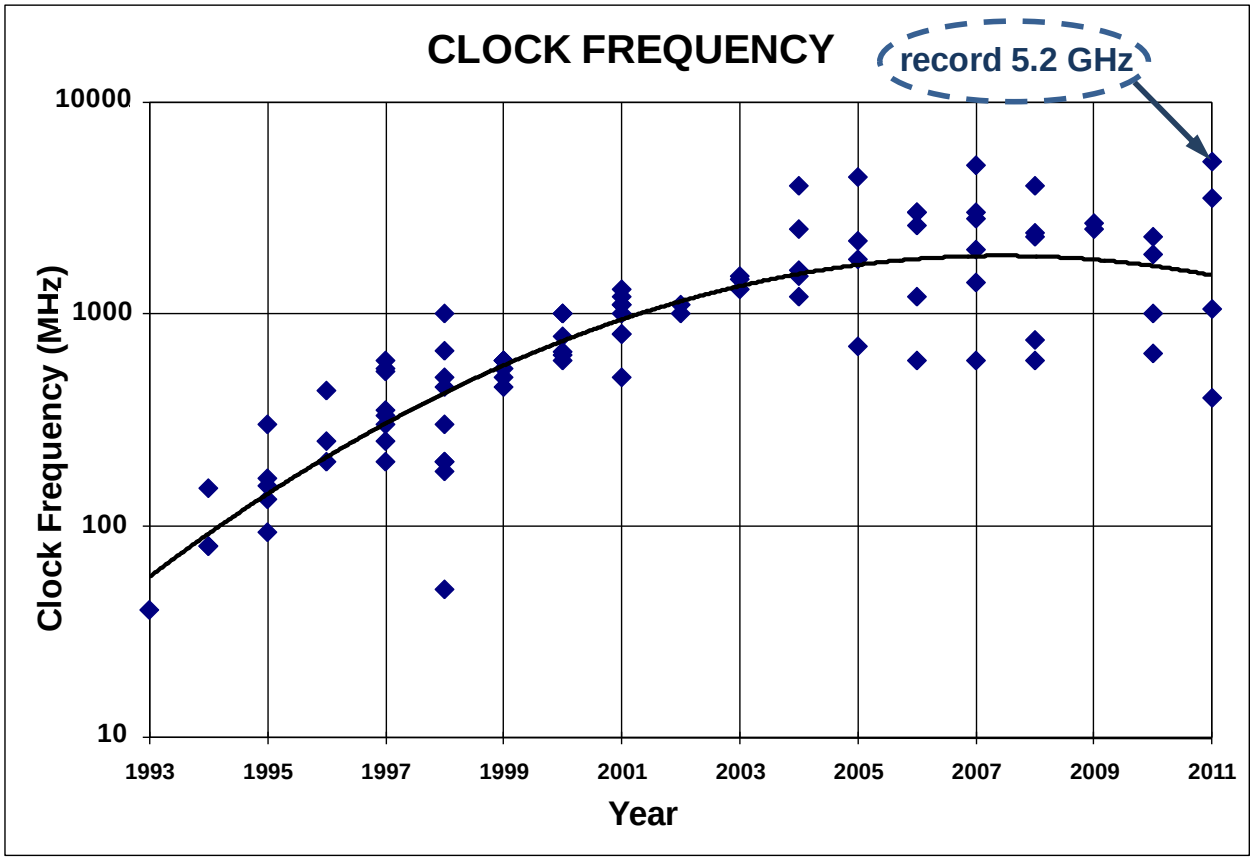
Aggressive processor power management and system-wide power optimization has become a requirement as technology has enabled the increasing trend of system integration onto the processor die. The trend of flat-to-down power in these systems continues as engineers leverage low-power design features to squeeze performance within existing power budgets. For example, the IBM zEnterprise system achieves a 20% frequency boost to a mind-numbing 5.2GHz with no power envelope increase over prior generation devices. The Godson-3B processor's focus on power enables that device to consume only 40W. The increased focus on power is helping rein in the immense demands, which PCs, servers, data centers, and similar systems put on power grids. The result will be lower cost, less cooling demands, and a greener product.

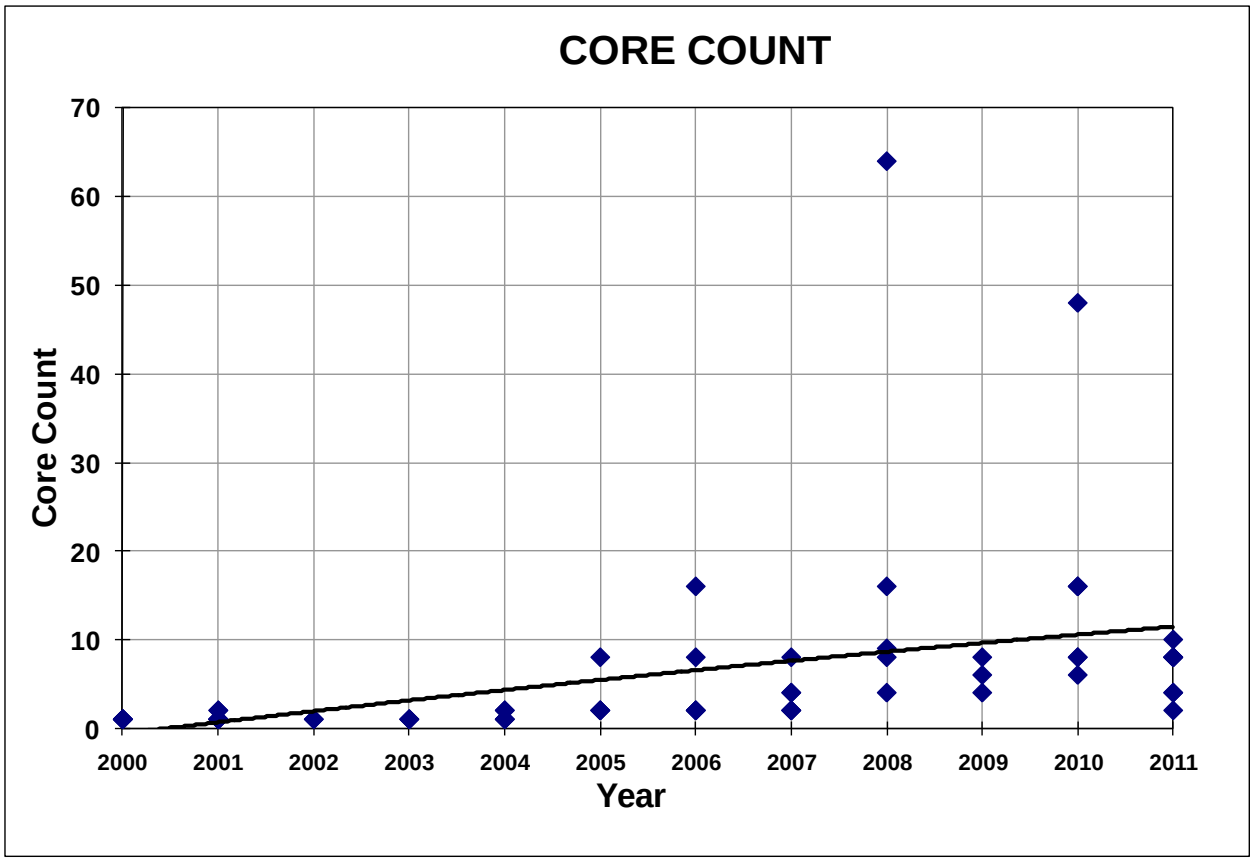
As a consequence of lower-power design requirements, system architects have been forced to innovate using multiple processor cores typically running parallel threads at lower frequencies. This enables processors to turn off when not actively doing computations. While ISSCC 2011 does not break ground in maximum core count, the body of work continues to emphasize this growing trend – IBM's zEnterprise is a 4-core machine, the Intel Westmere-EX delivers a 10-core solution, China's Godson-3B features 8 cores, and AMD's Bulldozer also delivers an 8-core CPU. This flexibility and scalability will enable adaptable system power profiles, further reducing power consumption and improving the end-user experience, as our multi-tasking lifestyle evolves.

These trends in integration, power consumption, and parallel computation, bring new challenges to processor development: New techniques are required to ensure robustness to power supply fluctuations; and improvements in power/clock delivery networks are required as multiple voltage domains become de facto on these chips. ISSCC 2011 will highlight many of these new building-block technologies.









IMAGERS, MEMS, MEDICAL & DISPLAYS

SUBCOMMITTEE

ISSCC 2011 – IMAGERS, MEMS, MEDICAL, AND DISPLAY

Subcommittee Chair: *Roland Thewes, TU Berlin, Germany*
Press Designate: *Christoph Hagleitner, IBM Research, Switzerland*

OVERVIEW

CONTEXT AND PRESENT STATE OF THE ART

- Micro-machined accelerometers and gyroscopes are commonly found in today's smart phones. **[6.1]**
- Optical molecular imaging is emerging as a powerful preclinical research tool for investigating and quantifying molecular events in living subjects. **[17.5]**
- Energy-harvesting research continues to draw great interest but remains an idea in need of more proof-of-concept implementations. **[17.8]**
- Current image sensors can capture millions of frames per second. **[23.4]**
- Large-area image sensors are required for applications which require high light-sensitivity (e.g., night-recording). **[23.5]**

MOST-SIGNIFICANT PAPERS

- New concepts in energy harvesting for autonomous systems! Several academic and industrial organizations report devices that utilize energy harvesting from photovoltaic, and mechanical (piezoelectric) processes, with one design even integrating the energy harvesting circuitry into the pixel structure itself. **[6.7, 6.8, 6.9]**
- First fully-implantable laser-based fluorescence detector. Stanford University's solution fits within a 1 cm^3 form factor weighing just 0.7g while achieving a 5x improvement in dynamic range, and a 10dB reduction in noise over conventional sample-and-hold-based solutions. **[17.5]**
- First bidirectional microdisplay enables eye-tracking on a head-mounted display. The Fraunhofer Institute for Photonic Microsystems integrates a 320x240 monochrome AMOLED display with a 160x120 image sensor in 0.35µm CMOS. **[17.8]**
- Fastest frame rate ever reported for an image sensor! An academic and industrial consortium around DALSA deliver an image sensor with a capture speed of 16Mframes/s. High light sensitivity is essential given the extremely high capture rate so the sensor incorporates state-of-the-art design techniques to optimize light sensitivity, including Backside Illumination (BSI) and Charge-Carrier Multiplication (CCM) for low-noise readout. **[23.4]**
- World's largest and most light-sensitive monolithic image sensor! Canon's new image sensor contains 1.6Mpixels with a 160µm pitch, and occupies an entire 12" (300mm) CMOS wafer. The huge pixel size, combined with a built-in 0 to 24dB programmable gain, enable an ultra-high light sensitivity of 25Melectrons/lux/sec. **[23.5]**

APPLICATIONS AND ECONOMIC IMPACT

- Energy harvesting circuits achieve power and efficiency levels which enable truly autonomous sensor systems that will allow the development of myriad new applications. **[6.7, 6.8, 6.9]**
- Fully-implantable optical molecular imaging devices enable new applications including early disease detection, therapeutic monitoring, and biological understanding. **[17.5]**
- The first bidirectional microdisplay paves the way for new smart-phone applications, and smaller handset designs due to the high level of integration achieved using a single device. **[17.8]**
- Image sensors with capture rates in the millions of frame-per-second range will enable new scientific breakthroughs for high-speed-imaging applications. **[23.4]**
- Large-area image sensors create new capture possibilities such as video recording of stars in the night sky, nocturnal animal behavior, and other low-light-level conditions. **[23.5]**

TRENDS IN IMAGING

- CMOS Imagers are coming to the compact Digital Still Camera (DSC) markets!
- High Dynamic Range (HDR) is (finally!) introduced in low-cost consumer imaging.
- The pixel race is alive and well as pixel sizes continue to shrink. Pixel resolution over 10M are commercially available employing enhanced small-size pixels.
- Backside illumination is becoming an indispensable technology for gaining the competitive edge in CMOS imagers, enabling increased market share.
- High-speed low-power low-noise column-parallel ADCs are becoming a key technology for high-definition video imagers.
- Rapid increases in integrated logic functionality are driving a dramatic increase in imager functions and features.
- 3D imagers are becoming a very hot R&D topic given the current push toward 3D entertainment.
- Increasing R&D investment is predicted in forthcoming years for automotive imaging, and for 3-D range-finding and time-of-flight (TOF) applications.

TRENDS IN DISPLAYS

- Chip-on-Glass (CoG) interfaces are becoming a common choice for high-speed interfaces in notebook applications. In addition, touch and 3D functionality are making their way into notebook PC's and LCD monitors.
- Small-sized display-driver ICs are seeing increased levels of integration, with the following features becoming commonplace: user-adjustable image enhancements, touch-sensor readouts and handlings, 3D-driving control signals, and temperature-sensor integration to minimize power consumption.
- Backlight strategies are seeing an increased level of effort and interest.
- Lots of attention is given to making displays "greener" (that is, more power-efficient, as well as using more environmentally-friendly manufacturing processes).

TRENDS IN MEDICAL

- Huge R&D activities in the field of bio-potential sensors capable of measuring neural activity.
- Neural techniques continue to propagate into more therapeutic applications. Clinical trials are ongoing for early diagnosis of depression.
- Chemical sensing is gaining ground in a neurological clinical setting. A pilot study has been completed on monitoring acute activity in the brain.
- Longer-term monitoring is facing similar challenges to glucose sensing in Diabetes. The need for chronic chemical sensors is critical. The ultimate goal is the development of solutions corresponding to an artificial pancreas.
- Cardiac therapies are focusing on ultra-miniaturization of existing devices. The goal is to eventually eliminate the leads, thereby simplifying cardiac surgery, which is currently a very invasive procedure. In addition, there is a push for instrumenting stents with miniaturized technology to add diagnostic capability to these widely-used devices.

TRENDS IN SENSORS AND MEMS

- Silicon MEMS resonators and oscillators are replacing quartz-based solutions. The market uptake for MEMS is growing exponentially.
- Single-packaged multiple-axis accelerometers and gyroscopes have been announced by several companies, including STmicroelectronics, Bosch, and Invensense. These devices are now widely used in game controllers and smartphones.
- 3-axis accelerometers and 3-axis magnetic field sensors are now becoming available.

MEMORY
SUBCOMMITTEE

ISSCC 2011 – MEMORY

Subcommittee Chair: *Kevin Zhang, Intel, Hillsboro, OR*
Press Designate: *Cormac O'Connell, TSMC, Ottawa, Canada*

OVERVIEW

CONTEXT AND PRESENT STATE OF THE ART

- The economics of Solid-State Discs (SSD) are driven by the price per bit of NAND-Flash versus that on a magnetic disc. Die size and process complexity directly contribute to SSD costs. Therefore smaller die contribute to lower price per bit, making SSD denser and cheaper. **[11.1, 11.3, 11.8]**
- Traditional non-volatile memories are facing ever increasing scaling challenges. New emerging memory technologies are being pursued to provide viable alternatives for future high-density and low-power applications. **[11.2, 11.6, 11.7]**
- SRAM continues to be the memory workhorse for embedded applications. SRAM bitcell scaling is experiencing increasing difficulty achieving those densities predicted by Moore's law. More advanced silicon technologies such as Hi-κ/Metal-Gate (HKMG), along with advanced circuit techniques are required for 32nm and beyond. **[14.1, 14.4]**
- Graphics applications continue to drive the need for high-memory-bandwidths. With each generation, it becomes ever more important to achieve high-data-rate memory interfaces. **[28.6]**
- In mobile applications, low-power memory is essential to meet increasing performance while maintaining low power consumption. Through-Silicon Via (TSV) technology is emerging to provide optimum power/bandwidth solutions. **[28.5]**

MOST-SIGNIFICANT PAPERS

- The smallest die size reported for a 64Gb MLC 2bit/cell NAND device at 151mm^2. Toshiba and Sandisk provide new programming algorithms which improve the Data-Write throughput of the device by 5%. **[11.1]**
- A very-high-speed 4Mb embedded SLC Resistive RAM with a 7.2ns Read-Write Random Access time and 160ns of MLC capability. High performance is achieved using a parallel-series reference cell scheme and a process and temperature aware dynamic bitline bias circuit. **[11.2]**
- First 32nm HKMG SOI SRAM employing bitline regulation and write-assist techniques. This IBM device enables low voltage operation down to 0.7V. **[14.1]**
- Smallest 28nm SRAM with a 0.12μm^2 bitcell. This design from MIT and TI enables high density embedded SRAM down to 0.6V for System-on-Chip Applications. **[14.4]**
- Highest data rate of 12.8GB/s in mobile wide-I/O DRAM. Samsung achieves 90% I/O-power reduction using 512 bit I/O, 2-stacked 2Gb mobile I/O with micro-bumps, and TSV technology. **[28.5]**
- Highest density of 2Gb GDDR5 Graphics DRAM achieved using 40nm CMOS. Samsung achieves data rates of 7Gb/s/pin using a channel-crosstalk-equalization scheme. **[28.6]**

APPLICATIONS AND ECONOMIC IMPACT

- The small die size for the 64Gb MLC NAND device will enable denser, lower-power solid-state discs (SSD) which are impacting almost every mobile consumer product from smartphones to digital camcorders. **[11.1]**
- Emerging non-volatile memory technologies include PCRAM, RRAM, and CBRAM. Any one of these technologies has the potential to change the industry and eventually supersede Flash, and even DRAM, as a mainstream memory technology **[11.2, 11.6, 11.7]**
- Improved SRAM designs offer lower power and improved robustness at low supply voltages, enabling dependable operation in the migration to deep submicron 32nm and 28nm CMOS. **[14.1, 14.3, 14.4]**
- The 2Gb GDDR5 Graphics DRAM will enable more lively gaming action for game consoles and graphic cards. **[28.3]**
- The mobile wide-I/O DRAM, which shows 4x higher data bandwidth than existing LPDDR2 DRAM, will increase the performance of mobile phones and smartphones. **[28.5]**

TRENDS IN MEMORY

Overall: Memory design has seen a number of trends over the years: process technology has steadily reduced its minimum feature size; a wide variety of techniques have been developed to improve packing-density; and a myriad of technology/circuit/system optimizations have been created to improve performance and reduce power dissipation. In addition, emerging technologies such as 3D chip stacking and new physical memory mechanisms are pushing the memory R&D frontier even-further forward. Some current state-of-the-art results from ISSCC 2011 include:

- 28nm 64Gb TLC NAND flash memory
- 7Gb/s-GDDR5 DRAM with 2Gb capacity
- 64Mb SRAM in High-κ Metal-Gate 32nm SOI technology with robust operation
- 28nm SRAM using 6T cells with low-voltage 0.6V operation
- Emerging memory technologies realizing non-volatile RAM: FeRAM (Ferrolectric RAM) with a novel sensing scheme, a fast read/write RRAM (Resistive RAM), and a large bandwidth CBRAM (Conductive-Bridging RAM) at 2.3GB/s.

Non-Volatile Memory (NVM): The performance of persistent Non-Volatile RAM (NVRAM) has evolved over time, with ISSCC faithfully tracking these developments over the years. ISSCC 2011 will report the highest read/write bandwidths for emerging NVRAM technologies such as Phase Change Memory (PCRAM) and Resistive RAM (RRAM) resulting from the use of new circuit and device technology (**Figure 1**). This is presenting new opportunities for extending the memory technology spectrum, together with existing NAND/MRAM/FeRAM/PCRAM technologies, as shown in **Figure 2**. Commercial uses of these new breeds of NVRAM have been very slow to appear because of the rapid reduction of per-bit costs of conventional flash memory technologies already in the market. However, these new technologies are sure to capture some specific markets for lower-power or zero stand-by system implementation in the coming age of green technology.

High-Performance Embedded Memory: Embedded memory plays a crucial role in today's VLSI applications from high-performance computing to low-power consumer electronics. While scaling of technology feature size down to 32nm or 28nm has enabled ever-larger and higher-performance on-die memories. However, scaling has also created growing challenges for the embedded memory designer. Growing device variability and power limitations are driving innovative solutions to maintain robustness and area-efficiency in such aggressively scaled memories. In particular, peripheral-circuit-assist features have become the key to maintaining cell read and write margins to enable low-voltage operation for dense SRAM caches. New strategies ranging from circuit-level techniques to fundamental changes in array architecture can also enable significant gains in area and power efficiency.

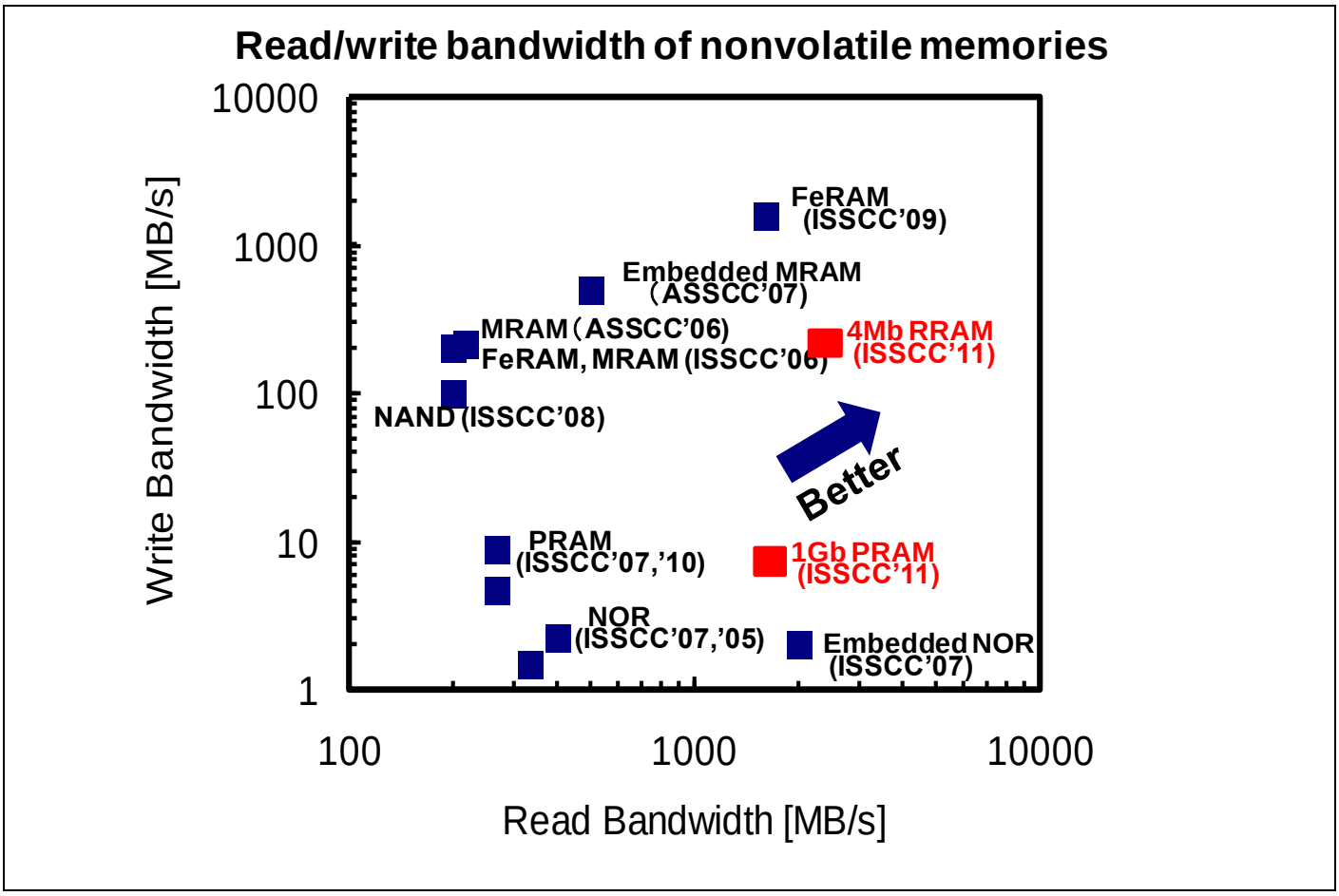


Figure 1: NVRAM Read/Write Bandwidth Trends

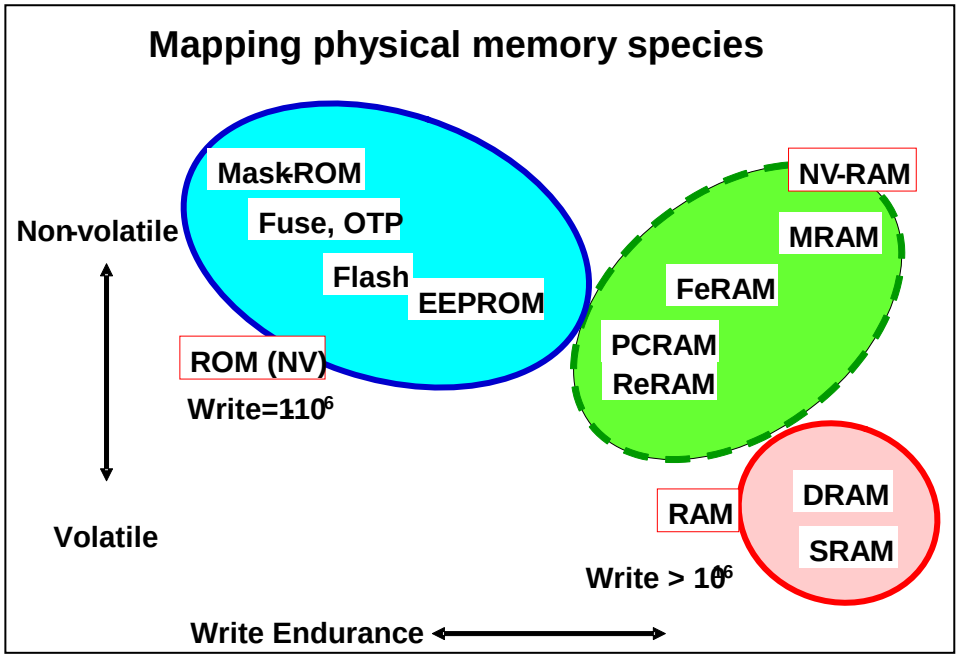


Figure 2: Comparison of NVRAM Technologies

NAND Flash Memory: Significant developments in NAND flash memory over the past few years are resulting in high-density, low-power, and low-cost storage solutions that are enabling the replacement of traditional hard-disk storage with solid-state disks (SSDs). At ISSCC 2011, a 64Gb/die capacity will be demonstrated using 24nm technology with 2b/cell operation. With physical scaling down accompanied by advancing multi-level-storage-cell concepts, a 64Gb/die capacity has been demonstrated in 24nm technology with 2 bits/cell operation. **Figure 3** shows the observed trend in NAND flash capacities presented at ISSCC over the past 17 years. Unfortunately, as process feature size shrinks, error rates continue to rise, requiring system designers to develop more-sophisticated controllers to offset this issue, some of which are utilized outside the NAND silicon in the system memory controller.

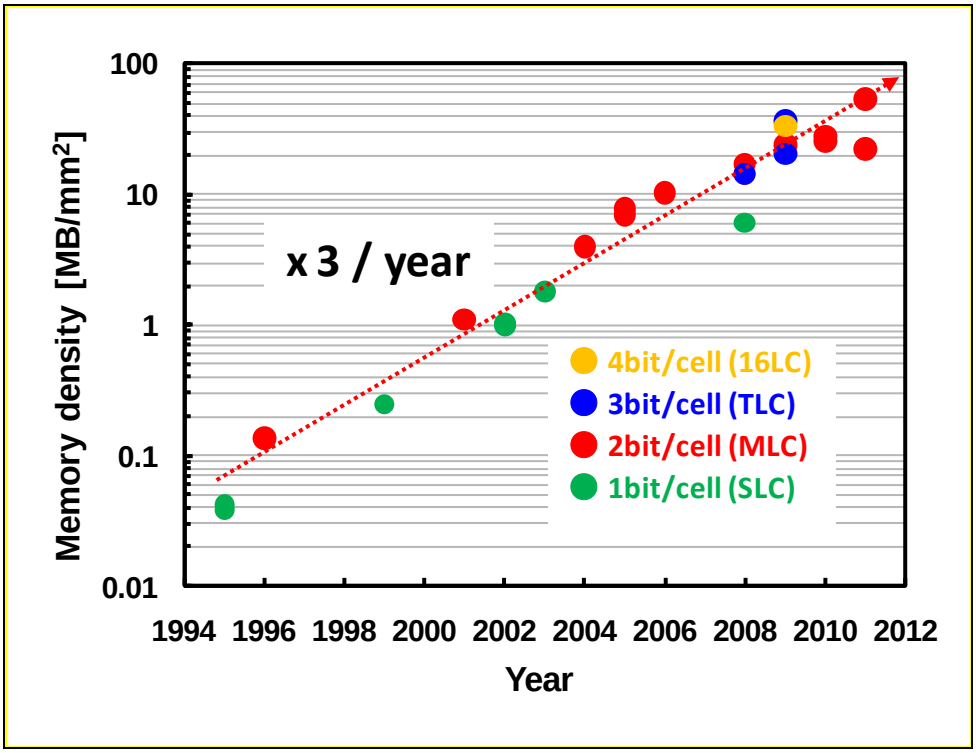


Figure 3: NAND Flash Memory Trends

SRAM Bitcell Design: Historically, a 50% area reduction in bitcell from node to node has been enabled by the scaling of technology feature size, resulting in a 2x improvement in on-die memory integration with each node reduction and continuing improvements in performance. However, the reduction in transistor geometry is increasing device variability, resulting in a slowdown in the scaling trend as shown in **Figure 4**. Between the 45nm and 32nm technology nodes, bitcell scaling has been reduced to less than the typical 50%. The introduction of High-κ Metal Gate technologies at the 45nm node has provided a significant reduction in the equivalent oxide thickness, thereby reducing the V_T mismatch and allowing further aggressive scaling of device dimensions needed to achieve the scaling of area. However, technology improvements alone are not sufficient to maintain area scaling. SRAM peripheral-circuit-assist features have become the key to maintaining cell stability, readability and write margins, and enable low-voltage operation. New strategies ranging from circuit-level techniques to fundamental changes in array architecture can also enable significant gains in area and power efficiency.

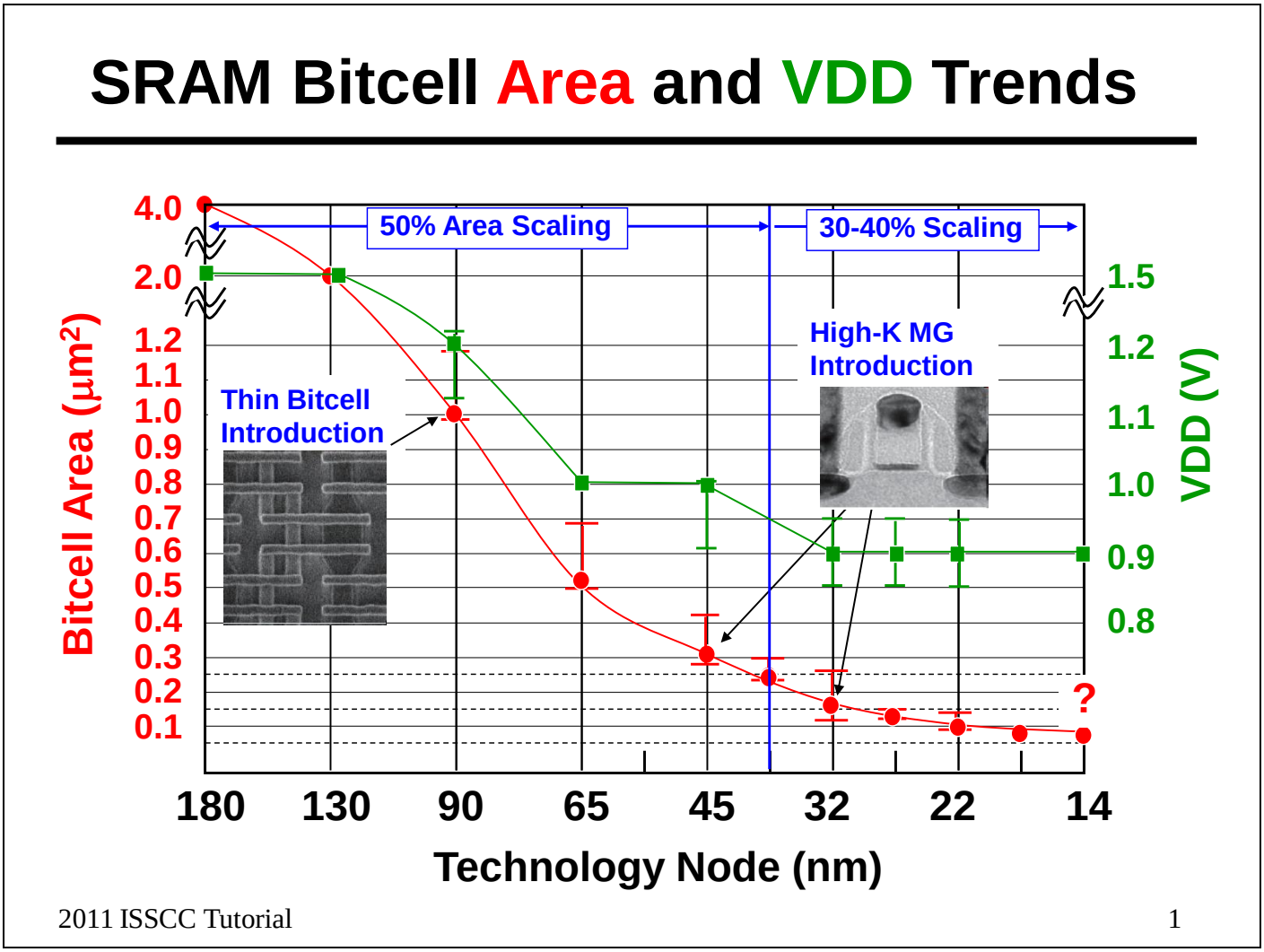


Figure 4: SRAM Bitcell Trends

DRAM & High-Speed I/O: Unfortunately, the gap between memory-core frequency and external-data rate continues to increase as conventional high-speed wired interface schemes such as DDRx and GDDRx for DRAM and NAND flash memory continue to evolve (**Figure 5**). This leads to the need for a larger prefetch size, which is emerging as a major problem in modern memory systems. However, alternatives which accommodate high data rates through the use of wider or differential interfaces will face the problem of increased pin-counts, and enlarged silicon areas. Combined with 3D integration of memory and memory/logic in near-future commercial products, new interface technologies will yield more memory stacking, along with lower-power and higher-bandwidth interfaces.

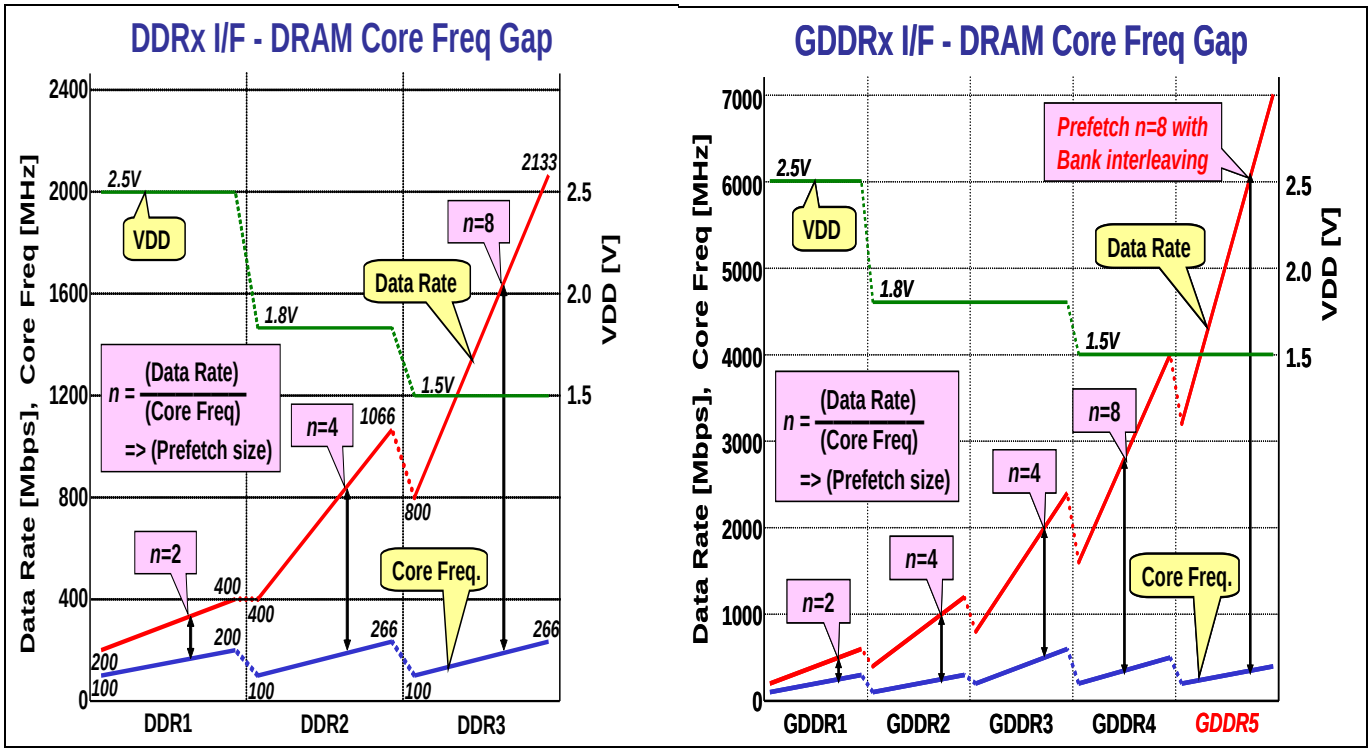


Figure 5: DRAM and High-Speed I/O Trends

RF Subcommittee

ISSCC 2011 – RF

Subcommittee Chair: *Nikolaus Klemmer, Texas Instruments, Dallas, TX*
Press Designate: *Chris Rudell, University of Washington, Seattle, WA*

OVERVIEW

CONTEXT AND PRESENT STATE OF THE ART

- Software-defined radios have long been promoted as the next big thing, but so far have not lived up to the hype due to a lack of adequate performance at a reasonable price point. **[3.1, 3.2, 3.6, 3.8, 26.6]**
- mm-Wave imaging solutions are still in their infancy. New advances in the fundamental-technology building blocks are required to finally open up exciting new application areas in security and healthcare. **[16.2, 16.3, 16.5, 16.6, 16.7]**
- Existing 801.11n wireless links in the 2.4 and 5GHz bands deliver speeds up to several hundred Mb/s, and efforts are underway to try and push data rates beyond the 1Gb/s barrier, up to 10Gb/s, using ICs in the mm-Wave band. **[16.7]**
- FMCW radars are an integral part of advanced automobile safety systems today that are becoming widespread throughout the automotive industry. **[16.8]**
- Existing health-monitoring requires bulky equipment that must be administered in over-crowded hospitals by overworked health care professionals, putting further strain on an already over-burdened system. **[16.9, 16.10]**
- Power amplifiers in CMOS have been restricted to non-linear switched-based topologies until now. Are the latest CMOS PA implementations ready for linear amplification prime-time? **[24.2, 24.4, 24.5]**
- Switched-Capacitor (SC) integrator stages have traditionally been limited to baseband frequencies for converter and filter applications. New SC circuit techniques are now being exploited at RF, for PA applications. **[24.3]**

MOST-SIGNIFICANT PAPERS

- New AD-PLL techniques remove impunity to interference in radio front ends enabling highly programmable radio front ends used in high-density environments. **[3.1, 3.2]**
- Radio receiver architecture has come full circle! Broadcom and UCLA will demonstrate the re-emergence of the old-school super-heterodyne receiver in 65nm with fully-integrated high-Q IF filters, and UCLA will demonstrate that the similarly-aged super-regenerative receiver can be put to good use in a very compact 186GHz low-power imaging application also in 65nm CMOS. **[3.5, 16.10]**
- Revolutionary advancements in fundamental millimeter-wave technology blocks. A variety of industrial and academic researchers deliver innovative techniques that yield revolutionary millimeter-wave building blocks capable of operating at frequencies up to 300GHz. **[16.2, 16.3, 16.5, 16.6, 16.7]**

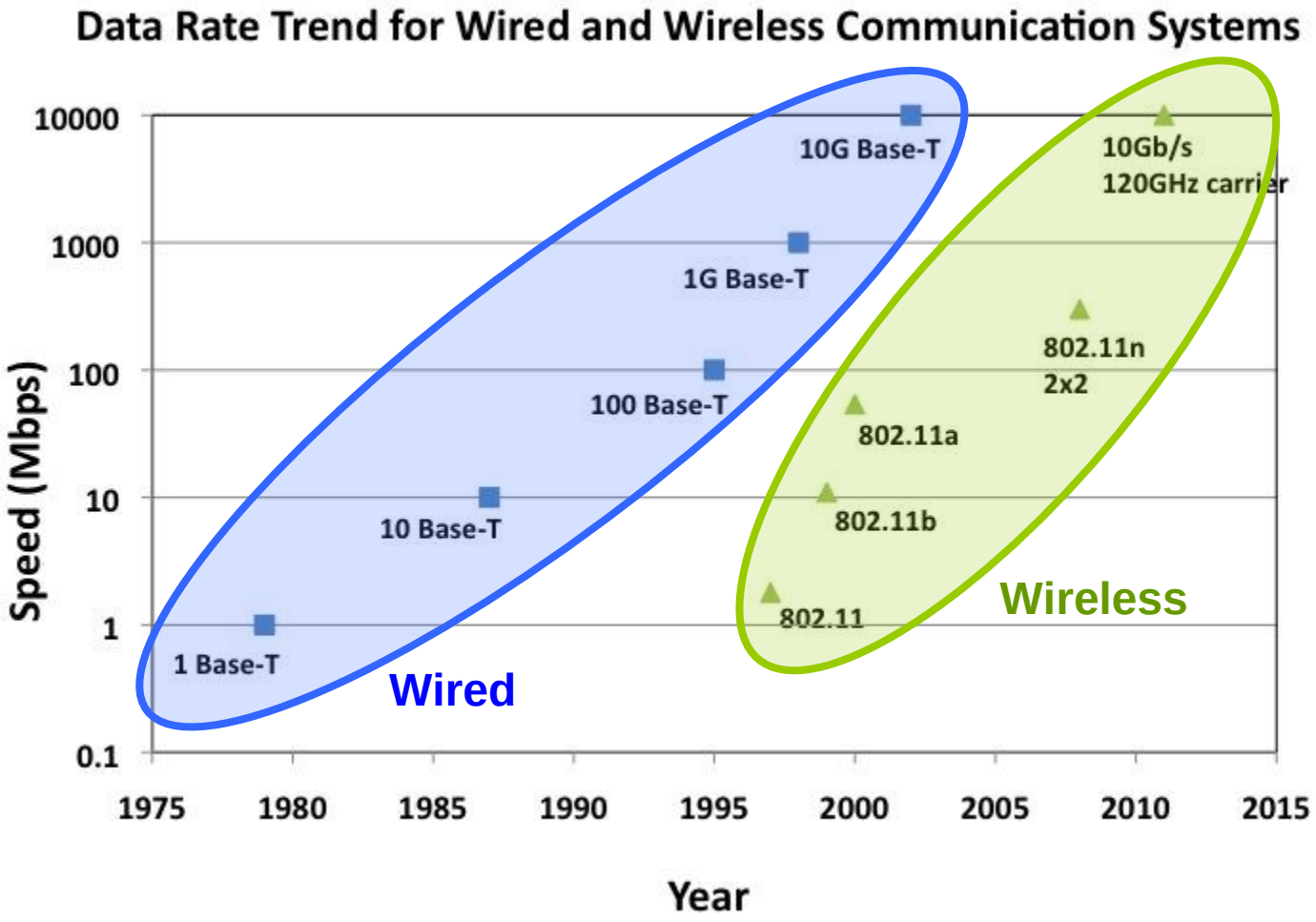
- New AD-PLL techniques dramatically enhance range and velocity resolutions of FMCW radars. An FMCW synthesizer radar by Toshiba achieves range and velocity resolutions of 10cm and 1.4km/h respectively thanks to a 2x wider bandwidth and 6x longer modulation period than previously reported solutions. **[16.8]**
- New radio techniques enable applications in the medical area by providing a very small form factor, low-cost solution for imaging using both UWB techniques and radio imaging in the 183GHz band. **[16.9, 16.10]**
- First demonstrations of linear PAs in CMOS. Intel and Samsung will deliver CMOS-only linear PA solutions addressing the WLAN and EDGE/GSM markets respectively. **[24.2, 24.4]**
- Demonstration of switched-capacitor techniques being applied to high-power signal processing. The University of Washington will demonstrate a 2GHz power amplifier delivering 25dBm, using purely switched-capacitor techniques for signal modulation. **[24.3]**
- Record power levels for a 60GHz PA in 65nm CMOS. UC Berkeley will demonstrate 18.6dBm saturation power using only 0.28mm² of silicon area! **[24.5]**

APPLICATIONS AND ECONOMIC IMPACT

- Continued enhancement of all-digital PLLs, and their migration to modern 65nm CMOS processes, will continue to improve sensitivity and reduce interference in wireless and wireline applications. The net result will be low cost solutions with even higher levels of performance. **[3.1, 3.2]**
- Software-defined radios are a step closer to reality with the newest implementation of broadband high-linearity, harmonic rejecting receivers, and multi-decade frequency synthesizers. **[3.6, 3.8, 26.6]**
- Millimeter-wave building blocks with frequencies up to 300GHz will play an important role in applications, such as security and 10Gb/s data-rate applications. **[16.2, 16.3, 16.5, 16.6, 16.7]**
- Improved FMCW radar performance will enable better automobile safety systems, leading to even greater adoption within the industry, which in turn will lower costs for the consumer due to increased product volumes and competitive marketing. **[16.8]**
- Patient healthcare monitoring is taken to a whole new level: Your vital signs can be monitored from the next room without wearing any electronics on your body with this UWB impulse radar in the GHz-range. In addition, extremely low-cost small form factor tereahertz imaging systems are now within our reach! **[16.9, 16.10]**
- Linear Power Amplifiers (PA) for 2.5G and 3G are currently the domain of GaAs technology which is expensive, and difficult to integrate into low-cost-handset designs. All-CMOS linear PAs promise lower costs and the possibility of greater levels of integration with other CMOS building blocks in future SoCs. **[24.2, 24.4]**
- New transmitter and Power Amplifier (PA) design techniques and topologies will substantially increase mobile phone battery life, allowing consumers to run their cell phones for several weeks before requiring a charge. **[24.3]**
- Achieving high transmission power levels in conventional CMOS will ensure low-cost solutions that can be tightly integrated, thereby enabling the continued adoption of 60GHz wireless technologies. **[24.5]**

TRENDS IN DATACOM TECHNOLOGIES

Increasing demand for higher data rates fueled by multimedia applications require communication systems to run at ever-increasing speeds. The bandwidth capabilities of wireline and wireless data communication systems are projected in the data-rate-trend chart shown below. As depicted, millimeter-wave frequency bands in the 120GHz range are enabling a new, potentially-disruptive technology. Using carrier frequencies in the 120GHz band, new wireless transceiver systems allow data rates up to 10Gb/s for short-range wireless data communication. This chart also indicates that wireless links are approaching the data rates traditionally realized with wireline solutions. Advances in wireless-communication data rates are being enabled by advanced nanometer-length CMOS technologies, combined with innovative circuit and radio-architecture implementations.



TECHNOLOGY DIRECTIONS SUBCOMMITTEE

ISSCC 2011 – TECHNOLOGY DIRECTIONS

Subcommittee Chair: *Siva Narendra, Tyfone, Portland, OR*
Press Designate: *Eugenio Cantatore, Eindhoven University of Technology, Eindhoven, The Netherlands*

OVERVIEW

CONTEXT AND PRESENT STATE OF THE ART

- Continuous monitoring of vital health signals will help reduce the cost of healthcare, enable proactive and preventive care, and reduce the need for routine clinical visits. **[2.1]**
- Sleep apnea is a life-threatening illness that requires bulky sensing systems, making the therapy highly inconvenient. **[2.2]**
- Terahertz signal sources have the potential to make the world safer by enhancing security screening and enabling aircraft to maneuver in low visibility. **[2.5, 12.5]**
- Fine-grain distributed sensors require the ability to scavenge energy efficiently. **[12.1, 12.3]**
- Organic electronics on plastic substrates has the ability to create the "Internet of things" because of its low-cost, large area coverage, and physical flexibility. **[18.1]**

MOST-SIGNIFICANT PAPERS

- A transceiver with ultra low energy (0.24nJ/b) and high sensitivity (250μV) for body-communication-channel-based Body Area Network. A design by KAIST has the potential to revolutionize wearable and continuous healthcare monitoring. **[2.1]**
- A 15-patch ultra-lightweight (400mg) low-power wearable sensor network. A design by KAIST, consuming less than 450μW, makes sleep-apnea monitoring and detection a true therapeutic solution! **[2.2]**
- Technology and architectural choices enable critical building blocks for Terahertz (300GHz to 3THz) based imaging. CEA-LETI-MINATEC and Universite Montpellier use a pixel embodying a single CMOS transmitter integrated with a bowtie antenna and low-noise amplifier; University of Wuppertal and IHP will present an 820GHz SiGe based chipset for THz active imaging. **[2.5, 12.5]**
- A low start-up voltage scavenging converter and a stand-alone self-powered electrical outlet energy monitor will accelerate the remote-sensor market. The University of Tokyo and STARC will present a voltage converter requiring only 95mV for start-up, with 72% system efficiency; NEC will present a realtime non-contact power-line-current sensor for home energy management. **[12.1, 12.3]**
- The world's first flexible organic substrate microprocessor! imec, et. al. will present an 8-bit processor running 6 instructions per second which foreshadows the future "Internet of things". **[18.1]**

APPLICATIONS AND ECONOMIC IMPACT

- Wearable sensors that use ultra-low-power and sensitive transceivers through enable proactive and preventative care through body-area communications. **[2.1]**
- Wearable print-on-fabric technology that includes both ultra-light-weight and low-power sensors shifts the paradigm of sleep monitoring for sleep-apnea patients from bulky and inconvenient to easy and comfortable. **[2.2]**
- 820GHz frontends and broadband low-cost CMOS THz imagers make security screening and other "see-through" industrial or transportation applications feasible. **[2.5, 12.5]**
- Real-time compact current waveform sensor achieves battery-free power monitoring of all appliances in the home, and paves the way to future fine-grain energy management. **[12.3]**

BODY-CHANNEL COMMUNICATIONS (BODY AREA NETWORKS)

Body Area Networks (BAN) is an emerging technology that has the potential to revolutionize next-generation healthcare, entertainment, and other personal applications. BAN, compared to other personal-area network solutions, targets a unique region of the power vs. data rate trade-off that makes novel personal applications possible (**Figure 1**).

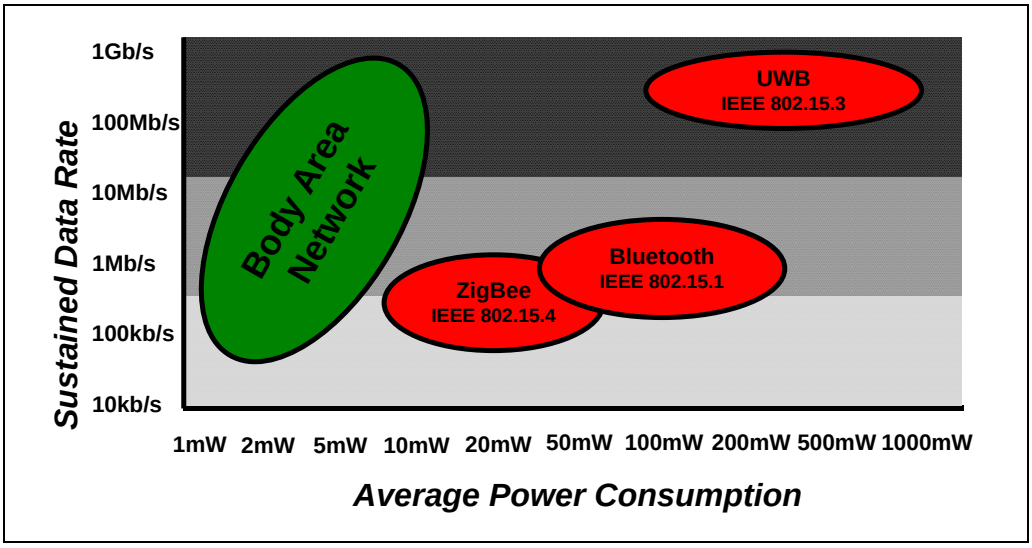


Figure 1: Modern Communication Technologies

Body-Channel Communication (BCC), a type of BAN which uses the human body as the signal-transmission medium, can achieve high-speed communication with low energy consumption compared to other personal-area network (PAN) solutions such as ZigBee, Bluetooth, and UWB (**Figure 2**).

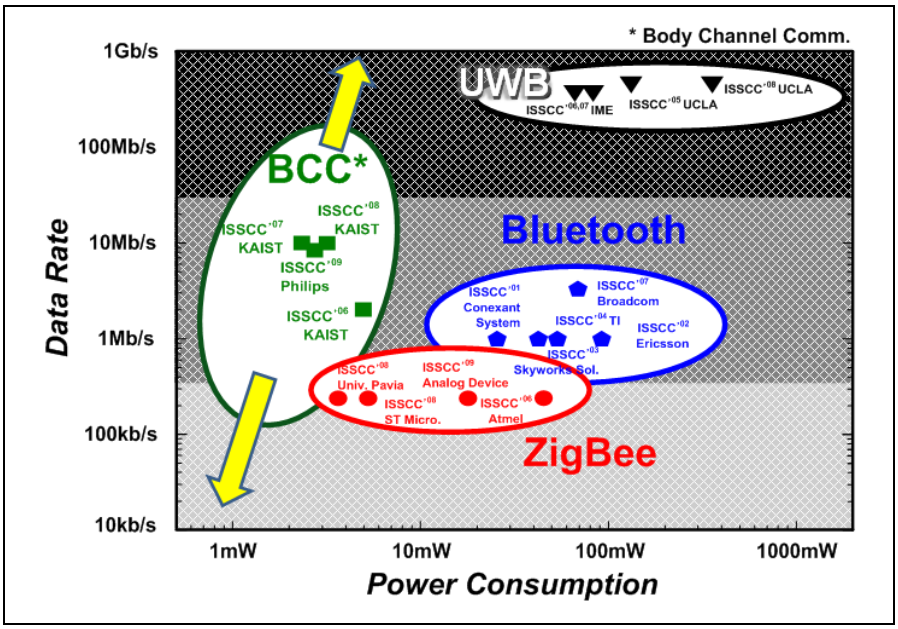


Figure 2: Energy Efficiency of Modern Communication Technologies

WIRELESS
SUBCOMMITTEE

ISSCC 2011 – WIRELESS

Subcommittee Chair: *David Su, Atheros Communications, San Jose, CA*
Press Designate: *Arya Behzad, Broadcom, San Diego, CA*

OVERVIEW

CONTEXT AND PRESENT STATE OF THE ART

- In the thrust towards Wireless-HD short-range communications for consumer markets, the feasibility of circuits for 60GHz Gb/s short range communications has been demonstrated. The main challenge in fulfilling 60GHz standards is productization, including antenna integration. **[9.2, 9.3]**
- In the thrust towards higher-data-rate and long-range capability in connectivity, fully-integrated 802.11n WLAN chipsets are common place in today's wireless markets. **[9.6]**
- The cellular evolution with yet more bands and higher data rates used to support multimedia access at low cost, is constantly pushing transceiver requirements. **[21.2, 21.3]**
- In multi-band receivers, bulky on-chip inductors and off-chip components must be replaced by reconfigurable and highly linear receivers. **[21.1, 21.4, 21.5]**
- 3G transmitters must be implemented as multi-standard transmitters without requiring external SAW-filters for noise suppression. **[21.6, 21.7, 21.8]**
- The ability to distinguish the large self-leakage from a small sensor signal poses a key challenge in RFID readers. This requires large non-integrated and potentially-expensive isolators. **[26.2]**
- The minimum energy requirement of RFID sensors limits their range and places significant power demands on RFID readers. **[26.1]**

MOST-SIGNIFICANT PAPERS

- First fully-integrated CMOS 60GHz transceivers reported, that address the new Wireless-HD and WiGig standards. Researchers from CEA-LETI-MINATEC and STMicroelectronics will deliver an industrially-packaged Wireless-HD solution capable of 3.8Gb/s operation, using an HTCC substrate, including glass antennas. SiBeam describes a 65nm chipset that supports the maximum Wireless-HD and WiGig data rates, using 32 transmitter and 32 reciever antennas. **[9.2, 9.3]**
- First 3-stream 3x3 MIMO WLAN SoC to improve throughput, range, and link robustness. A chip designed by National Taiwan University integrates three dual band WLAN transceivers and is backward-compatible with legacy IEEE 802.11 a/b/g networks. **[9.6]**
- First-reported single transceiver showing diversity-performance gains of 50-120%. A consortium including ST-Ericsson, Ericsson, and Lund University will deliver the smallest reported WCDMA/EDGE diversity receiver with a DigiRF interface. **[21.2]**

- Highest level of integration reported for a cellular chipset. Qualcomm will deliver a fully-integrated solution containing an embedded EDGE/UMTS RF section, digital baseband processor, memories, and audio processor, all on a single SoC. In addition, a novel DPLL architecture ensures very-low peak transmitter-battery current for GSM low-band operation. **[21.3]**
- First-reported all-digital multi-mode transmitter meeting the stringent 3GPP RX-band noise requirements. A collaboration between Infineon Technologies and DICE will deliver a low-power polar architecture with lowest-reported power consumption. **[21.7]**
- New RFID sensor with the widest frequency range ever reported. Collaboration between Graz University and Infineon yields an ultra-low-power sensor node, employing innovative design techniques to support a frequency range of 13MHz to 2.45GHz, while minimizing power dissipation by an additional 70% over the current state-of-the-art. **[26.1]**
- First self-correlation-based RFID reader is demonstrated. Researches from KAIST and PHYCHIPS will demonstrate an RFID reader which isolates small back-scattered sensor signals from self-leakage in the transmitter, eliminating the need for large off-chip isolators. **[26.2]**

APPLICATIONS AND ECONOMIC IMPACT

- Wireless transmission of multi-Gb/s data such as high-definition (HD) audio/video content will remove the clutter of HDMI cables between the HD video screen and the multiple sources of HD content. Wives around the world rejoice! **[9.2, 9.3]**
- A new generation of WLAN SoCs will push the throughput envelope to extreme levels, while providing a more robust link and being backward compatibility with older WLAN generations. Ubiquitous wireless multimedia, anyone? **[9.6]**
- Highly integrated multi-standard and multi-band transceivers extend multimedia access to low-cost handsets. This will provide media access to all handset users and promote new business models, globally. **[21.2, 21.3]**
- Reconfigurable cellular transmitters will promote low-cost high-performance chipsets, while multi-band-enabled transmitters significantly reduce the cost of adding more cellular bands. Ultimately these optimizations will further drive down the cost of handsets for consumers. **[21.7]**
- Large-scale integration of multiple functions including signal-level detection and temperature sensing will significantly reduce implementation cost and sensor size. As a result, we can expect wider deployment of sensing technologies for diverse applications spanning healthcare to inventory management. **[26.1]**
- Eliminating large external isolators greatly reduces the implementation cost of RFID readers, enabling their adoption in even more applications. **[26.2]**

WIRELINE
SUBCOMMITTEE

ISSCC 2011 – WIRELINE

Subcommittee Chair: *Franz Dielacher, Infineon, Villach, Austria*
Press Designate: *John T. Stonick, Synopsys, Hillsboro, OR*

OVERVIEW

CONTEXT AND PRESENT STATE OF THE ART

Shrinking CMOS technology is a boon for digital circuits and a bane for analog design. This year, at ISSCC, the groundwork is laid for overcoming these limitations in the next generation of wireline transceivers. Progress will be presented on many fronts: Pushing CMOS to record speeds, providing improvements in power efficiency, presenting record setting levels of equalization capability, and introducing innovative adaptation algorithms.

- Higher data rates will become ubiquitous only when power-efficient sophisticated equalization techniques are realized in silicon. **[20.2, 20.3, 25.6, 8.6]**
- Solutions to the problem of generating large signal swings from high-speed transmitters in low-cost CMOS are finally being discovered. **[8.8, 20.3]**
- Increases in data rates will come not only through improvements in transceivers but also through the development and deployment of new low-cost plastic transmission media (waveguide). **[8.5]**

MOST-SIGNIFICANT PAPERS

- The best equalization capability ever demonstrated by a receiver! Researchers from Fujitsu Laboratories will describe the first reported receiver that is able to accurately reconstruct an incoming signal while receiving less than 1% of the transmitted data energy! **[20.1]**
- New low-cost plastic materials are being developed to carry data signals. A co-operative venture between Sony and Caltech combines a new technology, plastic channel waveguides, and full-duplex transceiver technology to create a low-cost 25Gb/s interconnect. **[8.5]**
- The world's first CMOS 100Gb/s Ethernet gearbox has been developed! Engineers from Hitachi will present a 10:4 CMOS MUX/DEMUX gearbox for 100Gb/s Ethernet operation. **[8.4]**
- A new record for the "greenest" interface for display panels has been set! Researchers from Seoul National University will present a new video interface in 130nm CMOS that has both lower power and smaller area than the existing state-of-the-art. **[25.8]**
- The most sophisticated CMOS transceivers ever demonstrated. Engineers from LSI and Texas Instruments, along with Arda Technologies, have independently developed the first generation of transceivers with 10 or more taps of DFE correction and an operating rate of over 14Gb/s. **[20.2, 20.3]**

APPLICATIONS AND ECONOMIC IMPACT

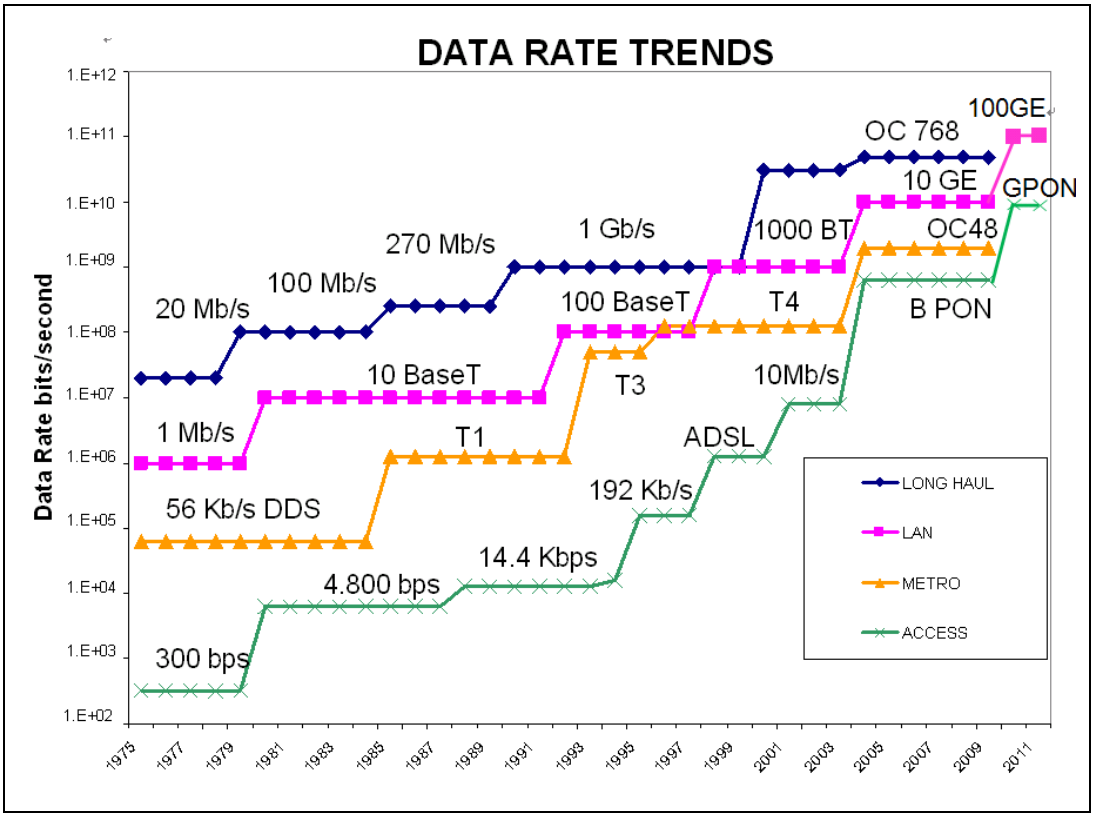
- No, you don't need to adjust the color of your television -- things have just gotten a little bit "greener" with the development of the lowest-power video interface, ever. **[25.8]**
- Imagine downloading the contents of a DVD in less than one second. We are one step closer to achieving this dream thanks to the demonstration of the first CMOS MUX/DEMUX gearbox for 100Gb/s Ethernet. **[8.4]**
- There is a lot of controversy about whether future communication channels will be made of copper or glass, but the shocker is that plastic waveguides may be the dark-horse winner! **[8.5]**
- Deep within the heart of the Internet, data traverses through a harsh environment that has created a bottleneck… until now! New higher-speed transceivers with greater equalization capabilities not only tolerate this inhospitable environment, but actually thrive within it! **[20.1, 20.2, 20.3]**

TRENDS IN WIRELINE COMMUNICATIONS

The trends in wireline communications today follow several seemingly conflicting paths. On one hand, there is a strong demand for transceivers that are highly-optimized for low power consumption for use with relatively low-loss channels. Simultaneously, there is a similarly strong demand for transceivers that, while still energy efficient, are optimized to provide signal levels and equalization capabilities that allow for communication over adverse channel conditions at speeds previously deemed impossible. At ISSCC 2011, papers in three sessions **[Session 8, Session 20, Session 25]** will describe a number of results that address these issues.

New applications are emerging, such as Internet multi-player gaming, network-based computing/data-storage, transaction-intensive Web 2.0 applications, and high-definition home-entertainment networks. The enabling technologies for these applications are high-performance transceivers for OC-768 (40Gb/s), 100Gb/s Ethernet, and high-speed "green" serial links for data centers. The demands of these applications will drive the advancement in equalization capability and robust-adaptation methodology. Additionally, the deployment of Gigabit Passive Optical Networks (GPON) in the near future will provide home-access data rates beyond 10Gb/s. PON technology reduces system cost by sharing the existing fiber infrastructure between multiple customers, but challenges transceiver designers by requiring burst-mode operation of amplifiers, and clock recovery with low latency at Gb/s data rates. We expect continuing innovation in this area for the foreseeable future.

As shown in the figure below, up to 100Gb/s data rates are now readily available using CMOS solutions. At these rates, an entire high-definition movie can be transferred in less than a second! Achieving such a high data rate at a reasonable level of power consumption requires advanced energy-efficient clock-and-data recovery, and equalization techniques, to conquer transmission-channel impairments and speed limitations of low-cost CMOS. Papers presented at ISSCC 2011 will cover a large selection of techniques in various CMOS nodes with impressively low power consumption.



ISSCC 2011
SESSION OVERVIEW
Press-Release Material

CONDITIONS OF PUBLICATION

PREAMBLE

- The Session Overviews to follow serve to capture the context, highlights, and potential impact, of the papers to be presented in each Session at ISSCC 2011 in February in San Francisco
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FOOTNOTE

- From ISSCC's point of view, the phraseology included in the box below captures what we at ISSCC would like your readership to know about this, the 58th appearance of ISSCC, on February 20th to the 24th, 2011, in San Francisco.

This and other related topics will be discussed at length at ISSCC 2011, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 20-24, 2011, at the San Francisco Marriott Marquis Hotel.

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The material presented here is preliminary.
As of November 1, 2010, there is not enough information to guarantee its correctness.
Thus, it must be used with some caution.

Session 2 Overview / Technology Directions

Technologies for Health

Session Chair: *Uming Ko, Texas Instruments, Dallas, TX*
Session Co-Chair: *Eric Colinet, CEA-LETI, Grenoble, France*

Technology advancement not only enables smaller biosensors, health-care monitoring and communication systems, but also reduces their power dissipation. Ease-of-use and a reduction in cost-of-ownership fuel portability and the increasing success of next-generation medical electronics. In this session, the latest advancements in technologies and healthcare applications are presented, encompassing Wireless Body Area Networks (WBAN), body sensor networks, wireless sensors, Ultra Wide Band (UWB) and Terahertz (THz) imaging. In addition, the session features two accurate timers for ultra-low-power wireless sensor nodes and high-speed communication applications.

WBAN is an emerging technology that combines health care and consumer electronics applications around the human body. Paper 2.1 [KAIST] presents the very first WBAN that fulfils the IEEE 802.15.6 Task Group specifications. Its extremely low energy consumption of 0.24nJ/b makes it very attractive for future body-area network applications. This is achieved by resonance matching, contact impedance monitoring, and a low-power scalable double-FSK modulation scheme. To enable excellent low-power performance circuit techniques like a reconfigurable LNA/driver, current-reuse wide-band demodulation, and a divider-based LO generator with duty-cycle correction are exploited. The 2.5×5mm^2 transceiver is fabricated in 0.18µm CMOS.

Paper 2.2 [KAIST] presents a wearable body-sensor network that realizes continuous sleep monitoring by ExG (EEG, EMG, EOG, and ECG) extraction from a sleeper's face, using 20mm fabric patch sensors. The consumption is 75µW for the real-time scalable network controller and 25µW for the ExG sensors. The form factor of this work is 10× smaller and 70× more energy-efficient than prior art, achieving a communication energy of 0.33pJ/b.

The increased incidence of diabetes makes non-invasive and continuous glucose monitoring a pressing demand. A wireless glucose sensor fully integrated into a contact lens is demonstrated in Paper 2.3 [U Washington]. The system has a measured sensitivity of 1.67µAmm^{-2}mM^{-1}. It is wirelessly powered, communicates by load-shift keying (LSK) at 2.4GHz and achieves a measurement range of 0-to-2 mM while consuming 3µW from a regulated 1V supply. The whole chip area is 0.5mm^2 and requires no external components.

Paper 2.4 [UC Cork; Tyndall National Inst; U Pisa; U Reggio Calabria] reports what we believe to be the first implementation, including experimental evidence, of an SoC UWB (3.1 to 10.6GHz) pulse radar front-end for respiratory rate monitoring. The radar sensor, based on a correlation receiver implemented in 90nm CMOS, consumes 73mW from a 1.2V supply. It can detect target movements up to 2cm at 70cm distance and the respiratory rate of a person under test at distance of 25cm.

Paper 2.5 [MINATEC; U Montpellier 2] presents a low-cost CMOS imager for Terahertz (THz) imaging based on a 0.13µm CMOS technology. A MOSFET is coupled to a bow-tie antenna. Self-mixing allows direct conversion to the low-frequency band used for light modulation. The imager includes an in-pixel low-noise amplifier and multiplexing circuitry for single video output. Measured electrical performance and images demonstrate a maximum responsivity of 90kV/W (12% higher than state-of-the-art), with a pixel power dissipation of only 95µW. This is a 57× improvement compared to prior art (5.5mW).

Paper 2.6 [National Chung Cheng U] highlights a 48µW, 0.81cm^3 implantable micro-stimulator SoC (IMSoC) with smart power management, sensors for closed loop stimulation, and a wireless telemetry/recharging system. The wireless telemetry, dissipating 10× less power than prior art in a 20× smaller footprint, handles the adjustable parameters for *in vivo* stimulation. Rat intracardiac electrograms are employed in an animal study.

Paper 2.7 [U Michigan] emphasizes that accurate synchronization cycle time measurement is required for ultra-low power wireless sensor nodes with a stringent power budget. A multi-stage temperature-compensated gate-leakage-based timer reduces rms jitter by 8.1× and synchronization uncertainty by 4.1× with a power consumption of just 0.66nW. Effective temperature sensitivity is reduced to 31ppm/°C, a 15× improvement from the prior art. The sub-nW timer makes synchronization of ultra-low-power sensor nodes a reality.

Very accurate local clocks play a fundamental role in modern communications, where high-precision references enable fast communication data rates. Paper 2.8 [CSEM] presents the first low-power CMOS RF lock loop highly integrated on-chip, for a Miniature Atomic Clock (MAC). An Allan deviation 1s intercept point of $\sigma y = 4 \times 10^{-10}$ is measured on a 10MHz clock using an RF loop locked on a ^{87}Rb cell for CPT interrogation.

Session 3 Overview / RF

RF Techniques

Session Chair: *Jan Craninckx, imec, Leuven, Belgium*
Session Co-Chair: *Jing-Hong Conan Zhan, Mediatek, HsinChu, Taiwan*

Wireless circuits have become the foundation of the way we live our lives, and this trend will only continue further in the future. Even in this mature field, new techniques are developed every year, and these inventions will allow the further integration of new technologies into every consumer product that will in no time become indispensible for the whole population, without people realizing the complex systems they have in their pockets.

The key enabler for this evolution is cost reduction and feature enrichment through implementation in advanced digital-based CMOS technologies, as will be evident from the papers presented in this session. Digital PLLs use less area and moreover incorporate such a rich variety of digital processing techniques that they actually outperform their analog counterparts. RF receivers as well use all the capabilities of deeply scaled CMOS to obtain state-of-the-art performance, and on top of that architectures and techniques that can handle large blockers are conceived. That avoids the need for expensive external RF blocker filters, which was the only remaining roadblock for multiband worldwide mobile terminals.

The first two papers of this session describe advances in digital phase-locked loops. Paper 3.1 [Texas Instruments] shows how the power of high-speed digital processing and dithering is used to overcome all spurious issues in an ADPLL. Implemented in 65nm CMOS within an area of 0.35mm^2, it dithers the crystal oscillator slicer to avoid ill-shaped quantization noise at near-integer fractional-N operation. It is also capable of phase modulation up to a bandwidth higher than the reference frequency, and succeeds in complete TX spectral mask requirements without any exceptions.

Reversing the obvious TDC into a Digital-to-Time converter (DTC), paper 3.2 [NXP Semiconductors] enables reduction in the phase detector quantization noise, which allows for easier and lower power implementation. The 5.3GHz fractional-N ADPLL implemented in a 65nm CMOS technology achieves an in-band phase noise floor of -96 dBc/Hz and in-band fractional spur power of -45 dBc after calibration.

The proof that CMOS scaling will continue also for RF circuits is given in paper 3.3 [Intel]. In this 32nm Hi-k MG completely digital technology, an ESD-protected 2.5GHz T/R switch and LNA are implemented, making clever use of the possibilities and the restrictions of the technology. The LNA uses nested coupled inductors, compatible with flip-chip bumps, and achieves 3.5dB NF, 11dB Gain, -5dBm P_{1dB} while drawing 11mA from a 1.8V supply. The TX thin-oxide switch has 1.1dB insertion loss and provides +300/-200V CDM ESD protection.

Paper 3.4 [Delft University of Technology] shows that high voltages needed in a base station PA driver are compatible with baseline 65nm CMOS, by using thin-oxide extended-drain high-voltage MOS devices at no extra mask cost. The pulse-width-controlled RF power driver delivers a maximum output swing of 8.04V_{pp} to a 50Ω load with 9V supply, from 0.9 to 3.6GHz.

The next two papers of this session present blocker-resilient receiver architectures paving the way for possible SAW filter removal. In paper 3.5 [Broadcom], a superheterodyne 65nm CMOS receiver utilizes impedance transformation to create a high-Q filter at RF and IF frequencies. The receiver consumes 12mA and occupies 0.67mm^2 while achieving 2.8dB NF and IIP3 of -8.5dBm.

A second 40nm CMOS receiver operating for both LNA-first and Mixer-first modes is presented in Paper 3.6 [imec]. The complete RX chain achieves 3dB NF, +10dBm out-of-band IIP3 and +80dBm IIP2, while tolerating 0dBm blockers at 20MHz offset using 2mm^2.

The last two papers of this session address problems faced by broadband receiver front-ends. Paper 3.7 [University of Twente] presents a frequency insensitive approximation for sine weighting through discrete-time switched-capacitor vector modulators for accurate beamsteering. Implemented in 65nm CMOS, the 4-element phased array demonstrates one-to-one mapping between control settings and phase shift. The array occupies 0.44mm^2, draws 308mW from 1.2V, and results in a 1.4° phase and 0.4dB gain error (RMS).

Paper 3.8 [Silicon Laboratories] demonstrates a 110nm CMOS harmonic rejection mixer for tuner applications. Critical matching is only required for IF amplifiers instead of for RF switches, providing a rejection ratio in excess of 52dB for the 3rd-, 5th- and 7th- order harmonics without calibration, while also achieving an IIP2 of 75dBm.

As is apparent from the papers presented in this session, continuing circuit and architecture innovations in advanced digital CMOS technologies pave the way to further integration and cost reduction!

Session 4 Overview / High-Performance Digital *Enterprise Processors and Components*

Session Chair: *Joshua Friedrich, IBM Systems and Technology Group, Austin, TX*
Session Co-Chair: *Takashi Miyamori, Toshiba, Kawasaki, Japan*

Session 4 focuses on significant new innovations in the development of enterprise class microprocessors. This year's enterprise designs feature the fastest clock frequency, the highest x86 core count, and the highest energy efficiency, and the highest transistor count ever achieved in commercial microprocessors. The trend of dramatically increasing the number of threads, special function units, and off-die interconnect contained within a single die also continues. These designs from IBM, Intel, AMD, and the Chinese Academy of Sciences also employ a variety of power-efficient circuit and micro-architectural techniques to continue Moore's Law in the face of the dramatic power challenge plaguing deep sub-micron technology

The first paper describes the microprocessor chip for the IBM zEnterprise 196 system, which is the first commercial processor chip to ship at a frequency in excess of 5 GHz. The 512mm2, 5.2GHz chip was built in IBM's 45nm Silicon-on-Insulator CMOS process with 13 levels of copper interconnect. It contains 4 processor cores, 1.5MB of private SRAM L2 cache per core, and an on-chip, high-speed 24MB shared L3 cache built from IBM's unique embedded DRAM technology that combines DRAM density with a high-speed digital logic process. To meet the incredibly high frequency objective, the design team made major cycle time enhancements, reduced core power consumption at constant PVT conditions by over 25% compared to the 65nm Z core, and improved the on-die power distribution. At the same time, the design added out-of-order instruction processing to further improve performance at constant frequency.

Paper 4.2 highlights a particularly crucial high speed component of IBM's zProcessor core – the dynamic hit logic and embedded 8Kbit SRAM used for L1 cache hit detection. The 14 bit hit logic described in this paper uses programmable launch and reset clocks along with a mix of dynamic and highly skewed static CMOS to achieve record operating frequencies (above 6.5GHz at lab conditions). In addition, its innovative use of a "search-for-a-hit" scheme minimizes power consumption without degrading performance. Array BIST provides both the hit logic and SRAM with full "at-speed" test coverage for the first time.

Paper 4.3 from Intel's lab in Bangalore, India, describes the next generation enterprise Xeon® processor consisting of 10 Westmere 32nm cores and a shared, inclusive L3 cache integrated on a monolithic die with link based IOs. The die contains the highest number of x86 cores ever integrated onto a single chip and contains significant innovations and circuit optimizations over its predecessor, Nehalem, targeting idle power reduction, robust high speed IO links at the next generation process node, and performance per watt improvements. The processor is implemented in 32nm CMOS using high-κ metal gate transistors and nine copper interconnect layers. It supports individually controlled power gating of each of the ten cores and implements macro clock gating of uncore and cache functions to drive idle power to new lows.

Energy efficient processing is also a key area of innovation, and the Godson-3B processor from the Chinese Academy of Sciences, described in Paper 4.4, reports the highest energy efficiency (3.2GFlops/Watt) among all state-of-art high-performance processors. Godson-3B is an 8-core design implemented on 65nm CMOS LP/GP mixed process with 7 layers of Cu metallization. It contains 582.6M transistors within 299.8mm2 area and operates at frequencies of up to 1.05GHz. Its peak performance is 128/256GFlops for double/single-precision with 40W power consumption.

Paper 4.5 from AMD describes the new x86-64 based 2-core CPU module (Bulldozer) that contains 213M transistors in 11-metal layer 32nm high-k metal-gates SOI CMOS process. In addition to the micro-architecture improvements, the components, such as the L1 and L2 caches, the integer unit and the Floating Point unit, are designed to achieve higher frequency, lower power consumption, and lower gate counts per cycle than the 45nm AMD core while maintaining IPC (Instructions per Cycles). It operates over 3.5GHz in an area (including 2MB L2 cache) of 30.9mm2.

The next paper 4.6 from AMD presents details of the 40-entry unified, out-of-order scheduler and integer unit of the Bulldozer. The scheduler issues four operations per cycle and the integer execution unit supports single-cycle bypass between four functional units. Instead of dynamic logic, skewed gates with static standard cell are extensively used. Furthermore, to minimize power consumption, the design reduces switching activity by manipulating pointers rather than moving large amounts of data within queues.

Paper 4.7 from Intel describes the clock generation system of a multi-core processor for server applications, fabricated on a 9-metal layer 32nm CMOS process. A growing number of CPU cores and integration of high speed I/O ports, such as QuickPath Interconnect, PCI express and DDR3, presents significant challenges to the clock generation and distribution systems. The proposed clock system architecture delivers low skew, low power and low latency with modularity and scalability for a ring-like architecture in spite of these challenges.

Finally, Paper 4.8 from Intel is the Itanium processor implemented in a 32nm CMOS process with 9 layers of copper interconnection. It contains 3.1 billion transistors within a 18.2 mm by 29.9 mm die. This transistor count represents a 50% increase over the previous Itanium processor and is the highest transistor count ever reported for a single die. The processor includes eight multi-threaded cores, a ring based system interface, and more than 54MB of cache memory. A three level cache hierarchy consists of a first level single cycle 16K Instruction (I) and Data (D) cache that is backed by two second level caches (a nine cycle 512K I cache and an eight cycle 256K D cache) and a 32MB the last level cache. The design implements twice as many as cores as the previous Itanium while lowering the thermal design power (TDP) by 15W to 170W. High speed links allow for peak processor-to-processor bandwidth of up to 128 GB/s and memory bandwidth of up to 45GB/s.

Together, these innovative enterprise processors and design components represent a new height of performance, integration, and energy efficiency. By continuing to deliver exponentially increasing performance and capability, these efficient engines will enable computers to analyze our world's most challenging scientific problems and manage the needs of increasingly complex global enterprise.

Session 5 Overview / Analog
PLLs

Session Chair: *Ivan Bietti, STMicroelectronics, Grenoble, France*
Session Co-Chair: *Tsung-Hsien Lin, National Taiwan University, Taiwan*

Frequency Synthesizers and clock generators are essential building blocks in almost all modern electronic systems. The Phase-locked loop (PLL) is the most suitable circuit architecture to perform the extremely diverse tasks required by the very different applications. In wireless transceivers, PLLs are used to generate high-frequency local oscillator signals with extremely low phase noise for up-conversion and down-conversion of the transmitted and received signals. For high-speed data communications very low-jitter clock signals are required. When used as clock generators for large processors, wide frequency range, fast locking time and very-low-power quiescent dissipation are absolutely mandatory. These tough specifications need to be achieved at the lowest possible power, both for the stringent requirements of portable systems, but also to reduce the issues associated with heat dissipation.

The relentless scaling of CMOS technology and the associated increase in computational power have allowed the introduction of sophisticated digital techniques to overcome the analog limitations of the scaled devices. This trend continues and has made the performance of the partly and all-digital fractional PLLs comparable to those achieved by the integer analog ones in terms of phase-noise and jitter. On the other hand, the usage of digital techniques gives superior flexibility and portability, lower sensitivity to the analog parameters and allows easier supply scaling. Digital techniques are also effective for adaptive supply noise cancellation, which is vital to maintain the PLLs' high performance in a real, noisy environment.

The papers presented in this session are all PLLs. The first two papers continue the progressive improvements in the design of the all-digital PLLs (ADPLLs) after their recent introduction.

Paper 5.1 (Politecnico of Milan) presents a new architecture for an ADPLL which represents a step forward in the design of these kind of synthesizers. Thanks to a 10b digitally compensated and finely programmable delay line, the time-to-digital converter (TDC) required by a classical ADPLL for accurate phase error detection is eliminated and replaced by a simple bang-bang phase detector. The combination of the achieved jitter and power results is the best ever presented for an ADPLL: jitter is lower than 0.56psrms and the circuit burns less than 5mW bringing to FoM very close to -240dB.

Paper 5.2 (Panasonic Wireless Research Laboratories) builds an ADPLL around a rotary-travelling-wave oscillator using its 32 phases, accurately spaced by 3.9ps. This technique does not require the period normalization circuits as in LC-tank based PLLs while keeps very good phase noise performance. The prototype, realized in 65nm CMOS, achieves -108dBc/Hz in band phase noise for a 1MHz loop BW.

In-band Phase Noise reduction is also addressed in the next 3 papers with different techniques.

Paper 5.3 (MediaTek) uses injection locking on a ring-oscillator-based PLL. The problem of aligning the phase of the injected reference clock to that resulting from the PLL loop is elegantly solved by driving both the VCO S/H used for phase comparison and the injecting circuit with the same exact signal. The PLL, integrated in 65nm CMOS, achieves an overall jitter integrated from 1kHz to 40MHz of 2.4ps while the PLL runs at 432MHz and consumes 6.9mW.

Paper 5.4 (POSTECH) implements a jitter reduction technique for the quantization noise of a fractional-N PLL, effective both in and out of band. Multiple phases of a ring oscillator are used in combination with a phase interpolator to reduce the quantization noise while an embedded 8- tap FIR is used to digitally filter the noise in front of the Phase Frequency detector. The Phase Noise reduction is 34dB, resulting in an in-band noise of -106dBc/Hz at 100kHz and an out of band noise of -107.5dBc/Hz at 6MHz.

Paper 5.5 (Toshiba) instead addresses the noise reduction problem by maximizing the loop bandwidth while keeping control of the reference spur. This is done using a high CMRR differential amplifier placed in front of a differentially controlled oscillator. The resulting jitter for the 65nm PLL prototype is 570fsrms while the reference spur is better than -40dBc even for a reference to bandwidth ratio of 10.

Paper 5.6 (Oregon State University) introduces an adaptive and quite efficient way to cancel the effect of the supply noise on the PLL jitter. This is particularly important for ring-oscillator-based PLLs since the supply sensitivity of this VCO is quite high. It is based on a background digital calibration using a test signal injected on the VCO supply. The effectiveness of the technique works over a wide range of frequencies (0.4 to 3GHz) and PVT variations. The achieved results are impressive: the effect of 30mVpp supply noise is completely removed and the PLL performances are equivalent to those with a clean supply.

Finally Paper 5.7 (Intel) presents a host-clock generator in 32nm CMOS. Several techniques are used to keep the design flexible, portable and process insensitive. Furthermore the main PLL parameters are automatically programmed according to the input/output frequency change to maintain unconditional loop stability. This is vital for Host-clock generators since the frequency working range is wide: 300MHz to 1.5GHz in this paper. The prototype is realized in 32nm CMOS. The current draw varies from 0.4 to 1.15mA, properly tracking the output frequency, from a 1V supply.

Session 6 Overview / IMMD

Sensors and Energy Harvesting

Session Chair: *Aaron Partridge, SiTime, Sunnyvale CA*
Session Co-Chair: *Christoph Hagleitner, IBM Research, Ruschlikon, Switzerland*

Sensors and energy harvesting are growing in importance, as many applications require environmental inputs and often must be placed in remote or inaccessible locations. Advanced MEMS sensors require highly precise interface circuitry that must usually transduce small or delicate signals and mitigate sensor limits, while in some cases the signals are large and must be isolated. When sensor systems function in inaccessible environments it can be difficult to power them. In these cases it is often advantageous to scavenge or harvest power from the system's immediate environments.

Paper 6.1 [STMicroelectronics; U Padova] presents a 3-axis gyroscope drive and transduction circuit. A 3.2×3.2mm2 3-axis 24µm-thick polysilicon surface micromachined gyro combining 3 tuning forks in a single vibrating element is sensed by a 0.13µm HCMOS multiplexed digital readout, achieving a 0.03dps/√Hz rate noise density, a ±0.04dps/°C ZRO and ±2% cross-axis sensitivities.

Paper 6.2 [Delft U] presents a low-power thermal wind speed and direction sensor. A 2-D thermal wind sensor is realized in a standard CMOS process. Two 2nd-order thermal ΔΣ modulators control and digitize the flow-dependent heat distribution in the sensor. The sensor measures wind speed and direction with errors of less than ±4% and ±2°, respectively. It dissipates only 50mW, 9× less than a previous CMOS design and less than that of MEMS-based wind sensors.

Paper 6.3 [U Freiburg; IMTEK] presents a telemetric stress sensor for orthodontic brackets. A CMOS stress-mapping system with 24 sensors is sensitive to in-plane shear stress or differences of normal stresses with a resolution better than 25kPa. The telemetrically powered system consisting of a chip and microcoil communicates at 13.56MHz. Its dimensions of 2×2.5mm² permit the development of smart brackets for a direct force feedback in orthodontic treatments.

Paper 6.4 [Delft U] presents a precision bridge transducer and ADC. The paper presents a 21b read-out IC (ROIC) with ±40mV full scale for precision bridge transducers and thermocouples. The ROIC employs dynamic element matching to achieve an INL of 5ppm and a gain drift of 1.2ppm/°C, multistage chopping to achieve a 1mHz 1/f noise corner at 16.2nV/√Hz, and nested chopping to achieve 200nV offset, while drawing only 270µA from a 5V supply.

Paper 6.5 [CEA-LETI – MINATEC; Schneider Electric] presents a shunt current sensor with integrated transformer signal coupling. An integrated current sensor including a shunt, 2 micro-transformers for 6 kV isolation, a chopper IC and a readout IC is presented. Current measurements are performed with a ±1.5 % nonlinearity over a 0.1-to-100A range. The signal BW ranges from DC to 20kHz, and the overall power consumption is 16mW. The microsystem fits into a 13×7.6mm2 SO20 package.

Paper 6.6 [Caeleste] presents a small and sensitive imaging X-ray sensor containing A 16×16 pixel X-ray photon-counting array for indirect detection, i.e. in combination with a scintillator. To count charge packets smaller than 100 electrons it has a noise floor and a comparator threshold of about 15 e-rms. Counting happens in a nonlinear fashion in the analog domain, yielding pixels with 27-to-40 transistors.

Paper 6.7 [U Idaho; National U Singapore] presents an implantable retinal image sensor that is powered by the light falling on the imaging array. A CMOS energy-harvesting and imaging (EHI) APS imager capable of 7.4fps video capture and 3.5µW power generation is designed, fabricated, and tested in 0.5µm CMOS. It has a 54×50 array of 21µm2 EHI pixels, a 10b supply-boosted SAR-ADC and charge-pump circuits consuming only 14.25µW from 1.2V resulting in the lowest power imager with 1.32pW/frame.pixel.

Paper 6.8 [imec - Holst Centre; Philips Research Laboratories] presents a circuit to convert optical power over a wide brightness range to readily usable voltage. A fully autonomous inductive boost converter for indoor photovoltaic harvesting with maximum power point tracking circuit is implemented in a commercial 0.25µm CMOS process. The converter can handle input power from 5µW up to 10mW and charge a battery or a super-capacitor up to 5V. Its control circuit consumes between 0.8 and 2.1µA depending on the input power level, resulting in a peak end-to-end efficiency of 70% when tracking a maximum input power of 17µW.

Paper 6.9 [U Michigan] presents a transduction circuit for a MEMS energy harvester that converts vibration to usable circuit power. A self-supplied energy harvester platform is developed including a MEMS harvester integrated with a power management IC, for autonomous charging of an energy reservoir. The volume of the system is <0.3cm3, and it can charge a reservoir from 0 to 1.25V in <15min under 0.3g vibration input at 69Hz.

Session 7 Overview / Energy-Efficient Digital *Multimedia and Mobile*

Session Chair: *Pascal Urard, STMicroelectronics, Crolles, France*
Session Co-Chair: *Michael Phan, Qualcomm, Raleigh, NC*

Since the release of the Avatar movie, 3DTV has become a primary focus for the multimedia industry, in order to deliver the most realistic 3D experience. This technology will soon reach your home, and then your mobile devices. Additionally, augmented reality blurs the line between what is real and what is computer-generated by enhancing what we see, creating a plethora of new applications. More embedded intelligence, more processing capability and always-improving energy efficiency are the main driving forces for these innovative products.

Paper 7.1 [NTU] demonstrates a state-of-the-art design for 3DTV decoding solutions, in H.264 format. It targets applications such as Quad Full HD, stereoscopic 3DTV, Multi-viewer stereoscopic 3DTV and Virtual Reality. This design is composed of an MVC decoder and a free-viewpoint engine able to synthesize multiple points of view. It is able to perform Quad Full HD (QFHD) / 2160p at 216fps consuming only 69.5mW at 240MHz under 0.9V supply and is realized in 40nm CMOS in 5.76mm^2.

Next we explore what could be the near-future H.265/HEVC video standard with Paper 7.2 [MIT]. This paper presents Context-Based Adaptive Binary Arithmetic Coding (CABAC), which addresses a key bottleneck in video-coding standards. The proposed coding scheme enables parallelization at the algorithmic level. In this 65nm CMOS chip, the decoder takes full advantage of this innovation and implements an easily scalable 5×16 parallel architecture that achieves QFHD/2160p decoding at 186fps while consuming only 77mW with a clock frequency of 125.5MHz under a 1.0V supply.

A heterogeneous multimedia processor for 3D graphics, image processing, and augmented reality integrated with a reconfigurable transceiver pool is discussed in Paper 7.3 [KAIST]. This 0.13µm CMOS multimedia solution is implemented in IC-stacking on SI-interposer. It embeds a configurable vector-processing unit for frame-level parallelism, a unified filtering unit with a memory-access-efficient texturing algorithm and a programmable shader integrating multiple cores, which achieves a throughput of 1.6Gpixels/s and 25Mpolygons/s, and consuming 275mW at 1.2V.

Paper 7.4 [KAIST] presents the first portable embedded neuro-fuzzy accelerator for object recognition and an intelligent reconfigurable integrated system, which realizes low power consumption and high-speed recognition, prediction and optimization for artificial intelligence applications. This analog/digital mixed-mode processor is realized in 0.13µm CMOS and achieves 57mW power consumption at 1.0V for the analog part and 1.2V for the digital part, leading to a power efficiency of 655GOPS/W in 13.5mm^2.

Paper 7.5 [TI] is a 28nm low-power CMOS processor based on a 4-issue, 32-register version of the TMS320C64x+ VLIW DSP. By utilizing ultra-low-voltage standard-cell libraries, SRAM with 6T bit-cells using hierarchical sensing, wordline boosting, pre-read during write techniques, and new statistical time analysis methodology. This DSP demonstrates working prototypes from 331MHz under 1.0V supply consuming 145mW, down to 14.4MHz under 0.6V consuming 5.9mW.

Paper 7.6 [ITRI] is a 49mm^2 WiMAX IEEE802.16e SoC consuming 600mW at 1.2V in 90nm CMOS. It implements a 2×2 MIMO digital baseband transmitter and receiver, and associated MAC and integrates an ARM-926, Flash memory, SDRAM controller, AES engine, and USB2.0. It also allows possible future extension to 802.16m/LTE. This WiMAX system is integrated in a dongle with relevant RF circuit and provides 5Mb/s downlink at 300km/h for mobile users in high-speed trains, and up to 30Mb/s reception in low-mobility-use cases.

The chipset solution presented in Paper 7.7 [MediaTek] is fully compliant with the IEEE 802.16e Mobile WiMAX corrigendum 1 and 2 and WiMAX forum Wave2 requirements. This chipset consists of a dual-band 2×2 MIMO RF transceiver chip and a fully integrated WiMAX modem/router chip. The RF transceiver chip is implemented in 11.05mm^2 in 65nm CMOS and has a power consumption of 364mW at 2.8V. Implemented in the same technology in 24.99mm^2, the modem/router chip targeting portable routers has a power consumption of 632.7mW at 1.3V. The total chipset reports a margin of up to 7dB versus WiMAX RCT requirements. This ensures that users in the field will get high link quality service.

Paper 7.8 [UCLA] presents the first Direct Digital Synthesizer (DDS) to eliminate Phase-Accumulator (PA) pipelining, thus opening the door to dynamic frequency hopping. It uses PA rounding and gets 2's complement conditional negations via 1's complement negation with no carry ripple. The chip operates at 260MHz and reports a power consumption of 16.5mW at 1.8V as an average over typical frequency control words. This gives an FoM of 0.0635mW/MHz which is the lowest reported to date for any 16b DDS. Its outputs have a 113dB SFDR and a 98dB SNR, virtually the best possible for a 16b DDS. This chip is fabricated in 0.18μm CMOS and has an area of 0.16mm^2.

Session 8 Overview / Wireline

Architectures and Circuits for Next Generation Wireline Transceivers

Session Chair: *Daniel Friedman, IBM T.J. Watson Research Center, Yorktown Heights, NY*
Session Co-Chair: *Koichi Yamaguchi, NEC, Sagamihara, Japan*

Meeting the challenges for next generation communication systems demands a combination of circuit and architecture innovation. Circuit innovation, by extending the performance achievable using CMOS technologies, yields increasingly flexible standard-compliant designs, allows data rates to be pushed to new levels, and enables the creation of new ways to mitigate deep submicron technology constraints. Architecture innovation will have longer-term impact in areas ranging from addressing serial link power challenges to creating entirely new serial link application spaces.

This session includes 8 papers that extend serial link state-of-the-art through both circuit and architecture avenues. It starts with the presentation of new approaches for increasing flexibility and then for improving echo-cancellation performance in the context of standard-compliant I/O. Various approaches to enable increases in data rates follow, driving not only toward 100GbE and 40Gb/s serial link solutions, but even to 12.5Gb/s full duplex data transmission over a plastic waveguide. The final papers in the session describe new architectures for power efficient link design, for achieving ultra-fast burst-mode CDR lock, and new ways to achieve target transmitter output swing using advanced-node thin-oxide devices.

Paper 8.1 (Broadcom) describes a SONET transceiver capable of supporting the NRZ and RZ data formats deployed in optical networks. To achieve this goal, a new transmitter architecture and a new receiver threshold adjustment circuit are introduced and integrated into a 65nm CMOS transceiver demonstrated at 11.3Gb/s, achieving 17ps TX rise/fall times and $5mV_{pp\text{-}diff}$ RX sensitivity with 0.54UI jitter tolerance. The transceiver consumes 214mW from a 1.0V supply.

An approach to achieving echo cancellation in a 10GBase-T transmitter that relaxes DAC linearity requirements is introduced in Paper 8.2 (Teranetics). Through the use of echo-cancelling DAC elements matched to transmit DAC elements, along with DSP-based control the transmitter achieves a residual linear echo <-30dBc and residual transmitter distortion <-65dBc. These results are demonstrated over a bandwidth of 1 to 400MHz with the transmitter driving a 50Ω load with $2V_{pp}$ output swing while consuming 250mW.

The state-of-the-art for high data-rate CMOS equalizing serial link designs is extended in Paper 8.3 (National Taiwan University), presenting a transmitter plus receiver chip set operating at 40Gb/s. In this work, a multi-tap FIR filter realized using an LC-based delay line is presented as an alternative to latch-based equalizer implementations. This approach is applied to both the transmitter and the receiver, and the resulting chip set is demonstrated with BER<10^{-12} over a channel with 19dB loss at 20GHz while consuming 457mW (135mW in TX from a 1.2V supply and 322mW in RX from a 1.6V supply).

Paper 8.4 (Hitachi) describes a gearbox LSI, a critical element of future 100Gb/s Ethernet systems. This 65nm CMOS design achieves its high performance while only consuming 2W from 1.0V and 1.8V supplies. A key power-reduction strategy is circuit architecture changes that enable the replacement of current-mode circuits with static CMOS circuits. The 25Gb/s interface in the LSI achieves a BER<10^{-12} with 34.3mV input sensitivity.

In Paper 8.5 (Sony), millimeter-wave wireless techniques are used to enable bidirectional 12.5Gb/s+12.5Gb/s communication over a plastic waveguide. This 40nm CMOS design, which suggests a path to achieve some of the benefits of optical links without requiring electrical-optical or optical-electrical conversion, uses 57GHz and 80GHz carrier frequencies and is demonstrated to operate over a 120mm waveguide at a BER of 10^{-12} while consuming 143mW from a 1.1V supply.

A charge-recycling approach to serial link transceiver design is presented in Paper 8.6 (Oregon State University). This 90nm CMOS design operates from 0.5 to 4Gb/s and uses stacked digital transmitter and receiver clock generators as a key technique to reduce power consumption; at 3.2Gb/s its power efficiency is 1.9mW/Gb/s with a BER<10^{-12} .

Paper 8.7 (University of Toronto) introduces a new phase interpolator-based approach for implementing a burst-mode CDR. The technique is demonstrated in a 65nm CMOS test chip, achieving lock in less than 1 UI for data rates between 1 and 6Gb/s while consuming 22mW from a 1.2V supply.

Finally, Paper 8.8 (IBM) describes techniques enabling the realization of a high-swing high-data-rate source series terminated transmitter using thin-oxide devices in a 45nm CMOS SOI technology. The 4-tap FFE transmitter achieves >1.28V_{pp} output swing at 14Gb/s while consuming 85.5mW from a dual supply (a main supply of 1V and an output driver supply of 2V).

This session presents work ranging from extending current state-of-the-art serial link designs to demonstrating possibilities for future link data-rate increases to proposing entirely new ways to consider serial-link implementation. The advances reported here will be crucial to increasing the capabilities of next-generation high-performance systems and to enabling serial link introduction into new application spaces.

Session 9 Overview / Wireless

Wireless and mm-Wave Connectivity

Session Chair: *Gangadhar Burra, Texas Instruments, Dallas, TX*
Session Co-Chair: *Yorgos Palaskas, Intel, Hillsboro, OR*

High-throughput and low power continue to demand advances in CMOS wireless technologies for connectivity in various applications. The papers in this session show these developments in the area of mm-Wave 60GHz-and-up systems, as well as conventional connectivity platforms such as WLAN, Bluetooth and mobile TV. The over-arching trends at 60GHz are phased-arrays for wider range, integrated antennas and low power to target mobile applications. Traditional connectivity technologies show higher levels of integration, digital-centric architecture implementations and overall innovative ideas for system cost reduction.

Paper 9.1 from the Tokyo Institute of Technology discusses a 60GHz transceiver compliant with the IEEE802.15.3c standard. The receiver shows a measured NF of <6.8dB and the transmitter PA efficiency is 8.8%. The 65nm CMOS transceiver with in-package antenna achieves 3.5Gb/s up to a distance of 2.7m and consumes 186mW in transmit and 106mW in receive modes respectively.

Paper 9.2 from CEA-LETI and STMicroelectronics discusses a fully integrated 60GHz transceiver also in 65nm CMOS. The transmitter with an external in-module PA achieves a P_{sat} of greater than 16dBm. The transceiver has a throughput rate of 3.8Gb/s at up to 1 meter with WirelessHD-compliant EVM parameters. This is obtained with a single in-module 5dBi antenna built on an HTCC substrate manufactured in an industrial packaging line.

The first beam-forming 60GHz transceiver compliant with both WirelessHD and draft IEEE 802.11ad standards is described in Paper 9.3 from SiBeam. This implementation contains up to 32 elements with antennas integrated in a ceramic package and achieves 3.8Gb/s at a non-line of sight range of 10 meters. The 65nm digital CMOS transceiver is capable of dynamic beam-steering in the presence of line-of-sight obstructions. Tradeoffs between rate, range, and power consumption are described.

Integrating multiple elements of a 60GHz phased-array radio requires careful optimization of power dissipation per element. Paper 9.4 from UC Berkeley discusses techniques that address achieving a low per-element power consumption of 34mW, including LO generation and distribution. The paper describes a stacked mixer/phase rotator and zero-voltage switching PA that improve transmitter efficiency. The techniques are demonstrated on a 65nm CMOS, phased-array transceiver with integrated PLL and 4-element receiver and transmitter.

Due to the high data rates involved in multi-Gb/s mm-Wave systems, digital baseband processing can also consume significant power. To overcome this issue, Paper 9.5 from National Taiwan University revisits an older analog technique, the Costas loop, to perform synchronization and demodulation in an 87GHz QPSK system. The 65nm CMOS chipset is combined with a low-cost waveguide adaptor that can directly drive a horn antenna for a point-to-point 3.5Gb/s link.

Wireless LAN SoC innovation is addressed in this session with a presentation of a 3x3 MIMO SoC in Paper 9.6 by Atheros. Architecture techniques associated with enhanced I/Q mismatch correction as well as phase-noise impact reduction are discussed. Both high (5GHz) and low (2.4GHz) band results with an integrated power amplifier show an output power of 25dBm and over-the-air throughput of >300Mb/s. The 65nm CMOS chip occupies 22m^2 and achieves an EVM floor of -39dB/-36dB at 2.4/5GHz.

Paper 9.7 from the University of Macau and Instituto Superior Tecnico, Lisbon, describes a multiband TV tuner covering the VHF-III, UHF and L bands for mobile applications. The paper addresses the reduction of the overall system cost by creating a single front-end for all bands without an external balun and describes techniques that achieve a 4dB noise figure and a +32dBm IIP2 across all bands. Implemented in 65nm CMOS, the device consumes 55mW and occupies an area of 0.46mm^2.

The next two papers discuss digital-intensive techniques for implementing transmitters and receivers respectively in scaled CMOS processes. Paper 9.8 from Toshiba Semiconductor describes an 8-DPSK Polar transmitter for Bluetooth EDR. The phase path uses a digital PLL with correction of the inherent DCO nonlinearity. The amplitude is introduced by a digital PA with constant output impedance for good linearity. The 0.56mm^2, 65nm CMOS chip delivers 0dBm output power while dissipating 42mW.

Recently VCO-based ADCs have been proposed for easy scalability and porting to future CMOS nodes. Paper 9.9 from KAIST presents a 0.2-to-1.8GHz receiver using a VCO-based ADC. The design takes advantage of the inherent integration of a VCO to implement a 2nd order $Sinc^2$ anti-aliasing filter for better interference rejection. The 90nm CMOS IC achieves -94dBm sensitivity over a 1MHz bandwidth, with 50dB rejection of aliased signals due to the $Sinc^2$ filter.

60GHz systems are moving to productization of high definition video over the air and other throughput-intensive wireless applications. New low-power and phased-array technologies are making 60GHz more feasible for mobile applications. In the interim, traditional connectivity technologies continue to optimize system performance and cost via innovative digital and RF architectures.

Session 10 Overview / Data Converters

Nyquist-Rate Converters

Session Chair: *Michael Flynn, University of Michigan, Ann Arbor, MI*
Session Co-Chair: *Michael Perrott, SiTime, Sunnyvale, CA*

The demands placed on high-speed communication are steadily increasing as services such as cloud computing, video-on-demand, and ever increasing web access, call for higher date rates with dramatically improved energy efficiency. In particular, optical network data rates are now approaching 100Gb/s, wireless cellular base stations are processing wide-spectrum content for multi-standard support, and cable modems and medical-imaging systems are striving to achieve GHz bandwidths. In response to these challenges, new analog-to-digital converter (ADC) and digital-to-analog converter (DAC) architectures are being developed that dramatically increase conversion rates and conversion efficiency by leveraging advanced CMOS, SiGe technology, and clever circuit techniques.

Paper 10.1 from NXP Semiconductors presents a very high speed ADC that leverages 65nm CMOS and an interleaving technique to achieve 2.6GS/s operation. To achieve such a high speed, an on-chip clock generator feeds 4 interleaved track-and-holds operating at 650MHz, which in turn feed 16 SAR stages for a total of 64-times interleaving. By also utilizing on-chip gain, offset, and DAC linearity calibrations, an SNDR of 48.5dB is achieved at the Nyquist frequency of 1.3GHz while consuming only 0.48W of power. This combination of speed and precision enables simultaneous capture of many channels in the 48 to 1002MHz TV band while offering a cost and power effective implementation since only one ADC is required.

Paper 10.2 from Texas Instruments focuses on improving resolution while still achieving 1GS/s operation through the use of 2-way interleaving within a SiGe BiCMOS technology. To achieve a peak SNR of 62dB and SFDR>67dB, DACs are included to address timing skew and bandwidth mismatch between the interleaved stages. By sharing most of the circuits between the interleaved pipeline stages, matching is improved between the stages and a power consumption of 575mW is achieved. Potential applications include high performance cable modems and signal processing approaches to power amplifier linearization.

Paper 10.3 from Broadcom focuses on reduced power consumption at 800MS/s conversion rate while still maintaining SNDR levels of 59dB. To achieve this high speed sample rate, 4-way interleaving is utilized with pipeline stages that are implemented in 40nm CMOS. To counter the reduced intrinsic gain offered by this process, a dual-residue technique is employed which leverages matching between pairs of open loop gain stages to remove the need for accurate gain such that only offset is the key concern for each pipeline stage. A fast background offset calibration algorithm takes care of this issue, and the overall ADC consumes 105mW.

Paper 10.4 from Analog Devices introduces a pipeline architecture that achieves a high resolution of 77dB SNDR at 80MS/s sample rates and an input frequency of 10MHz while also consuming only 100 mW in 0.18µm CMOS. Key circuit techniques include a dynamically driven deep N-well input sampling switch, an offset-cancelled comparator, and a back-gate- voltage biased amplifier. The resolution and bandwidth offered by this ADC opens the door to multi-standard wireless receivers that can be easily accommodate a wide range of data rates and modulation standard.

Paper 10.5 from the University of Macau focuses on the issue of power efficiency and low area by leveraging a resistor ladder to provide sub-ranging reference levels within a SAR architecture such that 2-bit conversion is achieved per conversion cycle. This approach allows 400MS/s conversion rates to be achieved without interleaving, and an SNDR>40dB with only 4mW of power consumption. Implemented in 65nm CMOS technology, the ADC occupies an area of 0.024mm^2. By achieving such low power and area with high sample rates, this ADC structure opens the door to new opportunities in mobile communication.

Paper 10.6 from MIT presents a reconfigurable 5 to 10bit SAR ADC, implemented in 65nm CMOS, with power consumption that is linear related to sampling speed. A reconfigurable DAC architecture and voltage scaling down to 0.4V maintain energy efficiency at low resolutions. The DAC power scales exponentially with resolution and voltage scaling further reduces the energy-per-conversion. Applications, such as sensor networks and medical monitoring, benefit from ADCs that can digitize with varying bandwidths and resolutions.

Finally, a pair of presentations advances the state-of-the-art in high performance CMOS current-steering digital to analog converters (DACs). As the first of these papers, Paper 10.7 from National Chiao Tung University describes a 1.2GS/s 12bit DAC, implemented in

90nm CMOS, that achieves SFDR greater that 70dB up to 500MHz. A digital random return-to-zero technique enhances dynamic performance. Background calibration ensures matching of compact current cells. The device consumes 128mW and occupies an active area of 0.83mm^2.

Paper 10.8 from Ciena presents a 56GS/s 6bit DAC that achieves a new record for DAC performance. A compact design facilitates very high speed clocking and data distribution. At 56GS/s the DAC achieves SFDR greater than 30dBc and ENOB greater than 4.3b up to an output frequency of 26.9GHz. In test pattern generation mode and running at 56GS/s power is less than 750mW. This very high speed DAC, implemented in 65nm CMOS, helps enable 100Gbps optical data communication.

The advancements provided by these ADC and DAC techniques will provide further fuel to the steady trend of using sophisticated signal processing to make better of use bandwidth to enable increasing data rates with better energy efficiency in next generation communication systems.

Session 11 Overview / Memory
Non-Volatile Memory Solutions

Session Chair: *Frankie Roohparvar, Micron Technology, San Jose, CA*
Session Co-Chair: *Sungdae Choi, Hynix Semiconductor, Icheon, Korea*

The question on everyone's mind is: "When is the NAND party over?" As other emerging technologies chase the leader with the advantages they bring to bear, beating the cost of NAND is very difficult. The hope for these technologies is that NAND would eventually run into a wall. However, NAND engineers manage to keep moving ahead and getting around barriers that laws of physics erect for them. There are always people proclaiming that the end of NAND is just around the corner, but that corner seems like a mirage. In the meanwhile, the emerging memories are not sitting idle either. They are making very good progress and are finding areas of opportunities where their technical advantages over NAND allow them be adopted in some applications. This year has a very exciting series of papers that showcase the progress that both NAND and emerging memories are making.

As NAND scaling issues are getting more and more difficult, the solution is moving towards a managed memory solution paradigm. One can think of a floating gate on NAND as a holding cell to capture and imprison electrons. Due to cost cutting measures everywhere, these prisons are also getting smaller and smaller; and these electrons are very good escape artists. We are getting to the point where we may have to give each individual electron a name tag and keep track of them individually since they hold our data. Use of more sophisticated controller technology as a part of non-volatile memory solutions is akin to making higher security prison systems. More and more sophisticated controllers are utilized to help with the issues that NAND is facing with process migration. These solutions are incorporated on the memory controllers that accompany the NAND devices and help the overall system provide acceptable storage solutions.

In this year's session, there are a series of exciting papers describing the progress being made in all these fronts. The session reports on eight papers ranging from the most advanced technology node for NAND to the smallest reported die size for NAND as well as the type of work being done on controllers to help with the NAND management. On the emerging memory side, there are papers on RRAM and conductive-bridge resistive memories as well as FeRAM. The session also has a short paper describing a very innovative low-current sense-amplifier circuit that is a key element in being able to detect the state of nonvolatile memories as their current is reduced.

Paper 11.1 reports on a 64Gb MLC NAND device with 14MB/s programming and 266MB/s data transfer fabricated in 24nm. This chip is the smallest die size reported to date for this density at 151mm^2 using a dual-plane architecture. A newly introduced two-program algorithm related to bitline precharging during a program operation is introduced that improves the program throughput of the device by 5% and reduces program operation current by 6%.

Paper 11.2 describes a 4Mb embedded SLC Resistive RAM that implements a 1T1R cell consisting of a NMOS selector and a HfO_2-based bipolar resistive memory element. This device features a 7.2ns read-write random-access time and 2bit-per-cell capability featuring 160ns write-verify operation. The high performance is achieved using a parallel-series reference-cell scheme and a process- and temperature-aware dynamic-bitline-bias circuit.

Paper 11.3 reports on a 32Gb MLC NAND Flash memory in 26nm technology. This device uses an innovative approach of applying negative voltage to the wordline of the NAND device as well as a new bit line compensation scheme to make the V_{th} distribution narrower. These allow for a larger V_{th} margin window that NAND cells can be programmed in, hence generating better reliability and performance.

Paper 11.4 describes techniques used by a solid-state drive (SSD) controller to improve the BER of Flash by 95% as well as reduce the power consumption by 43%. The controller algorithm uses an asymmetric coding scheme to reduce the population of high V_{th} states, resulting in an improvement of BER and a Stripe Pattern Elimination Algorithm avoiding the worst case writing pattern to achieve program current reduction

Paper 11.5 reports a sense amplifier that can detect a very low current of sub 100nA. The circuit described uses a very innovative technique of offset-tolerant current sampling. Compared to previous sense amplifiers, this circuit achieves seven times faster access time which is demonstrated on a 90nm OTP macro.

Paper 11.6 describes a 1Mb low-voltage FeRAM in 0.13µm with 1024 1T1C cells per bitline This device features a time-to-digital sensing scheme for expanded operating margin addressing the challenges of sensing small charge operating in low-voltage regime.

Paper 11.7 reports a 4Mb conductive-bridge resistive memory in 0.18µm CMOS. A folded BL cell array and direct sense in programming using common sense amplifier enable 2.3GB/s read and 216MB/s program. Using a planned 64B program size and 2 verify cycles, the device achieves a program throughput of over 1GB/s.

Paper 11.8 introduces a 64Gb in 20nm TLC Flash Memory for both high density and high speed I/O. A proposed 2-step verify ISPP scheme and fail-page copy-back program function enhance the program performance. The data are transferred to the page buffer through 200Mb/s DDR Interface. This device is the smallest geometry reported to date.

The lineup of papers this year is a testament to the ingenuity of the engineering community working on these technologies. At some point in the future of NAND, we have to face the fact that there is a wall out there; however, one can take comfort in the fact that these clever engineers keep finding ways not to crash into it.

Session 12 Overview / Technology Directions

Design in Emerging Technologies

Session Chair: *Azeez Bhavnagarwala, Advanced Micro Devices, Boston MA*
Session Co-Chair: *Tadahiro Kuroda, Keio University, Yokohama, Japan*

New advances in designing in emerging technologies of energy harvesting, smart power grid, silicon photonics, terahertz imaging and power management are reported in this session.

Harvesting energy from the environment by using thermoelectric generators or photovoltaic cells provides a solution for battery-free sensor networks or electronic healthcare systems. The power-management circuit converting harvested energy to practical supply voltage is in focus and one of the main challenges is the extremely low voltage that the energy harvesting generators can provide. The session begins with paper 12.1 from the University of Tokyo on a sub-100mV startup voltage step-up converter to a 0.9V output with 72% conversion efficiency without any external clock or mechanical assist in 65nm CMOS.

A smart meter is an enabling technology for realizing the smart grid. In order to further reduce the energy loss in the power grid rather than simply replacing conventional power meters with smart meters, an extremely fine-grain power monitoring system is desirable. However, this requires an enormous number of low-cost power meters. Printable organic devices on flexible films have great potential to realize low-cost power meters. In Paper 12.2, also from the University of Tokyo, a low-cost 100V AC power meter based on system-on-a-film (SoF) concept is demonstrated.

While energy management systems in homes or buildings may offer monitoring, reporting, and controlling of energy usage, these functions simply track intermittently the energy consumption and operational states of appliances and equipment. Further, since their sensing devices are not small, they cannot be attached to every appliance or piece of equipment. Paper 12.3 from NEC reports a battery-free realtime current waveform sensor in 90nm CMOS. It is small enough to be attached to any piece of equipment for continuously power consumption monitoring. Its key features are plug-less energy-harvesting (EH) from AC power lines, real-time sensing and transmitting. A half cycle time-to-digital convertor (TDC) is used to detect detailed information on current waveforms with the precise time-resolution and asymmetrical power consumption to help achieve high power RF transmission with only a limited EH power supply. It successfully demonstrates transmission of sensed current waveform information from several appliances such as a hair dryer, a TV, and a notebook PC.

The emerging field of silicon photonics targets monolithic integration of optical components in the CMOS process, potentially enabling high bandwidth, high density interconnects with dramatically reduced cost and power dissipation. Paper 12.4 from the IBM TJ Watson Research Center reports a monolithic 4×4 silicon photonic router with a custom 90nm bulk CMOS driver, routing 3×40Gb/s WDM data with a BER $<10^{-12}$, less than -10dB cross-talk and 7dB loss.

The spatial resolution of micro-wave and millimeter-wave imaging systems can be improved by increasing their operating frequencies into the submillimeter-wave range (300GHz to 3THz). Electronic terahertz sources and receivers are presently dominated by III-V semiconductor and waveguide packaging technologies. In Paper 12.5, a 0.25µm BiCMOS process with an upgraded SiGe HBT device technology is used to demonstrate an 820GHz TX/RX chipset for active terahertz imaging applications.

Standby power from household electric appliances driven by AC power such as TVs is lost at an AC-DC converter even when the appliances are turned off. Although an infrared remote controller is usually used in these appliances, no wake-up circuit has been reported for the infrared remote controller. Paper 12.6 proposes a receiver SoC in 0.13µm CMOS with wake-up function for the infrared remote controller.

Programmable devices such as SRAM-based FPGAs have the major challenges of power consumption and circuit area due to the excessive standby leakage current and a large footprint memory cell. In Paper 12.7 a programmable cell array and a 32×32 crossbar switch using a nonvolatile and rewritable solid-electrolyte switch (NanoBridge) on a 90nm CMOS platform is reported. A 72% reduction in chip-area compared with that of a standard-cell-based design is also achieved.

Wafer-level testing detects manufacturing problems and removes non-functional devices early in the fabrication process. It is performed by placing a probe card directly above a device under test (DUT) and establishing a mechanical contact between them with an array of probes.

This is an invasive technique that may cause damage to fragile low-k dielectric layers and deformation of pads or bumps. One solution is wireless probing. With a number of proposed techniques for establishing high-speed inductive-coupling data links and measuring DC analog signal wirelessly, the primary obstacle to non-contact wafer-level testing is supplying power to the DUT. Paper 12.8 proposes an inductive power transfer system in 0.18μm CMOS, capable of delivering up to 6W of DC power to the on-chip load.

GHz-range applications that operate in a variety of signal situations and/or multiple standards require highly programmable responses that cannot be provided by analog circuits. Paper 12.9 enables a five-orders-of-magnitude improvement in frequency capability compared to earlier work, using 65nm CMOS, making continuous time DSP a candidate for wideband GHz low-dynamic range applications, such as those found in pulse radio, spectrum sensing, and channel equalization.

Session 13 Overview / Analog
Analog Techniques

Session Chair: *Jafar Savoj, Xilinx, San Jose, CA*
Session Co-Chair: *Kimmo Koli, ST-Ericsson, Turku, Finland*

Design of state-of-the-art analog circuits for energy-efficient power delivery and high-performance amplification pose significant challenges in modern electronic systems. Advances with LED drivers have enabled a new frontier for energy efficient lighting technology. Progress in audio amplifier design has resulted in longer battery life for mobile devices and has affected our daily life with prolonged delivery of entertainment and information. Operational and instrumentation amplifiers have made interfacing of our real analog world to digital processing systems possible.

This session starts with description of two LED drivers as high brightness and high efficiency of LED devices begin a new era for lighting and LCD backlight technology and demonstrate superior performance in comparison to incandescent lamps. With projected growth of LED technology, design of high efficient drivers is an essential ingredient of green systems.

Paper 13.1 (Fairchild Semiconductor) describes a simple 3-pins buck-type LED driver with intelligent power factor correction function using digital control algorithm. The LED lamp driver is based on a peak- current-controlled PWM method. The proposed controller utilizes a sine-wave reference signal, in phase with AC line voltage, and synchronizes the LED current phase accordingly. The circuit achieves power factors of 0.98 and 0.92 and the THD of 18% and 16% at $110V_{ac}$ and $220V_{ac}$ with 5W LED load, respectively.

Paper 13.2 (Oregon State University) describes a 1.2A Buck-Boost LED driver, fabricated in a 0.5□m CMOS process, which regulates the LED current without any series current source or series sense resistor. The circuit employs a highly accurate current sensing scheme to directly regulate LED current and achieve more than 13% efficiency improvement. The LED driver operates at switching frequencies up to 2MHz with an off-chip 2.2μH inductor and a 10μF capacitor. The converter can drive the full load at an LED forward voltage of 3.6V. The proposed error-averaged current sensing technique achieves better than 2.8% of sensing accuracy.

High power efficiency, small size and reduced heat dissipation are highly desirable in battery-powered mobile systems and switched-mode Class-D amplifiers can readily satisfy these requirements. A full adoption of class-D technology in mobile systems has been limited due to limitations on signal distortion and noise, poor power supply noise rejection, electromagnetic interference (EMI) and the requirements for external LC filters. Paper 13.3 (Dialog Semiconductor) demonstrates a filter-less class-D audio amplifier with uniform pulse-width modulation architecture that achieves 0.0012% THD plus noise, delivering 1.2W into an 8Ω load with 93% power efficiency and 96dB of PSRR. The amplifier is fabricated in standard CMOS process and packaged in WLCSP with total chip area of $1.44mm^2$. It achieves 103dB SNR with quiescent current consumption of 4mA and maximum output power of 3.1W to loads as small as 4Ω. The circuit operates with a supply voltage ranging from 2.5V up to 5.5V.

Many operational amplifiers utilizing chopping techniques successfully reduce offset and low frequency drift, yet suffer from unwanted modulated output ripples. Analog techniques target unconditional stable chopper operation with the smallest input noise PSD.

Paper 13.4 (Analog Devices) reports a 5.9nV/√Hz unconditionally stable chopper operational amplifier with 1.47mA current at 2.5-5.5V supply voltages and $1.26mm^2$ die area, achieved by phase compensation using current attenuation. In addition, adaptive clock level shift and backgate biasing for the input chopping allows optimization for noise and offset, realizing 0.78μV maximum offset with a worst-case 28.3nV/C drift. The circuit is fabricated in 0.35μm CMOS.

Introduction of a gain error reduction loop suppresses modulated output ripples of a chopping amplifier and improves gain accuracy, gain drift, and linearity of current-feedback instrumentation amplifiers without resorting to trimming techniques. As described in Paper 13.5 (TU Delft), the gain error reduction loop continuously cancels the gain error of the amplifier and achieves gain error as low as 0.06%. This result represents a 4× improvement in power efficiency compared to the prior art. The circuit consumes 290μA from a 5V supply.

Many sensors demand energy-efficient precision voltage sensing interface with low noise performance at very low frequencies. Paper 13.6 (Robert Bosch) describes a digital sensor interface that minimizes noise folding with boxcar sampling and stabilizes the overall

interface gain with global feedback. The combination of nested chopping and auto-zeroing allows the interface to thoroughly reject low-frequency noise. The circuit is fabricated in a 0.35□m CMOS process and achieves a noise floor of 6.7nV/√Hz down to 0.1mHz while dissipating 6.6mW. The circuit draws only 2mA from a 3.3V supply.

High-voltage operational amplifiers are also used in signal conditioning circuits for industrial applications to ensure compatibility with legacy equipment. In such applications, good DC precision, low offset, offset drift and noise are essential requirements. Paper 13.7 (Texas Instruments) describes a 36V JFET-input bipolar operational amplifier with a maximum offset drift of 1μV/°C over a temperature range of -40 to 125°C, which represents a 3x improvement on the state-of-the-art. This is achieved with a drift-compensating circuit incorporated in the input stage that relies on a wafer-level 2-temperature laser trimming method. The amplifier has a GBW of 11MHz, a flat-band noise of 5.1nV/√Hz, a slew-rate of 20V/μs, a -126dB (0.00005%) total harmonic distortion plus noise ratio, and a quiescent current of 1.8mA. This combination of high slew rate and good noise-to-power ratio is accomplished through the use of a linearized class-AB boosting circuit in the input stage. Maximum supply voltage is 40V.

Fully differential operational amplifiers are considered a superior method of driving 100 to 500 MS/s ADCs with 12 to 16 bits of resolution. Prior art has utilized dielectrically isolated (DI) Silicon Germanium complementary bipolar processes for implementation of such blocks. Paper 13.8 (Intersil) describes the implementation of an operational amplifier using a 0.18μm SiGe NPN-only RF BiCMOS process. The circuit achieves 108dBc of IM3 at 100MHz using a feedforward nested Miller architecture. Operating from a 3.V supply voltage, the circuit delivers a $2V_{pp\text{-}diff}$ composite two tone output at 100MHz into 200 ohms. The circuit consumes only 120mW from a 3.3V supply and achieves an input noise of 0.85nV/√Hz and a 3dB bandwidth of 2.2GHz.

Session 14 Overview / Memory

High-Performance Embedded Memory

Session Chair: *Leland Chang, IBM T. J. Watson Research Center, Yorktown Heights, NY*
Session Co-Chair: *Peter Rickert, Texas Instruments, Richardson, TX*

Embedded memory plays a crucial role in today's VLSI applications – from high-performance computing to low-power consumer electronics. While scaling of technology feature size to the 32nm and 28nm nodes has enabled ever larger and higher performance on-die memories, it has also created growing challenges for the embedded memory designer. Growing device variability and power limitations are driving innovative solutions to maintain robustness and area efficiency in such aggressively scaled memories. In particular, peripheral circuit assist features have become the key to maintaining cell read and write margins to enable low voltage operation for dense SRAM caches. New strategies ranging from circuit-level techniques to fundamental changes in array architecture can also enable significant gains in area and power efficiency.

The first paper 14.1 from IBM describes peripheral circuit assist features implemented in 32nm high-k metal-gate SOI-CMOS to enable 0.7V operation of a 0.154μm^2 bit cell. A 64Mb macro demonstrates stability margin enhancement by using a regulation scheme to reduce the bitline precharge voltage level, thus limiting charge injection into the cell. Improved write margin is achieved by using a negative bitline technique with increased boost voltage as compared with previous work. A bitcell-tracking delay monitor circuit is also used to improve process-limited performance and yield.

The next paper 14.2 from IBM introduces architectural techniques to significantly improve the area, power, and performance of multi-ported register file arrays. A 144×78b macro for a 45nm SOI-CMOS 2.3GHz POWER™ processor is presented with double-pumped write ports that are operated twice in a single cycle and replicated read ports that are combined from duplicate data copies. A compact 2R1W memory cell is thus leveraged to perform a 4R2W function with near 2× area and read power reduction, low 190ps read latency, and fast error correction. The macro operates at up to 2.76GHz at a supply voltage of 0.9V.

Paper 14.3 presents the design of the 8MB level-3 cache in 32nm SOI-CMOS for AMD's next-generation Bulldozer architecture that operates above 2.4GHz at 1.1V. Area efficiency is improved by the use of a column-select aliasing technique, in which column select wires are shared between odd and even pairs for reads and writes, while leakage power is minimized by supply gating and floating bitlines. An efficient redundancy scheme is also implemented using centralized redundancy blocks instead of storing all redundant data in the data macro itself.

Finally, Paper 14.4 from MIT describes a 128kb SRAM macro featuring a 0.12μm^2 bit cell fabricated in a low-power 28nm CMOS process. A hierarchical bit-line architecture for low local bitline capacitance combined with delayed wordline boosting after a pre-read phase during write cycles improves stability and write margins to provide functionality down to 0.6V. The performance of this memory scales from 20MHz to 400MHz in the 0.6V to 1V operating voltage range while active power consumption scales from 2.8mW to 68.5mW.

The area, performance, and power of embedded memory will continue to improve well beyond the 32nm and 28nm nodes. The innovations presented in this session, including peripheral assist circuits, new architectural techniques, and low-power circuits, will drive such continued scaling into the nano-technology regime for high-performance embedded memories.

Session 15 Overview / High-Performance Digital
High-Performance SOCs and Components

Session Chair: *Shannon Morton, Icera, Bristol, UK*
Session Co-Chair: *Lew Chua-Eoan, Qualcomm, San Diego, CA*

Integration rules. Why?

Here's why. The number of transistors available on a die continues to grow in line with Moore's law. In the previous decade, designers hit a wall in terms of how to make a single core processor utilize the available transistors efficiently. So they added larger caches. When the performance advantages of these caches flat-lined, they added multiple processor cores. This trend has dominated the industry for many years. Until now. A revolutionary shift is underway.

Now, integration rules. Processors are integrating other chips and components from the system onto the processor die. This not only enables better use of the available silicon area, it also improves communication, reduces system complexity and cost, and lowers overall system power. This session presents "state of the art" high performance processors that integrate system level components, and describes those components in detail.

For many years high end microprocessors (CPU) and graphics processor (GPU) chips have competed for bragging rights on highest performance, largest complexity, and most cutting edge technology and design techniques. Now, finally, these two behemoths of the chip industry have come together, as disclosed in papers 15.1 and 15.4 from Intel and AMD.

Paper 15.1 (Intel) describes a fully integrated multi-CPU, GPU, and memory controller in 32nm technology. Known as "Sandy Bridge", the chip integrates four high performance X86 cores, an optimized graphics processing unit, DDR3 memory controllers, and a 20-lane PCIe interface. Power dissipation ranges from 95W for a high end desktop to only 17W for an optimized mobile product, employing impressive design techniques to enable low voltage operation. Additional design improvements include improved branch prediction, the addition of a micro-op cache, an advanced floating point unit, and the addition of vector extension (AVX) operation. The out-of-order cores are incorporated with a shared 8MB L3 and Ring Bus core communication topology. The design includes 6 power domains and independent PLLs per scalable domain to minimize skew.

Paper 15.4 (AMD) integrates two X86-64 "Bobcat" cores (each with a 512KB L2 cache) with a dedicated Radeon HD5000 series graphics and multimedia engine, DDR3 memory controller, client north bridge, and a 4X PCIe link. This "Zacate" SOC has over 450 million transistors and is manufactured in a 40nm technology with 10 metal layers. The design employs advanced power management techniques including separate supply rails for CPU and GPU domains, and rigorous power gating to minimize power.

Similarly, switch fabric chips are increasing in complexity, requiring more compute power and higher integration. Paper 15.2 (Renesas Electronics, University of Tsukuba) is an 80Gbps communication SOC in 45nm CMOS technology with four 4X PCIe links (instead of Infiniband 4X) and eight CPU cores for flow control, packetization, and adaptive network routing, thereby enabling highly robust communication. A direct DDR3 interface is also provided, and an internal high speed system bus enables low latency communication. The 80 Gbps communication SOC achieves 0.04 W/Gbps and can revert to a single lane with CDR disabled in low BW mode to save transmission power.

These chips integrate some of the biggest and most important components of the system, such as the CPU, GPU, memory controllers, and channel controllers, but there are other system components also on the leading edge of monolithic integration. Examples include on-die DC/DC converters and advanced encryption engines. Integrating these can save cost and enable greater security for end users.

In paper 15.3 (Harvard University), a novel approach to integrating a DC/DC converter on chip is presented. Unlike pure switched capacitance converters or buck converters requiring large external inductors, this paper describes a hybrid approach merging the best of both. An on-die inductor and a 3-level switched capacitor are merged on a monolithic die in 0.130um technology. The converter delivers up to 0.85A load current with reasonable efficiency, and can regulate output voltages from 0.4V to 1.4V given an input voltage

of 2.4V. The design offers voltage scaling across 1V within 20ns setting time within a small footprint. Overall, integrating such a DC/DC converter should provide a net cost benefit to the system.

Clock generators form the backbone of high performance SOCs, and optimizing their performance is critical to the success of such products. In paper 15.5 (University of Minnesota) a programmable adaptive phase-shifting PLL is presented that compensates for resonant supply noise by modulating the output frequency. Using such a technique, the clock phase stretches in line with the data path delay whenever a short-term supply droop event takes place. This ultimately enables a higher average case frequency or a lower operating voltage to be achieved. Improvements of up to 7.4% in maximum operating frequency were achieved for a standard pipeline on a 65nm chip.

Paper 15.6 (CEA-LETI-MINATEC) tackles an important issue that concerns us all – security. Every day you trust encryption engines to keep your personal details secure, but just how immune are they to focused attacks? This paper enlightens us on the unscrupulous methods available to would-be electronic thieves, and provides a novel mechanism for thwarting such attacks on die. Complementary data paths are implemented to maintain uniform power consumption, and the data paths are mixed to prevent targeted fault attacks from being detected. A test chip occupying 1336μm x 1411.8μm in 130nm CMOS validates that secret keys are not disclosed even after more than one million acquisitions.

The integration provided by these high speed SOCs is impressive and continues to progress following Moore's Law. The industry faces huge challenges associated with utilizing the available silicon technologies in the most efficient way possible – attaining the best energy per unit work performed. More importantly though, the higher levels of integration also enable lower overall system cost, while allowing for higher levels of functionality. The continued SOC integration trend will lead to greater overall cost savings and greater user satisfaction as we scale towards smaller geometries.

Session 16 Overview / RF

mm-Wave Design Techniques

Session Chair: *Andreia Cathelin, ST Microelectronics, Crolles, France*
Session Co-Chair: *Brian Floyd, North Carolina State University, Raleigh, NC*

The increasing capabilities of advanced silicon technologies are enabling new market opportunities at 60GHz and above. For these markets to succeed, highly integrated, low-cost and low-power-consumption solutions are required. This session includes circuit demonstrations from 5 to 300GHz for high-speed communications, radar, and imaging applications, implemented in 130- to 45nm CMOS technology. The 60GHz band offers great opportunities for high-data-rate communications for consumer wireless high-definition video streaming and ultra-fast file transfer applications.

The first part of this session focuses on 60GHz circuits, with an emphasis on low power and low phase-noise local oscillator generation. The second part of the session focuses on circuits for radar, imaging, and data communications at frequencies up to 300GHz. These papers establish new benchmarks for high-frequency data communications, imaging, and radar systems. They demonstrate the high performance and low-power capabilities of advanced CMOS technologies for 3-to-300 GHz operation.

One critical challenge for 60GHz radios is the power-efficient generation of low-phase-noise local oscillator signals. These LO signals can be generated either directly at the fundamental frequency or at a sub-harmonic and multiplied up to the mm-Wave band. Paper 16.1 (NXP Semiconductors) presents a sub-harmonic approach, where a 21.7-to-27.8GHz frequency synthesizer is realized in 45nm CMOS. Power consumption is 40mW and phase noise at 1 MHz offset is -93.4 dBc/Hz, when used with a times-two frequency multiplier.

Papers 16.2 and 16.3 present building blocks for a fundamental frequency 60GHz synthesizer. In paper 16.2 (University of Pavia), a quadrature VCO is demonstrated in 65nm CMOS, leveraging weakly coupled transformers to reduce phase noise and power consumption. The VCO operates from 56 to 60.4GHz and achieves -95 dBc/Hz phase noise at 1MHz offset. In paper 16.3 (University of Pavia), a low-power frequency divider is presented. This inductorless divider uses standard differential amplifiers clocked as dynamic latches, operates from 20 to 70GHz, and consumes 6.5 mW. Finally, paper 16.4 (University of Michigan) presents an approach to eliminate the reference oscillator for a 60GHz PLL, suitable for short-range wireless sensor networks. The 0.13 m CMOS circuit measures the standing wave on an on-chip antenna to frequency lock the oscillator to the resonant frequency of the antenna with a standard deviation of 195MHz around 59.3GHz.

Another important and growing research area is the development of sources and detectors at 70 to 300GHz for applications including data communications, radar, imaging, and spectroscopy. Paper 16.5 (Cornell University) presents a 220-to-275GHz frequency doubler implemented in 65nm CMOS that is capable of generating -6.6dBm output power while consuming 40mW of power. Paper 16.6 (Caltech) presents a distributed approach to on-chip generation, multiplication, and radiation of a 300GHz signal. A 2x2 array of these distributed active radiators is implemented in 45nm CMOS, generates 80 W of output power at 291GHz, and achieves an EIRP of -1dBm. Paper 16.7 (KU Leuven) presents a 120GHz transmitter capable of >10Gb/s data rates. The circuit integrates an LO buffer, a quadrature hybrid, a 4:1 multiplexer functioning as a phase modulator, and a six-stage driver amplifier, all in 65nm CMOS. Paper 16.8 (Toshiba) presents an 82.1-to-83.8GHz FMCW synthesizer designed for 77GHz automotive radar and implemented in 65nm CMOS. A combination of analog and digital PLL techniques is applied to achieve a 1.5GHz modulation range, 10ms modulation period, and 180kHz frequency error. Paper 16.9 (University of Southern California) presents an impulse based ultra-wideband wireless sensor for the monitoring of people's movement and vital signs. The 0.13 µm CMOS radar circuit operates over 2 to 5GHz, consumes 695mW, and achieves a range and resolution of <15m and <1cm, respectively.

Finally, paper 16.10 (UCLA) presents a 183GHz receiver for mm-Wave imaging. A regenerative architecture is employed to reduce power consumption to 13.5mW per pixel while providing time-encoded outputs of the detected radiation.

Session 17 Overview / IMMD

Biomedical and Displays

Session Chair: *Sam Kavusi, Bosch Research and Technology Center, Palo Alto, CA*
Session Co-Chair: *Young-Sun Na, LG Electronics, Seoul, Korea*

This session features recent advances in biomedical and display circuits and systems. Biomedical highlights of this session include advances in dry electrode EEGs, neural signal acquisition and stimulation systems, and implantable pressure monitors. Another highlight involves fluorescence molecular imaging and lifetime-imaging ICs.

Paper 17.1 [IMEC; Delft U] presents an EEG system that employs gel-free active electrodes and achieves 82dB CMRR and 2GΩ input impedance. A chopper-stabilized amplifier is operated at 500Hz that leads to a total input-referred noise of 0.8μVrms (0.5 to 100Hz).

Paper 17.2 [UC Berkeley] discusses an effort to reduce the area of a DC-coupled neural-signal acquisition system by 3× compared to the state of the art. The chip is implemented in 65nm CMOS and consumes 5.04μW from a 0.5V supply and achieves 49nVrms/√Hz input noise. The system has been verified with live recordings from the motor cortex of an awake rat.

Paper 17.3 [IMMS; U Ulm] describes an AC-powered transcutaneous infrared data link for implantable systems that achieves 2Mb/s data transfer and sub-nJ/b energy consumption. Charge-balanced arbitrary stimulation waveform generation in neural stimulators intended for a 1024 electrode epiretinal stimulator is the subject of Paper 17.4 [U Ulm]. The stimulator achieves 50dB DR and is suitable for a 1024-electrode system.

Continuous epi-fluorescence-based molecular imaging is demonstrated in Paper 17.5 [Stanford U]. The system consists of a monolithically integrated GaAs detector, a vertical-cavity surface-emitting laser, and a 77dB DR readout circuit chip, implemented in 0.18μm CMOS, in a 0.7g 1cm^3 package.

Paper 17.6 [U Michigan] demonstrates a 1mm^3 intraocular pressure monitor allowing optimal implantation to track glaucoma. It achieves 0.5mmHg resolution with a MEMS sensor and ΔΣ converter. The system wirelessly transmits the data consuming 4.7nJ/b and harvests solar energy to recharge its battery.

The last medical paper in the session, Paper 17.7 [Delft U], presents a 160×128 pixel array, which can detect photons with 55ps resolution. Each pixel comprises a counter, a time-to-digital converter, and a 10b memory, while a frame is read out every 20μs. The sensor is well-suited for applications such as fast fluorescence lifetime imaging.

The second part of this session showcases 3 display papers. Active-matrix OLED (AMOLED) is a promising technology for small size applications due to its self-emitting and superior display characteristics. Accurate and fast current control is essential to fully reap the benefits of AMOLED.

Paper 17.8 [Fraunhofer Institute for Photonic Microsystems] presents a bidirectional microdisplay combining a near-to-eye AMOLED display with an eye-tracking image sensor, which enables gaze-based human-display interactions. Paper 17.9 [KAIST] proposes a 0.014mm^2 9b switched-current DAC structure with 1μs/b conversion rate for AMOLED displays.

Efforts to realize area-efficient DACs for higher resolution LCD source drivers are underway. Paper 17.10 [National Tsing Hua U] proposes a 10b Resistor-Resistor-String DAC (RRDAC) that eliminates loading effects with simple current sources and achieves 30% area savings with respect to an 8b RDAC.

Session 18 Overview / Technology Directions

Organic Innovations

Session Chair: *Chris Van Hoof, imec, Leuven, Belgium*
Session Co-Chair: Masaitsu *Nakajima, Panasonic, Moriguchi, Japan*

Implementing transistors, circuits and sensors on arbitrary substrates has great potential for a wide range of low-cost electronic products such as flexible displays, disposable biochemical sensors and large-area artificial skin. This vision is gradually becoming a reality thanks to continuing innovations in low-temperature-processed organic thin-film transistor (OTFT) technology. However, because of the limited palette of available devices and the large process variations in OTFT fabrication, the complexity achieved by organic circuits has so far been rather limited. Also, to achieve ultra-low-cost manufacturing, fully printed organic technology is needed, while most OTFT technologies are still using photolithography. The low-cost potential has therefore not been adequately demonstrated yet.

System-on-foil applications require distributed sensing and actuation over a large area. Such large-area sensors are typically organized in a matrix fashion, where data are collected and processed by crystalline silicon circuitry on the edges. To enable mechanical flexibility and low cost, data conversion and processing should be integrated on the foil. Last year's ISSCC already showcased the first organic ADCs. The first paper in this session demonstrates a microprocessor made with OTFTs that completes this vision. Similarly, large-area distributed actuators on foil can be substantially improved when digital-to-analog conversion is taking place at the pixel level. The second paper in this session addresses an organic DAC showing good speed and accuracy.

Paper 18.1 [IMEC; KU Leuven; Polymer Vision; TNO; KHLim], introduces the first 8b organic microprocessor in a dual-gate, pentacene (p-type only) TFT technology on 25μm thin plastic foils. The design consists of a microprocessor foil and an instruction foil, in which a program is hardcoded. The basic DSP functionality is demonstrated using a running average program at clock frequencies up to 6Hz for a 10V supply.

Paper 18.2 [IMS CHIPS; Max Planck Institute for Solid State Research; U Stuttgart] presents a 3.3V 6b binary-weighted current-steering D/A converter using organic p-type thin-film transistors (OTFTs). The circuit occupies 12mm^2 and is fabricated on a glass substrate using silicon stencil shadow masks. The converter consumes 260μW at an output swing of 2V and has a maximum update rate of 100kS/s. The measured DNL and INL at an update rate of 1kS/s are -0.69 LSB and 1.16 LSB, respectively.

Disposable sensors and circuits on foil will open up new applications such as low-cost RFID product labeling and sensors integrated in product wrappings. To achieve these functionalities, low-cost circuits and memories should be available: printing can be an effective manufacturing approach to achieve this goal. The third and fourth papers demonstrate innovations in this domain.

Paper 18.3 [U Minnesota; Optomec] presents the first DRAM cell realized in a printable, flexible and low-voltage ion-gel electrolyte organic TFT technology. At an operating voltage of 1.0V, the retention time of the implemented gain cell array can exceed one minute and the refresh power is less than 10nW per cell. Full read and write functionality is verified using an 8×8 printed organic DRAM test chip.

Paper 18.4 [CEA-LITEN; STMicroelectronics] presents a fully printed organic CMOS technology on flexible substrates that shows good device performance and enables both digital and analog circuit functionality. These are the natural stepping stones to more complex designs. A test chip includes single devices, inverters, ring oscillators and analog building blocks such as current mirrors and differential pairs. An additional significant contribution of this work is that both n- and p-type semiconductors are printed in a low-cost and scalable process on foil demonstrating the feasibility of fully-printed organic CMOS technology.

These four innovative achievements are very important steps towards a complete organic circuit technology platform integrating sensors, analog circuits, memory, and microprocessor functionality. A technology platform relying entirely on printing technology and roll-to-roll processing will ensure low-cost manufacturing. Such platform will enable new application domains such as large-area distributed sensing, actuation and organic smart labels.

Session 19 Overview / Energy-Efficient Digital *Low-Power Digital Techniques*

Session Chair: *Stephen Kosonocky, Advanced Micro Devices, Fort Collins, CO*
Session Co-Chair: *Ming-Yang Chao, Mediatek, Hsinchu, Taiwan*

Next-generation low-power applications such as biological signal processing, energy scavenging and wireless communications require new technologies and circuit techniques to achieve the lowest energy-per-operation. These applications are driving new techniques for efficient on-die clock generation, level conversion, non-volatile storage, low-power clocking, and reliable low-voltage operation. Energy-efficient systems must be optimized to maximize the utility of power shut down during idle and low-activity periods while also maintaining low-energy operation and high throughput during active modes to meet performance targets. The papers selected for this session highlight technology enhancements, novel circuit techniques, and system designs targeting these goals.

Biological signal-processing applications require very low energy and high performance to enable small form factors for non-intrusive human-body monitoring. Paper 19.1 [IMEC] describes a voltage-scalable 13pJ/cycle, 1MHz operation at 0.4V supply, event-driven wireless sensor node SoC for human-body signal processing, targeting applications such as electrocardiogram (ECG) and electroencephalogram (EEG) monitoring, allowing high-speed, energy-efficient data collection, while maintaining low-power idle modes using multiple scenario-based configurations. The SoC is constructed in 90nm LP CMOS and is voltage-scalable from 0.4 to 1.2V, running at 100MHz at the highest voltage.

Paper 19.2 [TI] introduces a low-power 16b microcontroller in an SoC designed for supporting applications that require energy harvesting. A dedicated 16KB FeRAM memory array is integrated on a 0.13µm CMOS die with fast fail detection ensuring uninterrupted refresh cycles, reducing active current consumption to 82µA/MHz for code executing from the NVM with less than 3A standby current at 85°C.

Paper 19.3 [STMicorelectronics] compares a 65nm LP PD-SOI technology combined with an enhanced power gate device utilizing automatic adaptive body bias, to a standard LP CMOS bulk implementation, demonstrating an 802.11n LDPC codec. The authors show how a low resistivity produced with forward body bias of the power switch, combined with PD-SOI can reduce leakage current by 52.4% vs. bulk and increase the frequency by 20% at 1.2V, while decreasing power by 30% at 360MHz.

Paper 19.4 [Toshiba] describes a low clock capacitance single-phase D-flip/flop that saves 77% energy over a transmission-gate flop at zero-data activity, and 24% power reduction on a wireless LAN application. The new configuration uses a low transistor count and employs an adaptively weakening state-retention coupling scheme for reliable low-voltage operation under device variations in 40nm CMOS.

Paper 19.5 [U Freiburg] describes a standard-cell library utilizing Schmitt-trigger-enhanced logic cells to minimize leakage while demonstrating reliable circuit functionality at 62mV supply in standard 0.13 µm CMOS. The digital circuits are tested using 8×8 multipliers demonstrating reduced minimum voltage up to a subthreshold-slope-limited point. This low single supply voltage is suitable for applications utilizing energy harvesting and low energy-per-operation.

Paper 19.6 [U Michigan] proposes circuit and architectural techniques to improve energy efficiency in aggressively voltage-scaled circuits. The approaches are validated in a high-throughput 1024-pt complex FFT core that utilizes super-pipelining in 65nm CMOS, to achieve 30MHz operation at 270mV supply, producing 234Ktransforms/s consuming only 17.7nJ per 1024-pt complex FFT operation.

Session 20 Overview / Wireline

High-Speed Transceivers and Building Blocks

Session Chair: *Jae-Yoon Sim, Pohang University of Science and Technology, Pohang, Korea*
Session Co-Chair: *Masafumi Nogawa, NTT, Atsugi, Japan*

Transceivers designed for very high-speed wireline communication must contend with significant channel loss, crosstalk, and reflections by employing various equalization techniques in the transmitter and receiver. Confronting these challenges becomes even more difficult as data rates increase beyond 10Gb/s and designs become power-constrained. The first four papers in this session describe transceivers that address these concerns. The remaining papers describe key building blocks for next-generation transceivers with a focus on various receive equalizer adaptation techniques and spread-spectrum clock generation for EMI reduction.

Paper 20.1 from Fujitsu demonstrates a 10.3Gb/s transceiver in 90nm CMOS that achieves an adaptation for both of phase and amplitude distortions for the first time. It combines an analog linear equalizer, a decision-feedback equalizer (DFE), and a driver with pre-emphasis to adaptively compensate up to 41dB channel loss.

Paper 20.2 from LSI Corporation presents a multimedia transceiver implemented in 40nm CMOS. It proposes a new baseline wander correction scheme with a linear equalizer, a 10-tap DFE, and a 4-tap feed-forward equalizer (FFE) for operation over a wide range of data rates from 1.0625 to 14.025Gb/s.

Texas Instruments and Arda Technologies describe their latest transceiver in paper 20.3. This SerDes supports a data rate of 16Gb/s and uses a 14-tap DFE and analog equalizer along with an enhanced-swing voltage-mode driver to generate a 1.2V differential output to compensate 34dB of channel loss.

In Paper 20.4, SnowBush-Gennum demonstrates a 4-lane multistandard-compliant transceiver that supports data rates ranging from 1 to 12Gb/s to satisfy standards including PCIe, SATA, and 1-to-10Gb/s Ethernet without using on-chip inductors.

Paper 20.5 from University of Toronto and Fujitsu Laboratories describes an adaptive engine for a 6Gb/s DFE for a 2× blind ADC-based receiver. This engine digitally extracts the optimum coefficients for the DFE irrespective of the sampling phase of the blind clock.

Paper 20.6 from National Taiwan University presents a 6Gb/s receiver in 90nm CMOS with an adaptive IIR-based DFE compensating a channel loss of 32.7dB.

Yonsei University details a new receive equalizer adaptation technique using asynchronous-sampling histograms in Paper 20.7. The equalizer, implemented in 0.13μm CMOS, demonstrates successful adaptation at 5.4Gb/s over various lossy channels.

Finally, Paper 20.8 from Korea University demonstrates a 3.5GHz spread-spectrum clock generator in 0.13m CMOS with a memoryless nonlinear Newton-Raphson modulation profile achieving an EMI reduction of 19.14dB.

Session 21 Overview / Wireless
Cellular

Session Chair: *Myung-Woon Hwang, Future Communication IC(FCI), Sungnam, Korea*
Session Co-Chair: *Taizo Yamawaki, Renesas Electronics, Japan*

In most parts of the world the cellular mobile terminal market is starting to move from 2G and 3G to 4G systems in order to support higher date rates in the popular smart phones, netbooks and other mobile devices. These higher data rates are enabled by 3G standards such as WCDMA/HSPA and by 4G standards such as LTE . Another evolving direction is the removal of external components, aiming at lower-cost mobile devices and a higher integration level of functions, including a large number of bands and multistandard operation to guarantee global coverage.

The first three papers in this session will address multimode CMOS transceiver solutions.

Paper 21.1 [MediaTek] presents a 65nm CMOS SAW-less GSM/GPRS/EDGE receiver, embedded in SoC. By using a Class-AB low noise amplifier and passive mixer with current-mode LPF, the Rx achieves a high P_{1dB} of +1dBm without performance degradation of sensitivity or IIP2/IIP3, while consuming 58.9mA from 2.8V voltage supply.

A 9-band WCDMA/EDGE transceiver with full RX diversity will be presented in paper 21.2 by ST-Ericsson. Realized in a 90nm RFCMOS process, the SAW-less 2G/3G RX has an NF of 2.3 to 2.5dB, with an IIP2 of +58dBm and an IIP3 of -6dBm. The transmitter achieves EVM below 1.5% for 2G and 4% for 3G, occupying a die area of 14.4 mm^2. The 2G RX/TX+LO consume 129mW/126mW, while the 3G TX+RX+LO consumes 269mW.

Paper 21.3 [Qualcomm] addresses the first SoC with embedded quad-band GSM/EDGE and triple-band 3G transceiver, mixed signal, audio, DSP and memory cores in a 65nm CMOS process. The SAW-less 3G Rx/Tx consumes battery current of 38.3mA/48.2mA in LB and 45.3mA/47.8mA in HB respectively with sensitivity of -111.4dBm. The RF circuitry runs at 1.3V, while analog baseband blocks use 2.2V.

The following 2 papers discuss an inductorless front-end topology with feedback techniques achieving small area.

Paper 21.4 [Media Tek] presents a 65nm CMOS 2G/3Greceiver with inductor-less front-end by shunt-shunt feedback topology, achieving an out-of-band IIP3 of -2dBm and an NF below 2.5dB up to 2.2GHz. The front-end area is 0.9mm^2. The implemented LNA consumes 21.7, 4.8, and 2mA in high-, mid-, and low-gain modes respectively, from a 1.5V supply.

Paper 21.5 [NXP Semiconductors] presents another technique in a 45nm CMOS inductor-less receiver using a translational loop for input matching without NF degradation. The receiver achieves 2.2dB NF in the 3G 900MHz band, 2.4dB NF in the GPS 1.5GHz band, and 2.7dB NF in the 3G 2.1GHz band, consuming 7.3 mA from a 1.3V supply.

The last 3 papers discuss a low-noise modulator targeted for 4G LTE and polar architecture for 3G application, aiming at removing external SAW filters.

Multiband LTE SAW-less modulator is presented in paper 21.6 by IMEC in 40nm CMOS. The modulator achieves RX-band noise down to -162 dBc/Hz and OP_{1dB} up to +11dBm in all LTE FDD bands including the most challenging VII, XI, and XII bands, consuming 24.8 to 38.5 mW.

Paper 21.7 [Infineon Technologies] proposes a fully digital polar transmitter with 17bits (3G) and 19bits (2.5G) RFDAC supporting GSM /EDGE /EDGEEvo /WCDMA /HSPA+ using a 65nm CMOS process. The transmitter achieves -160 dBc/Hz far off noise at all 3GPP Rel.7 specified duplex distance and consumes 35mA DG09 weighted current in 3G mode (1.2V for digital and 2.5V for RFDAC).

Paper 21.8 [Broadcom] presents a 65nm polar transmitter based on a two-point PLL. The transmitter achieves -42dBc ACLR1, -159dBc/Hz noise at 45MHz, and 2.9% EVM at 0dBm with 40mA current from the battery by linearizing VCO gain with a wideband frequency-locked loop nested inside the PLL.

Highly integrated multiband multimode CMOS-based solutions presented in this session demonstrate advances in functionality, maturity, reduced area, power consumption, and performance required to realize current 2G and 3G as well as coming 4G systems.

Session 22 Overview / Analog
DC-DC Converters

Session Chair: *Francesco Rezzi, Marvell Semiconductors, Pavia, Italy*
Session Co-Chair: *Baher Haroun, Texas Instruments, Dallas, TX*

Market trends today are driving for highly efficient power conversion in high volume portable applications. This highlights the need for high-level single-chip integration of DC-DC converters in leading edge processes with other signal-path systems. This high-level of integration is driven by system cost and form factor. Moreover, system performance and cost and special design challenges at these advanced process nodes require taking into account the voltage and reliability limitations of nanometer technologies on switching converter designs. While power efficiency is of paramount importance, other system issues are driving new methods for design robustness and ease of test. The speakers in this session present the latest integration efforts and novel techniques to improve the performance and cost of DC-DC converters.

Paper 22.1 (ST Ericsson) demonstrates the tradeoffs involved in integrating a complete power management system enabling direct battery connection at 5.5V and charger control at 20V using 3V capable devices in a 65nm CMOS cellular handset chip.

Paper 22.2 (Infineon Technologies) demonstrates up to 90% efficient DC-DC converters in the most advanced CMOS process to date, a Hi-K 28nm metal gate CMOS, leading the way to enabling integration and direct battery connection up to 5.5V in future systems.

Paper 22.3 (MIT) demonstrates a digital pulse-width modulator and switched-capacitor bias techniques that provide high efficiency for a wide range of load conditions (20μA to 100mA) from 75% to 87.4% over that range. Both Papers 22.2 and 22.3 exploit the dense and power efficient digital capabilities of the advanced CMOS nodes to implement digital control algorithms.

However, digital techniques also enable near optimal implementation of the control loop and in Paper 22.4 (Arizona State University), a novel capability that uses an accurate inductor self-measurement technique is employed. The measured inductance and series resistance values are used to optimize the converter digital control loop parameters. That approach also provides a novel built-in self-test capability for the inductor used in the system. The paper demonstrates an accuracy of 2.1% for a range of 3.7μH to 22.3μH, 3.6% for a range of DCR 15mΩ to 75mΩ, and 2% for load current sensing for a range of 100mA to 750mA.

There are many other areas that require improvements in non-integrated systems to enhance power efficiency, to reduce system component count, to improve transient response and to reduce EMI. The rest of the papers in this session address these issues from different angles. In Paper 22.5 (KAIST), injection of a small saw-tooth waveform is used in a control loop of a boost converter to generate the timing signals needed to minimize the freewheeling time. This technique results in an 88% efficiency for a 3.7V input to 8V output and offers high efficiency over a wider load range.

Paper 22.6 (KAIST) improves efficiency by reducing, to near zero, the dead-time using adaptive delay gate drivers, dead-time sensing and control loop. The converter achieves 90% efficiency at 1MHz switching to generate a 1.5V output from a 3.3V input.

Paper 22.7 (Fudan University), on the other hand, presents a single inductor with dual output that presents a novel dual saw-tooth extended pulse-width modulator to allow multiple modes of buck/boost to cover a wider range of input and output. This approach offers high efficiency and automatic shift between modes with peak efficiency of 90% reached at a supply voltage of 3V and the two outputs set to 1.8V/214mA and 5V/150mA.

Another important angle is the coexistence of the switching power supplies with analog and RF subsystems. Spurious elimination becomes essential in such systems. Paper 22.8 addresses this issue with a novel frequency hopping scheme that eliminates spurs while minimally impacting the supply noise floor keeping it below -70dBm in any 100Hz bandwidth across a wideband measured to 60MHz.

Session 23 Overview / IMMD

Image Sensors

Session Chair: *Tetsuo Nomoto, Sony, Kanagawa, Japan*
Session Co-Chair: *Jan Bosiers, DALSA Professional Imaging, Eindhoven, The Netherlands*

Higher speeds, increased dynamic range and improved performance for small pixels are clearly driving the imaging industry. This session introduces several interesting new approaches, based on combinations of imager design, technology and architecture, to achieve better performance on these competitive imaging aspects.

The first two papers present approaches to achieve low readout noise and high dynamic range for CMOS imagers.

Paper, 23.1 [Shizuoka U] presents a column-parallel folding-integration and cyclic ADC to achieve a variable gray-scale resolution of 13b through 19b by changing the number of samples. 1.2e^-_{rms} temporal noise is achieved when using 64-fold sampling, resulting in 82dB DR in a 7.5×7.5μm^2 4T pixel.

Paper 23.2 [CSEM] introduces a CMOS imager with 256x256 11□m pixels that achieves 0.86e^-_{rms} readout noise. The pixels have PMOS transistors in an open-loop voltage amplification architecture. This results in a dynamic range of 90dB, with a conversion factor 300□V/e^-.

Paper 23.3 [CEA-LETI — MINATEC] introduces a readout IC with a 15b pixel-level ADC for cooled hybrid infrared image sensors. When indium is bump-bonded to a long-wave infrared HgCdTe detector array, an SNR of 90dB is measured on the detector that has 320×256 pixels with a 25μm pixel pitch.

Then, Paper 23.4 [Kinki U; DALSA PI; U Arizona; NHK] introduces a backside-illuminated CCD imager capable of storing 117 consecutive images recorded at up to 16Mfps. The CCD has 362×456 pixels of 43.2×43.2μm^2. The high fill factor resulting from backside imaging combined with an electron-multiplication CCD readout significantly increases the sensitivity, as low as 7 photons/pixel.

Paper 23.5 [Canon] introduces a 12-inch wafer-scale 1.4Mpixel stitched CMOS imager with 160×160□m^2 pixels with in-pixel 0-to-24dB variable-gain voltage amplifier, fabricated in 0.35□m CMOS. By simultaneously reading out the reset and integrated signals through a pair of column lines a random noise of 13e^-_{rms} is achieved at 100fps in global shutter mode.

Paper 23.6 [U Edinburgh] presents a 128×96 pixel, 44.65□m pitch, digital 3D camera SoC. Each pixel comprises an SPAD (single photon avalanche diode) and phase-domain ΔΣ loop for on-chip computation of distance. 3D images are obtained at 20fps with sub-16cm repeatability error and ±0.5cm linearity over a range of 0.4 to 2.4m.

Paper 23.7 [Cornell U] presents a new approach to 3D imaging by providing local diffraction gratings over each pixel. The imager with 400×384 pixels of 7.5×7.5μm^2 fabricated in a 0.18μm CMOS process enables post-capture refocus and range finding with ±1.3cm accuracy at 50cm by using only one lens and ambient light.

The last four papers present several innovations to improve the performance of small-pixel CMOS imagers for mobile imaging, and high resolution and high speed for digital still and video-camera applications.

Paper 23.8 [Aptina] describes a 1/13-inch VGA SoC CMOS image sensor, with a 1.75μm pixel pitch capable of outputting 30fps at full resolution. To limit the size of the imaging core, a very small separate reference pixel array is used to generate the dark reference. The sampling capacitors for signal and reset are laid out with double pitch and stacked on top of each other. There is only one horizontally routed metal wire per pixel alternating in time as RST and TX. The result is an imaging core of only 1.77mm^2 .The pixel has a dynamic range of 63.8dB with 3000e^- full well and a conversion factor of 300μV/e^-.

Paper 23.9 [Samsung Electronics] presents a back-side-illuminated 1/2.33-inch, 1.4µm pixel pitch, 14.6Mpixel CMOS image sensor. A floating diffusion boosting scheme is implemented with an additional row-wise metal line, with no penalty on QE because of the backside illumination. The QE is 71%, which is 30% higher compared to front-side illumination, and a SNR of 10 is achieved at 87lux.

Paper 23.10 [Aptina] describes a 16Mpixel CMOS image sensor with 23.3mm diagonal optical format with 14b SAR-ADC and 8-lane LVDS output. A dynamic response pixel with 4.78µm pitch is realized by adding an additional transistor switch to the standard 4T pixel. By closing or opening the connection of a physical capacitor to the FD node, the pixel operates in low- or high-sensitivity mode. In low-sensitivity mode, the full well capacity is 50ke$^-$ at 16e$^-_{rms}$ readout noise; in high-gain mode the full well is 18ke$^-$, with 2.2e$^-_{rms}$ readout noise. The pixel with ring gate transistors and no STI achieves 62% QE in green.

The last paper, Paper 23.11 [Sony] presents a 17.7Mpixel CMOS image sensor with a 27.5mm diagonal optical format, using 90nm CMOS. By employing 16 channels of scalable low-voltage signaling interface with embedded clock operating at 2.376Gb/s combined with a single-slope ADC at 2.376GHz, a data rate of 34.8Gb/s is realized. This allows 120fps imaging at 12b full resolution.

Session 24 Overview / RF
Transmitter Blocks

Session Chair: *Francesco Svelto, Università degli Studi di Pavia, Italy*
Session Co-Chair: *Shoji Otaka, Toshiba, Kawasaki, Japan*

Over the recent past, we have witnessed an impressive progress towards the integration of analog/RF circuit blocks together with digital circuits for wireless communication SoCs. Digitally assisted calibration of RF parameters is nowadays extensively applied to ensure performance over process, voltage and temperature variations. Among transceiver circuit blocks, power amplifiers have been difficult to integrate and CMOS has been limited to applications with constant envelope modulation such as GSM. The successful implementation of commercially available switching PAs has further motivated the investigation of PA solutions with a robust linearity in the presence of amplitude-modulated signals. This session presents advances in state-of the-art design. It opens with a wideband transmitter with built-in auto-calibration, then presents three linear RF PAs and concludes with a highly efficient 60GHz CMOS realization.

Paper 24.1 (Broadcom) introduces a TX architecture for calibrating OFDM transmitter non-idealities leveraging RX resident hardware. Transmitter image, local oscillator feedthrough (LOFT) and output power are calibrated by sub-sampling the transmitter spectrum. The TX attains ACPR>55dBc and IM3<-64dBc up to 200MHz baseband frequency. The digitally assisted system assures an IR of 55dBc, a 40dBc LOFT and a ±0.6dB gain accuracy over PVT up to 1.6GHz LO frequency.

A Class-AB PA with shielded concentric transformer in 32nm CMOS is presented in Paper 24.2 (Intel). The device is flip-chip packaged and achieves 28dBm P_{sat} with peak PAE of 31.9%, and P_{1dB} of 26.5dBm. Average power is 21dBm with 16% PAE meeting -25dB EVM for OFDM 64-QAM without digital predistortion linearization. Paper 24.3 (University of Washington) presents a 90nm PA achieving EER/Polar operation via switched-capacitor techniques. The PA delivers a peak output power of 25.2dBm with 55.2% PAE. Average power and PAE are 17.7dBm and 32.1%, respectively. An EVM of 2.9% with a 64-QAM OFSM modulated signal is measured in the 2.4GHz band. Paper 24.4 (Samsung Electro-Mechanics) reports the last RF PA in the session, which is a dual mode quad-band CMOS PA with integrated passive device, assembled in a 5x5mm^2 QFN package. The linear PA for edge mode achieves an average output power of 28.5dBm, a PAE of 22%, an ACPR of -57dBc and an EVM_{rms} of 1.6% for GSM/EGSM bands. The presented PA satisfies requirements for power class-E2 operation. As a switching amplifier, the PA shows an output power of 34.5dBm with PAE of 55% for GSM application.

An effort toward compact, low area mm-Wave PAs still able to deliver output powers in the tens to hundreds of mW is underway. Paper 24.5 (University of Berkeley) presents a 65nm digital CMOS PA with 1V supply, using an efficient 4-input transformer power combiner. The PA achieves 18.6dBm P_{sat}, 15dBm P_{1dB} and 15.1% PAE while using only 0.28mm^2 silicon area. The presented solution is 2x smaller in size and achieves highest PAE at peak power of 18.6dBm over prior art. The PA maintains 17.8dBm P_{sat} and 12.6% PAE over the IEEE band from 58GHz to 64GHz.

The techniques and implementation approaches presented in this session pave the way to advances in wireless transmitters, ranging from DSP-assisted calibration, to robust and linear RF PAs, to high-output-power mm-Wave PAs.

Session 25 Overview / Wireline

CDRs and Equalization Techniques

Session Chair: *SeongHwan Cho, KAIST, Daejon, Republic of Korea*
Session Co-Chair: *Tatsuya Saito, Hitachi, Tokyo, Japan*

The explosive demand for high-bandwidth low-power chip-to-chip communication in severe channel conditions calls for innovations in transceiver architectures and circuits. Clock-and-data recovery (CDR) and equalization are both essential techniques in wireline communications to produce low-jitter clock and low-BER data. The first four papers in this session address challenges in CDRs by employing digital-friendly techniques for nanometer CMOS processes. The next three papers present innovative equalization techniques to address the adverse effects of lossy channels such as inter-symbol interference, crosstalk, and dispersion. The last paper addresses issues in emerging video interface using an embedded clock technique.

Paper 25.1 (University of Toronto) presents an adaptive DFE for a 2× blind ADC-based receiver. The work employs a triangular waveform to adjust the equalization coefficients in order to shape the equalizer output with blind sampling. The adaptive engine restores a 5Gb/s received eye over a channel with 13dB of attenuation at Nyquist frequency to an equivalent of 320mV of vertical opening. The digital CDR is implemented in 65nm CMOS and consumes 78mW from a 1.2V supply.

Paper 25.2 (Oregon State University) shows a reference-less half-rate digital CDR with very wide frequency acquisition range, while improving the tolerance to input duty cycle errors. The recovered clock is generated by passing the random input data sequence through a series of dividers which results in a sub-harmonic spectral peak. Fabricated in 0.13µm CMOS, the CDR consumes 6.1mW at 2Gb/s from a 1.2V supply and operates from 0.5 to 2.5Gb/s.

Paper 25.3 (Oregon State University) describes a digital CDR that combines linear and bang-bang phase detectors to decouple the design trade-off between jitter generation and jitter transfer. Fabricated in 0.13µm CMOS, it achieves an operating range of 0.5 to 3.2Gb/s. The chip consumes 7mW from a 1.2V supply when operating at 2.5Gb/s with the recovered rms jitter of 6ps.

Paper 25.4 (Broadcom) presents a digital CDR using a double-edge triggered shift register to speed up the phase rotation and a latency-minimized loop filter to widen the bandwidth. It achieves ±1.56% tracking range and up to 10MHz tracking bandwidth at 8Gb/s in 40nm CMOS. At 8Gb/s, the CDR consumes 12mW from a 0.81V supply.

Paper 25.5 (National Taiwan University) presents an adaptive equalizer using blind sampling, which consists of an analog equalizer and a DFE. Fabricated in 65nm CMOS, it achieves a data rate of 20Gb/s with BER<10^{-12} over a 35cm FR4 board while consuming 52mW from a 1.2V supply.

Paper 25.6 (Caltech) demonstrates a 2-tap DFE receiver by using a switched-capacitor S/H/summer front-end, which enables FEXT cancellation with 33µW/Gb/s/lane power overhead. Implemented in a 45nm SOI technology, it equalizes 15Gb/s data over a link with >14dB loss and dissipates 7.5mW from a 1.2V supply.

Paper 25.7 (NetLogic Microsystems) presents a transmit equalizer designed for 10Gb/s serial communication which features half-UI IIR and FIR taps. Both SFI transmitter waveform dispersion penalty and data-dependent jitter specifications are met with a single transmitter configuration. The circuit, fabricated in 40nm CMOS, dissipates 125mW and occupies 0.22 mm^2.

Paper 25. 8 (Seoul National University) presents a 3.0Gb/s video-data interface that minimizes the complexity in the receiver. The DLL generates multiphase clocks that sample 8b data from a data stream with 3b-wide delimiter of zero-to-one transition. Fabricated in 0.13m CMOS, the receiver operates from 1.36 to 3.0Gb/s with a BER of <10^{-12} while consuming 13.8mW from a 1.2V supply at 3.0Gb/s.

The architectures and circuit innovations presented in this session provide important techniques to satisfy the demand for higher aggregate bandwidth and lower power consumption.

Session 26 Overview / Wireless

Low-Power Wireless

Session Chair: *Jan Crols, AnSem, Leuven, Belgium*
Session Co-Chair: *Stefan Heinen, RWTH Aachen University, Aachen, Germany*

RFID and remotely powered sensors will be ubiquitous in the future in applications as diverse as healthcare and inventory management. These applications represent a new paradigm for data transfer in the information age in that this technology combines remote powering and wireless data transmission resulting in the need for low-power solutions. A key component is the sensor node, which monitors and transfers the data from a remote site. A reader might provide the radio frequency energy to remotely power up the sensor, as well as detect its information. This session features major breakthroughs related to key aspects of the implementation.

Paper 26.1 [Graz University of Technology and Infineon Technologies] presents the first sensor remotely powered by the electromagnetic field in the frequency range from 13MHz to 2.45GHz. The analog front-end uses a new concept for lowering the forward voltage drop in the AC/DC rectifier. Also, a new concept is used to control the combined shunt and modulator device. The DC current consumption of the system is 70% of previous published designs. The multipurpose sensor block enables on-chip voltage monitoring, temperature sensing, RSSI measurement and has an interface to supply off-chip sensors with a power consumption up to the mW range. The ADC of the sensor block achieves an FOM of 419fJ/conversion step. A fully passive multi-frequency EPC compatible RFID sensor node is fabricated in a 0.13µm CMOS process. The chip operates from 13.56MHz to 2.45GHz, the RF sensitivity is -10.3dBm, and the overall power consumption is 7.9µW.

Paper 26.2 [KAIST and PHYCHIPS] presents an isolator-less, low-power RF front-end architecture for mobile UHF RFID readers. The work presented is the first to replace the commonly used bulky isolator by a small 45° phase shifter. A self-correlation receiver aligns the LO phase and the TX leakage to eliminate the additive noise from a strong TX leakage. A highly efficient system is realized by implementing a polar ASK TX with envelope feedback linearization. A high dynamic range exceeding 30dB is achieved, while a good PA efficiency up to 33% is maintained. This front-end is the first mobile RFID reader solution that achieves a high system efficiency and integration level simultaneously.

Paper 26.3 [Holst Centre / imec] reports on the first super-regenerative RX that integrates RF front-end, quench generator, analog baseband, digital baseband and PLL. The presented ultra-low-power OOK single-chip transceiver for WBAN applications in 90nm CMOS is intended for operation in the 2.4GHz medical BAN and ISM bands. The transmitter uses pulse-shaped OOK with 0dBm peak power, and consumes 2.59mW with 50% OOK. Including the digital part, the Rx consumes 715µW at 1Mb/s data rate, which is oversampled at 3MHz. The work presented achieves the highest published data rate (5Mb/s) of a super-regenerative RX frontend at a sensitivity of -75dBm.

Paper 26.4 [University of Washington] reports a 120µW MICS/ISM band receiver for wireless sensing using a 130nm CMOS technology. The low-IF FSK receiver achieves a -90dBm sensitivity at 200kp/s data rate. A low-power mode reduces the power to 44µW while maintaining -70dBm sensitivity. 9x frequency multiplication is used, allowing a 44.5MHz LO as a foundation for the low power consumption. The injection-locked LO has a settling time below 100ns. The proposed receiver represents a 3x improvement over previously published state-of-the art MICS band receivers both in terms of energy/bit and total power consumption

Paper 26.5 [MediaTek] presents a host-based GPS/Galileo SoC, which achieves 2.0dB NF resulting in a -165dBm chip-in tracking sensitivity. The device can sustain out-of band blockers as high as +16dBm at its antenna port without the need of external LNA and inter-stage SAW filter. By using the proposed scheme of in-band blocker cancellation, this SOC can withstand 12 inband CW blockers simultaneously. The chip occupies 6.6mm^2 in a 65nm CMOS process. The receiver exhibits a -5dBm out-of-band IIP3 while consuming a total power of 18mW, where 8.6mW are due to the RF portion which is the lowest power consumption ever reported.

Paper 26.6 [HKUST] presents a frequency synthesizer for software-defined radios covering all wireless standards from 47MHz to 10GHz (including 14-band MB-OFDM UWB), as well as the 802.15.3c standard from 57 to 66GHz. The synthesizer is implemented in a 0.13µm CMOS process and occupies an active area of 3mm^2. Power consumption ranges from 33mW to 83mW, for a phase noise of -139.6dBc/Hz at 3MHz offset from a 1.7GHz carrier. Employing novel circuits, including a dual-band quadrature VCO, a x3/x5/x7 injection-locked frequency multiplier, single-sideband mixers for UWB, and x2/x3 sub-harmonic injection-locked oscillators at mm-

Wave with automatic peak calibration, the synthesizer offers a superior performance compared to existing solutions in terms of frequency coverage, phase noise, spur level, and power consumption.

In Paper 26.7 [University of California] a low-spur, multiplying, injection-locked delay locked loop using a 90nm CMOS process is presented. Spurs and jitter due to reference clock injection mismatch are minimized by tuning the aperture timing, using a phase interpolator in the feedback path and an adaptive tuning algorithm based on duty-cycle estimation. With these adaptation techniques, the MDLL achieves a -46dBc of reference spur, 1ps of rms and 1.1ps of peak-to-peak jitter, while operating at a reference clock frequency of 570MHz and output clock frequency of 4.6GHz.

The papers in this session show the continuing achievements in reducing the power consumption of integrated wireless sensor nodes as well of wireless building block as part of SoC implementations. This session contributes to the progress of low-power wireless systems that drive low-cost consumer applications.

Session 27 Overview / Data Converters

Oversampling Converters

Session Chair: *Kong-Pang Pun, Chinese University of Hong Kong, Hong Kong SAR, China*
Session Co-Chair: *Lucien Breems, NXP Semiconductors, Eindhoven, The Netherlands*

Oversampling delta-sigma (ΔΣ) data converters are widely used for high-resolution A/D and D/A conversions of low-to-medium bandwidth signals with applications ranging from sensor networks and audio interfaces to wireless communications. The performance of these converters is advancing in several fronts including resolution, bandwidth and power efficiency. This session presents papers that highlight such advancements to unprecedented levels, including continuous-time (CT) ΔΣ A/D converters with signal bandwidths up to 125MHz, discrete-time (DT) ΔΣ A/D converters with power efficient architecture and functional blocks, and audio ΔΣ D/A converters with improved accuracy-enhancement methods. Three unconventional ΔΣ converters, one demonstrating a new technique to realize the noise shaping, one operating under a 0.25V supply, and one presenting a new architecture for time-to-digital conversion, expand the boundaries of oversampling converters in other dimensions.

The session starts with Paper 27.1 from NXP Semiconductors and Delft University of Technology, which describes a high-speed multi-bit CT ΔΣ A/D converter that is sampled at 4GHz. Stable operation is accomplished by using a high-speed filter topology that absorbs the pole originating from the input capacitance of the 4b quantizer in combination with a direct feedback loop around the quantizer. The ADC realizes 70dB DR and -74dBFS THD over a 125MHz bandwidth while consuming 256mW from a dual supply of 1V and 1.8V. The 45nm CMOS chip occupies 0.9mm^2.

In Paper 27.2 from Ulm University, a 25MHz bandwidth 63.5dB SNDR CT ΔΣ modulator is presented that instead of using dynamic element matching uses a digital background calibration to compensate for the feedback DAC errors and enhance the SFDR to -81dB. A pseudo-random binary test signal is injected in the DAC and the error estimation is done by means of correlation. All feedback amplifiers are compensated for finite gain-bandwidth effects. The 3rd-order single-loop modulator has a FOM of 125fJ/conversion-step and is sampled at 500MHz while consuming 8mW from a 1.2V core supply and occupying 0.15mm^2 in 90nm CMOS.

A third-order DT ΔΣ modulator with a single-slope quantizer using modified bi-directional discharging is demonstrated next in Paper 27.3 by Oregon State University. The single-slope quantizer provides one additional order of noise-shaping of the quantization noise and produces a multi-bit output while using only a single comparator. Therefore, it does not require offset calibration. The multi-bit feedback DAC employs DWA for linearization. The 0.18µm CMOS ΔΣ ADC realizes 78.2dB SNDR in 1MHz while consuming 2.9mW from a 1.5V supply and achieving a FOM of 210fJ/conversion-step.

Paper 27.4 from KU Leuven presents an ultra-low-voltage switched-capacitor ΔΣ modulator in 0.13µm CMOS which is accomplished using a near-threshold-voltage biased CMOS inverter technique. This approach guarantees reliable operation of the inverter-based integrators over temperature while running at a supply voltage of only 0.25V. The ADC achieves 61dB over a 10kHz bandwidth at a power consumption of 7.5µW.

Paper 27.5 from the University of Pavia shows an energy-efficient 84dB SNDR 100kHz bandwidth ΔΣ modulator. The noise-shaping characteristic is third-order due to a second-order loop filter in combination with an additional first-order error feedback loop. A low power consumption of 140µW is achieved by a time-interleaved two integrators scheme with a single slew-rate boosted amplifier. The 0.18µm CMOS ADC occupies 0.5mm^2, consumes 140µW from a 1.5V supply, and has a FOM of only 54fJ/conversion-step.

The time-to-digital converter described in Paper 27.6, from K.U. Leuven, SCK-CEN, and KH Kempen, is based on a 1-1-1 MASH ΔΣ architecture. The ΔΣ TDC has a time resolution of 5.6ps while consuming 1.7mW. At an oversampling ratio of 250, the ENOB is 11b over a 100kHz bandwidth. Radiation hardness of the 0.13µm CMOS TDC is verified for future nuclear and space applications.

The session concludes with two ΔΣ audio DAC papers that utilize different mismatch shaping techniques. Paper 27.7 from Analog Devices demonstrates a CT 8b oversampling DAC architecture which measures 120dB SNR and 100dB THD+N. The audio DAC employs a 3-level rotational data shuffling scheme. The DAC consumes 21.5mW from a dual supply of 5V and 2.25V, and occupies 1.35mm^2 area per channel and is fabricated in a 0.35µm DPQM CMOS process.

Finally, Paper 27.8 from Texas Instruments presents an algorithm that concurrently shapes static mismatch errors and dynamic inter-symbol interference (ISI) errors. The audio DAC achieves a THD better than -120dBFS with spurious tone free operation at low signal levels. The 45nm CMOS DAC occupies 0.16mm^2 and consumes 0.875mW from a dual supply of 1.45V and 1.1V with a 0.5V_{rms} output.

The oversampling converter session demonstrates the state-of-the-art advances in ΔΣ architectures, circuit designs and digital enhancement techniques. The boundaries of ΔΣ A/D and D/A converters are pushed to much higher bandwidths and resolutions, extremely low supply voltages and high power efficiencies. The plurality of benefits of ΔΣ modulation is also finding its way in other application domains such as time-to-digital converters used in radiation hostile environments.

Session 28 Overview / Memory

DRAM and High-Speed I/O

Session Chair: *Yasuhiro Takai, Elpida,Sagamihara, Japan*
Session Co-Chair: *Heinz Hoenigschmid, Elpida Europe, Munich, Germany*

In this session advancements in memory and high-speed I/O interfaces are presented that significantly increase system performance and reduce power. Recently, demand for high-speed I/O interface has increased in various memory application areas such as mobile applications, solid-state disc (SSD), digital appliances and server or cloud computing. This year, 4 papers will be discussed reaching data rates up to 12Gb/s by introducing dual-band interconnect, inductive-coupling techniques and impedance matching.

On the memory side, bit density and shrinking process technology are the key market demands for further industry growth. A new record in bit density and smallest process technology is shown this year in the GDDR5 graphics DRAM area. Furthermore, a LPDDR2-N interface has been implemented in a 1Gb phase change memory bridging DRAM and Flash worlds.

Paper 28.1 [UCLA] reveals 8.4Gb/s 2.5pJ/b dual-band signalling for mobile memory I/O interface using simultaneous bi-directional data communication. The chip is designed in a 1V 65nm CMOS technology and uses not only conventional baseband but also RF band on transmission line.

Paper 28.2 [Keio U] discloses 2.7Gb/s/mm^2 0.9pJ/b/chip inductive-coupling interface for NAND flash memory in 0.18µm. The design utilizes 0.1× area-efficient 1 coil/channel interface and 0.5× energy-efficient coupled resonant based CDR compared with the latest work.

Paper 28.3 [Keio U] reveals 12Gb/s non-contact interface for memory card using transmission lines as coils implemented in 90nm. Well-designed termination of transmission lines, transmitter and receiver improves data rate 5× faster than the previous study.

Paper 28.4 [Seoul National U] discloses impedance-matched bi-directional multi-drop DQ bus for large density DRAM server system using 0.13µm process technology. This eliminates reflections at stubs of a 4-slot 8-drop channel, and shows the possibility of 4.8Gb/s bus

In Paper 28.5 [Samsung] a 1.2V 1Gb mobile SDRAM with 4×128 I/Os is discussed for usage in portable electronic devices. This wide-I/O DRAM shows 4× higher data bandwidth than existing LPDDR2, exhibits nearly same standby power and shows 90% reduction of I/O power compared to previous designs. A stack of 2 dies is fabricated using a 7.5µm via diameter TSV technology.

Paper 28.6 [Samsung] demonstrates the first 1.5V 2Gb GDDR5 graphics DRAM in 40nm technology for high speed graphic cards and game consoles. Using a crosstalk equalizing scheme for the transmitter which has a programmable signal ordering capability, a data rate of 7Gb/s/pin with 10% jitter reduction is achieved.

Paper 28.7 [Samsung] exhibits a 1.8V 1Gb PRAM in 58nm technology using a LPDDR2-N interface for low power mobile applications. A data comparison write concept with inversion flag to enhance the core write performance enables 6.4MB/s programming bandwidth with core-write performance 1.5× faster than previous designs. For a faster read, a mid-array pre-charge scheme is presented.

Paper 28.8 [Hynix] demonstrates a self dynamic voltage scaling technique for consumer DRAMs. The design is fabricated in 44nm CMOS technology and uses 1.8V power supply. Using this concept an operating frequency of consumer DRAM at 1.4Gb/s/pin across process skew and operating frequency is maintained, while minimizing the standby power by 12%.

In Paper 28.9 [Toshiba] an embedded 32KB DRAM macro for high-performance NAND Flash memories is discussed. For the first time, an embedded DRAM macro is using a 32nm standard NAND flash memory process. 100mV cell signal and 90ns cycle time are achieved.

Paper 28.10 [University of Minnesota] presents the first gain cell eDRAM macro implemented in 65nm CMOS technology without boosted supplies. A truly logic compatible implementation is enabled achieving 700MHz random-access frequency.

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Low-Energy Vital Information via the Human Body!

A Body Area Network (BAN) seeks to monitor local vital signals from various parts of a human body using distributed sensors and to communicate the acquired information through the wireless medium around the body or directly through the body channel. Occupying the intersection of consumer electronics and human healthcare, BAN can be especially useful for the realization of ubiquitous health monitoring. To make BANs practical, small low-power low-cost sensors and transceivers are necessary. Such practical features are important so as to minimize the inconvenience with daily activities of the monitored patient, to maximize the lifetime of the electronics, to maintain the biocompatibility, and to make the technology broadly available.

At ISSCC 2011, KAIST **[2.1]** will report on a transceiver that uses the body as a communication medium to implement BAN. Its notable advances are the transceiver's low energy consumption (0.24nJ/b) and high receiver sensitivity (250μV). These advances are made possible by a design that considers the physics of signal propagation through the human body, and the development of the low-power double-FSK-modulation scheme compatible with the recently defined BAN standards, thereby significantly advancing the state-of-the-art in BAN technologies.

Advances such as this are essential to aging societies in the industrialized world, as well as to developing countries lacking conventional medical infrastructure.

This and other related topics will be discussed at length at ISSCC 2011, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 20-24, 2011, at the San Francisco Marriott Marquis Hotel.

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Better Sleeping Through Sensing!

Sleep apnea is a surprisingly common problem, with current estimates indicating over 20 million sufferers within the USA alone. The resulting loss in productivity due to elevated levels of fatigue during daylight hours can end up significantly affecting economies worldwide. One of the difficulties with treating the condition is the complexity of the monitoring process required to properly diagnose the condition; with observed sleeping within a hospital environment being the norm. However, a new innovative solution will open the door to monitoring and diagnosis within the comfort of your own home, and, most importantly, your own bed!

At ISSCC 2011, engineers from KAIST **[2.2]** will present the first compact, light, and pervasive sleep monitoring system. Their solution utilizes 15 penny-sized patches, each of which weighs less than 400mg, or less than one fifth of a penny! It can continuously and silently monitor the EEG, EMG, EOG, and ECG signals during sleep. The only thing that you need to do is to attach the patches on your face before sleep and remove them when you awake. Your personal physiological conditions will be automatically collected and stored within each patch. This comfortable sleep monitoring solution is enabled by an intelligent network controller SoC, using a low-energy and fault-tolerant sensor network protocol.

The system contains 14 sensor patches and 1 network controller patch including an integrated 10mAh coin-battery. Each sensor patch consumes 25μW and the network controller patch consumes 75μW resulting in the total system power consumption of just 425μW. A reader device is then used to touch the controller patch, similar to RFID, in order to extract the information from the system prior to its disposal.

By the combination of extremely-low power consumption, very-small light form factors, and completely-wearable printing-on-fabric technology, KAIST engineers shift the paradigm from a bulky and inconvenient one in a sterile hospital setting, to a simple and comfortable one within the comfort of your own home!

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A Safer Alternative to X-rays to See Through…!

Ultra-high frequency terahertz (THz) mm-wave imaging is a great alternative to traditional X-ray technology. It can provide a safe and reliable system for non-invasive medical diagnostics, security screening, and many other applications where imaging through thin materials is desirable. Processing sub-millimeter THz signals in practical systems, including portable ones, requires integrated solutions and advanced radio architectures.

At ISSCC 2011, cutting-edge results in THz imaging will provide a window into new advances in the field, and describe a wide range of architectures for addressing its inherent challenges. At one end of the range researchers from CEA and Université Montpellier **[2.5]** will present a two-dimensional wideband antenna array for 3D imaging with a rectifier detector frontend followed by a low frequency (30-100 KHz) LNA. And at the other end of the range researchers from the University of Wuppertal and IHP **[12.5]** will present a high frequency (820GHz) frontend with sub-harmonic mixers implemented in BiCMOS (SiGe) technology and multiple antennas for beamforming.

In the past THz imaging has been used extensively in expensive and complicated astronomy and advanced radar systems. However, thanks to advances in semiconductor technology including BiCMOS (SiGe), CMOS, and new circuit architectures, this promising technology can now be implemented as a SoC solution with low power consumption, for short-range imaging which will enable many new disruptive medical and industrial applications in cost-effective form factors!

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Transistor Integration Drives Multi-Core Processor Innovation

Microprocessor transistor count has historically doubled every two years, following the trend recognized in 1965 by Gordon Moore and subsequently dubbed "Moore's Law". That trend has fueled processor innovation for the past 3 decades, most recently enabling the development of multi-core processors with enormous amounts of on-chip memory. Increasingly, both general purpose and specialized processors (such as for graphics and multimedia) are being integrated on a single silicon die to reduce system power and cost. At ISSCC 2011, the processor lineup contains several of these processors with significant innovations enabled by transistor integration in state-of-the-art manufacturing processes.

First, Intel will present the largest and most complex microprocessor ever developed. The 32nm "Poulson" processor developed by Intel **[4.8]** contains over 3 billion transistors integrated onto a single 544mm^2 silicon die. The chip, designed around Intel's 64-bit Itanium architecture, contains 8 processor cores and a total of 54MB of on-chip cache linked by an on-chip ring-like interconnect bus. The chip features a new floorplan and extensive circuit and logic changes which enable a doubling of cores over its predecessor "Tukwila" (presented at ISSCC 2008), while reducing thermal design power (TDP) by 15W and squeezing onto a smaller silicon die.

The IBM zEnterprise 196 server processor **[4.1]** is manufactured in a 45nm technology and implements 4 processing cores and 30MB of cache memory using 1.4 billion transistors. The 5.2GHz chip adds features to enable out-of-order instruction execution while integrating co-processors and memory and I/O controllers, while meeting the same power envelope as its 65nm predecessor at a 20% increased frequency. Intel ups the ante on x86 CPU count with the 10-core Westmere-EX processor **[4.3]** built in a 32nm process. Significant reductions in idle power through circuit innovations and transistor improvements enable a 25% core increase over the original Westmere design on which it is based.

Transistor density has also enabled increasingly integrated System-on-a-Chip processors (SoCs). At ISSCC 2011, two processors follow last year's innovation of integrating Graphics Processor Units (GPU) onto a single silicon die with multiple CPU cores. Such processors enhance graphics performance while reducing power and system cost compared to processors with off-chip graphics solutions. The 32nm Intel Sandy Bridge processor **[15.1]** incorporates 4 processors with an on-die GPU and 8MB of L3 cache. Not to be outdone, AMD will present their 40nm Zacate processor **[15.4]**, called an Application Processor Unit (APU), which incorporates 2 CPU cores, a powerful GPU, multimedia ports, and memory and I/O controllers using over 450M transistors.

The unprecedented levels of integration afforded by the latest transistor manufacturing processes are powering a new generation of microprocessors. Powering laptops, desktops, and servers, these chips will bring major advances to computing technologies including mobile graphics, powerful gaming machines, and data center computing.

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IBM Shatters the 5GHz Processor Speed Barrier!

For the past 10 years, processor speed increases have largely stopped in order to control the power density that keeps chips from melting down as they incorporate ever increasing transistor counts and densities. While many saw parallelism with higher core counts as a way to avoid unmanageable increases in chip power density, single-thread performance still remains a critical system bottleneck, due to the inability of today's software applications to fully utilize parallel implementations.

At ISSCC 2011, IBM will demonstrate the first commercial processor breaking the 5GHz speed "barrier". The IBM team utilizes a comprehensive design approach combining detailed power modeling and reduction techniques, with programmable timing control and a number of high-performance process-technology features in order to achieve this speed breakthrough within the available power envelope.

The new microprocessor chip for the IBM zEnterprise 196 system **[4.1]** contains 4 processor cores running at 5.2GHz, with significantly enhanced performance through out-of-order execution, and one of the largest reported L3 caches based on 24MB of shared eDRAM. The chip is implemented in 45nm SOI CMOS technology with two additional process features: First, two thick-metal wiring planes are added, bringing up the metal stack to 13 levels total, in order to solve the critical latency issues in cross-chip block communication. Secondly, low-threshold transistors are added to the process to speed up critical paths. The limited wire-delay scaling and logic added for out-of-order execution and error-checking necessitated extensive programmable timing control for all critical paths. This key timing feature decreases the impact of process variation on robustness of timing margins, enabling hardware-based tuning for maximum operating frequency.

The IBM design shows that processor performance scaling continues strongly along two system dimensions: increased thread count, and critical single-thread performance. This achievement is enabled by an orchestrated engineering effort – ranging from new process technology features to circuit/microarchitecture innovation and comprehensive design methodology.

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Processors Pushing Power Management

Despite the best efforts of processor designers, the laws of physics continue to hold! In order to cope with increasing transistor density, while maintaining chip power density levels, high-performance processor designers continue to apply aggressive power management techniques. Systems presented at ISSCC 2011 continue to demonstrate the growth of this trend. Subsystems, long held to be analog in nature, are also arriving on the digital scene, and foreshadow the next generation of power solutions arriving in the near future.

Most microprocessors are now composed of multiple processor cores. To save power, cores on the latest Westmere-EX processors from Intel **[4.3]** as well as the Bulldozer from AMD **[4.5]** integrate power-control gates. This enables the processor to turn-off cores when not being used, which can result in substantial power savings. Other processors such as Godson-3B from the Chinese Academy of Sciences **[4.4]** also implement dynamic voltage scaling to reduce the voltage required on the chip when computation requirements are lower.

Dynamic on-chip power supply converters are becoming required as processors continue to proactively modify the supply voltage to meet performance requirements at reduced power levels. At ISSCC 2011 Harvard University will present a DC-DC converter **[15.3]** which supports dynamic voltage scaling with nanosecond timing resolution. Noise in the power supply is also a significant problem for processors, as it impacts the timing on the critical paths as well as the robustness of caches: Researchers from the University of Minnesota will demonstrate a PLL that adapts to power-supply variation **[15.5]**, modulating processor clocks to eliminate the impact of this noise on timing in critical paths. Components such as these are increasingly needed to enable ever-finer levels of voltage control on these high-performance dies.

In future years, these aggressive power management trends will continue to proliferate within the microprocessor world, enabling "green" processors that continue to deliver aggressive performance scaling for a range of supercomputing and commercial applications.

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First Chinese High-Performance Processor at ISSCC!

ISSCC is the ***International*** Solid-State Circuits Conference and 2011 marks the arrival of the first general-purpose high-performance processor designed in China to be accepted for technical presentation at ISSCC, the Godson-3B **[4.4]**! The Godson family of processors embodies China's goal of developing a home grown x86-compatible processor to reduce reliance on the major international processor vendors and to forge ahead in the supercomputing arena. The Godson line started in 2002 with the 32-bit Godson-1 and was subsequently refreshed in 2005 with the 64-bit Godson-2. Godson-3B represents a significant leap in capability from prior generations of the processor line.

At ISSCC 2011 researchers from the Institute of Computing Technology, Chinese Academy of Science will describe the Godson-3B which features 8 embedded cores and a 4MB L2 cache. The processor utilizes 500 million transistors and running at a 1GHz clock frequency in a 65nm CMOS process, The Godson-3B delivers 128 billion double-precision floating-point operations per second while consuming only 40W of power through the use of state-of-the-art power reduction techniques such as dynamic voltage scaling. The processor implements a MIPS-processor instruction set augmented with 200 instructions to promote x86 compatibility. Furthermore, the processor is designed to integrate with up to 8 identical devices in a super-computing configuration, generating 1 trillion double-precision floating point operations per second.

With the Godson-3B, China has delivered a home-grown processor with capabilities that will influence the industry for years to come!

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Keeping the Band Leader Undistracted

All modern electronic systems use timing signals to coordinate their activities. In a microprocessor, a timing signal called the clock triggers the circuitry that executes the instructions specified by the software; the faster the clock, the faster the computer. In a communication system, a timing signal called a local oscillator is an essential part of the signal processing used to transmit and receive data. In both cases, the quality of the timing signals is essential. If the intervals marked by the timing signals are not highly uniform, that is, if the timing signals are "noisy," they can limit the speed of microprocessors, and cause communication systems to inaccurately transmit and receive data.

Most commonly, the timing signals are generated by blocks called phase-locked loops (PLLs). Since a PLL keeps time for the overall system, it can be viewed as the bandleader. Unfortunately, PLLs often have to be integrated with many other circuit blocks which tend to generate electrical signals that can couple into the PLL's circuitry, and cause the timing signal it generates to become noisy. Furthermore, all PLLs inevitably contain components that introduce their own corrupting signals, which further cause the timing signal to become noisy. Both of these problems tend to become worse as CMOS IC technology advances, and more and more components are integrated on the same IC. In such cases, the bandleader gets distracted and is unable to keep time accurately, and this degrades the music!

Several papers will be presented at ISSCC 2011 that address these problems: Researchers from the Politecnico di Milano **[5.1]** will present a digital PLL that uses a 10-bit controllable delay element to cancel delta-sigma quantization noise, and a bang-bang phase detector in place of the noisier so-called time-to-digital converter traditionally used in such PLLs. Researchers from Oregon State University **[5.6]** will present a digital PLL that incorporates a new technique to suppress the effects of noise from the power supplies. Heretofore, such noise has plagued PLLs when integrated in system-on-chip ICs. A digital calibration signal is used to facilitate cancellation of the deleterious effects of power supply disturbances. Designers from Intel **[5.7]** will present a microprocessor clock PLL that incorporates various techniques which make it possible to implement the PLL accurately in today's most highly-advanced CMOS technologies.

And so, the band plays on – even better than before!

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Sensors on the Move!

Smart sensors are essential parts of today's smartphones and mobile devices. A new generation of self-powered sensors can be implanted in, or applied on, our bodies to realize completely new applications. ISSCC 2011 will highlight several innovations in the developments of such autonomous sensors.

Motion sensors such as accelerometers and gyroscopes enable new gesture-based user interfaces and games. However, the challenge is how to do 3D-motion sensing at low-cost and in a small form factor. A new gyroscope from ST Microelectronics **[6.1]** represents a big step in this direction, enabling 3D-rotation sensing with a single chip.

But, mobile sensors need mobile power sources. However, batteries run down, and need to be changed. An alternative approach is to scavenge environmental energy. The University of Idaho **[6.7]** and the University of Michigan **[6.9]** will demonstrate systems that are able to extract energy from ambient light or vibration. The imec-Holst Centre **[6.8]** describes a chip that efficiently harnesses solar energy to charge a battery using an innovative solar cell integrated within an imager's pixel circuitry.

Minimizing power consumption is a perennial challenge due to the limited amount of power available to autonomous sensors. Delft University of Technology **[6.2]** will describe a low-power thermal wind sensor that works on a thermal principle and can sense wind speed and direction without any moving parts. The University of Freiburg **[6.3]** will demonstrate a wireless stress sensor that is small enough to fit inside a dental bracket.

Overall, sensors are becoming ubiquitous components of our everyday life. Innovations in sensor design are leading to advancements in user-interface design and entertainment experience for the everyday consumer. At the same time, engineers are hard at work addressing the shortcomings of existing sensor designs, primarily that of their finite battery capacity. Aggressive power minimization and research into energy harvesting techniques are advancing us towards the ultimate goal of self-powered sensors that will enable new applications such as fully-implantable healthcare devices, destined to improve our quality of life in the future!

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Highly-Intelligent Multimedia ICs

Multimedia signal processing is increasingly complex, requiring different solutions for consumer and mobile applications. Recent advances in 3D-TV processing enables ultimately unlimited views from multiple viewpoints. Further, optimizations of architecture with algorithms have generated a new algorithm called context-adaptive binary arithmetic coding (CABAC), which has enabled parallel implementations of future video codecs, resulting in a significant performance improvement. On another front, mixed-mode signal processing technology is becoming essential to neuro-fuzzy learning accelerator designs, for their power and area efficiencies. For all these applications, DSP for mobile communications is going deep down to near threshold voltages to maximize their energy efficiency.

At ISSCC 2011, several highly-intelligent multimedia ICs will be highlighted. National Taiwan University **[7.1]** will present a state-of-the-art QFHD 3D-TV SoC that incorporates a multiview video-coding decoder and free-viewpoint view-synthesis techniques for 3D-TV applications. MIT **[7.2]** will unveil a silicon implementation of a parallel CABAC algorithm proposed for a H.265 codec. KAIST **[7.4]** will describe an intelligent mobile vision-processing chip that utilizes a mixed-signal approach for a neuro-fuzzy accelerator design to achieve power and area efficiency. Texas Instruments and MIT **[7.5]** will disclose an ultra-low-voltage DSP for multimedia mobile applications. This DSP uses low-voltage logic and memory design techniques to operate at 0.6V in an advanced 28nm CMOS technology.

All of these innovations in ICs for multimedia applications, together with algorithmic level co-optimizations, will bring an unprecedented level of user experience and new multimedia functionality to the masses!

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High-Connectivity Mobile Communications

Mobile-communication ICs are essential in providing seamless Internet connectivity everywhere for everyone. But, these ICs need to use less power, enabling extended battery life. At the same time, there is a need to improve connectivity bandwidth. Currently, optimized SoCs for the WiMAX standard are providing a solution to this technical challenge. WiMAX is a wireless network standard that provides high-speed full mobile-Internet access. The next generation of advanced WiMAX SoCs will strengthen the growth of the market, delivering higher performance levels than ever before.

At ISSCC 2011, engineers from ITRI and National Taiwan University **[7.6]** will disclose a WiMAX baseband SoC, with OFDMA and 2x2 MIMO technology. This high-mobility WiMAX modem extends coverage to fast-moving users, for instance in high-speed trains, while maintaining a connected data rate of 5Mb/s. In addition, MediaTek **[7.7]** will present a low-power WiMAX portable modem/router chipset with an unheard of combination of performance and energy efficiency. Increasing the sensitivity margin by 7dB while occupying only 11mm^2, together with a baseband IC of 25mm^2, this leads to an overall power consumption of around 1W. This routing functionality will serve to connect groups of people to the mobile Internet, seamlessly and conveniently!

Such innovations, to be revealed at ISSCC 2011, will lead to strongly-improved Internet coverage, without connectivity interruptions due to changing environmental conditions. In the end, these developments will serve to create a pervasively-connected world!

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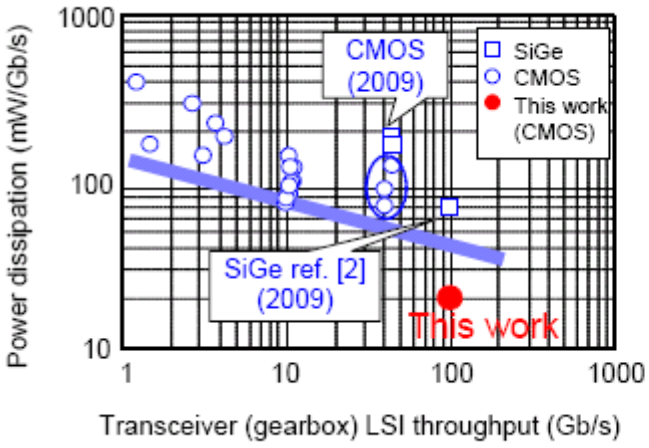
Ultra High Speed – What Is The Limit?

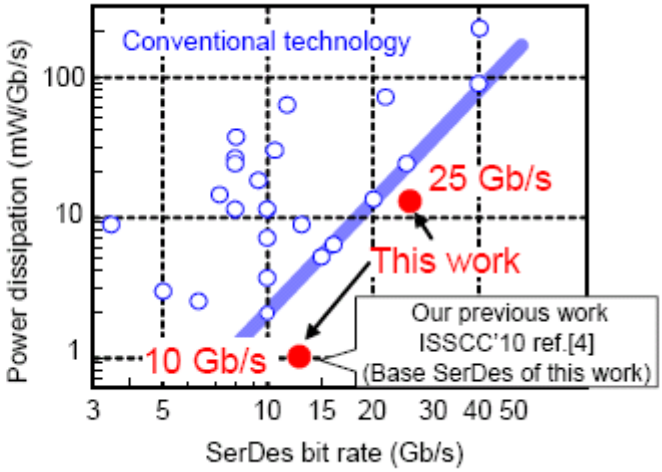
Today, consumers and their smart phones have a seemingly insatiable appetite for data bandwidth, as they continue to demand more feature- and multimedia-rich user experiences. At the same time, consumers continue to demand lower costs and extended battery lifetime in today's "green" driven world. Meeting these challenges for the next generation of communication systems demands a combination of circuit and architectural innovation. ISSCC 2011 will feature an entire session **[Session 8]** devoted to demonstrating the possibilities for future link data-rate increases, and proposing entirely new ways to consider serial-link implementation.

The results presented in this session address the difficult requirements that must be met to enable deployment of future 100Gb/s Ethernet systems in low-cost CMOS. Engineers from Hitachi **[8.4]** will report on a very high-performance 100Gb/s Ethernet gearbox solution whose total power consumption is just 2W, which is 75% less than that of prior-art designs!

Researchers from Sony and Caltech **[8.5]** employ millimeter-wave wireless techniques over a plastic waveguide to enable simultaneous bi-directional 12.5Gb/s communication. In this design, serial data streams are upconverted to 57GHz and 80GHz carrier frequencies and simultaneously transmitted over the waveguide. This 40nm CMOS design thus suggests a path to achieve some of the benefits of optical links without requiring the costly electrical-optical or optical-electrical conversions present in traditional solutions today!

So remember: plastic is the new copper, and that soon waiting for a download to complete will be something we will need to explain to our children along with dial-up modems and FAX machines!





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Latest News from the 60GHz Wireless Frontier

In 2011 we will see a wide assortment of cutting-edge signal-processing and audio/visual technologies finding a home in our living rooms, yielding a brave new world in home entertainment! Yet, despite these advances, we find ourselves tethered to physical cables for interconnecting all of this high tech wizardry together, frustrating both audio/videophiles and wives alike. However, all hope is not lost! New ultra-high-speed wireless communication systems will deliver us from this tied-down reality. 7GHz of colossal bandwidth and 1.5Gb/s of data-rate should enable us to move gigabytes of audio/video between devices almost instantly. But, what is the catch? This bandwidth is only available in the 60GHz range, for a long time considered beyond reach for integrated CMOS radios… until now!

Over the last few years, many research groups have developed radio IP in advanced CMOS technologies, showing that integrated 60GHz solutions can be achieved. Now, the forthcoming Wireless-HD and IEEE 802.11ad standards will enable panning for gold in the 60GHz frontier!

This year, at ISSCC 2011, several companies will demonstrate their plans for how the 60GHz frontier will be crossed! A French-based consortium of CEA-LETI-MINATEC and STMicroelectronics **[9.2]** will unveil a fully integrated 60GHz transceiver module capable of setting up an ultra-high-speed wireless link over a 1 meter distance. Joining them on their journey into the frontier is Sunnyvale-based SiBEAM **[9.3]** who will demonstrate their 60GHz phased-array transceiver pair for 10m non-line-of-sight transmission. Both solutions offer data rates over 3.8Gb/s, and are implemented in conventional 65nm CMOS technologies for significant cost savings over more exotic RF-specific processes.

These bold pioneers will serve as trail blazers, leading us into the 60GHz frontier – a land where vast improvements lay waiting to be discovered for those innovative enough to discover them!

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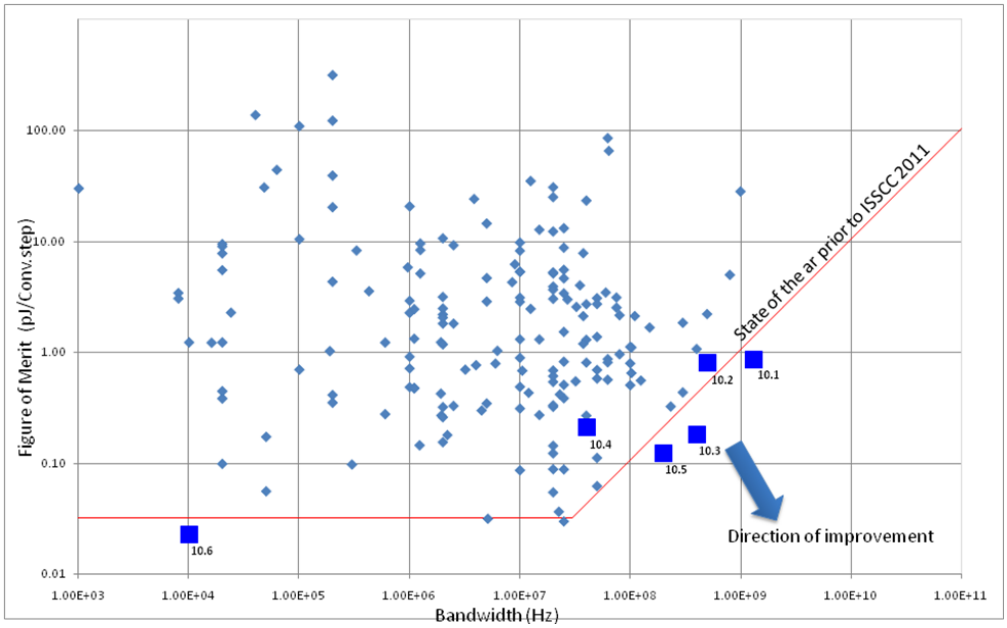
Digitally-Assisted Converters Push the Envelope

Converters between the analog and digital signal domains (i.e., ADCs and DACs) are the key components to interface the "real world" with the cyberspace of digital data processing, computing, and global connectivity. The thirst for high-speed conversion (bandwidth) necessitates improved speed and resolution of ADCs and DACs. But, analog performance is impaired by the reduced supply voltages and lower intrinsic gain in nanometer CMOS technologies which favor high-speed digital logic. Thus, the capabilities of digital circuits improve dramatically with scaling of feature size. Consequently, more and more data converters are incorporating digital assistants to enhance their capabilities.

While "digitally-assisted analog" has been around for several years, ISSCC 2011 demonstrates further improvements in this direction. A large contingent of papers from NXP **[10.1]**, Texas Instruments **[10.2]**, Broadcom **[10.3]**, the University of Macau **[10.5]**, and the National Chiao Tung University **[10.7]**, boost converter performance with digital calibration. Alternatively, MIT **[10.6]** and Ciena **[10.8]** employ digitally-programmable re-configurability and digitally-enabled test functions to achieve their performance gains.

The chart below shows the impact of these techniques on performance in terms of the energy it takes to resolve a quantization-step as a function of bandwidth. At low frequencies this energy is largely bandwidth independent, but increases with frequency at higher bandwidths. Several high-performance converters that extend the state-of-the-art will be presented at ISSCC2011. MIT **[10.6]** improves the energy efficiency at low bandwidths, while papers NXP **[10.1],** Broadcom **[10.3]** and University of Macau **[10.5]** demonstrate enhanced performance for large bandwidths.



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NAND Keeps Marching On As Emerging Memories Struggle for Air

The question on everyone's mind is: "When is the NAND-Flash party over?" As other emerging technologies chase the leader with the advantages they bring to bear, beating the cost of NAND (Flash) is proving to be very difficult. The hope for new technologies is that NAND will eventually run into a wall. However, the wall seems more like a mirage since as we get close to it, it seems more like a soft sponge rather than a wall. In the meanwhile, emerging memory technologies are not sitting idle either. They are making very good progress and are finding applications where their technical advantages over NAND make them the better choice.

ISSCC 2011 will feature a very exciting collection of results that showcase the progress that NAND and emerging memories are making in their respective fronts, both old and new. For example, researchers from the University of Tokyo and SIGLEAD **[11.4]** will present an intelligent NAND Controller for SSD. Perhaps the days when NAND was being sold as a standalone memory are numbered and NAND is starting to be delivered as a part of a managed system solution. Their work demonstrates how the use of technology outside of the NAND die, specifically on memory controllers, can help NAND stay in the game even longer.

On the NAND front, Toshiba and Sandisk **[11.1]** will demonstrate a 64Gb MLC NAND with 14MB/s programming and 266MB/s data transfer fabricated in 24nm CMOS. This chip is the smallest die size reported to date for a 64Gb NAND Flash at 151mm^2. In addition, Samsung **[11.8]** will report on a 20nm NAND memory implementing three bits per cell. Their work will show that despite the odds, NAND still has room to scale thanks to the use of advanced technologies.

On the emerging-memory-technology front, two resistive memory efforts will be described. The first solution utilizes resistive RAM technologies developed by researchers from a Taiwanese consortium **[11.2]** to deliver a 4Mb macro capable of a 7.2ns read-write time. Engineers from Sony **[11.7]** utilize a conductive-bridging approach to deliver a 4Mb macro with a 2.3GB/s read throughput. Both of these solutions demonstrate the progress being made towards real-product applications by these emerging technologies.

Despite the seemingly never-ending prophecies of its demise, conventional non-volatile memory such as NAND-Flash continues aggressively to achieve higher density and lower cost per bit, seemingly despite all expectations! In the meantime, emerging memory technologies continue their slow and steady march towards the mainstream, struggling for air time, while invoking the mantra that good things come to those who wait…

This and other related topics will be discussed at length at ISSCC 2011, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 20-24, 2011, at the San Francisco Marriott Marquis Hotel.

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Renewable Energy in Your Pocket: A Step Towards Battery-Less Electronics

The drive towards sustainable energy solutions for "green" living has made "energy scavenging" an important research area. Its goal is to enable portable miniature devices to derive their own energy from the environment. However, the voltage levels generated from readily-available environmental energy sources such as vibration, heat, and light, can be very low when using small form-factor transducers. Hence, a crucial requirement of the energy-scavenging circuitry is to "boost" these low voltages up to levels that are needed to drive the rest of the electronics. In practice, this often leads to a Catch-22 situation: the energy-scavenging circuitry cannot start boosting the input voltage without itself receiving an input voltage "kick" of sufficient amplitude, but that "kick" is not available until the boost circuitry starts. For example, a solar cell in a dark office environment, or a thermoelectric generator with a 2-degree temperature difference, will typically provide only 100 mV output voltage, which to date has not been sufficient to activate the energy scavenging circuitry itself.

At ISSCC 2011, a research team from the University of Tokyo and the Semiconductor Technology Academic Research Centre of Yokohama, Japan **[12.1]** will provide a solution to this conundrum. They will present the development of an energy-scavenging system capable of operating from a start-up voltage as low as 95mV, without the use of bulky external components such as mechanical switches. This performance is achieved by using an ultra-low-voltage ring oscillator to clock a "pre-charge" capacitor until it is charged to a sufficiently high-voltage level to drive the boost circuitry. To ensure that the ring oscillator functions even at input supply voltages below 100mV the characteristics of the NMOS and PMOS transistors must be well-controlled. This is achieved by post-manufacture trimming of the device. This principle will be demonstrated in a 65nm CMOS process, where the system can generate an output close to 1V at up to 72% efficiency from a minimum start-up voltage of just 95 mV. This represents world-record performance for a fully-integrated solution!

Such developments open up the possibility for portable electronic devices able to re-charge themselves wirelessly and wherever they are – perhaps even in your pocket!

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"Go Green" with Inexpensive Organic Power Meters…

The continuing push towards the "greening" of electronic systems has highlighted the importance of monitoring the power and energy consumption of these systems. Technically, this is a simple function, but the difficulty arises when considering the cost of such monitoring capabilities as widespread adoption mandates very-inexpensive solutions. While organic electronics are slow compared to traditional silicon technologies, they are inexpensive and able to tolerate high voltages, making them perfect candidates for energy-monitoring applications, as will be demonstrated at ISSCC 2011!

At ISSCC 2011, researchers from the University of Tokyo and Dai Nippon Printing **[12.2]** will describe a 100 Volt AC power meter implemented as a System-on-a-Film (SoF) using organic electronics. This design uses 100V organic PMOS rectifiers to generate a 20V supply voltage for logic, generates a line-frequency clock signal for the logic, and implements the logic using 20V CMOS organic transistors. The logic consists of a frequency divider and high-gain pseudo-CMOS inverters, all compensated for variations using a novel concept of floating gates. The design also integrates organic light-emitting diodes for display purposes.

This remarkable solution provides the first-ever power measurement capability using organic electronics! The prototype demonstrates a 2W power measurement at 100V, and has potential to replace the bulky power meters employed today with inexpensive organic System-on-a-Film technology.

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Fine-Grain Home-Energy Monitoring Enables Smart Power Grids

Ever increasing energy costs, and the push to reduce one's carbon footprints is resulting in a surge in the demand for sophisticated energy-management systems (EMS) driven by information technology, such as Smart Grid. Managing energy consumption in our homes requires real-time knowledge of how energy is being consumed, so that unnecessary activities can be reduced or even eliminated. Hence, a cost-effective compact solid-state electronic system that monitors energy consumption of all appliances in a home is highly desired.

At ISSCC 2011, researchers from NEC **[12.3]** will present an integrated-circuit solution for use in current-waveform sensors that can be as small as a quarter! Their sensor utilizes proximity connection to the power line near AC outlets, sensing the AC current waveform generated by the appliance plugged in to the outlet. This waveform is transmitted to a centralized server through the power line, where it is used for energy management. The sensor samples the current waveform at 50kS/s and transmits the data to the server at a rate of 3.3Mb/s. The server recognizes the appliance and the energy consumption by analyzing the received waveforms, as demonstrated via experimentation with appliances such as hair dryers, televisions, and laptop computers. The sensor harvests energy directly from the AC power line so it does not need any other energy source such as a battery.

NEC's effort represents a key advancement in the development of fine-grained energy monitoring which will serve as the basis for the development of sophisticated Smart-Grid systems that will help reduce carbon footprints around the developed world. Furthermore, the ease of use of NEC's solution, thanks to its battery-free operation and proximity-based sensing and communications, will help to accelerate the adoption of these "green" technologies.

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Light Beams on Silicon Chips: A Reality?

The idea of using light beams (i.e., photonics) to replace wires now dominates all long-distance communications and is progressively taking over in networks over shorter distances, as well. But, is photonics appropriate for very short distances present inside digital computers, possibly connecting between silicon chips, or even within a chip itself? Recent developments in the field of optical interconnects have made the prognosis for the use of optics in digital computing and switching much more optimistic and realistic.

The desirability of on-chip photonic interconnects has been discussed for more than 20 years, but to date it has not been possible to actually implement it because the necessary components were much too large to integrate on silicon, and required far too much power to be practical. Even with recent developments, many challenges to implementing on-chip photonic global interconnects remain, including packaging, cost, reliability, and acclimatization.

At ISSCC 2011, IBM Research **[12.4]** will demonstrate a solution that addresses the emerging and challenging field of silicon photonics. Their solution targets monolithic integration of optical components in a CMOS process, potentially enabling high bandwidth, and high density interconnects with dramatically-reduced cost and power dissipation. One of the key components for silicon photonics is the broadband photonic switch used in reconfigurable networks. IBM's proposed monolithic-silicon photonic router is composed of 6 2x2 switches, fabricated and flip-chip bonded with a 90nm bulk CMOS driver. It allows the routing of 3 different wavelengths with very high bandwidth (40Gb/s) through wavelength-division multiplexing (WDM).

Continued innovations such as the high bandwidth and small size hybrid integration of photonic devices on an IC-driver substrate developed by IBM represent important steps towards making light-beam communications/switching on silicon chips a reality!

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New-School Analog: Switching and Chopping Toward a Bright Green Future

The "old" analog world of graceful sine waves and sinuous transients is not dead, but it has certainly been upstaged by a host of aggressive new switching techniques. Unlike the mellow continuous signals we usually think of as analog, these new circuits abruptly slam the signals from one extreme to another. And it works! At ISSCC 20011, **Session 13** will showcase astonishing new levels of power- and signal-performance that would have been unthinkable in previous generations.

The initial presentations in the Session advance the frontier of switching technology for highly efficient power manipulation. Such power switching toggles the drive signal from one power supply to another so as to deliver high energy to the load without dissipating power within itself. For example, Fairchild Semiconductor **[13.1]** will describe a convenient way to efficiently drive LED-based lamps directly from the wall socket without any bulky hardware. Connect this IC to 110 or 220 VAC. and you can drive a 5W LED with power factor correction and full standards compliance.

Chopping also uses switches, but it operates on small signals. It takes a differential analog signal and abruptly reverses it in a periodic way, so as to transform DC signals into AC waveforms. Although this sounds violent, it cleverly sidesteps all the traditional problems of precision measurement like DC offset, flicker noise, and drift. The result is amazing performance improvement. Using this approach, a researcher at Analog Devices **[13.4]**, will present an operational amplifier with a world-record noise level of only 5.9 μV/√Hz, and a tiny input offset of no more than 0.78μV.

Armed with the tools of switching and chopping, the new age analog designer is even better prepared to deliver more performance to a greener world!

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High-Performance Embedded Memory is Diversifying into High-Performance and Low-Power Applications

Innovative design techniques and process technology improvements are enabling the development of high-performance embedded SRAM memories for a variety of applications, both in high-performance and low-power applications.

At ISSCC 2011 engineers from IBM **[14.1]** will describe the first 32nm embedded SRAM SOI implementation that enables low-power operation down to 0.7V. IBM utilizes a 0.154μm^2 bit cell to create a 64Mb macro which demonstrates stability-margin enhancement using bit-line regulation, increased write margins using an improved negative bit-line-boosting technique, and better process-limited performance and yield, using a bit-cell-tracking-delay monitor circuit.

In addition, IBM **[14.2]** will also discuss architectural techniques to significantly improve the area, power, and performance of multi-ported register file arrays. By leveraging a small 2R1W memory cell, double-pumped write ports and replicated read ports, they achieve nearly 2x area and read-power reduction, low read latency, and fast error correction in a register file for a 45nm SOI-CMOS POWER™ processor.

Not to be outdone, engineers from AMD **[14.3]** will describe the architecture of an 8MB Level-3 cache found in their 32nm SOI-CMOS Bulldozer core. Area efficiency is improved by the use of a Column-Select Aliasing technique, while leakage power is minimized by supply gating and floating bit-lines. An efficient redundancy scheme is also implemented using centralized redundancy blocks. The cache operates above 2.4GHz at 1.1V.

Finally, researchers from MIT and Texas Instruments **[14.4]** will unveil the smallest SRAM reported to date in a 28nm low-power process with a 0.12μm^2 bit cell. Their 128kb SRAM macro features a hierarchical bit-line and word-line boosting scheme to improve stability and write margin and provide functionality down to 0.6V. The performance of this memory scales from 20MHz to 400MHz for a 0.6V to 1V operating range, where active-power consumption scales from 2.8mW to 68.5mW.

Hence, SRAM continues to be the industry workhorse for embedded applications, despite the scaling challenges which continue to increase for the higher densities and lower power consumption needed to meet product requirements. As a result, designers are realizing that they require advanced technologies and design techniques going hand in hand in order to produce optimal density and performance.

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Advanced Technology Drives Graphics Integration Within x86 Processors

In the unrelenting drive for ultimate performance/cost/power optimization, a Graphics Processing Unit (GPU) is integrated with multiple CPU cores on a single die. The migration to more advanced processes provides higher density and smaller die size, with an increase in performance and reduced power dissipation. However, the path of GPU integration with multiple CPU cores has significant technological hurdles such as managing the combined power consumption of a high-performance GPU and CPUs within packaging thermal limits and battery capacity in mobile platforms.

At ISSCC 2011, the most recent designs from AMD and Intel are addressing these challenges by adopting design approaches to minimize the CPU and GPU supply voltages, and by deploying DVFS (Dynamic Voltage Frequency Scaling), with embedded power-gating for optimal power consumption. AMD will describe its first Fusion Application Processor codenamed Zacate **[15.4]**, which combines x86 CPUs, Client Northbridge (CNB), IO, and sophisticated graphics and multimedia engines on a single die for mobile computing devices. Zacate's x86 processing power is provided by a pair of AMD's latest Bobcat cores. Each Bobcat core has a dedicated 512KB L2 cache and provides nearly 90% of mainstream CPU performance in a substantially lower area and power profile. Graphics processing is provided by a DirectX 11 Radeon HD5000 series GPU core. Zacate's GPU delivers a peak of 80 GFLOPS per second which provides sufficient compute capability for gaming or compute applications. A Graphics Memory Controller (GMC) arbitrates between graphics, video, and display clients in a well-ordered stream of requests through the integrated CNB to system memory. For optimal power consumption, CPU and GPU cores operate on separate DVFS systems. Bobcat cores support up to eight predefined operation stages for frequency and voltage optimization of the workload. Dynamic power gating is automatically applied to individual CPU cores, the GPU, the GMC, and the video engines. The combination of power-saving techniques enables Zacate to operate with an average power consumption of less than 1.8W, allowing for exceptional battery life. Zacate is manufactured in a 10-layer metal 40nm bulk CMOS technology, with 450 million transistors on a single die.

Intel will demonstrate its Sandy Bridge processor **[15.1]**, a fully integrated multi-CPU, GPU, and memory controller in 32nm CMOS process technology. Sandy Bridge integrates up to 4 high performance Intel-Architecture (IA) CPU cores, a power/performance-optimized GPU, memory controller, and PCIe interface on the same die. The CPUs and GPU share the same 8MB level-3 cache memory. Architectural and implementation improvements have been made to boost CPU core performance without increasing the thermal-power dissipation envelope, or the average power consumption, preserving battery life in mobile systems. The die is powered by 6 different power planes. Power gating is applied to individual CPU/GPU cores and the L3 cache. This allows the majority of the cache to remain in a low-power data-retention mode while only the section of the cache being accessed is fully connected to the power supply. Temperature control via 2 different types of thermal diodes is used to maximize performance by modulating the operating frequency to maintain a given thermal envelope. Temperature information is also used to control the system fan, and to shut the CPU down in case of a catastrophic thermal event. Sandy Bridge thermal dissipation power ranges from 17W to 45W for a 2-core and a 4-core mobile part, and up to 95W for high-end desktop parts. The CPU cores and GPU are powered from variable power supplies ranging from 0.7V to 1.15V.

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These two cutting edge processor designs utilize a dizzying array of techniques to achieve a never before seen level of integration of CPU and GPU technologies. All aspects of the design and its implementation are optimized; from the underlying process technology, to the circuit design, and up into the power management and architectural regimes, yielding an impressive display of engineering innovation. The consumer is the ultimate benefactor of all of this ingenuity as they gain access to new feature-rich products with impressive levels of performance, on both the computational and multimedia fronts, at even lower cost points due to the high level of integration that is achieved.

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Breathe Easy, Healthy Electronics to the Rescue!

Silicon scaling through Moore's Law continues to present exciting opportunities for research and design engineers to push the fundamental limits of semiconductor technologies with respect to speed, bandwidth, and power consumption. The advent of nanometer-length transistor dimensions has enabled designers to realize circuits capable of operating well beyond hundreds of Gigahertz, using inexpensive CMOS electronics. The implications of such extreme circuit speed, coupled with incredibly small-form-factor silicon devices, are the realization of new chips for communications, radar, and healthcare applications. The increased speed of CMOS transistors has opened up new frequencies in the 90GHz, 120GHz, and 180GHz bands for use in imaging applications, while the small transistor-feature size easily allow a single imaging pixel to be arrayed numerous times on a single chip, thus vastly improving resolution in security and healthcare applications. Other developments enabled by advanced silicon processes include extremely wideband radio frontends which are exploited for health-monitoring applications and increased data rates in wireless-communication systems.

Researchers continue to challenge the assumption that data rates above a few hundreds of Mb/s has been exclusive to the realm of wireline solutions. Now, at ISSCC 2011, researchers from KU Leuven **[16.7]** will demonstrate that wireless data rates as high as 10Gb/s are possible. Their wireless approach to rapidly transferring data between devices will impact many consumer-electronic devices. For example, imagine being in a rush at the airport, and simply passing your smart phone by a kiosk which downloads an entire full-length, high-definition movie, in fractions of a second! This 65nm CMOS transmitter could make the vision of instant wireless data transfer a reality for future mobile electronics!

Increasingly, more sophisticated and practical single-chip devices for imaging applications are highlighted at ISSCC. A research team at the University of California, Los Angeles **[16.10]** will present their work on an all-CMOS digital Regenerative Receiver for mm-wave imaging system. Their work exploits the 183GHz band for imaging. The exceptionally-high frequency, combined with the small-feature size of a standard 65nm CMOS process, leads to a single-pixel receiver with dimensions of 1.3x104μm^2, allowing integration of large arrays which further improve image quality. A chip of this dimension will enable low-cost, small-form factor imaging systems for a variety of healthcare and security applications.

While high-speed CMOS electronics has traditionally been limited to communication applications, researchers at the University of Southern California (USC) **[16.9]** have realized a new approach to healthcare monitoring using an impulse-radar radio with an Ultra-Wide Bandwidth (UWB) frontend. As demonstrated in Figure 1, this system is applied towards a subject 75cm away from the radar device for monitoring of respiratory patterns; breathing patterns are clearly visible as ripples in the bottom right plot of the figure. The advances presented in this work will allow future generations to "breathe easier", knowing that new electronics will allow healthier living through non-intrusive monitoring systems.

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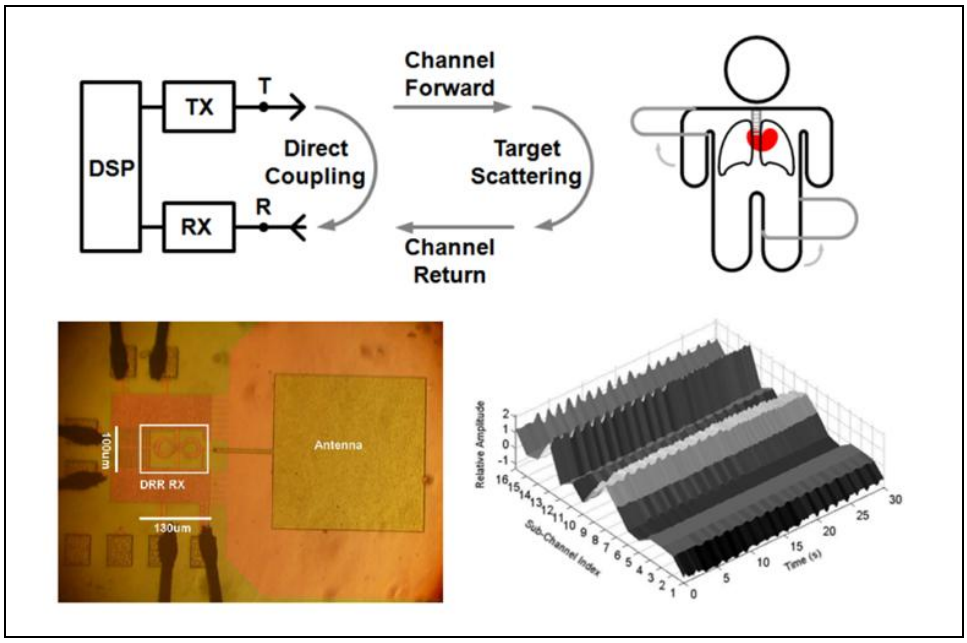

Figure 1: USC UWB-IR chip and systems for healthcare monitoring, breathing patterns shown on the lower right.

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Advanced Image Sensors for Better Living

3D technology is currently thrusting its way into everyday lives through the television and the automobile. US college football games, world cup soccer, and golf's Masters Tournament are to be broadcast and (hopefully!) viewed in 3D this year. Hollywood is betting on 3D as a way to get people back into the movie theaters by enhancing the entertainment experience beyond the current trend of bigger, louder explosions, and more elaborate CGI. In addition, smart vehicles equipped with 3D image sensors are capable of calculating the distance to nearby obstacles, enabling safe navigation on today's congested highways. ISSCC 2011 will highlight 3D-image sensors which advance the state of the art. The University of Edinburgh and ST Microelectronics **[23.6]** will describe a large 3D imager based on Single Photon Avalanche Diodes. In addition, Cornell University **[23.7]** will describe a chip that uses a revolutionary technique based on angular information to create a 3D image.

At the same time, the advent of new higher-resolution image sensors with faster readout rates make it possible for digital SLR and high-definition video cameras to achieve improved image quality without blur. At ISSCC 2011, new devices from Samsung **[23.9]**, Aptina **[23.10]**, and Sony **[23.11]** will illustrate this trend.

Currently, image sensors are implemented with light passing between multiple layers of metal before entering the pixel photodiodes. These structures block some of the light entering the sensor, degrading the final image that is captured. Sensors of the future will overcome this impairment by having the substrate thinned to a few micrometers, thereby allowing light to enter from the backside and exposing the entire sensor without being blocked by metal routing and pixel circuitry. Samsung **[23.9]** and a consortium around DALSA **[23.4]** will describe new backside-illuminated image sensors which enable brighter and crisper images at no additional cost.

Finally, mobile displays are moving towards higher resolution to improve image quality and enable document browsing on hand-held devices. Innovative techniques are being used to increase the display-driver resolution in a smaller die area, and thus at a lower cost than their predecessors. At ISSCC 2011, KAIST **[17.9]** will present a novel display driver for upcoming AMOLED displays, and the Fraunhofer Institute **[17.8]** will present a driver for a combined OLED display and sensor chip.

Hence, technology rushes to toward the goal of relieving sensory deprivation!

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Flexible Intelligence

Organic integrated circuits built on plastic substrates are of significant research interest due to their potential applications in flexible printable large-area electronics, which lie beyond the normal reach of silicon (CMOS) integrated circuits. In addition, their low-cost fabrication processes bodes well for their ubiquitous use. Many key developments in this area have been reported in the past few years at ISSCC. This year sees that trend continue with an exciting new development!

At ISSCC 2011, researchers from imec, the Catholic University of Leuven, TNO, and Polymer Vision **[18.1]** will report on a microprocessor, which, for the first time ever, is directly constructed on a flexible foil using organic semiconductors. The 8-bit processor, utilizing a hard-wired program, integrates more than four thousand transistors, which represents an unprecedented level of complexity in the area of organic electronics on plastic substrates. Despite its currently low speed with 6 instructions per second, this work suggests a new level of organic integrated circuits with substantially increased complexity and computing power.

This work paves a way to "smart foils with digital intelligence," with applications such as: a wall paper that can change patterns and colors adapted to its environment; a wrap that can sense and process the degree of freshness of food; and a window-embedded photovoltaic film capable of efficiently generating power adapted to the illumination condition. Indeed, it is difficult to "wrap" our heads around all of the potential applications of this new technology!

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Green Digital Circuits Boost Energy Efficiency

In this new world of "green consciousness", new ultra-low-voltage adaptive green digital circuits are highlighted at ISSCC 2011, for various applications ranging from broadband wireless communication to biomedical measurement. Green digital circuits, combined with appropriate algorithms and architectures enable practical systems operating with long battery life, or that are able to operate autonomously using energy harvesting.

Engineers from University of Freiburg and HSG-IMIT **[19.5]** will show reliable operation of combinational logic and flip-flops down to 62mV, the lowest voltage ever for such applications. Texas Instruments and MIT **[7.5**] will introduce an ultra-low power DSP in an advanced 28nm low-power process technology. The DSP is able to operate continuously from nominal voltages down to a low voltage of 0.6V using digital-circuit library enhancements. imec and NXP **[19.1]** will present an event-driven system for control of voltage and frequency, for biomedical signal processing within a wireless sensor network.

In addition, this year a Forum at ISSCC 2011 **[F4]** is highlighting how consumer and mobile applications are "going green" by reducing power by optimizing across the spectrum from basic circuit structures up to the entire system. This Forum will bring together experts from the field to discuss aspects and details of energy-efficient circuits, building-block optimizations, power-management schemes, and system-level aware software and hardware that work in harmony to create ever-increasing-energy-efficient systems.

Please come join us at ISSCC 2011! Attendees will see firsthand how high-energy-efficient digital circuits are enabling intelligent multimedia signal processing in future green IT applications.

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Unequaled Equalizers!

The prevalence of the Internet and high-speed data plans has made us numb to the sheer magnitude of the technical innovation necessary to make this all work so seamlessly. As a result, we take for granted the fact that it is trivial to download data from halfway around the world in the blink of an eye. In reality, though, the path that the data takes is quite treacherous. But, we are blissfully unaware as to how difficult the journey really is! Our blissful ignorance is afforded by the efforts of cutting-edge transceiver designers who continually improve the robustness of these links. This year, at ISSCC 2011, some remarkable advancements will be reported that, once again, have been made to protect our data!

The best equalization capability ever demonstrated by a receiver will be described by researchers from Fujitsu Laboratories **[20.1]**. This receiver is able to accurately reconstruct an incoming signal while receiving less than 1% of the transmitted data energy.

Engineers from LSI **[20.2]** will report on a 14Gb/s transceiver that uses advanced equalization techniques to smooth out even the bumpiest of channels. You can rest easy knowing that no reflection will harm your data thanks to their floating-tap decision-feedback equalizer. If you still harbor any concerns for your data's integrity, you can rest assured knowing that researchers from Texas Instruments and Arda Technologies **[20.3]** will describe a chip with very advanced equalization, that will speed your data along at data rates of up to 16Gb/s over channels previously limited to 10.3Gb/s operation.

So like the old Greyhound bus ads used to say: "Relax, and leave the driving (of your data) to us!".

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Multimedia for Every Phone

The cellular world today is dominated globally by the GSM/EDGE cellular standards. However, the migration to smart phones, netbooks, and other feature-rich mobile devices has introduced a need for the higher data rates provided by 3G standards such as WCDMA/HSPA. As well, the rapidly growing use of multimedia-enabled devices has prompted a frequency-band explosion to support even more traffic in fulfillment of the users' insatiable demand for multimedia content. At ISSCC 2011, cutting-edge work seeks to address these issues using innovative design techniques and never-before-seen levels of integration and functionality, all in conventional CMOS process technologies.

One of the main challenges for the cellular industry is to deliver solutions for multi-band multi-standard highly-integrated solutions, both for legacy systems and evolved 3G standards. At ISSCC 2011, Qualcomm engineers **[21.3]** will describe a never-before-seen level of flexibility and integration with a combined quad-band GSM/GPRS/EDGE and tri-band HSDPA SoC that includes a full-digital baseband processor with multimedia capabilities. This transceiver reduces the PCB size and enables advanced performance in low-cost handsets.

Not to be outdone, ST-Ericsson engineers team up with researchers from Lund University **[21.2]** to deliver a transceiver that supports configurations with up to 5 WCDMA bands and 4 EDGE bands. This solution includes a diversity receiver which can be configured for a 2x2 MIMO 64QAM downlink for HSPA Evolution, enabling robust multimedia streaming at extended ranges.

The adoption of these innovative cellular-phone techniques in conventional low-cost CMOS technologies will ensure that future advanced wireless devices will deliver unparalleled levels of multimedia performance, while costing less than ever before, thereby enabling their continued widespread adoption around the world.

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"Running Longer" with Digitally-Enhanced Power

The exploding demand for applications such as smartphones and tablet computers (e.g, iPads) is driving semiconductor technologies to continue to shrink as these devices require the integration of diversified functions on one chip with lower power and lower cost. Digital techniques, which take advantage of the ever-shrinking sizes of transistors, enable implementation of functions vital for cost and size reduction, and are trespassing into the regime traditionally held by analog techniques. At ISSCC 2011 there will be two presentations that highlight this trend:

The first presentation considers the requirement of versatile DC-DC conversion that is needed to power increasingly complex ICs, while providing a longer battery cycle, and higher-performance operation. Researchers at Infineon Technologies **[22.2]** will show the design of an embedded DC-DC converter, using a state-of-the-art 28nm Metal Gate CMOS process, that uses the speed of digital transistors to change the way by which the control loop and pre-drive circuitry is implemented.

The efficiency of any power supply relies heavily, not only on the quality of the active circuitry, but also on the quality of the passive components around them. Interestingly, silicon is an enabling technology that can extend its reach outside the bounds of an IC to improve and optimize the reliability of the whole system. The presentation from Arizona State University **[22.4]** will show how an integrated digital function can be used to measure the characteristics of the associated external power inductors and capacitors of the DC-DC converter. This has the potential to improve the efficiency, and maximize the lifetime and reliability of the power supply. Correspondingly, it will either open up new applications with stringent fault detection and tolerance requirements, or maybe just make your gadget last another year!

Whether it is the battery life of portable equipment or the lifetime of the products, the innovations presented at ISSCC 2011 will help ensure that your devices will run far longer in the future.

This and other related topics will be discussed at length at ISSCC 2011, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 20-24, 2011, at the San Francisco Marriott Marquis Hotel.

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Highly-Efficient Multi-GHz CMOS Power Amplifiers Are Well On The Way!

Power amplifiers (PAs) are one of the most challenging blocks to design in a multi-GHz transmitter. Exotic processes such as InP and GaAs have traditionally been the technologies of choice when it comes to designing highly efficient PAs operating in the GHz range. However, in recent years power amplifiers built in standard CMOS have shown to be capable of operating efficiently in the GHz band.

At ISSCC2011, researchers from the University of Washington **[24.3]** will report on a novel Envelope-Estimation-and-Restoration (EER) power amplifier that achieves high performance using a digitally-controlled switched-capacitor modulator. The power amplifier is implemented in standard 90nm CMOS. It delivers a peak (average) output power of 25.2 (17.7) dBm with a peak (average) PAE of 55.2% (32.1%) for a 64 QAM OFDM modulated signal in the 2.4GHz band.

Engineers from Samsung Electro-Mechanics **[24.4]** will report a CMOS quad-band RF PA and its module for GSM/EDGE applications designed with Integrated Passive Devices (IPDs). The measured PAM efficiency is 23% in EDGE mode and 48 to 55% in GSM mode.

Finally, researchers from the University of California at Berkeley **[24.5]** will present a fully-integrated 60GHz, 18.6dBm CMOS PA. The PA achieves 18.6dBm PSAT, 15dBm P-1dB and 15.1% PAE at 1V supply while only occupying 0.28 mm^2 of silicon area.

Being able to design power amplifiers in a standard CMOS technology will enable single-chip implementations of transceivers, which will ultimately reduce the cost and the total system footprint, both being key in enabling low-cost portable applications.

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Advancements in Clock-And-Data Recovery

Every day, our lives depend upon the transfer of massive amounts of information from one location to another. For example, when downloading a file from the Internet, unbeknownst to us, the data typically travels chip-to-chip through an enormous number of different links and media. At the heart of these data transmissions are clock-and-data-recovery circuits that are able to reliably receive and recover billions, and even trillions, of bits of information. Making these feats all the more remarkable is the fact that these circuits face increasing pressure on many fronts including lowering costs and reducing electromagnetic interference.

For the first time, innovative solutions to these issues will be addressed at ISSCC 2011 **[Session 25].** Researchers from Oregon State University **[25.2]** will report a technique that significantly lowers system costs for clock-and-data recovery by eliminating the need for an external reference clock. A key feature of their work is that the frequency-acquisition range is unlimited, which is a breakthrough in clock-recovery ICs whose performance has traditionally been severely limited by the narrow frequency-capture range. Not to be outdone, engineers from Broadcom **[25.4]** will be working to make our everyday lives safer by demonstrating a digital clock-and-data-recovery circuit that can allow for unprecedented levels of electromagnetic-emission suppression.

So even though engineers are often portrayed as cold and calculating, remember that they act that way because they care about the environment and about you!

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How Low Can You Go? (With RFID System Cost and Power That Is…)

RFID is a technology that most people take for granted, despite the benefits that it delivers all throughout our lives, such as its contribution to reducing costs at the local retail stores through improved supply-chain tracking and management, and reduction in surcharges due to shoplifting discouraged by ubiquitous theft-provention tagging. Technically speaking, RFID represents a new paradigm for data transfer in the information age, in that this technology combines remote powering and wireless data transmission. This makes it possible for RFID-based devices to monitor data in harsh environments where batteries cannot be replaced or it is not otherwise possible to power communication devices.

RFID systems consist of two key components: a sensor element which monitors and transfers the data from a remote site, and a reader that provides the radio-frequency energy to remotely power up the sensor and read out its information. ISSCC 2011 features two breakthroughs related to both aspects of such implementations. A key challenge in any reader is the ability to distinguish the small received signal sent back from the sensor from the large transmitted radio frequency signal transmitted by the reader. Traditionally these signals, which can differ in power by several orders of magnitude (think of trying to hear a whisper while yelling at the top of your lungs!) are distinguished using large, external components called isolators, which can add significantly to the cost of the reader. Researchers from KAIST and PHYCHIPS **[26.2]** will describe an integrated technique that can cancel the self-leakage from the transmitter on the reader using a novel self-correlation approach. Their suppression of the large transmitter leakage can be achieved using low-cost components, eliminating the need for, and cost of, external isolators!

A key challenge for the RFID sensor arises from the need to reduce its operating-power consumption, and to minimize the amount of incident radio energy required to provide this power. Researchers from Graz University and Infineon Technologies **[26.1]** will present a new approach for reducing the minimum incident radio energy required for sensor operation through a novel concept involving the signal rectifier used to detect it. In addition, they utilize innovative design techniques to reduce the sensors' power consumption by over 70% compared to the existing state-of-the-art. The RFID device can support operation from 13MHz to 2.45GHz, while integrating multiple operations such as signal level detection, voltage monitoring, and temperature sensing.

Innovations such as those described above on both the RFID reader and sensor are the key to ensuring future ubiquitous deployment of RFID and sensing technology in a wide range of applications. Thereby, we will be allowed to continue to reap the benefits of existing applications such as inventory management and theft prevention. As well, we can look forward to new applications, such as healthcare monitoring and safety, enabled thanks to the continued reductions in cost and power consumption.

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Oversample and Conquer!

Oversampling and noise-shaping techniques have traditionally been used to design high-resolution converters, with the advantage that they greatly relax matching requirements. In the past, their signal bandwidths have been restricted to several tens of kilohertz for high resolutions (15 bits and beyond), and few tens of megahertz for resolutions in the 12-bit range. But, over the years, the energy efficiency and bandwidths of these converters have steadily improved. Now, ISSCC 2011 presents a variety of oversampling converters that push the envelope on several fronts: bandwidth, power efficiency, and low-voltage operation.

Engineers from NXP **[27.1]** will present a continuous-time delta-sigma modulator with a signal bandwidth of 125MHz, which achieves a dynamic range of 70dB in 45nm CMOS. This represents the first CMOS oversampling converter achieving a signal bandwidth in excess of 100MHz, and demonstrates the efficiency of continuous-time delta-sigma techniques in nanometer CMOS processes. Researchers from Ulm University **[27.2]** will present a low-power modulator, with 5MHz bandwidth using an innovative DAC linearization technique that works in the background, achieving 81dB SFDR with 8mW of power.

As well, at ISSCC 2011, several interesting circuit techniques that improve the performance of discrete-time oversampling converters will be disclosed. Researchers from Oregon State University **[27.3]** will demonstrate a low-power modulator which combines an internal integrator and a multibit quantizer into one small power-efficient unit. In another design that pushes the envelope of low-voltage operation, researchers from Katholic University in Leuven **[27.4]** will disclose a 10-bit modulator operating at a supply voltage of 250mV. Not to be outdone, researchers from the University of Pavia **[27.5]** will present a power-efficient converter that achieves a high resolution in a 100kHz bandwidth.

ISSCC 2011 will also feature two high-performance audio digital-to-analog converters employing oversampling techniques. Engineers from Analog Devices **[27.7]** will disclose a DAC that achieves 120dB SNR using improved dynamic element-matching algorithms. A very-low-power DAC that achieves 108dB dynamic range in a 45nm CMOS process will be presented by Texas Instruments **[27.8]**, which uses an innovative mismatch and inter-symbol-interference shaping algorithm.

Such innovations result in significant reduction in power and area, which will enable the next generation of low power systems-on-chip implemented in nanometer CMOS technologies.

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Record-Setting DRAM Interface Speeds and Densities

High bit density and shrinking process technologies are the key market drivers for growth in the memory industry. Recently, demand for high-speed I/O interface has increased even more in various memory-application areas, such as mobile applications, solid-state discs (SSDs), digital appliances, and cloud/server computing.

At ISSCC 2011, a number of companies, including Samsung **[28.5, 28.6, 28.7]**, Hynix **[28.8]** and Toshiba **[28.9]**, along with researchers from various universities, will discuss advanced design techniques that achieve data rates up to 12Gb/s by introducing dual-band interconnect, inductive coupling, and impedance matching.

In addition, a new record in bit density, and the smallest process technology used thus far (for this application), will be demonstrated at ISSCC 2011 for a GDDR5 graphics DRAM by Samsung **[28.6]** with their 2Gb Graphics DRAM in 40nm. By using a crosstalk equalizing scheme, data rates of 7Gb/s/pin can be achieved, improving the performance of future 3D-gaming consoles. Samsung will also demonstrate a Low-Power DDR2-N interface in 58nm CMOS for a 1Gb phase-change memory (PCRAM), which successfully bridges the worlds of DRAM and Flash memory technologies **[28.7]**.

The seemingly never-ending resourcefulness of today's memory designers continues to deliver advanced circuit-design techniques and new silicon technologies that continue to drive up memory-data-transfer rates at lower energy levels. Such innovation is essential in meeting increasing bandwidth demands for future applications in both the high-performance and low-power market spaces.

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