IEEE SOLID-STATE CIRCUITS SOCIETY

ADVANCE PROGRAM

2011 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE

FEBRUARY 20, 21, 22, 23, 24

CONFERENCE THEME:

ELECTRONICS FOR HEALTHY LIVING

SAN FRANCISCO
MARRIOTT MARQUIS HOTEL

NEW THIS YEAR:
Plenary Roundtable
(in addition to 3 Plenary talks)
Industrial Demo Session

5-DAY PROGRAM

SUNDAY ALL-DAY: 2 FORUMS:
Transmitters for Wireless Infrastructure; ULV Circuits for Energy-Efficient Systems

9 TUTORIALS: nm Layout; SC Noise Analysis; Power-Delay Tradeoffs; Silicon-Body Interface; Digital - Ultra Low Voltage & Power; Embedded Memory; LC Oscillators; Rx Distortion; DPLL CDR

EVENING: 2 SPECIAL-TOPIC SESSIONS & STUDENT RESEARCH PREVIEW

THURSDAY ALL-DAY: 4 FORUMS:
Personalized Medical Care; Green Microprocessors; 3D Image Sensors; High-Speed Xceivers

SHORT-COURSE: Cellular and Wireless LAN Transceivers

ISSCC VISION STATEMENT

The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and application to maintain technical currency, and to network with leading experts.

CONFERENCE TECHNICAL HIGHLIGHTS

On **Sunday, February 20th**, the day before the official opening of the Conference, ISSCC 2011 offers:

- A choice of up to 4 of a total of 9 Tutorials
- A choice of 1 of 2 Advanced-Circuit-Design Forums

The 90-minute tutorials offer background information and a review of the basics in specific circuit-design topics. In the all-day Advanced-Circuit-Design Forums, leading experts present state-of-the-art design strategies in a workshop-like format. The Forums are targeted at designers experienced in the technical field.

On Sunday evening, there are three events: Special-Topic Sessions entitled, "**Data-Converter Breakthroughs...** and **Wireless Sensor Systems...**" will be offered starting at 8:00pm. In addition, the **Student Research Preview**, featuring short presentations by selected graduate-student researchers from around the world will begin at 7:30 pm. A distinguished circuit designer, Professor Paul Gray will provide introductory remarks at the Preview.

On **Monday, February 21st**, ISSCC 2011 offers three plenary papers on the theme: "Electronics for Healthy Living". This will be followed by a Technology Roundtable on challenges to be faced in the next 10x reduction in power, with six renowned panelists, a moderator, and three domain experts to pose questions. On Monday afternoon, there will be five parallel technical sessions, followed by a Social Hour open to all ISSCC attendees, and a Women's Networking Reception. The Social Hour held in conjunction with the Book Display will also feature posters from the winners of the joint ISSCC/DAC Student-Design Contest. Monday evening features a panel discussion on "**20 Years of Broadband Evolution…**", as well as two Special-Topic Sessions on "**Future System and Memory Architectures…"** and **"Body-Area Networks (BAN)…".**

On **Tuesday, February 22nd**, ISSCC offers five parallel morning and afternoon technical sessions. A Social Hour open to all ISSCC attendees will follow the afternoon session. The Social Hour will include Industrial Demo Sessions. Tuesday evening sessions include an evening panel on "**20/22nm Technology Options and Design Implications**", as well as two Special-Topic Sessions on "**Gb/s+ Portable Wireless Communications**" and "**Technologies for Smart Grid and Smart Meter**".

Wednesday, February 23rd, features five parallel sessions morning and afternoon.

On **Thursday, February 24th**, ISSCC offers a choice of five events:

- A Short Course on **"Cellular and Wireless LAN Transceivers: From Systems to Circuit Design"**
- Four Advanced-Circuit-Design Forums

Registration for educational events will be filled on a first-come, first-served basis. Use of the ISSCC Web-Registration Site (http://www.isscc.org) is strongly encouraged. Registrants will be provided with immediate confirmation on registration for Tutorials, Advanced-Circuit-Design Forums and the Short Course.

Need Additional Information?
Go to: www.isscc.org

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T1: Integrated LC Oscillators

This tutorial will go through the fundamentals of LC oscillator and LC VCO design, such as basic phase-noise theory, design for low power, low phase noise and, large tuning range (including varactor choice). It will also include other key issues such as supply pushing, LDO-VCO co-design, routing/buffering the oscillator signals in large SoCs, and PLL-VCO co-design for fully integratable frequency synthesis. The goal it to give a thorough overview that will be easy to follow yet comprehensive and in touch with the latest significant research results (e.g. DCOs with extremely fine tuning steps for use in DPLLs) of one of the truly key blocks in today's and tomorrow's radios.

Instructor: Pietro Andreani received the M.S.E.E. degree from the University of Pisa, Italy, in 1988, and the Ph.D. degree from the Dept. of Electrical and Information Technology (EIT), Lund University, Sweden, in 1999. Between 2001 and 2007, he was Chair Professor at the Center for Physical Electronics, Technical University of Denmark. Since 2007, he has been Associate Professor at EIT, Lund University, working in analog/mixed-mode/RF IC design. He is also a part-time IC designer at ST-Ericsson in Lund. He is a TPC member of both ISSCC and ESSCIRC. He has published several papers on oscillator phase noise and VCOs.

T2: Embedded Memories for SoC: Overview of Design, Test, and Applications and Challenges in the Nano-Scale CMOS

This tutorial provides a detailed description of the workhorse static memory, the 6T SRAM. Multi-port and content-addressable memories are introduced next with special design considerations beyond the 6T cell. Embedded DRAM is described, as well as its advantages in the SoC ecosystem. Special considerations for SOI memory design are described. State-of-the-art industry techniques that improve power and voltage scaling in the nanoscale regime are also reviewed. Finally, an overview of Built-In-Self-Test is provided.

Instructor: Harold Pilo is a Senior Technical Staff member at IBM Systems and Technology Group. He joined IBM in 1993 to develop OEM SRAM products for the IT industry. He currently leads the circuit IP development for ASIC SRAM Technology Development. Prior to joining IBM, he worked at Motorola from 1989 to 1993. Harold has presented many papers at the ISSCC, VLSI and ITC. He holds over 50 US Patents and is currently a member of the ISSCC Memory Sub-committee. He graduated with a BSEE from the University of Florida in 1989.

T3: Ultra Low-Power and Low-Voltage Digital-Circuit Design Techniques

Until some 15 years ago there was no attention for low-power CMOS design, due to the 'C'omplementary nature of logic gates. Despite this beautiful property power dissipation has become the limiting factor in many fields of CMOS design, from high-performance computing to wireless autonomous transducer systems (wireless sensor nodes).

In this tutorial an overview will be given of low-power and low-voltage digital circuit design techniques with a focus on truly energy-limited systems, such as wireless sensor nodes. Circuit techniques for super-threshold toward sub-threshold, impact on speed, area, and power, and consequently on architectures will be highlighted.

Instructor: Jos Huisken joined Philips Research after graduation from the University of Twente in digital signal processor design in 1984. Since then he has been involved in architectural synthesis for digital signal processors and has applied these techniques to the first Digital Audio Broadcast (ETSI-DAB) ICs in the 1990s. Since then he has been driving low-power design from an architectural point of view. After investigating turbo and LDPC decoders, and being involved in creating a spinoff company from Philips, he joined Holst Centre / imec Netherlands in 2007 to work on ultra-low-power DSP for wireless sensor nodes, specifically for body-area networks, with a strong focus on low-voltage and low-power circuit design.

T4 : Layout – The Other Half of Nanometer Analog Design

The layout of analog blocks has for a long time been a critical aspect to achieving the theoretical performance of a circuit. Perhaps more importantly, when the layout fails to match the design, the project can fail in schedule, cost, or performance. In nanometer CMOS there are many layout-induced effects that alter the transistor characteristics, and this means that matching the layout to the design is becoming more difficult and critical. This tutorial provides an overview of those effects, and provides some strategies and approaches to combat them. Even if you don't do the layout yourself, every designer should be able to guide the process through to success.

Instructor : Jed Hurwitz received his Electronics BEng from Nottingham University, United Kingdom, in 1987. He joined Plessey Semiconductors, working on mixed-signal CMOS and design-related process issues. From 1990, he worked on videotelephony circuits at MatraMHS. In 1995, he joined a start-up, Vision (later acquired by STMicoelectronics), which became one of the pioneers of CMOS imaging, were he led all aspects of the architecture, design, and development of CMOS image-sensor systems (from photons to applications) and their optimization for the mobile cellular market. In 2005 he co-founded Gigle Networks, which has since successfully introduced powerline and anywire solutions on nanometer technologies.

T5: DPLL-Based Clock and Data Recovery

The purpose of this tutorial is to introduce attendees to Digital Phase-Locked Loop (DPLL) based Clock-and-Data Recovery (CDR). The talk will start with an overview of different types of CDRs to frame where DPLL-based CDRs fit into the overall landscape. Next, the basic theory behind DPLL-based CDRs will be presented with an eye towards practical application. Following this, the performance of DPLL-based CDRs in the face of various practical impairments such as ISI, random jitter, deterministic jitter, slicer offset, etc will be explored. This part of the talk will also tie into jitter budgets and electrical tables found in standards. Finally, the talk will conclude with an example to show how all the concepts come together into a design.

Instructor: John T. Stonick received his Ph.D. in ECE from North Carolina State University in 1992. From 1993 to 1997 he held a postdoctoral research position in the ECE department at Carnegie Mellon University. From 1997 to 2000, he was an Assistant Professor with the ECE department at Oregon State University and a co-director of the NSF Center for the Design of Analog-Digital Integrated Circuits (CDADIC). Starting in 2000 he was a Principal Design Engineer with Accelerant Networks until they were acquired by Synopsys in 2004. Since 2004 he has remained with Synopsys where he holds the title of Synopsys Scientist. His interests include system architecture and simulation, clock-and-data recovery, and using adaptive digital techniques to compensate for analog circuit imperfections in transceivers.

T6: Practical Power-Delay Design Trade-offs

Design of high-speed, power-optimized circuits is an increasingly large part of the digital circuit designer's responsibilities. Circuit and block design trade-offs between delay, active, and leakage power are vital to meeting power and delay goals. This tutorial begins with basics of digital circuit delay and power consumption. Discussion turns to methods for reducing power and delay, active/leakage power trade-offs, and a review of circuit styles and their power-delay characteristics. Design and synthesis tools and methods to meet timing and power goals will also be discussed. Finally, system-level power management problems, solutions, and trade-offs are discussed.

Instructor: Tim Fischer has worked in high-speed digital circuit design for 22 years. He earned the Masters Degree in Computer Engineering from the University of Cincinnati in 1989. Tim then worked for Digital Equipment in Hudson, Massachusetts until 1998 designing VAX and Alpha CPUs. From 1998 to 2006, he worked on Itanium CPU design with Hewlett-Packard and Intel in Fort Collins, Colorado. Since 2006 Tim has been an AMD Fellow working on CPU circuit design and methodologies. His interests include high-speed CMOS circuits, latching/clocking structures, and power-efficient design.

T7: Distortion in Cellular Receivers

In this tutorial we discuss how noise and distortion limits the dynamic range of cellular receivers. The connection between the narrow-band cubic nonlinearity and the properties of typical radio receivers, both for narrow- and wide-band signals, is explained. First the properties of the cubic nonlinearity and its relation to several important narrow-band distortion types are explained. The concept of intercept points and their use to characterize weak MOS and BJT device nonlinearities as well as amplifiers entering compression, with and without feedback, is highlighted. Some linearization techniques are introduced, and the impact of third-order intermodulation for general receivers and second-order intermodulation for low- and zero-IF receivers is explained with circuit examples. Finally, the effects of more wide-band signals are coupled to the narrow-band approximations.

Instructor: Sven Mattisson received his PhD in Applied Micro Electronics from Lund University in 1986. From 1987 through 1994 he was an Associate Professor in Applied Micro Electronics in Lund where his research was focused on circuit simulation and analog ASIC design. 1995 he joined Ericsson in Lund to work on cellular hand-set development. Presently he is with Ericsson in Lund, where he holds a position as senior expert in analog system design. Since 1996 he is also an Adjunct Professor at Lund University. Dr. Mattisson is one of the principal developers of the Bluetooth concept.

T8: Noise Analysis in Switched-Capacitor Circuits

Switched-capacitor (SC) circuits are ubiquitous in CMOS mixed-signal ICs. The most fundamental performance limitation in these circuits stems from the thermal noise introduced by MOSFET switches and active amplifier circuitry. This tutorial reviews hand analysis techniques that allow the designer to predict the noise performance of switched-capacitor circuits at various levels of complexity. The material will focus on practical examples ranging from basic passive and active track-and-hold stages, integrators and examples of SC filters. Simulation examples using periodic noise analysis tools are included throughout the tutorial to complement and verify the theory.

Instructor: Boris Murmann is an Associate Professor in the Department of Electrical Engineering, Stanford, CA. He received the Ph.D. degree in electrical engineering from the University of California at Berkeley in 2003. From 1994 to 1997, he was with Neutron Mikrolektronik GmbH, Hanau, Germany, where he developed low-power and smart-power ASICs in automotive CMOS technology. His research interests are in the area of mixed-signal integrated circuit design, with special emphasis on data converters and sensor interfaces. In 2008, Dr. Murmann was a co-recipient of the Best Student Paper Award at the VLSI Circuit Symposium and the recipient of the Best Invited Paper Award at the Custom Integrated Circuits Conference (CICC). In 2009, he received the Agilent Early Career Professor Award.

T9: Interfacing Silicon with the Human Body: A Primer on Applications, Interface Circuits and Technologies for the Medical Market

This tutorial will provide a holistic overview of modern circuit techniques for interfacing to the human body: both sensing of key biomarkers as well as delivery of stimulation. A brief summary of constraints for safety and the biological environment will be provided to motivate general considerations for medical circuit techniques. Special emphasis will be put on power and noise issues as well for portable, ambulatory devices. A review of exemplary circuit blocks for sensing and design techniques such as dynamic offset compensation will then be discussed, with representative applications from cardiac sensing, brain-machine interfacing, electrochemical monitoring and cochlear prosthesis to drive home key points. A short review of future trends will close out the tutorial.

Instructor: Tim Denison is the Director of Neuroengineering for Medtronic Neuromodulation, and a Technical Fellow for Medtronic, the world's leading manufacturer of medical devices. In this role Tim helps guide the creation of sensor, actuator and algorithmic building blocks and architectural frameworks for future devices intended to treat nervous system disorders. Tim received his A.B. in Physics with honors from the University of Chicago, and an S.M. and Ph.D. in Electrical Engineering from MIT. He continues to actively support academic students through the MIT 6-A co-op program, as well as serving as a frequent guest instructor for courses such as TU Delft Smart Sensor Systems and the NYAS Brain Forum. His extramural roles include serving on the IMMD section of the ISSCC technical program committee and the organization committee for the National Academy of Engineering's "Frontiers in Engineering."

F1: Advanced Transmitters for Wireless Infrastructure

Organizers: **Gabriele Manganaro,** *Analog Devices, Wilmington, MA*
Domine Leenaerts, *NXP Semiconductors, Eindhoven, The Netherlands*

Chair: **Francesco Dantoni,** *Texas Instruments, Dallas, TX*

Committee: **Andrea Baschirotto,** *University of Milan-Bicocca, Milan, Italy*
Bogdan Staszewski, *Technical University of Delft, Delft, The Netherlands*
Nikolaus Klemmer, *Texas Instruments, Dallas, Texas*
Seongchol Hong, *KAIST, Daejeon, Korea*

This forum will cover present and future transmitters in wireless infrastructure applications, like basestations for cellular mobile communication. Future digitized transmitter architectures will most likely be based upon the use of advanced RF-DACs or ultra-high speed DACs in combination with up-conversion techniques. These digital transmitter architectures need flexible (re-configurable) power amplifiers that make use of advanced techniques like multiway Doherty or envelope tracking. Enhanced linearization techniques need to be applied in the transmitter to cope with the stringent linearity demands, while advanced calibration techniques and other design techniques will be needed to overcome circuit block impairments.

Forum Agenda

Time	Topic
8:00	Breakfast
8:20	**Introduction** **Francesco Dantoni,** *Texas Instruments, Milan, Italy*
8:30	**Begin at the Beginning for Transmitter Design** **Earl McCune,** *RF Communications Consulting, Santa Clara, CA*
9:15	**Flexible Digital-Centric RF-DAC Based Transmitter** **Renato Negra,** *RWTH Aachen University, Aachen, Germany*
10:00	Break
10:15	**Current-Steering DACs for Direct RF Transmission** **Klaas Bult,** *Broadcom, Bunnik, The Netherlands*
10:45	**Dynamic Element Matching and Calibration for Nyquist-Rate DACs** **Ian Galton,** *University of California, San Diego, CA*
11:15	**Low-Power RF Domain PA Linearization for Infrastructure Transmitters** **Olivier Charlon,** *Scintera Networks, Sunnyvale, CA*
11:45	**Flexible Doherty Power Amplifiers for Base Station Applications -Multiway and ET Operations** **Bumman Kim,** *Pohang University of Science and Technology, Pohang, Korea*
12:15	Lunch
1:15	**Case Study: System and Design Aspects of State-of-the-Art Communication DACs** **Martin Clara,** *Lantiq, Villach, Austria*
1:45	Panel Discussion
2:45	Conclusion

F2: Ultra-Low Voltage VLSIs for Energy-Efficient Systems

Organizer/Chair: **Ken Takeuchi,** *University of Tokyo, Tokyo, Japan*
Co-Chair: **Ken Chang,** *Xilinx, San Jose, CA*

Committee: **Ken Takeuchi,** *University of Tokyo, Tokyo, Japan*
Ken Chang, *Xilinx, San Jose, CA*
Kevin Zhang, *Intel, Hillsboro, OR*
Tadaaki Yamauchi, *Renesas Electronics, Itami, Japan*
Roberto Gastaldi, *Numonyx, Brianza, Italy*

Energy efficient VLSIs with an ultra-low voltage power supply down to 0.5V are in growing demand for various applications, (e.g., secure card, sensor node, and medical systems) where power is supplied by RF wave, solar cells and small batteries. Various technological challenges, including PVT variations, low operating voltage margin, increased stand-by power consumption and low driving current, must be addressed. This forum provides an overview of the technical challenges as well as most recent circuit advances in key building blocks for digital/analog VLSI applications.

Forum Agenda

Time	Topic
8:00	Breakfast
8:20	**Introduction** **Ken Takeuchi,** *University of Tokyo, Tokyo, Japan*
8:30	**Squeezing a IA Computer in a Smartphone** **Ticky Thakkar,** *Intel, Hillsboro, OR*
9:20	**FDSOI: an Innovative Technology for Low-Vdd / High-performance Logic** **Frederic Boeuf,** *ST Microelectronics, Crolles, France*
10:10	Break
10:25	**Pitfalls in Deep-Volt Logic Design** **Takayasu Sakurai,** *University of Tokyo, Tokyo, Japan*
11:15	**Ultra Low Voltage Logic and Embedded Memories** **Kaushik Roy,** *Purdue University, West Lafayette, IN*
12:05	Lunch
1:00	**Low Energy Consumption as a Qualifying Factor for Embedded Non Volatile Memories** **Guido De Sandre,** *ST Microelectronics, Agrate Brianza, Italy*
1:50	**System Tradeoffs for Efficient Embedded Power Management** **Baher Haroun,** *Texas Instruments, Dallas, TX*
2:40	Break
2:55	**Voltage Generator with Supply Below the Bandgap Voltage** **Philip K.T. Mok,** *Hong Kong University of Science and Technology, Hong Kong, China*
3:45	**Voltage Scaling Trade-offs in VCOs, PLLs and I/Os** **Peter Kinget,** *Columbia University, New York, NY*
4:35	**Make the Low Voltage ADC/DAC Energy Efficient** **Akira Matsuzawa,** *Tokyo Institute of Technology, Tokyo, Japan*
5:25	Conclusion

ES0: STUDENT RESEARCH PREVIEW (SRP)

The Student Research Preview (SRP) will highlight selected student research projects in progress. The SRP consists of 18-or-so, 5-minute presentations by graduate students (Masters and PhDs) from around the world, which have been selected on the basis of a short submission concerning their on-going research. Selection is based on the technical quality and innovation of the work. This year, the SRP will be presented in three sessions: Analog & Mixed-Signal Circuits, RF & Wireless Circuits, and Technology Directions & Bio-Related Sensors.

The Student Research Preview will begin with a brief talk by the distinguished circuit designer, Professor Paul Gray, UC Berkeley. It is scheduled for the evening of Sunday, February 20th, starting at 7:30pm, and is open to all ISSCC registrants.

Chair:	**Jan Van der Spiegel**	*University of Pennsylvania*
Co-Chair:	**Makoto Ikeda**	*University of Tokyo, Japan*
Co-Chair:	**Eugenio Cantatore**	*Technical University Eindhoven, The Netherlands*
Secretary:	**SeongHwan Cho**	*KAIST, Korea*
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SeongHwan Cho	*KAIST, Korea*
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Elio Guidetti	*STMicroelectronics, France*
Hossein Hashemi	*University of Southern California*
Makoto Ikeda	*University of Tokyo, Japan*
Adreas Kaiser	*ISEN, France*
Takayuki Kawahara	*Hitachi, Japan*
Shen-luan Liu	*National Taiwan University, Taiwan*
Kofi Makinwa	*Technical University Delft, The Netherlands*
Akira Matsuzawa	*Tokyo Institute Technology, Japan*
Dejan Marković	*University of Californian, Los Angeles*
Shahriar Mirabbasi	*University of British Columbia, Canada*
Boris Murmann	*Stanford University*
Sameer Sonkusale	*Tufts University*
Jan Van der Spiegel	*University of Pennsylvania*
Marian Verhelst	*Intel*
Zhihua Wang	*Tsinghua University, China*

ES1: Data Converter Breakthroughs in Retrospect

Organizer: **Boris Murmann,** *Stanford University, Stanford, CA*
Chair: **Venu Gopinathan,** *Texas Instruments, Bangalore, India*

The performance of data converters has been pushed relentlessly over the years, leveraging advancements in scaling and design techniques that exploit the high density and speed of modern process technology. However, most of the underlying architectures in use today were conceived decades ago, and are nowadays considered fundamental in nature. Were these architectures viewed as fundamental, potentially long lasting breakthroughs when they were first demonstrated? In this session, we bring together four pioneers of data converter design to review the invention and progression of the basic data converter architectures.

Time	Topic
8:00	**The Evolution of Oversampling ADCs** **Bruce A. Wooley,** *Stanford University, Stanford, CA*
8:30	**MOS A/D Converters: Development of Capacitor Array ADCs and Digital Self-Calibration** **Hae-Seung Lee,** *MIT, Cambridge, MA*
9:00	**Early Monolithic Pipelined ADCs** **Stephen H. Lewis,** *University of California, Davis, CA*
9:30	**High Sample Rate Signal-Reconstruction DACs - a Retrospective** **Doug Mercer,** *Analog Devices, Wilmington, MA*

ES2: Wireless Sensor Systems: Solution and Technology

Chair/ Co-organizer **Pascal Urard,** *STMicroelectronics, Crolles, France*
Co-organizer **Jun Ohta,** *NAIST, Nara, Japan*

We are beginning to see Wireless Sensor Network (WSN) solutions introduced in the market. However, the business is not booming. Does it mean we need additional innovation to boost market adoption?

The aim of this SET is to present current WSN solutions, and understand what additional innovations may be necessary to boost WSN adoption.

This session will present some existing commercial solutions, plus some advanced techniques on ultra-low-power design, energy scavenging, energy storage, and sensor integration that could be applied to WSN. Added values of these techniques in WSN will be explained.

Time	Topic
8:00	**Commercial WSN: Low Power Hardware, Efficient Stacks** **Kris Pister,** *Dust Networks, Hayward, CA*
8:20	**Ultra-Low Power Design for WSN** **Dennis Sylvester,** *University of Michigan, Ann Arbor, MI*
8:40	**Heterogeneous Integration for Sensing and Wireless Systems** **Masayoshi Esashi,** *Tohoku University & Memsas, Sendai, Japan*
9:00	**Advanced Energy Storage Techniques** **Raphaël Salot,** *CEA-LITEN, Grenoble, France*
9:20	**Advanced Energy Harvesting Techniques** **Ruud Vullers,** *imec/Holst Centre, Eindhoven, The Netherlands*
9:40	**Open Discussion**

PLENARY SESSION — INVITED PAPERS

Chair: **Anantha Chandrakasan,** *Massachusetts Institute of Technology, Cambridge, MA*
ISSCC Conference Chair

Associate Chair:
Wanda Gass, *Texas Instruments, Dallas TX*
ISSCC Program Committee Chair

FORMAL OPENING OF THE CONFERENCE **8:15AM**

1.1 **New Interfaces to the Body Through Implantable System Integration** **8:30AM**
Stephen Oesterle, *Senior VP, Medtronic, Minneapolis, MN*

The pace of technological change continues to enable new possibilities of how we interface with our world. An engine of that change is highlighted by Moore's law, which has driven the semiconductor market for the last 40 years. This engine enabled a diverse set of capabilities for sensing, processing, actuating, and communicating with the environment; it is also being applied to revolutionize health care.

From the first implantable cardiac pacemaker, semiconductor electronics were applied to both save lives and improve quality of life. The initial success from pacing transferred into new applications, including modulation of cellular networks for treating neurological disorders and systems that grow ever closer to realizing an artificial pancreas. Emerging technological possibilities promise to continue this trend of expanding applications with greater capabilities. To optimize treatment, however, a systems approach must be taken when designing both the implanted device and the entire care pathway.

The system to support an implantable device requires attention to three key design abstractions: the interfaces to the device, how information flows and is processed, and energy management. As Moore's law slows for simple planar scaling of integrated circuits, electronics packaging technologies and other complimentary work termed "More than Moore" are enabling new system strategies that address these abstracted constraints in a symbiotic manner:

Interfaces: The primary physical interface is the interaction of the device and the human body. The goal is to make the device as small as possible while not trading off other performance metrics. Smaller devices enable less-invasive procedures with less morbidity, yielding simpler and lower-cost procedures to an expanded group of implanters. Advanced miniaturization also enables new form factors for shorter leads, potentially leadless systems, and independent devices that communicate with each other as a body area network. Another key interface is the transfer of data to and from the implant, highlighting the need for information management.

Information Flow and Processing: Better connected devices represent the increased expectations patients and physicians have for seamless information exchange. Increased amounts of data, however, must also be processed into high-value information and communicated securely to physicians and electronic medical records. Systems that incorporate sensors, algorithms and closed-loop feedback offer these opportunities for better therapies and management of chronic disease. The challenges to realize the full promise of "smart" systems include: sensor biostability, power-efficient signal processing, acceptable algorithm sensitivity, and specificity in real-world environments.

Energy Management: In order to fully reap the benefit of a smaller smarter implant, an acceptable energy strategy must also be identified. Advancements in integration are also introducing new methods for storing and managing power. Lower power and energy requirements for circuit functions directly translate to being able to use a smaller battery for the device.

Despite recent technological advancements, significant unmet needs remain, and integrated circuit technologies have the opportunity to be further optimized for application in the medical-device space. This requires careful attention to system-level objectives concerning what problems are being solved. While none of these new technologies will transform care in isolation, if integrated as part of a well-defined system, they can make significant contributions to improving patient outcomes and easing clinical burden.

1.2 Game-Changing Opportunities for Wireless Personal Healthcare and Lifestyle **9:05AM**

Jo De Boeck, *Senior VP, imec / Holst Centre, Leuven, Belgium*

Silicon is playing a key enabling role in the emerging healthcare paradigm: disease-centric medical care, patient-centric decision making and therapy, proactive personalized and ubiquitous diagnosis and treatment. The necessity of healthcare which is personalized, predictive, preventive, and participatory, all at the same time, implies massive amounts of measurement, data, and associated ICT infrastructure.

In this vision, the data will be taken mostly "on the move" in residential or desolate settings, with minimal intervention from trained professionals. Patient-centric data, currently mostly self-reported, are key in performing clinical trials, reaching a diagnosis, checking on treatment evolution, evaluating post-treatment health-related quality of life, and, increasingly also in the creation of patient social networks. The quality of self-reported data is often questioned. Connected devices that provide such data in an acceptable unobtrusive way, with guaranteed quality, privacy, and identity, will make all the difference. Such infrastructure will further enable daily monitoring of so-called high- yielding micro-events that announce a problematic situation well before symptoms arise.

In multiple studies, even relatively simple wireless ECG (Electro-Cardiogram) patches are starting to impact the efficiency of care and the reduction of hospitalization time. The next-generation multi-sensory smart patch will be a game changer in health care and a prime driver for a technology roadmap with radical steps in efficiency and effectiveness of system energy consumption, signal acquisition, signal conditioning, on-board signal processing and decision making, and wireless data transmission.

We will see patches and other body-worn devices connect to the healthcare infrastructure with further extended power autonomy and with the ability to smell, to listen, and even to feel. We will need technologies to deliver these in flexible stretchable formats. To achieve this, cost-effective and ecological manufacturing challenges will also have to be tackled. For each application, hard constraints will have to be met on system reliability (QoS), cost, and energy budget.

Game changers at the level of the technology are only meaningful and efficient if they are driven by application needs. There is rapid progress in-close and in-depth interactions between the medical and the electronics community illustrated by the world-wide healthcare-related trials with wireless sensors in body-area-network configurations. This technology validation for personal diagnostic and theranostic products clearly drives game-changing circuit-, system-, and business-model innovation.

Many visionary applications such as brain-computer interfaces sound like magic. However, with every new generation of technology and application algorithms, wearable wireless systems become less obtrusive and more autonomous. The well-targeted use of these future generations for monitoring stress, emotions, etc, will revolutionize how we live, play, and work. None of these developments heralds a "Brave New World", but, instead, fosters and strengthens the individual in their quest for a healthier, happier, and longer life.

1.3 Eco-Friendly Semiconductor Technologies for Healthy Living **9:40AM**

Oh-Hyun Kwon, *President, Samsung Electronics, Giheung, Korea*

In the history of human kind, we have witnessed remarkable development and growth of industry. Everywhere, from home appliances to space shuttles, such industrial growth has made human life more productive and convenient. However, it has also created unprecedented levels of pollution, environmental destruction and climate change, and, ironically, has become a serious threat to healthy human life.

To rescue mankind from the global environmental crisis, all industry is now expected to convert to eco-friendly technologies in a significantly greater degree than before. Recent studies have shown that this crisis is caused mainly by an extensive amount of energy consumption and green-house gas creation, and, therefore, the key effort is to reduce energy requirements of all industry.

Thus, as an important segment of world industry, the semiconductor manufacturers must participate in this effort to slow down the environmental crisis and enable healthy human life. As semiconductor products are pervasive, constituting a large portion of global energy consumption, reduction of their power consumption is one effective way to contribute. As well, the semiconductor manufacturing process consumes large amounts of energy; thus, the industry itself must reduce the energy used in its processing and make it more efficient.

From the semiconductor product perspective, it is useful to expand the usage of semiconductor products and in replacing conventional sizable mechanical parts, which are very energy hungry with relatively small and energy-efficient semiconductor products. But, the semiconductor industry must make an effort to improve energy-efficiency of each such product.

Energy efficiency in semiconductor products is achievable through coordination of the entire cycle of product development: design (including architecture), design methodology, process technology, and packaging. Moreover, co-operation with other industries can be very useful in reducing world-wide energy consumption: early interaction with software-industry providers and users will increase product efficiency; interaction with the electrical- power equipment-manufacturing, generation, and distribution industries, will increase the efficiency of the world's electric-power infrastructure and likely impact the design and application of products. Recent progress in the creation of low-power multi-core processors, green memory solutions, high-bandwidth memory interfaces, 3D-packaging technologies, low-leakage/low-supply process technology, low-power design methodologies, and smart-grid power systems are already indicative of such achievements.

Concerning the use of energy in semiconductor manufacturing itself, the industry is reviewing the main causes of energy inefficiency in manufacturing equipment and operation, with a view to reducing the large standby-power loss within and across manufacturing equipment. To address the inefficiency of fabrication equipment, semiconductor manufacturers must lead a collaboration with equipment suppliers. Such collaboration is likely to lead to reduced energy consumption of individual pieces of equipment, as well as, of entire manufacturing facilities.

The semiconductor industry continues to respond to society's ongoing challenges for products supporting a better life. In this continuing process, energy-efficient semiconductor products and eco-friendly manufacturing processes are the answers to new environmental challenges, likely to enable an improving environment, ultimately saving us and our planet!

BREAK **10:15AM**

ISSCC, SSCS, IEEE AWARD PRESENTATIONS **10:30AM**

1.4 Beyond the Horizon: The Next 10x Reduction in Power - Challenges and Solutions **10:50AM**

Moderator: **Jan Rabaey**, *University of California, Berkeley, Berkeley, CA*

Domain Experts: **Hugo DeMan**, *imec, Leuven, Belgium*
Takayasu Sakurai, *University of Tokyo, Tokyo, Japan*
Mark Horowitz, *Stanford University, Palo Alto, CA*

The energy efficiency of electronic circuits has dramatically improved over the past two decades. At the same time, computation, storage, and communication demands continue to grow with emerging wireless multimedia devices. In this inaugural Plenary Technology-Roundtable event, experts will discuss the opportunities to achieve the next order-of-magnitude reduction in energy consumption across various domains, including analog, digital, RF, and memory. The line between analog and digital continues to blur, as analog circuits are enhanced by applying digital corrections to compensate for increased analog component variability with process scaling. As well, digital will incorporate more analog to become more adaptive; for example, to optimize operating voltages at a fine-grain to match workloads and process variations. Memory circuits will need to use a system-level approach which requires bit-cell optimization, low-voltage operation with integrated regulators, 3D Through-Silicon Vias (TSV), and process optimization. RF transceivers will continue to trend toward highly-digital architectures.

The role of process-technology innovation and CAD tools will also be discussed. Future process technology will deliver new transistor structures and higher-mobility channel materials for low-voltage digital circuits. TSVs will be important in reducing I/O power and the length of on-chip interconnects. For RF, integrated inductors and transformers with significantly lower resistance will be the challenge. Future CAD tools optimizing energy will focus on co-design of packaging, architecture, power sources, and antenna to provide the best system solution. Domain experts will challenge the distinguished panelists to suggest directions and help create a roadmap for next-generation energy-efficient electronics.

Panelists:

Jack Sun, *TSMC, Hsin-Chu, Taiwan*
Dan Dobberpuhl, *Consultant, Monterey, CA*
Kiyoo Itoh, *Hitachi, Tokyo, Japan*
Philippe Magarshack, *STMicroelectronics, Crolles, France*
Asad Abidi, *University of California, Los Angeles, Los Angeles, CA*
Hermann Eul, *Infineon Technologies, Neubiberg, Germany*

CONCLUSION 12:05PM

TECHNOLOGIES FOR HEALTH

Session Chair: ***Uming Ko,*** *Texas Instruments, Dallas, TX*
Associate Chair: ***Eric Colinet,*** *CEA-LETI, Grenoble, France*

2.1 A 0.24nJ/b Wireless Body-Area-Network Transceiver with Scalable Double-FSK Modulation — 1:30 PM

J. Bae, K. Song, H. Lee, H. Cho, L. Yan, H-J. Yoo
KAIST, Daejeon, Korea

A 0.24nJ/b with 250μV sensitivity body channel transceiver is presented for full WBAN compatibility. Its low energy consumption is possible by resonance matching, context-aware sensor, and low-power scalable double-FSK modulation scheme, which adopts the reconfigurable LNA/driver, current-reuse wide-band demodulator, and divider-based LO generation with duty-cycle corrector. The 2.5×5mm^2 transceiver is fabricated in 0.18μm CMOS.

2.2 A 75μW Real-Time Scalable Network Controller and a 25μW ExG Sensor IC for Compact Sleep-Monitoring Applications — 2:00 PM

S. Lee, L. Yan, T. Roh, S. Hong, H-J. Yoo
KAIST, Daejeon, Korea

A 5g compact sleep-monitoring system is proposed based on a 75μW real-time scalable network controller and 25μW ExG sensors. Its form factor is 1/9th that of the previous work with energy consumption of 0.33pJ/b. The low power consumption is made possible by a Linked List Manager, Adaptive Dual-Mode Controller, and Continuous Data Transmitter.

2.3 A 3μW Wirelessly Powered CMOS Glucose Sensor for an Active Contact Lens — 2:30 PM

Y-T. Liao, H. Yao, B. Parviz, B. Otis
University of Washington, Seattle, WA

This paper presents a non-invasive wireless glucose sensor for continuous health monitoring. The glucose sensor has a measured sensitivity of 1.67μAmm^{-2}mM^{-1}. The system is wirelessly powered and achieves a measured glucose range of 0-to-2mM while consuming 3μW from a regulated 1V supply. The whole chip area is 0.5mm^2 and requires no external components.

Break 3:00 PM

2.4 A 90nm CMOS SoC UWB Pulse Radar for Respiratory Rate Monitoring — 3:15 PM

D. Zito[1,2], D. Pepe[2], M. Mincica[2,3], F. Zito[4]
[1]University College Cork, Cork, Ireland
[2]Tyndall National Institute, Cork, Ireland
[3]University of Pisa, Pisa, Italy
[4]University of Reggio Calabria, Reggio Calabria, Italy

A fully integrated UWB pulse radar for the RF contactless detection of vital signs is implemented in 90nm CMOS. The radar consumes 73mW from a 1.2V supply. The measurements show that the radar sensor detects movements (up to 2cm) of targets at 70cm and the respiratory rate of the person under test at 25cm.

2.5 A Broadband THz Imager in a Low-Cost CMOS Technology **3:45 PM**

F. Schuster[1,2], H. Videlier[2], A. Dupret[1], D. Coquillat[2], M. Sakowicz[2], J-P. Rostaing[1], M. Tchagaspanian[1], B. Giffard[1], W. Knap[2]
[1]CEA-LETI-MINATEC, Grenoble, France
[2]Université Montpellier 2 -CNRS UMR, Montpellier, France

A CMOS Imager for Terahertz imaging is presented. A MOSFET is coupled to a bow-tie antenna. Self-mixing allows direct conversion to the low frequency band used for light modulation. The imager includes an in-pixel low noise amplifier, and multiplexing circuitry for single-video output. Measurement results are presented with electrical performances and images.

2.6 A Programmable Implantable Micro-Stimulator SoC with Wireless Telemetry: Application in Closed-Loop Endocardial Stimulation for Cardiac Pacemaker **4:15 PM**

S-Y. Lee[1], Y-C. Su[1], M-C. Liang[1], J-H. Hong[1], C-H. Hsieh[1], C-M. Yang[1], Y-Y. Chen[2], H-Y. Lai[3], J-W. Lin[4], Q. Fang[5]
[1]National Chung Cheng University, Chia-Yi, Taiwan
[2]National Yang-Ming University, Taipei, Taiwan
[3]National Chiao Tung University, Hsinchu, Taiwan
[4]National Taiwan Univeristy, Hospital Yun-Lin Branch, Taiwan
[5]RMIT University, Melbourne, Australia

A 48μW implantable micro-stimulator SoC (IMSoC) with smart powering management, immediate signal acquisition, and wireless telemetry-and-recharging system, is proposed. A 0.81cm^3 wireless telemetry with accuracy protection handles the adjustable stimulus parameters for *in vivo* stimulated objective. Rat intracardiac electrograms are employed in the animal study.

2.7 A 660pW Multi-Stage Temperature-Compensated Timer for Ultra-Low-Power Wireless Sensor Node Synchronization **4:30 PM**

Y. Lee, B. Giridhar, Z. Foo, D. Sylvester, D. Blaauw
University of Michigan, Ann Arbor, MI

Accurate synchronization cycle time measurement is required for ultra-low-power wireless sensor nodes with stringent power budget. A multi-stage temperature-compensated gate-leakage based timer reduces rms jitter by 8.1× and synchronization uncertainty by 4.1× with 660pW power consumption. Effective temperature sensitivity is reduced to 31ppm/°C.

2.8 A Low-Power Fully Integrated RF Locked Loop for Miniature Atomic Clock **4:45 PM**

D. Ruffieux, M. Contaldo, J. Haesler, S. Lecomte
CSEM, Neuchatel, Switzerland

Miniature atomic clocks (MAC) need carefully designed RF electronics, which have to consume low power without affecting the clock accuracy. A low-power CMOS fully integrated frequency lock loop for MACs is presented. An Allan deviation 1s intercept point of $\sigma_y = 4\times10^{-10}$ is measured on a 10MHz clock for a 26.3mW consumption of the RF loop locked on an Rb^{87} cell for CPT interrogation.

Conclusion 5:15 PM

RF TECHNIQUES

Session Chair: ***Jan Craninckx,*** *imec, Leuven, Belgium*
Associate Chair: ***Jing-Hong Conan Zhan,*** *MediaTek, HsinChu, Taiwan*

3.1 Spur-Free All-Digital PLL in 65nm for Mobile Phones — 1:30 PM

R. B. Staszewski[1], K. Waheed[2], S. Vemulapalli[2], F. Dulger[2], J. Wallberg[2], C-M. Hung[2], O. Eliezer[2]
[1]Delft University of Technology, Delft, The Netherlands
[2]Texas Instruments, Dallas, TX

A 65nm all-digital PLL for cellular phones features arbitrary high data rate of modulating samples, free from injection-pulling spurs and ill-shaped quantization noise of TDC by means of dithering with dynamic adjustment of differential pair mismatches. Low power techniques, such as speculative clock retiming and asynchronous counter are used.

3.2 A 5.3GHz Digital-to-Time-Converter-Based Fractional-N All-Digital PLL — 2:00 PM

N. Pavlovic, J. Bergervoet
NXP Semiconductors, Eindhoven, The Netherlands

A digital-to-time converter (DTC)-based ADPLL architecture is presented. The DTC is used to lower the quantization noise of the phase detector. The 5.3GHz fractional-N ADPLL implemented in a 65nm CMOS technology achieves an in-band phase noise floor of -96dBc/Hz and in-band fractional spur power of -45dBc.

3.3 A 2.5GHz 32nm 0.35mm^2 3.5dB NF -5dBm P_{1dB} Fully Differential CMOS Push-Pull LNA with Integrated 34dBm T/R Switch and ESD Protection — 2:30 PM

C-T. Fu, H. Lakdawala, S. S. Taylor, K. Soumyanath
Intel, Hillsboro, OR

A flip-chip-packaged 2.5GHz, 0.35mm^2, 32nm Hi-k MG CMOS fully differential LNA integrated with TX/RX switch achieves 3.5dB NF, 11dB Gain, -5dBm P_{1dB} while drawing 11mA from a 1.8V supply. The TX switch handles 34dBm power with 1.1dB insertion loss and provides +300/-200V CDM ESD protection. This performance is enabled by push-pull topology and nested coupled inductors.

3.4 A 65nm CMOS Pulse-Width-Controlled Driver with 8V_{pp} Output Voltage for Switch-Mode RF PAs up to 3.6GHz — 2:45 PM

D. A. Calvillo-Cortes[1], M. Acar[2], M. P. van der Heijden[2], M. Apostolidou[2], L. C. de Vreede[1], D. Leenaerts[2], J. Sonsky[3]
[1]Delft University of Technology, Delft, The Netherlands
[2]NXP Semiconductors, Eindhoven, The Netherlands
[3]NXP-TSMC Research Center, Leuven, Belgium

An 8V_{pp} and pulse-width-controlled RF power driver is realized in baseline 1.2V 65nm CMOS, having an active area size of 0.16mm^2. The chip delivers a maximum output swing of 8.04V_{pp} to a 50Ω load with 9V supply, from 0.9 to 3.6GHz. The maximum on-resistance of the driver is 4.6Ω. A linear duty-cycle control range of 30.7% to 71.5% is observed at 2.4GHz. The high voltage reliable operation of the driver is obtained by using thin-oxide extended-drain MOS devices.

Break 3:00 PM

3.5 A Low-Power Process-Scalable Superheterodyne Receiver with Integrated High-Q Filters — 3:15 PM

A. Mirzaei[1], H. Darabi[1], D. Murphy[2]
[1]Broadcom, Irvine, CA
[2]University of California, Los Angeles, CA

A superheterodyne receiver utilizing integrated high-Q filters to condition the desired signal to be digitized by a bandpass ADC at an IF of 110MHz achieves a NF of 2.8dB and an IIP3 of -8.5dBm. Built of inverters, switches and MOS capacitors, it follows technology scaling, and is reconfigurable through a clock. The receiver including the dividers and LO path draws 12mA of battery current, and occupies 0.67mm^2 in 65nm CMOS.

3.6 A 40nm CMOS Highly Linear 0.4-to-6GHz Receiver Resilient to 0dBm Out-of-Band Blockers — 3:45 PM

J. Borremans[1], G. Mandal[1], V. Giannini[1], T. Sano[2], M. Ingels[1], B. Verbruggen[1], J. Craninckx[1]
[1]imec, Leuven, Belgium
[2]Renesas Electronics, Itami, Japan

A 2mm^2 highly-linear software-defined receiver in 40nm CMOS is presented that uses a 2.5V LNA and impedance-translational RF blocker filter for SAW-less operation. The complete RX chain of LNA, mixer, blocker rejection, channel filter and VGA achieves 3dB NF, +10dBm out-of-band IIP3 and +80dBm IIP2, while tolerating 0dBm blockers at 20MHz offset with acceptable blocker NF.

3.7 A 1.0-to-4.0GHz 65nm CMOS Four-Element Beamforming Receiver Using a Switched-Capacitor Vector Modulator with Approximate Sine Weighting via Charge Redistribution — 4:15 PM

M. C. Soer[1], E. A. Klumperink[1], B. Nauta[1], F. E. van Vliet[1,2]
[1]University of Twente, Enschede, The Netherlands
[2]TNO Science and Industry, The Hague, The Netherlands

A 4-element phased array receiver, with discrete-time switched-capacitor vector modulators, occupies 0.44mm^2 in 65nm CMOS while drawing 308mW from 1.2V. Approximate-sine weighting is implemented through charge-redistribution. This enables a one-to-one mapping between control settings and effective phase shifts, resulting in a 1.4° phase and 0.4dB gain error (RMS).

3.8 A Harmonic Rejection Mixer Robust to RF Device Mismatches — 4:45 PM

A. A. Rafi, A. Piovaccari, P. Vancorenland, T. Tuttle
Silicon Laboratories, Austin, TX

A harmonic-rejection mixer that has reduced sensitivity to mismatches in RF devices is fabricated in a 0.110µm CMOS process. While conventional HR mixers achieve HR ratios only in the 30-to-40dB range, this mixer achieves 3rd, 5th and 7th HR ratios in excess of 52dB. This mixer also rejects flicker noise, has improved quadrature matching and has a high IIP2 of 75dBm.

Conclusion 5:15 PM

ENTERPRISE PROCESSORS & COMPONENTS

Session Chair: ***Joshua Friedrich,*** *IBM, Austin, TX*
Associate Chair: ***Takashi Miyamori,*** *Toshiba Center for Semiconductor Research and Development, Kawasaki, Japan*

4.1 A 5.2GHz Microprocessor Chip for the IBM zEnterprise™ System — 1:30 PM

J. Warnock[1], Y. Chan[2], W. Huott[2], S. Carey[2], M. Fee[2], H. Wen[3], M. Saccamango[2], F. Malgioglio[2], P. Meaney[2], D. Plass[2], Y-H. Chan[2], M. Mayo[2], G. Mayer[4], L. Sigal[5], D. Rude[2], R. Averill[2], M. Wood[2], T. Strach[4], H. Smith[2], B. Curran[2], E. Schwarz[2], L. Eisen[3], D. Malone[2], S. Weitzel[3], P-K. Mak[2], T. McPherson[2], C. Webb[2]
[1]IBM Systems and Technology Group, Yorktown Heights, NY
[2]IBM Systems and Technology Group, Poughkeepsie, NY
[3]IBM Systems and Technology Group, Austin, TX
[4]IBM Systems and Technology Group, Boeblingen, Germany
[5]IBM Research, Yorktown Heights, NY

The microprocessor chip for the IBM zEnterprise 196 system contains 4 processor cores running at 5.2GHz, and includes an on-chip high-speed 24MB shared DRAM L3 cache. To meet this high-frequency design objective, many challenges were met, including significant timing, power and noise problems which had to be resolved.

4.2 Dynamic Hit Logic with Embedded 8Kb SRAM in 45nm SOI for the zEnterprise™ Processor — 2:00 PM

A. R. Pelella, Y. H. Chan, B. Balakrishnan, P. Patel, D. Rodko, R. E. Serton
IBM Systems and Technology Group, Poughkeepsie, NY

Dynamic hit logic with an embedded 8Kbit SRAM is described. The 14b hit logic uses a search-for-a-hit scheme with programmable launch and reset clocks. Array BIST provides both the hit logic and SRAM with full at-speed test coverage. The SRAM (1R/1W) uses 45nm SOI 6T cell with domino hierarchical dual-read bitlines.

4.3 A 32nm Westmere-EX Xeon® Enterprise Processor — 2:15 PM

S. Sawant, U. Desai, G. Shamanna, L. Sharma, M. Ranade, A. Agarwal, S. Dakshinamurthy, R. Narayanan
Intel, Bangalore, India

This monolithic 10-core Xeon® Processor is designed in a 32nm 9M process with a shared L3 cache. Low power modes are introduced to cut idle power compared to the previous generation processor. A 2nd order CTLE and temperature compensation are implemented in the I/O receiver to enable link survivability even with low RX margins. Core- and cache-recovery techniques maximize yield.

4.4 Godson-3B: A 1GHz 40W 8-Core 128GFLOPS Processor in 65nm CMOS — 2:30 PM

W. Hu[1,2], R. Wang[1,2], Y. Chen[1,2], B. Fan[1,2], S. Zhong[1,2], X. Gao[2], Z. Qi[1,2], X. Yang[2]
[1]Chinese Academy of Sciences, Beijing, China
[2]Loongson Technologies, Beijing, China

The Godson-3B processor is an 8-core high-performance processor implemented in a 65nm CMOS LP/GP mixed process with 7 layers of Cu metallization. It contains 582.6M transistors in a 299.8mm^2 area. The highest frequency of Godson-3B is 1.05GHz. Its peak performance is 128/256GFLOPS for double/single-precision with 40W power consumption.

Break 3:00 PM

4.5 Design Solutions for the Bulldozer 32nm SOI 2-Core Processor Module in an 8-Core CPU — 3:15 PM

T. Fischer[1], S. Arekapudi[2], E. Busta[1], C. Dietz[3], M. Golden[2], S. Hilker[2], A. Horiuchi[1], K. A. Hurd[1], D. Johnson[1], H. McIntyre[2], S. Naffziger[1], J. Vinh[2], J. White[4], K. Wilcox[4]
[1]AMD, Fort Collins, CO
[2]AMD, Sunnyvale, CA
[3]AMD, Austin, TX
[4]AMD, Boxborough, MA

The Bulldozer 2-core CPU module contains 213M transistors in an 11-metal layer 32nm high-k metal-gate SOI CMOS process and is designed to operate from 0.8 to 1.3V. This micro-architecture improves performance and frequency while reducing area and power over a previous AMD x86-64 CPU in the same process. The design reduces the number of gates/cycle relative to prior designs, achieving 3.5GHz+ operation in an area (including 2MB L2 cache) of 30.9mm^2.

4.6 40-Entry Unified Out-of-Order Scheduler and Integer Execution Unit for the AMD Bulldozer x86-64 Core — 3:45 PM

M. Golden, S. Arekapudi, J. Vinh
AMD, Sunnyvale, CA

A 40-instruction out-of-order scheduler issues four operations per cycle and supports single-cycle operation wakeup. The integer execution unit supports single-cycle bypass between four functional units. Critical paths are implemented without exotic circuit techniques or heavy reliance on full-custom design. Architectural choices minimize power consumption.

4.7 Clock Generation for a 32nm Server Processor with Scalable Cores — 4:15 PM

S. Li, A. Krishnakumar, E. Helder, R. Nicholson, V. Jia
Intel, Santa Clara, CA

This paper describes the clock generation system of a multi-core processor on a 32nm CMOS process, featuring Intel® QuickPath Interconnect, PCI Express and DDR3. The clock system is designed for modularity and scalability, with a unique clock distribution structure for low skew and low power. A dedicated PLL is used for the internal high-speed data link for low data-transport latency.

4.8 A 32nm 3.1 Billion Transistor 12-Wide-Issue Itanium® Processor for Mission-Critical Servers — 4:45 PM

R. J. Riedlinger[1], R. Bhatia[1], L. Biro[2], B. Bowhill[2], E. Fetzer[1], P. Gronowski[2], T. Grutkowski[1]
[1]Intel, Fort Collins, CO
[2]Intel, Hudson, MA

An Itanium® processor implemented in 32nm CMOS with 9 layers of Cu contains 3.1 billion transistors. The die measures 18.2×29.9mm^2. The processor has 8 multi-threaded cores, a ring-based system interface and combined cache on the die is 50MB. High speed links allow for peak processor-to-processor bandwidth of up to 128GB/s and memory bandwidth of up to 45GB/s.

Conclusion 5:15 PM

PLLs

Session Chair: ***Ivan Bietti,*** *STMicroelectronics, Grenoble, France*
Associate Chair: ***Tsung-Hsien Lin,*** *National Taiwan University, Taipei, Taiwan*

5.1 A 2.9-to-4.0GHz Fractional-N Digital PLL with Bang-Bang Phase Detector and 560fs_{rms} Integrated Jitter at 4.5mW Power — 1:30 PM

D. Tasca, M. Zanuso, G. Marzin, S. Levantino, C. Samori, A. L. Lacaita
Politecnico di Milano, Milan, Italy

A ΔΣ fractional-N digital PLL combining a single-bit TDC and a 10b feedback controllable delay achieves RMS jitter (3kHz to 30MHz) lower than 560fs_{rms} over the 2.92-to-4.05GHz range, even in the worst-case of fractional spur falling within the PLL bandwidth. The 40MHz reference spur is below -72dBc. The power dissipation is 4.5mW and the core area is 0.22mm^2 in 65nm CMOS.

5.2 An Injection-Locked Ring PLL with Self-Aligned Injection Window — 2:00 PM

C-F. Liang, K-J. Hsiao
MediaTek, Hsinchu, Taiwan

An architecture for injection-locked ring PLL is proposed to ensure the injection timing. Unlike previous works, it adjusts the injection window automatically without introducing extra delay-locked loops. By applying this technique with a 27MHz crystal oscillator, the phase noise within a 5MHz bandwidth is significantly reduced while the loop stability is well maintained. The 55nm CMOS PLL achieves integrated rms jitter (1kHz to 40MHz) of 2.4ps, while consuming 6.9mW and occupying 0.03mm^2.

5.3 A 0.4-to-3GHz Digital PLL with Supply-Noise Cancellation Using Deterministic Background Calibration — 2:30 PM

A. Elshazly, R. Inti, W. Yin, B. Young, P. Hanumolu
Oregon State University, Corvallis, OR

A digital PLL uses deterministic background calibration to accurately cancel supply-noise over a wide operating range (0.4 to 3GHz) and PVT variations. Fabricated in 0.13μm CMOS, the ring-oscillator-based DPLL consumes 2.65mW at 1.5GHz, and the cancellation circuitry reduces its peak-to-peak jitter from 330ps to 50ps in the presence of 30mV_{pp} supply noise.

Break 3:00 PM

5.4 A 0.1-f_{ref} BW 1GHz Fractional-N PLL with FIR-Embedded Phase-Interpolator-Based Noise Filtering **3:15 PM**

D-W. Jee, Y. Suh, H-J. Park, J-Y. Sim
Pohang University of Science and Technology, Pohang, Korea

A 1 GHz ΔΣ fractional-N PLL with noise filtering by FIR-embedded phase interpolator is implemented in a 0.13μm CMOS technology. The designed PLL reduces phase noise by 34dB, showing an in-band noise of -106dBc/Hz at 100kHz and out-of-band noise of -107.5dBc/Hz at 6MHz, which are integer-N PLL comparable result even with 0.1f_{ref} BW.

5.5 A Scalable sub-1.2mW 300MHz-to-1.5GHz Host-Clock PLL for System-on-Chip in 32nm CMOS **3:45 PM**

H-J. Lee, A. M. Kern, S. Hyvonen, I. A. Young
Intel, Hillsboro, OR

A compact low-power 300-to-1500MHz PLL with a resistor-less loop filter providing process scalability is presented for host clocking of a system-on-chip. The PLL occupies 0.046mm^2 in a 32nm CMOS process and draws 0.4 to 1.15mA from a 1V supply. The PLL loop bandwidth automatically tracks reference frequency to maintain unconditional loop stability.

5.6 A 570fs_{rms} Integrated-Jitter Ring-VCO-Based 1.21GHz PLL with Hybrid Loop **4:15 PM**

A. Sai, T. Yamaji, T. Itakura
Toshiba, Kawasaki, Japan

A 1.21GHz PLL with a hybrid loop consisting of a type-II all-digital PLL and a type-I analog PLL is presented. The analog PLL with a divider-less 3-input PFD suppresses the phase noise of a ring digital/voltage-controlled oscillator within the loop bandwidth. The PLL achieves the integrated rms jitter of 570fs, draws 43mA from 1.2V supply and occupies 0.12mm^2 in 65nm CMOS.

5.7 A Rotary-Traveling-Wave-Oscillator-Based All-Digital PLL with a 32-Phase Embedded Phase-to-Digital Converter in 65nm CMOS **4:45 PM**

K. Takinami, R. Strandberg, P. C. Liang, G. Le Grand de Mercey, T. Wong, M. Hassibi
Panasonic, Cupertino, CA

This paper discusses the use of a rotary-traveling-wave oscillator (RTWO) in an ADPLL. The RTWO provides a natural structure for high precision phase-to-digital conversion that does not require period normalization. The prototype in 65nm CMOS achieves 5.6d° (3.9ps at 4GHz) phase resolution which results in -108dBc/Hz in-band phase noise for a 1MHz loop bandwidth. It consumes 45mW while generating 4GHz carrier frequency.

Conclusion 5:15 PM

SENSORS & ENERGY HARVESTING

Session Chair: ***Aaron Partridge,*** *SiTime, Sunnyvale, CA*
Associate Chair: ***Christoph Hagleitner,*** *IBM Research, Ruschlikon, Switzerland*

6.1 A Low-Power 3-Axis Digital-Output MEMS Gyroscope with Single Drive and Multiplexed Angular Rate Readout — 1:30 PM

L. Prandi[1], C. Caminada[1], L. Coronato[1], G. Cazzaniga[1], F. Biganzoli[1], R. Antonello[2], R. Oboe[2]
[1]STMicroelectronics, Cornaredo, Italy
[2]University of Padova, Vicenza, Italy

A 3.2×3.2mm² 3-axis 24µm-thick polysilicon surface micromachined gyro combining 3 tuning-forks in a single vibrating element is sensed by a 0.13µm HCMOS multiplexed digital readout electronics, achieving a 0.03dps/√Hz rate noise density, a ±0.04dps/°C ZRO and ±2% cross-axis sensitivities.

6.2 A 50mW CMOS Wind Sensor with ±4% Speed and ±2° Direction Error — 2:00 PM

J. Wu[1,2], Y. Chae[2], C. P. van Vroonhoven[2], K. A. Makinwa[2]
[1]Tsinghua University, Beijing, China
[2]Delft University of Technology, Delft, The Netherlands

A 2D thermal wind sensor is realized in a standard CMOS process. Two 2nd-order thermal ΣΔ modulators control and digitize the flow-dependent heat distribution in the sensor. The sensor measures wind speed and direction with errors of less than ±4% and ±2°, respectively. It dissipates 50mW, 9x less than a previous CMOS design and less than that of MEMS-based wind sensors.

6.3 A Telemetric Stress-Mapping CMOS Chip with 24 FET-Based Stress Sensors for Smart Orthodontic Brackets — 2:30 PM

M. Kuhl[1], P. Gieschke[1], D. Rossbach[1], S. A. Hilzensauer[1], P. Ruther[1], O. Paul[1], Y. Manoli[1,2]
[1]University of Freiburg - IMTEK, Freiburg, Germany
[2]HSG-IMIT, Villingen-Schwenningen, Germany

A CMOS stress-mapping system with 24 sensors is sensitive to in-plane shear stress or differences of normal stresses with a resolution better than 25kPa. The telemetrically powered system consisting of chip and microcoil communicates at 13.56MHz. Its dimensions of 2x2.5mm² permit the development of smart brackets for a direct force feedback in orthodontic treatments.

Break **3:00 PM**

6.4 A 21b ±40mV Range Read-Out IC for Bridge Transducers — 3:15 PM

R. Wu, J. H. Huijsing, K. A. Makinwa
Delft University of Technology, Delft, The Netherlands

This paper presents a 21b read-out IC (ROIC) with ±40mV full scale for precision bridge transducers and thermocouples. The ROIC employs dynamic element matching to achieve an INL of 5ppm and a gain drift of 1.2ppm/°C, multi-stage chopping to achieve a 1mHz 1/f noise corner at 16.2nV/√Hz, and nested chopping to achieve 200nV offset, while drawing 270µA from a 5V supply.

6.5 A ±1.5% Nonlinearity 0.1-to-100A Shunt Current Sensor Based on a 6kV Isolated Micro-Transformer for Electrical Vehicles and Home Automation — 3:45 PM

F. Rothan[1], H. Ihermet[1], B. Zongo[1], C. Condemine[1], H. Sibuet[1], P. Mas[2], M. Debarnot[2]
[1]CEA-LETI-MINATEC, Grenoble, France
[2]Schneider Electric, Grenoble, France

An integrated current sensor including a shunt, 2 micro-transformers for 6kV isolation, a chopper IC and a readout IC is presented. Current measurements are performed with a ±1.5% nonlinearity over a 0.1-to-100 A range. The signal BW ranges from DC to 20kHz, and the overall power consumption is 16mW. The microsystem fits in a 13×7.6mm² SO20 package.

6.6 Indirect X-ray Photon-Counting Image Sensor with 27T Pixel and 15e$^-_{rms}$ Accurate Threshold **4:00 PM**

B. Dierickx[1,2], B. Dupont[1], A. Defernez[1], N. Ahmed[1]
[1]Caeleste, Antwerp, Belgium
[2]Vrije Universiteit Brussel, Brussels, Belgium

A 16×16 pixel X-ray photon-counting array for indirect detection, i.e. in combination with a scintillator. To count charge packets smaller than 100 electrons it has a noise floor and a comparator threshold of about 15e$^-_{rms}$. Counting happens in a nonlinear fashion in the analog domain, yielding pixels with 27-to-40 transistors.

6.7 A 1.32pW/frame·pixel 1.2V CMOS Energy-Harvesting and Imaging (EHI) APS Imager **4:15 PM**

S. U. Ay
University of Idaho, Moscow, ID

A CMOS energy-harvesting and imaging (EHI) APS imager capable of 7.4fps video capture and 3.5μW power generation is designed, fabricated, and tested in 0.5μm CMOS. It has a 54×50 array of 21μm^2 EHI pixels, 10b supply-boosted SAR-ADC and charge-pump circuits consuming 14.25μW from 1.2V resulting in a lowest power imager with 1.32pW/frame·pixel.

6.8 5μW-to-10mW Input Power Range Inductive Boost Converter for Indoor Photovoltaic Energy Harvesting with Integrated Maximum Power Point Tracking Algorithm **4:45 PM**

Y. Qiu[1], C. Van Liempd[1], B. Op het Veld[2], P. G. Blanken[2], C. Van Hoof[3,4]
[1]imec - Holst Centre, Eindhoven, The Netherlands
[2]Philips Research Laboratories, Eindhoven, The Netherlands
[3]imec, Leuven, Belgium
[4]KU Leuven, Leuven, Belgium

An autonomous inductive boost converter for indoor photovoltaic harvesting with maximum power point tracking circuit is implemented in a commercial 0.25μm CMOS process. The converter can handle input power from 5μW up to 10mW and charge a battery or a super-capacitor up to 5V. Its control circuit consumes between 0.8 and 2.1μA depending on the input power level, resulting in a peak end-to-end efficiency of 70% when tracking a maximum input power of 17μW.

6.9 A Self-Supplied Inertial Piezoelectric Energy Harvester with Power-Management IC **5:00 PM**

E. Aktakka, R. L. Peterson, K. Najafi
University of Michigan, Ann Arbor, MI

A self-supplied energy-harvester platform is developed including a hybrid piezoelectric MEMS harvester integrated with power management IC for autonomous charging of an energy reservoir. The volume of the system is <0.3cm^3, and it can charge a 1mF reservoir from 0V to 1.25V in <15min with an applied 0.3g vibration at 69Hz.

Conclusion **5:15 PM**

ES3: Future System and Memory Architectures: Transformations by Technology and Applications

Chair/Co-organizer **Nicky Lu,** *Etron Technology, Hsinchu, Taiwan*
Co-organizer **Leland Chang,** *IBM, Yorktown Heights, NY*
Co-organizer **Daisaburo Takashima,** *Toshiba, Yokohama, Japan*

The emergence of new enabling technologies and applications paradigms will likely drive radical changes in the memory architecture of future systems. With multi-core CPU dies sporting embedded DRAM caches, ever-improving NAND flash storage densities for SSD and SCM, and 3D-integration technologies to bring everything together into a single package, possibilities abound for system enhancements throughout the memory hierarchy. At the same time, applications needs are rapidly evolving as the world shifts from a product-centric economy to a service- and experience-oriented economy focused on hardware such as smartphones, set-top boxes, and 3D digital TV. This evening session will discuss future system and memory architectures from perspectives spanning the 3 C's: computing, consumer electronics, and communications – considering both what new technology might offer and what new applications might need.

Time	Topic
8:00	**Using New Technologies in Post Scaling Era** **Jim Kahle,** *IBM, Austin, TX*
8:30	**Digital TV System Design and Future TV Direction** **Tomofumi Shimada,** *Toshiba, Tokyo, Japan*
9:00	**Smartphone Memory Architecture Challenges and Opportunities** **Raj Talluri,** *Qualcomm, San Diego, CA*
9:30	**Memory Architectures in the Petascale Era and Beyond: Challenges and Opportunities** **Stephen Pawlowski,** *Intel, Hillsboro, OR*

ES4: Body Area Networks: Technology, Solutions, and Standardization

Organizer: **Hoi-Jun Yoo,** *KAIST, Daejeon, Korea*
Chair: **Alison Burdett,** *Toumaz Technology, Abingdon, United Kingdom*

Recently, wireless protocols related to BAN (Body Area Networks) are under standardization by the IEEE 802.15 (Personal Area Networks, PAN) committee, to enable interoperability of a wide range of applications in the areas of medical support, healthcare monitoring and consumer wellness electronics. BAN requirements are closely related to PAN or WSN (wireless sensor network) technologies; however a major difference in BAN applications is that human body should be carefully considered not only as a possible communication medium or an obstacle to the signal transport, but also taking into account the possibility of physiological effects resulting from the chosen EM wave frequency.

This Special Evening Topic session will present the current status of Body Area Network standard development, and explore proposed solutions and applications with a strong focus on integrated circuit implementations.

Time	Topic
8:00	**Standardization of BAN: History, Major Issues & Current Status of TG6** **Arthur Astrin,** *Astrin Radio, Palo Alto, CA*
8:20	**MAC & Security Network Solutions for BAN** **Okundu Omeni,** *Toumaz Technology, Abingdon, United Kingdom*
8:40	**PHY Realization for BAN using Ultra-Wideband Technology** **Huang-Bang Li,** *NICT, Yokosuka, Japan*
9:00	**PHY Layers Issues and Narrowband Solutions for BAN** **Anuj Batra,** *Texas Instruments, Dallas, TX*
9:20	**BAN Realization with Body-Channel Communication** **Seong-Jun Song,** *Samsung, Suwon, Korea*
9:40	**Wireless Propagation and Coexistence for Medical BAN** **David Davenport,** *GE Global Research, Niskayuna, NY*
10:00	**Open Discussion**

EP1: Good, Bad, Ugly - 20 Years of Broadband Evolution: What's Next?

Organizer: **Jerry Lin**, *Ralink Technology, Hsinchu, Taiwan*
Co-Organizer: **Franz Dielacher**, *Infineon Technologies, Villach, Austria*
Co-Organizer: **Jing-Hong Conan Zhan**, *MediaTek, Hsinchu, Taiwan*
Moderator: **Bob Payne**, *Texas Instruments, Dallas, TX*

Internet users today have extremely high demands for bandwidth consuming content wherever they are and on multiple platforms, ranging from tiny screened phones to high-definition 3D home theaters. This has driven the rapid deployment of multiple broadband access solutions including legacy infrastructure-driven DSL and cable, the almost limitless bandwidth provided by optical fiber to the home (FTTH), and the on-the-go appeal of wireless solutions including 3G/4G cellular or WiMAX.

Over the past two decades, each of these technologies has successfully competed for the consumer's dollar, partly due to the differentiated ways data is accessed – televisions were naturally connected to the CATV infrastructure and cell phones were linked to a wireless basestation. These traditional boundaries are blurring as cell phone calls are placed over WiFi networks and video content is delivered via an ISP. The common denominator is data access and the delivery method is irrelevant to the end user.

As DSL continues to compete with cable and FTTH in the wireline space, more and more users are choosing wireless broadband solutions such as 3G, 4G, or even WiMAX for their home access. In this panel, we will review the good, the bad, and the ugly aspects of the recent history of broadband evolution and provide a vision of the future. What are the pros and cons of each technology? Do we need so many competing solutions? What will be the successful business models in the future – will everyone (or anyone) make money? Which ones will be the winners ten years from now? Experts from academia, chip suppliers, and broadband systems vendors will share their visions on future broadband markets and technologies. Take your seat and enjoy the debate!

Panelists:

Michiel Steyaert, *K. U. Leuven, Heverlee, Belgium*
Larry DeVito, *Analog Devices, Wilmington, MA*
Sven Mattisson, *Ericsson, Lund, Sweden*
David Borison, *Ralink Technology, Cupertino, CA*
Eric Yeh, *MediaTek, Hsinchu, Taiwan*
Stephen Palm, *Broadcom, Irvine, CA*

MULTIMEDIA & MOBILE

Session Chair: ***Pascal Urard,*** *STMicroelectronics, Crolles, France*
Associate Chair: ***Michael Phan,*** *Qualcomm, Raleigh, NC*

7.1 A 216fps 4096×2160p 3DTV Set-Top Box SoC for Free-Viewpoint 3DTV Applications — 8:30 AM

P-K. Tsung, P-C. Lin, K-Y. Chen, T-D. Chuang, H-J. Yang, S-Y. Chien, L-F. Ding, W-Y. Chen, C-C. Cheng, T-C. Chen, L-G. Chen
National Taiwan University, Taipei, Taiwan

A 216fps 4096×2160p 3DTV set-top box SoC is realized on a 5.76mm^2 die in 40nm CMOS. An MVC decoder and a free-viewpoint view synthesis (FVVS) engine are integrated to generate unlimited views for 3DTV/virtual reality. The developed 6D FVVS flow and a texture reorder cache provide a 9× to 40.5× higher throughput, save 93% of system bandwidth, and achieve 6.6× to 229× improvement in power efficiency.

7.2 A Highly Parallel and Scalable CABAC for Next-Generation Video Coding — 9:00 AM

V. Sze, A. P. Chandrakasan
Massachusetts Institute of Technology, Cambridge, MA

A 65nm silicon prototype of a pre-standard algorithm developed for HEVC ("H.265") called Massively Parallel CABAC that addresses a key bottleneck in the video decoder is presented. The scalable test-chip achieves a throughput of 24.11bins/cycle, which enables it to decode the max H.264/AVC bit-rate (300Mb/s) with a 16MHz clock at 0.7V, consuming 12.3pJ/bin. At 1.0V, it decodes a peak of 3026Mbins/s for a bit-rate of 2.3Gb/s, enough for QFHD at 186fps.

7.3 A 275mW Heterogeneous Multimedia Processor for IC-Stacking on Si-Interposer — 9:30 AM

H-E. Kim, J-S. Yoon, K-D. Hwang, Y-J. Kim, J-S. Park, L-S. Kim
KAIST, Daejeon, Korea

A multimedia processor embedding a reconfigurable transceiver pool is presented for IC-Stacking on Si-interposer. Configurable vector processing units for frame-level parallelism, a unified filtering unit with memory-access-efficient texturing algorithm, and a programmable shader integrating multiple cores are used to achieve 140GOPS/W, 5.8GFLOPS/W in full operation.

Break **10:00 AM**

7.4 A 57mW Embedded Mixed-Mode Neuro-Fuzzy Accelerator for Intelligent Multi-core Processor — 10:15 AM

J. Oh, J. Park, G. Kim, S. Lee, H-J. Yoo
KAIST, Daejeon, Korea

A 57mW mixed mode neuro-fuzzy accelerator with 655GOPS/W power efficiency is implemented for a portable embedded accelerator. It uses 1024 reconfigurable analog processing elements to enhance parallel computing power and a digital learning accelerator for energy-efficient learning operations. Using the delay predictor to reduce data transfer overhead, this chip achieves 8.5× higher energy efficiency and 53.5% power reduction compared to the previous work.

7.5 A 28nm 0.6V Low-Power DSP for Mobile Applications 10:45 AM

G. Gammie[1], N. Ickes[2], M. E. Sinangil[2], R. Rithe[2], J. Gu[3], A. Wang[1], H. Mair[1], S. Datla[1], B. Rong[1], S. Honnavara-Prasad[1], L. Ho[1], G. Baldwin[1], D. Buss[1], A. P. Chandrakasan[2], U. Ko[1]
[1]Texas Instruments, Dallas, TX
[2]Massachusetts Institute of Technology, Cambridge, MA
[3]Texas Instruments (now with MaxLinear), Dallas, TX

A DSP processor SoC is fabricated in a 28nm low-power process technology. Designed for high-performance multimedia applications at 1.0V, techniques are used to enable Ultra-Low Voltage (ULV) operation. Through library enhancements, a custom ULV SRAM, and a custom ULV statistical static timing analysis methodology, the DSP is able to operate continuously from 1.0V down to 0.6V.

7.6 A MIMO WiMAX SoC in 90nm CMOS for 300km/h Mobility 11:15 AM

G. C. Chuang[1], P-A. Ting[1], J-Y. Hsu[1], J-Y. Lai[1], S-C. Lo[1], Y-C. Hsiao[1], T-D. Chiueh[2]
[1]ITRI, Hsinchu, Taiwan
[2]National Taiwan University, Taipei, Taiwan

This paper presents a 49mm^2 WiMAX IEEE 802.16e baseband SoC implementing two 2×2 MIMO modes. The SoC integrates an ARM-926, flash and SDRAM controller, AES engine, USB 2.0, and a MAC structure with possible future extension to 802.16m/LTE. This chip can deliver data rates up to 30Mb/s in low mobility and 5Mb/s at 300km/h.

7.7 A 70Mb/s -100.5dBm Sensitivity 65nm LP MIMO Chipset for WiMAX Portable Router 11:45 AM

J-S. Pan, M-Y. Chao, E. Yeh, W-W. Yang, C-W. Hsueh, S. Liao, J-B. Lin, S-A. Yang, C-T. Liu, T-P. Lee, J-R. Chen, C-H. Chou, M. Chen, D-K. Juang, J-H. Yeh, C-W. Liao, P-H. Chen, K. Kao, C-H. Wu, W-T. Huang, S-H. Liao, C-H. Shih, C-H. Tung, Y-P. Lee
MediaTek, Hsinchu, Taiwan

This chipset consists of a dual-band 2×2 MIMO RF transceiver chip and a fully integrated WiMAX modem/router chip. The RF transceiver chip has low-power consumption of 364mW and up to 7dB sensitivity margin, and occupies 11.05mm^2. The WiMAX modem/router chip is targeted for portable routers with power consumption of 632.7mW and up to 7dB sensitivity margin, and occupies 24.99mm^2.

7.8 A Direct Digital Frequency Synthesizer with Minimized Tuning Latency of 12ns 12:15 PM

A. Willson, M. Ojha, S. Agarwal, T. Lai, T-C. Kuo
University of California, Los Angeles, CA

We present a direct digital synthesizer (DDS) to: (a) eliminate phase-accumulator (PA) pipelining; (b) raise SNR by using PA rounding; (c) get 2's complement conditional negations via 1's complement negations with no carry ripple. The prototype chip (at 260MHz) yields 0.0635mW/MHz as an average over typical frequency control words. Its outputs have a 113dB SFDR and a 98dB SNR. Core area is 0.16mm^2 in 0.18μm CMOS.

Conclusion 12:30 PM

ARCHITECTURES & CIRCUITS FOR NEXT-GENERATION WIRELINE TRANSCEIVERS

Session Chair: ***Daniel Friedman,*** *IBM Thomas J. Watson Research Center, Yorktown Heights, NY*

Associate Chair: ***Koichi Yamaguchi,*** *Renesas Electronics, Kawasaki, Japan*

8.1 11.3Gb/s CMOS SONET-Compliant Transceiver for Both RZ and NRZ Applications — 8:30 AM

N. Kocaman, A. Garg, B. Raghavan, D. Cui, A. Vasani, K. Tang, D. Pi, H. Tong, S. Fallahi, W. Zhang, U. Singh, J. Cao, B. Zhang, A. Momtaz
Broadcom, Irvine, CA

An 11.3Gb/s CMOS SONET-compliant transceiver is designed to work in both RZ and NRZ data formats. The TX driver exhibits 17ps rise/fall times, 0.25ps$_{rms}$ RJ, and 2ps$_{pp}$ DJ. The RX has a multi-stage vertical threshold adjustment circuit. It achieves 5mV$_{pp\text{-}diff}$ RX input sensitivity with 0.54UI jitter tolerance. The transceiver core area occupies 1.36mm^2 in 65nm CMOS and consumes 214mW from a 1V supply.

8.2 A Full-Duplex 10GBase-T Transmitter Hybrid with SFDR >65dBc Over 1 to 400MHz in 40nm CMOS — 9:00 AM

G. Chandra, M. Malkin
Teranetics, San Jose, CA

A digitally assisted transmitter and echo cancellation hybrid architecture for IEEE 10GBase-T Ethernet is presented. Implemented in 40nm CMOS, the transmitter has a residual linear echo < -30dBc and residual transmitter distortion < -65dBc over a bandwidth of 1 to 400MHz, while driving a 50Ω load with 2V$_{pp}$ output swing.

8.3 A 40Gb/s TX and RX Chip Set in 65nm CMOS — 9:30 AM

M-S. Chen, Y-N. Shih, C-L. Lin, H-W. Hung, J. Lee
National Taiwan University, Taipei, Taiwan

This paper introduces an integrated wireline TX and RX chip set at 40Gb/s. The transmitter incorporates a 5-tap FIR with LC-based delay line, which is precisely adjusted by a closed-loop delay controller. The receiver employs a similar 3-tap FIR as an equalizer with digital adaptation. The TX plus RX can deliver 40Gb/s data across a Rogers channel of 20cm (19dB loss at 20GHz) with BER < 10^{-12} while consuming 457mW (135mW in TX from a 1.2V supply and 322mW in RX from a 1.6V supply).

Break **10:00 AM**

8.4 10:4 MUX and 4:10 DEMUX Gearbox LSI for 100-Gigabit Ethernet Link — 10:15 AM

G. Ono[1], K. Watanabe[1], T. Muto[1], H. Yamashita[1], K. Fukuda[1], N. Masuda[1], R. Nemoto[2], E. Suzuki[1], T. Takemoto[1], F. Yuki[1], M. Yagyu[1], H. Toyoda[1], A. Kambe[1], T. Saito[1], S. Nishimura[1]
[1]Hitachi, Tokyo, Japan
[2]Hitachi, Ibaraki, Japan

A 2W 100Gb/s Ethernet gearbox LSI combining a 10:4 MUX and a 4:10 DEMUX in 65nm CMOS is presented. Replacing current-mode logic circuits with CMOS circuits by decreasing clock frequency and effective circuit-operation speed reduces power by 75% compared to that of a conventional LSI. The 25Gb/s interface in the LSI achieves BER < 10^{-12} with 34.3mV$_{pp}$ input sensitivity.

8.5 A 12.5+12.5Gb/s Full-Duplex Plastic Waveguide Interconnect 10:45 AM

S. Fukuda[1], Y. Hino[1], S. Ohashi[1], T. Takeda[1], S. Shinke[1], M. Uno[1], K. Komori[1], Y. Akiyama[1], K. Kawasaki[1], A. Hajimiri[2]
[1]Sony, Tokyo, Japan
[2]California Institute of Technology, Pasadena, CA

A 12.5+12.5Gb/s full-duplex low-power millimeter-wave-based end-to-end dielectric waveguide interconnect solution with an active footprint of 0.40mm^2 is demonstrated in 40nm CMOS. A pair of two-carrier transceivers operating simultaneously at 57GHz and 80GHz achieves a full-duplex connection over a 120mm plastic waveguide with a BER of less than 10^{-12}.

8.6 A Highly Digital 0.5-to-4Gb/s 1.9mW/Gb/s Serial-Link Transceiver Using Current-Recycling in 90nm CMOS 11:15 AM

R. Inti[1], A. Elshazly[1], B. Young[1], W. Yin[1], M. Kossel[2], T. Toifl[2], P. Hanumolu[1]
[1]Oregon State University, Corvallis, OR
[2]IBM Zurich Research Laboratory, Zurich, Switzerland

A serial link transceiver uses current-recycling and highly digital clock generation and recovery to reduce power. Fabricated in 90nm CMOS, it operates from a 1.2V supply and achieves 0.5-to-4Gb/s operating range. At 3.2Gb/s, it achieves 1.9mW/Gb/s power efficiency with a BER of $<10^{-12}$.

8.7 A 1-to-6Gb/s Phase-Interpolator-Based Burst-Mode CDR in 65nm CMOS 11:45 AM

B. Abiri[1], R. Shivnaraine[1], A. Sheikholeslami[1], H. Tamura[2], M. Kibune[2]
[1]University of Toronto, Toronto, Canada
[2]Fujitsu Laboratories, Kawasaki, Japan

This paper presents a burst-mode clock recovery scheme based on phase interpolation between two quadrature clocks. Samples of the quadrature clocks at each data transition form the interpolation coefficients for the same quadrature clocks. Measured results in a 65nm CMOS test-chip confirm the burst-mode CDR acquires lock in less than 1 UI for data rates within 1 to 6Gb/s. The receiver occupies an area of 250µm×70µm and consumes 22mW from a 1.2V supply.

8.8 A 14Gb/s High-Swing Thin-Oxide Device SST TX in 45nm CMOS SOI 12:00 PM

C. Menolfi[1], T. Toifl[1], M. Rueegg[2], M. Braendli[1], P. Buchmann[1], M. Kossel[1], T. Morf[1]
[1]IBM Zurich Research Laboratory, Rueschlikon, Switzerland
[2]Miromico, Zurich, Switzerland

A 14Gb/s high-swing source-series-terminated (SST) TX is presented that features up to twice the signaling amplitude of a conventional SST design. The 4-tap FFE TX is based on a high-voltage, thin-oxide device SST output driver stage whose pull-up and pull-down switches are driven from separate, split supply pre-drivers. Implemented in 45nm CMOS SOI, the circuit consumes 85.5mW at 14Gb/s from a nominal supply of 1V and an output driver supply of 2V.

Conclusion 12:15 PM

WIRELESS & mm-WAVE CONNECTIVITY

Session Chair: ***Gangadhar Burra,*** *Texas Instruments, Dallas, TX*
Associate Chair: ***Yorgos Palaskas,*** *Intel, Hillsboro, OR*

9.1 A 60GHz 16QAM/8PSK/QPSK/BPSK Direct-Conversion Transceiver for IEEE 802.15.3c — 8:30 AM

K. Okada, K. Matsushita, K. Bunsen, R. Murakami, A. Musa, T. Sato, H. Asada, N. Takayama, N. Li, S. Ito, W. Chaivipas, R. Minami, A. Matsuzawa
Tokyo Institute of Technology, Tokyo, Japan

This paper presents a 60GHz direct-conversion transceiver using 60GHz quadrature oscillators. The 65nm CMOS transceiver realizes the IEEE 802.15.3c full-rate wireless communication for every 16QAM/8PSK/QPSK/BPSK mode. The maximum data rates with an antenna built in the package are 8Gb/s in QPSK mode and 11Gb/s in 16QAM mode within a BER of $< 10^{-3}$, and the transmitter and the receiver consume 186mW and 106mW, respectively.

9.2 A 65nm CMOS Fully Integrated Transceiver Module for 60GHz Wireless HD Applications — 9:00 AM

A. Siligaris[1], O. Richard[2], B. Martineau[2], C. Mounet[1], F. Chaix[1], R. Ferragut[3], C. Dehos[1], J. Lanteri[1], L. Dussopt[1], S. Yamamoto[2], R. Pilard[2], P. Busson[2], A. Cathelin[2], D. Belot[2], P. Vincent[1]
[1]CEA-LETI-MINATEC, Grenoble, France
[2]STMicroelectronics, Crolles, France
[3]STMicroelectronics, Grenoble, France

A fully integrated WirelessHD-compatible 60GHz transceiver module covering the four standard channels is presented. The 65nm CMOS die, external PA and high aperture antennas are flip-chipped atop a low cost HTCC substrate using an industrial packaging line. The module achieves a 16-QAM OFDM modulation wireless link over 1 meter distance.

9.3 A 60GHz CMOS Phased-Array Transceiver Pair for Multi-Gb/s Wireless Communications — 9:30 AM

S. Emami, R. F. Wiser, E. Ali, M. G. Forbes, M. Q. Gordon, X. Guan, S. Lo, P. T. McElwee, J. Parker, J. R. Tani, J. M. Gilbert, C. H. Doan
SiBEAM, Sunnyvale, CA

A 60GHz phased-array transceiver pair is integrated in 65nm CMOS and packaged with an embedded antenna array, supporting the WirelessHD and draft IEEE 802.11ad standards. EVM of -19.2dB meets the spectral mask for 10m non-line-of-sight transmission of 3.8Gb/s over 16-QAM OFDM. Trade-offs between rate, range, and power consumption are described.

9.4 A 65nm CMOS 4-Element Sub-34mW/Element 60GHz Phased-Array Transceiver — 9:45 AM

M. Tabesh, J. Chen, C. Marcu, L. Kong, S. Kang, E. Alon, A. Niknejad
University of California, Berkeley, CA

This paper describes a 60GHz 4-element 65nm CMOS phased-array transceiver consuming <34mW/element including LO synthesis and distribution. These results are achieved by utilizing a baseband phase-shifting architecture and holistic impedance optimization.

Break 10:00 AM

9.5 An 87GHz QPSK Transceiver with Costas-Loop Carrier Recovery in 65nm CMOS **10:15 AM**

S-J. Huang, Y-C. Yeh, H. Wang, P-N. Chen, J. Lee, National Taiwan University, Taipei, Taiwan

This paper presents a fully integrated QPSK transceiver operating at E-band (carrier frequency = 87GHz). Including RF front-end, Costas-loop-based carrier and data recovery, and antenna assembly technique, this prototype achieves 3.5Gb/s data link with BER < 1e-11 while consuming 212mW (TX) and 166mW (RX) from a 1.2V supply.

9.6 A 65nm Dual-Band 3-Stream 802.11n MIMO WLAN SoC **10:45 AM**

S. Abdollahi-Alibeik[1], D. Weber[1], H. Dogan[1], W. W. Si[1], B. Baytekin[1], A. Komijani[1], R. Chang[1], B. Vakili-Amini[2], M. Lee[1], H. Gan[1], Y. Rajavi[1], H. Samavati[1], B. Kaczynski[1], S-M. Lee[1], S. Limotyrakis[1], H. Park[1], P. Chen[2], P. Park[2], M. S-W. Chen[1], A. Chang[1], Y. Oh[1], J. J-M. Yang[1], E. C-C. Lin[3], L. Nathawad[1], K. Onodera[1], M. Terrovitis[1], S. Mendis[1], K. Shi[1], S. Mehta[1], M. Zargari[2], D. Su[1]

[1]Atheros Communications, San Jose, CA; [2]Atheros Communications, Irvine, CA

[3]Atheros Communications, Hsinchu, Taiwan

An 802.11n 3-stream 3x3 MIMO WLAN SoC, incorporating three transceivers, is implemented in 65nm CMOS with a die area of 22mm^2. The design employs on-chip IQ mismatch calibration and a reference clock doubler to achieve an EVM floor of -39dB/-36dB at 2.4/5GHz.

9.7 A 0.46mm^2 4dB-NF Unified Receiver Front-End for Full-Band Mobile TV in 65nm CMOS **11:15 AM**

P-I. Mak[1], R. Martins[1,2]

[1]University of Macau, Macau, China; [2]Instituto Superior Tecnico, Lisbon, Portugal

A unified receiver front-end for full-band mobile TV shows 4dB NF, +32dBm IIP2 and -3.4dBm IIP3. A gain-boosting current-balancing-balun LNA improves IIP2 and wideband output balancing. A current-reuse mixer-LPF realizes quadrature/harmonic-rejection mixing and 3rd-order post filtering. A direct injection-locked 4-/8-phase LO generator relaxes the master LO frequency.

9.8 An All-Digital 8-DPSK Polar Transmitter with Second-Order Approximation Scheme and Phase Rotation-Constant Digital PA for Bluetooth EDR in 65nm CMOS **11:45 AM**

H. Kobayashi, S. Kousai, Y. Yoshihara, M. Hamada, Toshiba Semiconductor, Kawasaki, Japan

An all-digital 8-DPSK polar transmitter for Bluetooth EDR is fabricated in 65nm CMOS. It implements a second-order approximation scheme in the gain calculation of DCO and a phase rotation-constant digital PA and achieves a DEVM of 6.1% at 0 dBm in sending 8-DPSK signal, draws 35 mA from 1.2V supply and occupies an area of 0.75mm x 0.75mm.

9.9 A Digital-Intensive Receiver Front-End Using VCO-Based ADC with an Embedded 2nd-Order Anti-Aliasing Sinc Filter in 90nm CMOS **12:00 PM**

J. Kim[1], W. Yu[1], H-K. Yu[2], S. Cho[1], [1]KAIST, Daejeon, Korea; [2]ETRI, Daejeon, Korea

A 0.2-to-1.8GHz digital-intensive receiver front-end using a VCO-based ADC running at 1.4Gs/s in 90nm CMOS is described. To improve the out-of-band rejection, a 2nd-order anti-aliasing Sinc filter is proposed, which can be embedded in the VCO-based ADC. The receiver achieves -94dBm of sensitivity at 1MHz bandwidth and -6.8dBm of IIP3, while providing 50dB rejection of aliased signals.

Conclusion 12:15 PM

NYQUIST-RATE CONVERTERS

Session Chair: ***Michael Flynn,*** *University of Michigan, Ann Arbor, MI*
Associate Chair: ***Michael Perrott,*** *SiTime Corporation, Sunnyvale, CA*

10.1 A 480mW 2.6GS/s 10b 65nm CMOS Time-Interleaved ADC with 48.5dB SNDR up to Nyquist — 8:30 AM

K. Doris, E. Janssen, C. Nani, A. Zanikopoulos, G. van der Weide
NXP Semiconductors, Eindhoven, The Netherlands

This work presents a 64× interleaved 2.6GS/s 10b 65nm CMOS successive-approximation-register ADC with on-chip gain, offset and DAC linearity calibration. The ADC combines interleaving hierarchy with an open-loop buffer array operated in feedforward-sampling and feedback-SAR mode and achieves an SNDR of 48.5dB at Nyquist with 110fs jitter while consuming only 0.48W.

10.2 A 12b 1GS/s SiGe BiCMOS Two-Way Time-Interleaved Pipeline ADC — 9:00 AM

R. Payne[1], C. Sestok[1], W. Bright[1], M. El-Chamas[1], M. Corsi[1], D. Smith[1], N. Tal[2]
[1]Texas Instruments, Dallas, TX
[2]Texas Instruments, Raanana, Israel

A 2-way time-interleaved pipeline ADC built in a 0.18um BiCMOS SiGe process uses a switched-current architecture. Most circuits are shared between the two interleaving branches to reduce power to 575mW. To address the interleaving artifacts, DACs are included to remove timing skew and bandwidth mismatch. ENOB is 10.2b with measured SNR of 62dB and SFDR>67dB.

10.3 An 800MS/s Dual-Residue Pipeline ADC in 40nm CMOS — 9:30 AM

J. Mulder, F. M. van der Goes, D. Vecchi, J. R. Westra, E. Ayranci, C. M. Ward, J. Wan, K. Bult
Broadcom, Bunnik, The Netherlands

An 800MS/s 4×-interleaved 12b pipeline ADC, occupying 0.88mm2 in 40nm CMOS, achieves an SNDR of 59dB. Power consumption of 105mW is achieved using low open-loop-gain amplifiers in a dual-residue topology, resulting in a FOM of 0.18pJ/conversion. A fast background offset calibration algorithm removes the offsets of the MDAC stages.

Break 10:00 AM

10.4 A 16b 80MS/s 100mW 77.6dB SNR CMOS Pipeline ADC — 10:15 AM

J. Brunsilius[1], E. Siragusa[1], S. Kosic[1], F. Murden[2], E. Yetis[1], B. Luu[1], J. Bray[1], P. Brown[1], A. Barlow[1]
[1]Analog Devices, San Diego, CA
[2]Analog Devices, Greensboro, NC

A 16b pipeline ADC that achieves 77.6dBFS SNR, 77.4dBFS SNDR and 93dBc SFDR at 80MS/s with a 10MHz input while consuming 100mW is presented. The design includes a dynamically driven deep N-well input sampling switch, an offset-canceled comparator, and a back-gate voltage-biased MDAC amplifier. The ADC is fabricated in a 1P5M 0.18µm CMOS process.

10.5 A 0.024mm² 8b 400MS/s SAR ADC with 2b/Cycle and Resistive DAC in 65nm CMOS **10:45 AM**

H. Wei[1], C-H. Chan[1], U-F. Chio[1], S-W. Sin[1], S-P. U[1], R. Martins[1,2], F. Maloberti[3]
[1]University of Macau, Macau, China
[2]Instituto Superior Tecnico, Lisbon, Portugal
[3]University of Pavia, Pavia, Italy

An 8b 400MS/s SAR ADC with 2b-per-cycle architecture is fabricated in a 65nm CMOS process. The ADC uses a single resistive DAC and occupies 0.024mm². At maximum conversion rate with a 1.9MHz input signal, the prototype consumes 4mW exhibiting an SNDR of 44.5dB with an SFDR of 54.0dB. The FOM is 73fJ/conversion-step at 400MS/s from a 1.2V supply and 42fJ/conversion-step at 250MS/s from a 1V supply.

10.6 A Resolution-Reconfigurable 5-to-10b 0.4-to-1V Power Scalable SAR ADC **11:15 AM**

M. Yip, A. P. Chandrakasan
Massachusetts Institute of Technology, Cambridge, MA

This paper presents a reconfigurable 5-to-10b SAR ADC in 65nm CMOS, operating from 2MS/s at 1V to 5kS/s at 0.4V, with power that is linear with sample rate. The DAC power scales exponentially with resolution and voltage scaling further reduces the energy-per-conversion. The FOM is 22.4fJ/conversion-step in 10b mode at 0.55V.

10.7 A 12b 1.25GS/s DAC in 90nm CMOS with >70dB SFDR up to 500MHz **11:45 AM**

W-H. Tseng, C-W. Fan, J-T. Wu
National Chiao Tung University, Hsinchu, Taiwan

A DAC is fabricated in90nm CMOS enhances dynamic performance by applying digital random return-to-zero and by using compact current cells. Current matching is ensured by background calibration. The chip consumes 128mW and the active area is 1100×750μm². At 1.25GS/s sampling rate, the DAC achieves an SFDR of better than 70dB up to 500MHz input frequency.

10.8 A 56GS/s 6b DAC in 65nm CMOS with 256×6b memory **12:15 PM**

Y. M. Greshishchev, D. Pollex, S-C. Wang, M. Besson, P. Flemeke, S. Szilagyi, J. Aguirre, C. Falt, N. Ben-Hamida, R. Gibbins, P. Schvan
Ciena, Ottawa, Canada

A 6b 56Gs/s 65nm CMOS DAC operates with 1.1V and 2.5V supplies delivering SFDR>30dB and ENOB>4.3b in 26.9GHz output bandwidth. It combines 256×6b data test memory, 16:1 CMOS MUX with (28-14-7-3.5) GHz clock grid generator, DAC current-steering matrix with four unary- and two binary-weighted segments. For a 56Gb/s 256b PRBS pattern mode differential V_{out} is greater than $400mV_{pp}$ into 50Ω.

Conclusion 12:30 PM

NON-VOLATILE MEMORY SOLUTIONS

Session Chair: ***Frankie Roohparvar,*** *Micron Technology, San Jose, CA*
Associate Chair: ***Sungdae Choi,*** *Hynix Semiconductor, Icheon, Korea*

11.1 A 151mm² 64Gb MLC NAND Flash Memory in 24nm CMOS Technology — 8:30 AM

K. Fukuda[1], Y. Watanabe[1], E. Makino[1], K. Kawakami[1], J. Sato[1], T. Takagiwa[1], N. Kanagawa[1], H. Shiga[1], N. Tokiwa[1], Y. Shindo[1], T. Edahiro[1], T. Ogawa[1], M. Iwai[1], O. Nagao[1], J. Musha[1], T. Minamoto[1], K. Yanagidaira[1], Y. Suzuki[1], D. Nakamura[1], Y. Hosomura[1], H. Komai[1], Y. Furuta[1], M. Muramoto[1], R. Tanaka[1], G. Shikata[1], A. Yuminaka[1], K. Sakurai[2], M. Sakai[3], H. Ding[3], M. Watanabe[3], Y. Kato[3], T. Miwa[3], A. Mak[4], M. Nakamichi[3], G. Hemink[3], D. Lee[4], M. Higashitani[4], B. Murphy[4], B. Lei[4], Y. Matsunaga[1], K. Naruke[1], T. Hara[1]
[1]Toshiba Semiconductor, Yokohama, Japan; [2]Toshiba Memory Systems, Yokohama, Japan
[3]Sandisk, Yokohama, Japan; [4]Sandisk, Milpitas, CA

A 64Gb 2bit/cell NAND Flash memory capable of 14MB/s programming and 266MB/s data transfer is fabricated in 24nm CMOS technology. A 151mm² die size is realized with a two-plane configuration enabled by low-resistance wordline material and a new bitline hook-up architecture. Program algorithms improve program throughput by 5% and operation current by 6%.

11.2 A 4Mb Embedded SLC Resistive-RAM Macro with 7.2ns Read-Write Random-Access Time and 160ns MLC-Access Capability — 9:00 AM

S-S. Sheu[1], M-F. Chang[2], K-F. Lin[2], C-W. Wu[2], Y-S. Chen[1,2], P-F. Chiu[1,2], C-C. Kuo[2], Y-S. Yang[2], P-C. Chiang[1], W-P. Lin[1], C-H. Lin[1], H-Y. Lee[1], P-Y. Gu[1], S-M. Wang[1], F. T. Chen[1], K-L. Su[1], C-H. Lien[2], K-H. Cheng[3], H-T. Wu[1], T-K. Ku[1], M-J. Kao[1], M-J. Tsai[1]
[1]ITRI, Hsinchu, Taiwan; [2]National Tsing Hua University, Hsinchu, Taiwan
[3]National Central University, Jhongli, Taiwan

A 4Mb embedded SLC resistive RAM with 7.2ns random-access time is proposed. A parallel-series-reference-cell scheme and a process-and-temperature-aware dynamic bitline-bias circuit achieves stable high-speed read operation. With the proposed sensing scheme and designed write-verify procedure, a 160ns write-verify operation on MLC mode is demonstrated.

11.3 A 32Gb MLC NAND Flash Memory with V_{th} Margin-Expanding Schemes in 26nm CMOS — 9:30 AM

T-Y. Kim, S-D. Lee, J-S. Park, H-Y. Cho, B-S. You, K-H. Baek, J-H. Lee, C-W. Yang, M. Yun, M-S. Kim, J-W. Kim, E-S. Jang, H. Chung, S-O. Lim, B-S. Han, Y-H. Koh
Hynix Semiconductor, Icheon, Korea

The 26nm 32Gb MLC flash memory device has a chip size of 181.5mm² using the schemes of negative wordline, all-bitline(ABL) parallel program and ABL with BL compensation. A negative wordline scheme is introduced to control the V_{th} distribution using negative region under 0V.

Break 10:00 AM

11.4 95%-Lower-BER 43%-Lower-Power Intelligent Solid-State Drive (SSD) with Asymmetric Coding and Stripe Pattern Elimination Algorithm — 10:15 AM

S. Tanakamaru[1], C. Hung[1], A. Esumi[2], M. Ito[2], K. Li[2], K. Takeuchi[1]
[1]University of Tokyo, Tokyo, Japan; [2]SIGLEAD, Yokohama, Japan

SSD techniques are presented that result in 95% lower bit-error rate and 43% lower power. It is shown that the memory cell errors in data retention and program disturb as well as the power consumption strongly depend on the data pattern. Asymmetric coding reduces the population of high V_{TH} states to decrease the cell error by 95%. A stripe pattern elimination algorithm saves bitline charging and reduces the power by 43%.

11.5 An Offset-Tolerant Current-Sampling-Based Sense Amplifier for Sub-100nA-Cell-Current Nonvolatile Memory **10:45 AM**

M-F. Chang[1], S-J. Shen[1], C-C. Liu[1], C-W. Wu[1], Y-F. Lin[1], S-C. Wu[1], C-E. Huang[1,2], H-C. Lai[1,2], Y-C. King[1], C-J. Lin[1], H-J. Liao[2], Y-D. Chih[2], H. Yamauchi[3]
[1]National Tsing Hua University, Hsinchu, Taiwan; [2]TSMC, Hsinchu, Taiwan
[3]Fukuoka Institute of Technology, Fukuoka, Japan

An offset-tolerant current-sampling-based sense amplifier is proposed for reading sub-100nA cell current in non-volatile memory. Compared to the previous sense amplifiers, this circuit achieves 7× faster access time for 100nA cell current and a minimum access time of 26ns at 1.2V, demonstrated in a 90nm 512Kb OTP macro.

11.6 A Low-Voltage 1Mb FeRAM in 0.13µm CMOS Featuring Time-to-Digital Sensing for Expanded Operating Margin in Scaled CMOS **11:00 AM**

M. Qazi[1], M. Clinton[2], S. Bartling[2], A. P. Chandrakasan[1]
[1]Massachusetts Institute of Technology, Cambridge, MA; [2]Texas Instruments, Dallas, TX

A 1MB 1T/1C FeRAM fabricated in 0.13µm CMOS operates from 1.5 to 1.0V with corresponding access energy from 25 to 10.2pJ/b. The challenges of sensing small charge and developing circuits compatible with the scaling of FeRAM technology to low-voltage and more advanced CMOS nodes are addressed with a time-to-digital sensing scheme.

11.7 A 4Mb Conductive-Bridge Resistive Memory with 2.3GB/s Read-Throughput and 216MB/s Program-Throughput **11:15 AM**

W. Otsuka[1], K. Miyata[1], M. Kitagawa[1], K. Tsutsui[1], T. Tsushima[1], H. Yoshihara[2], T. Namise[2], Y. Terao[2], K. Ogata[2]
[1]Sony, Kanagawa, Japan; [2]Sony LSI Design, Nagasaki, Japan

A 4Mb conductive-bridge resistive memory in 0.18µm CMOS is demonstrated with 2.3GB/s read-throughput and 216MB/s program throughput. The design features a direct-sense method in which programmed data is concurrently verified by sensing program pulse currents. The concept contributes to an improved program performance.

11.8 A 7MB/s 64Gb 3-Bit/Cell DDR NAND Flash Memory in 20nm-Node Technology **11:45 AM**

K-T. Park, O. Kwon, S. Yoon, M-H. Choi, I-M. Kim, B-G. Kim, M-S. Kim, Y-H. Choi, S-H. Shin, Y. Song, J-Y. Park, J-E. Lee, C-G. Eun, H-C. Lee, H-J. Kim, J-H. Lee, J-Y. Kim, T-M. Kweon, H-J. Yoon, T. Kim, D-K. Shim, J. Sel, J-Y. Shin, P. Kwak, J-M. Han, K-S. Kim, S. Lee, Y-H. Lim, T-S. Jung
Samsung Electronics, Hwasung, Korea

We present a 64Gb 3-bit/cell cell NAND Flash with 7MB/s write rate and 200Mb/s asynchronous DDR interface in a 20m-node technology.

Conclusion **12:15 PM**

DESIGN IN EMERGING TECHNOLOGIES

Session Chair: ***Azeez Bhavnagarwala,*** *AMD, Boxborough, MA*
Associate Chair: ***Tadahiro Kuroda,*** *Keio University, Yokohama, Japan*

12.1 A 95mV-Startup Step-Up Converter with V_{TH}-Tuned Oscillator by Fixed-Charge Programming and Capacitor Pass-On Scheme — 1:30 PM

P-H. Chen[1], K. Ishida[1], K. Ikeuchi[1], X. Zhang[1], K. Honda[1], Y. Okuma[2], Y. Ryu[2], M. Takamiya[1], T. Sakurai[1]
[1]University of Tokyo, Tokyo, Japan
[2]Semiconductor Technology Academic Research Center, Yokohama, Japan

A 95mV startup-voltage step-up converter with capacitor pass-on scheme for energy-harvesting applications is described. The post-fabrication V_{TH} trimming improves the minimum operating voltage of the clock generator at startup. The step-up converter achieves the low startup voltage in standard 65nm CMOS without mechanical assist.

12.2 100V AC Power Meter System-on-a-Film (SoF) Integrating 20V Organic CMOS Digital and Analog Circuits with Floating Gate for Process-Variation Compensation and 100V Organic PMOS Rectifier — 2:00 PM

K. Ishida[1], T-C. Huang[1], K. Honda[1], T. Sekitani[1], H. Nakajima[2], H. Maeda[2], M. Takamiya[1], T. Someya[1], T. Sakurai[1]
[1]University of Tokyo, Tokyo, Japan; [2]Dai Nippon Printing, Chiba, Japan

A system-on-a-film integrating: i) 20V organic CMOS opamp with variation-compensation capability, ii) 20V organic CMOS frequency divider with high-gain pseudo-CMOS inverters, iii) 100V organic PMOS rectifier for generating 50Hz clock and 20V DC power is developed for realizing a 100V AC power meter.

12.3 Real-Time Current-Waveform Sensor with Plugless Energy Harvesting from AC Power Lines for Home/Building Energy-Management Systems — 2:30 PM

S. Takahashi, N. Yoshida, K. Maruhashi, M. Fukaishi
NEC, Kawasaki, Japan

A TX-integrated battery-free current-waveform sensor with plugless energy harvesting from AC power lines is fabricated in 90nm CMOS with 560×300μm^2. A realtime sampler that use a half cycle time-to-digital convertor and RF-power-management to enable -5.5dBm RF power at the 50kS/s with a harvesting power supply of 1mW.

Break 3:00 PM

12.4 A 3.9ns 8.9mW 4×4 Silicon Photonic Switch Hybrid Integrated with CMOS Driver — 3:15 PM

A. Rylyakov, C. Schow, B. Lee, W. Green, J. Van Campenhout, M. Yang, F. Doany, S. Assefa, C. Jahnes, J. Kash, Y. Vlasov
IBM T. J. Watson Reseach Center, Yorktown Heights, NY

A monolithic 4×4 silicon photonic router, composed of 6 2×2 2mW 3.9ns 300×50μm^2 Mach-Zehnder interferometer switches, is flip-chip bonded with a custom 90nm bulk CMOS driver, routing 3×40Gb/s WDM data with BER <10^{-12}, less than -10dB cross-talk and 7dB loss. The size of the micro-assembly is 1×2×2mm^3.

12.5 A 820GHz SiGe Chipset for Terahertz Active Imaging Applications **3:45 PM**

E. Öjefors[1], J. Grzyb[1], Y. Zhao[1], B. Heinemann[2], B. Tillack[2], U. R. Pfeiffer[1]
[1]University of Wuppertal, Wupppertal, Germany; [2]IHP, Frankfurt (Oder), Germany

A 820GHz TX and RX chipset for active terahertz imaging in a 0.25µm process with an upgraded SiGe HBT technology is presented. The chipset consists of a four-channel spatial power combining transmitter with -17dBm effective isotropic radiated power and a subharmonic 2×2-element receiver array with -22dB conversion gain and 47dB NF.

12.6 A 130µA Wake-Up Receiver SoC in 0.13µm CMOS for Reducing Standby Power of An Electric Appliance Controlled by An Infrared Remote Controller **4:15 PM**

H. Ishihara[1], T. Umeda[1], K. Ohno[2], S. Iwata[2], F. Moritsuka[1], T. Itakura[1], M. Ishibe[2], K. Hijikata[2], Y. Maki[2]
[1]Toshiba, Kawasaki, Japan; [2]Toshiba, Ome, Japan

We present a low-power receiver SoC in 0.13µm CMOS for an infrared remote controller with wake-up function. The receiver controls connection of the AC power supply to the electric appliance to reduce the standby power. The receiver consumes only 130µA and works even with strong ambient light. The communication range of the receiver is more than 10m.

12.7 Programmable Cell Array Using Rewritable Solid-Electrolyte Switch Integrated in 90nm CMOS **4:30 PM**

M. Miyamura[1], S. Nakaya[2], M. Tada[1], T. Sakamoto[1], K. Okamoto[1], N. Banno[1], S. Ishida[1], K. Ito[1], H. Hada[1], N. Sakimura[1], T. Sugibayashi[1], M. Motomura[2]
[1]NEC, Sagamihara, Japan; [2]NEC, Kawasaki, Japan

A programmable cell array, which has a rewritable switch plane in the interconnect layers using a nonvolatile solid-electrolyte switch, is proposed and its fundamental operation is confirmed using a test vehicle and a 32×32 crossbar circuit. A drastic 81% reduction in programmable cell area and a 72% reduction in total chip area is achieved while using a practical chip design.

12.8 6W/25mm² Inductive Power Transfer for Non-Contact Wafer-Level Testing **4:45 PM**

A. Radecki, H. Chung, Y. Yoshida, N. Miura, T. Shidei, H. Ishikuro, T. Kuroda
Keio University, Yokohama, Japan

For non-contact wafer-level testing 6W DC power is delivered by inductive coupling to a 5mm² chip over a 0.32mm distance. A 135° phase-offset-control scheme and a DLL-based synchronous rectifier at 150MHz operation improve power transfer efficiency to 17% and reduce output voltage ripple to 65mV.

12.9 GHz-Range Continuous-Time Programmable Digital FIR with Power Dissipation that Automatically Adapts to Signal Activity **5:00 PM**

M. Kurchuk[1], C. Weltin-Wu[1], D. Morche[2], Y. Tsividis[1]
[1]Columbia University, New York, NY; [2]CEA-LETI-MINATEC, Grenoble, France

A continuous-time 3b 6-tap ADC/DSP-DAC system is realized in 65nm CMOS for GHz applications with a 0.8-to-3.2GHz bandwidth, occupying a core area of 0.08mm². It has activity-dependent alias-free sampling and power dissipation from 1.1 to 10mW, achieving a maximum effective sampling rate of 45GS/s with an SNDR of 20dB.

Conclusion **5:15 PM**

ANALOG TECHNIQUES

Session Chair: ***Jafar Savoj,*** *Xilinx, San Jose, CA*
Associate Chair: ***Kimmo Koli,*** *ST-Ericsson, Turku, Finland*

13.1 A Simple LED Lamp Driver IC with Intelligent Power-Factor Correction — 1:30 PM

J. Hwang, K. Cho, D. Kim, M. Jung, G. Cho, S. Yang
Fairchild Semiconductor, Bucheon, Korea

A simple 3-pin buck-type LED lamp driver with intelligent power-factor correction is presented. It uses digital control algorithm to achieve power factors of 0.98 and 0.92 with the THD of 18% and 16% which meets standard IEC 1000-3-2 (EN61000-3-2) at $110V_{ac}$ and $220V_{ac}$ with 5W LED load, respectively.

13.2 A 1.2A Buck-Boost LED Driver with 13% Efficiency Improvement Using Error-Averaged SenseFET-Based Current Sensing — 2:00 PM

S. Rao[1], Q. Khan[1], S. Bang[2], D. Swank[2], A. Rao[2], W. McIntyre[2], P. K. Hanumolu[1]
[1]Oregon State University, Corvallis, OR
[2]National Semiconductor, Grass Valley, CA

A 1.2A Buck-Boost LED driver, fabricated in a 0.5µm CMOS process, that regulates the LED current without any series current source or series sense resistor is presented. The proposed error-averaged current sensing technique achieves better than 2.8% sensing accuracy and improves the converter efficiency by more than 13%.

13.3 Filterless Integrated Class-D Audio Amplifier Achieving 0.0012% THD+N and 96dB PSRR When Supplying 1.2W — 2:30 PM

M. Teplechuk, T. Gribben, C. Amadi
Dialog Semiconductor, Edinburgh, United Kingdom

Filterless class-D audio amplifier with uniform pulse-width modulation architecture achieves 0.0012% THD+N delivering 1.2W into 8Ω with 93% power efficiency and 96dB PSRR. Amplifier is fabricated in a standard CMOS process and packaged in WLCSP with total chip area of $1.44mm^2$. Amplifier achieves 103dB SNR with quiescent current of 4mA and maximum output power of 3.1W.

Break **3:00 PM**

13.4 A 5.9nV/√Hz Chopper Operational Amplifier with 0.78µV Maximum Offset and 28.3nV/°C Offset Drift — 3:15 PM

Y. Kusuda
Analog Devices, Wilmington, MA

A 5.9nV/√Hz chopper operational amplifier with phase compensation using current attenuation is implemented in 0.35µm CMOS process with 1.47mA supply current and $1.26mm^2$ die area. Adaptive clock level and backgate biasing for the input chopping allows the optimization for noise and offset, realizing 0.78µV offset with 28.3nV/C drift at worst case.

13.5 A Current-Feedback Instrumentation Amplifier with a Gain Error Reduction Loop and 0.06% Untrimmed Gain Error **3:45 PM**

R. Wu, J. H. Huijsing, K. A. Makinwa
Delft University of Technology, Delft, The Netherlands

A gain error reduction loop (GERL) is presented that improves the gain accuracy and linearity of a current-feedback instrumentation amplifier (CFIA). The GERL continuously cancels the CFIA's gain error, therefore eliminating the need for trimming. The CFIA achieves a gain error of 0.06%. This represents a 4× improvement in power efficiency compared to prior art.

13.6 A 6.7nV/√Hz Sub-mHz-1/f-Corner 14b Analog-to-Digital Interface for Rail-to-Rail Precision Voltage Sensing **4:15 PM**

C. D. Ezekwe, J. P. Vanderhaegen, X. Xing, G. K. Balachandran
Robert Bosch, Palo Alto, CA

A digital sensor interface minimizes noise folding with boxcar sampling and stabilizes the overall interface gain with global feedback. The combination of nested chopping and autozeroing allows the interface to thoroughly reject low-frequency noise. The interface is fabricated in 0.35µm CMOS and achieves a noise floor of 6.7nV/√Hz down to 0.1mHz while dissipating 6.6mW.

13.7 A 36V JFET-Input Bipolar Operational Amplifier with 1µV/°C Maximum Offset Drift and -126dB Total Harmonic Distortion **4:30 PM**

M. F. Snoeij, M. V. Ivanov
Texas Instruments, Erlangen, Germany

A 36V JFET-input bipolar operational amplifier is presented with a maximum offset drift of 1µV/°C from -40 to 125°C. This is realized with a drift-compensating circuit and a 2-temperature trimming method. By using input class-AB boosting, a good slew rate (20V/µs), excellent THD+N ratio (-126dB) and low noise (5.1nV/√Hz) are paired with low quiescent current (1.8mA).

13.8 A 3.3V-Supply 120mW Differential ADC Driver Amplifier in 0.18µm SiGe BiCMOS with 108dBc IM3 at 100MHz **4:45 PM**

G. F. Luff
Intersil, Harlow, United Kingdom

A fully differential ADC driver amplifier in 0.18µm NPN-only SiGe BiCMOS achieves 108 dBc IM3, delivering 2Vpp-diff composite two tone output at 100MHz into 200 ohms. Input noise is 0.85 nV/√Hz and 3dB bandwidth 2.2GHz. Consuming only 120mW from 3.3V supply, it has half the distortion at half the power of previous designs.

Conclusion 5:00 PM

HIGH-PERFORMANCE EMBEDDED MEMORY

Session Chair: ***Leland Chang,*** *IBM T.J. Watson Research Center, Yorktown Heights, NY*

Associate Chair: ***Peter Rickert,*** *Texas Instruments, Richardson, TX*

14.1 A 64Mb SRAM in 32nm High-k Metal-Gate SOI Technology with 0.7V Operation Enabled by Stability, Write-Ability and Read-Ability Enhancements — 1:30 PM

H. Pilo[1], I. Arsovski[1], K. Batson[1], G. Braceras[1], J. Gabric[1], R. Houle[1], S. Lamphier[1], F. Pavlik[1], A. Seferagic[1], L-Y. Chen[2], S-B. Ko[2], C. Radens[2]
[1]IBM Systems and Technology Group, Essex Junction, VT
[2]IBM Systems and Technology Group, Hopewell Junction, NY

A 64Mb SRAM macro is fabricated in a 32nm high-k metal-gate SOI technology. The SRAM features a 0.154μm^2 bitcell. A 0.7V V_{DDMIN} operation is enabled by three assist features. Stability is improved by a bitline regulation scheme that reduces charge injection into the bitcell. Enhancements to the write path include an increase of 40% of bitline boost voltage. Finally, a bitcell-tracking delay circuit improves both performance and yield across the process space.

14.2 A 4R2W Register File for a 2.3GHz Wire-Speed POWER™ Processor with Double-Pumped Write Operation — 2:00 PM

G. S. Ditlow[1], R. K. Montoye[1], S. N. Storino[2], S. M. Dance[2], S. Ehrenreich[3], B. M. Fleischer[1], T. W. Fox[1], K. M. Holmes[4], J. Mihara[5], Y. Nakamura[5], S. Onishi[5], R. Shearer[2], D. Wendel[6], L. Chang[1]
[1]IBM T. J. Watson Reseach Center, Yorktown Heights, NY
[2]IBM Systems and Technology Group, Rochester, MN
[3]Hoerner & Sulger, Schwetzingen, Germany
[4]IBM Systems and Technology Group, Essex Junction, VT
[5]IBM Systems and Technology Group, Kyoto, Japan
[6]IBM Systems and Technology Group, Boeblingen, Germany

A 2.3GHz 144×78b 4R2W register file leverages a small 2R1W cell by double-pumping write ports and combining read ports from replicated cells. This technique achieves near 2× area and read power reduction at 190ps read latency in 45nm SOI-CMOS. System performance is improved by using a fast parity code for error correction.

14.3 An 8MB Level-3 Cache in 32nm SOI with Column-Select Aliasing — 2:30 PM

D. Weiss[1], M. Dreesen[1], M. Ciraula[1], C. Henrion[1], C. Helt[1], R. Freese[1], T. Miles[1], A. Karegar[1], R. Schreiber[2], B. Schneller[1], J. Wuu[1]
[1]AMD, Fort Collins, CO, [2]AMD, Austin, TX

An 8MB level 3 cache, composed of 4 independent 2MB subcaches, is built on a 32nm SOI process. It features column-select aliasing to improve area efficiency, supply gating and floating bitlines to reduce leakage power, and centralized redundant row and column blocks to improve yield and testability. The cache operates above 2.4GHz at 1.1V.

14.4 A 28nm High-Density 6T SRAM with Optimized Peripheral-Assist Circuits for Operation Down to 0.6V — 2:45 PM

M. E. Sinangil[1], H. Mair[2], A. P. Chandrakasan[1]
[1]Massachusetts Institute of Technology, Cambridge, MA, [2]Texas Instruments, Dallas, TX

A 128kb SRAM macro employing a 0.12μm^2 6T high-density bitcell is fabricated in a low-power 28nm CMOS process. Hierarchical bit-line architecture, signal-boosting and pre-read-during-write schemes enable operation down to 0.6V. Performance of the memory scales from 20 to 400MHz in 0.6 to 1V operating voltage range where active power consumption scales from 2.8 to 68.5mW.

Break 3:00 PM

HIGH-PERFORMANCE SoCs & COMPONENTS

Session Chair: ***Shannon Morton,*** *Icera, Bristol, United Kingdom*
Associate Chair: ***Lew Chua-Eoan,*** *Qualcomm, San Diego, CA*

15.1 A Fully Integrated Multi-CPU, GPU and Memory Controller 32nm Processor **3:15 PM**
M. Yuffe, E. Knoll, M. Mehalel, J. Shor, T. Kurts, Intel, Haifa, Israel

This paper describes the 32nm Sandy Bridge processor that integrates up to 4 high-performance Intel Architecture (IA) cores, a power/performance optimized graphic processing unit (GPU) and memory and PCIe controllers in the same die. The paper describes some of the integration methods, power saving techniques and the clock distribution network.

15.2 An 80Gb/s Dependable Communication SoC with PCI Express I/F and 8 CPUs **3:45 PM**
S. Otani[1], H. Kondo[1], I. Nonomura[2], A. Ikeya[2], M. Uemura[2], Y. Hayakawa[1], T. Oshita[1], S. Kaneko[1], K. Asahina[2], K. Arimoto[1], S. Miura[3], T. Hanawa[3], T. Boku[3], M. Sato[3]
[1]Renesas Electronics, Itami, Japan, [2]Renesas Electronics, Kodaira, Japan
[3]University of Tsukuba, Tsukuba, Japan

An 80Gb/s dependable communication 45nm SoC with four 4X PCIe Rev 2.0 ports and 8 CPUs acts as a communication link in an HPC cluster and can extend its role to the computing nodes in embedded systems. To achieve a highly dependable network, the communication SoC continuously monitors the network conditions and performs adaptive routing dynamically. The power consumption is 0.8W/port and consumes 51.5% less power than 4X InfiniBand.

15.3 A Fully-Integrated 3-Level DC/DC Converter for Nanosecond-Scale DVS with Fast Shunt Regulation **4:00 PM**
W. Kim, D. M. Brooks, G-Y. Wei, Harvard University, Cambridge, MA

A fully integrated 3-level DC-DC converter, a hybrid of buck and switched-capacitor converters, is implemented in 0.13µm CMOS technology. The converter delivers up to 0.85A load current while regulating output voltages from 0.4 to 1.4V from a 2.4V input supply. The converter offers voltage scaling across 1V within 20ns and voltage-noise reduction using a shunt regulator.

15.4 A Low-Power Integrated x86-64 and Graphics Processor for Mobile Computing Devices **4:15 PM**
S. R. Gutta[1], D. Foley[2], A. Naini[1], R. Wasmuth[3], D. Cherepacha[4]
[1]AMD, Hyderabad, India, [2]AMD, Boxborough, MA, [3]AMD, Austin, TX, [4]AMD, Markham, Canada

Zacate is AMD's first generation Fusion SoC that combines x86 CPU and Radeon™ GPU on a single 40nm bulk CMOS die. The SoC uses an internal bus architecture and design techniques to optimize performance and memory bandwidth without compromising on power savings. Fine-grain power gating, dynamic voltage/frequency scaling and enhanced display refresh are key enablers for low-power operation.

15.5 A Programmable Adaptive Phase-Shifting PLL for Clock Data Compensation Under Resonant Supply Noise **4:45 PM**
D. Jiao, C. H. Kim, University of Minnesota, Minneapolis, MN

A digitally programmable phase-shifting PLL adaptively modulates the clock period under resonant supply noise to compensate for the increased circuit delay. Bit-error rate measurement results from a 1.2V 65nm test chip demonstrate a 3.7 to 7.4% improvement in maximum operating frequency for a standard pipeline circuit.

15.6 A Side-Channel and Fault-Attack Resistant AES Circuit Working on Duplicated Complemented Values **5:00 PM**
M. Doulcier-Verdier[1,2], J-M. Dutertre[2], J. Fournier[1,2], J-B. Rigaud[2], B. Robisson[1,2], A. Tria[1,2]
[1]CEA-LETI-MINATEC, Gardanne, France
[2]Ecole Nationale Supérieure des Mines de Saint-Etienne, Gardanne, France

A secure AES chip is implemented in HCMOS9gp 0.13µm STM technology. The counter-measures are based on duplication (for detecting faults) and work on complemented values in parallel (for protecting against side channel attacks). The chip is tested against side-channel and fault attacks and is resistant to both, illustrating the efficiency of the approach.

Conclusion **5:15 PM**

TIMETABLE OF ISSCC 2011 SESSIONS

Sunday, February 20th	**ISSCC 2011 TUTORIALS**					
8:00AM	**T1**: Integrated LC Oscillators		**T2:** Embedded Memories for SoC: Overview of Design, Test and Applications and Challenges in the Nano-Scale CMOS			
10:00AM	**T3:** Ultra Low-Power and Low-Voltage Digital-Circuit Design Techniques		**T4:** Layout – The Other Half of Nanometer Analog Design		**T5:** DPLL-Based Clock and Data Recovery	
12:30PM	**T6:** Practical Power-Delay Design Trade-offs		**T7:** Distortion in Cellular Receivers			
2:30PM	**T8:** Noise Analysis in Switched-Capacitor Circuits		**T9:** Interfacing Silicon with the Human Body: A Primer on Applications, Interface Circuits and Technologies for the Medical Market			
	ISSCC 2011 FORUMS					
8:00AM	**F1:** Advanced Transmitters for Wireless Infrastructure			**F2:** Ultra-Low Voltage VLSIs for Energy-Efficient Systems		
	ISSCC 2011 EVENING SESSIONS					
	7:30 PM ES0: Student Research Review		**8:00 PM ES1:** Data-Converter Breakthroughs in Retrospect		**8:00 PM ES2:** Wireless Sensor Systems: Solutions & Technology	
Monday, February 21st	**ISSCC 2011 PAPER SESSIONS**					
8:15AM	**Session 1:** Plenary Session					
1:30PM	**Session 2:** Technologies For Health	**Session 3:** RF Techniques	**Session 4:** Enterprise Processors & Components	**Session 5:** PLL	**Session 6:** Sensors & Energy Harvesting	
5:15PM	Social Hour: Poster Session - DAC/ISSCC Student-Design-Contest Winners; Author Interviews, Womens Reception					
	ISSCC 2011 SESSIONS					
8:00PM	**ES3:** Future System and Memory Architectures: Transformations by Technology and Applications		**ES4:** Body Area Networks (BAN): Technology, Solutions, and Standardization		**EP1:** Good, Bad, Ugly - 20 Years of Broadband Evolution: What's Next?	
Tuesday, February 22nd	**ISSCC 2011 PAPER SESSIONS**					
8:30AM	**Session 7:** Multimedia & Mobile	**Session 8:** Architectures & Circuits for Next Gen Wireline Xceivers	**Session 9:** Wireless & mm-Wave Connectivity	**Session 10:** Nyquist Rate Converters	**Session 11:** Non-Volatile Memory Solutions	
1:30PM	**Session 12:** Design in Emerging Technologies	**Session 13:** Analog Techniques	**Session 14:** High-Performance Embedded Memory **Session 15:** High-Performance SoCs & Components		**Session 16:** mm-Wave Design Techniques	**Session 17:** Biomedical & Displays
5:15PM	Industrial Demo Session (4-7), Author Interviews, Social Hour					
	ISSCC 2011 EVENING SESSIONS					
8:00PM	**ES5:** Gb/s+ Portable Wireless Communications		**ES6:** Technologies for Smart Grid and Smart Meter		**EP2:** 20-22nm Technology Options and Design Implications	
Wednesday, February 23rd	**ISSCC 2011 PAPER SESSIONS**					
8:30AM	**Session 18:** Organic Innovations **Session 19:** Low-Power Digital Techniques		**Session 20:** High-Speed Transceivers & Building Blocks	**Session 21:** Cellular	**Session 22:** DC/DC Converters	**Session 23:** Image Sensors
1:30PM	**Session 24:** Transmitter Blocks	**Session 25:** CDRs & Equalization Techniques	**Session 26:** Low-Power Wireless	**Session 27:** Oversampling Converters	**Session 28:** DRAM & High-Speed I/O	
5:15 PM	Author Interviews					
Thursday, February 24th	**ISSCC 2011 SHORT COURSE**					
8:00 AM	Cellular and Wireless LAN Transceivers: From Systems to Circuit Design					
	ISSCC 2011 FORUMS					
8:00AM	**F3:** Towards Personalized Medicine and Monitoring for Healthy Living	**F4:** Design of "Green" High-Performance Processor Circuits		**F5:** Image Sensors for 3D Capture	**F6:** High-Speed Transceivers: Standards, Challenges, and Future	

mm-WAVE DESIGN TECHNIQUES

Session Chair: ***Andreia Cathelin,*** *STMicroelectronics, Crolles Cedex, France*
Associate Chair: ***Brian Floyd,*** *North Carolina State University, Raleigh, NC*

16.1 A 21.7-to-27.8GHz 2.6-Degrees-rms 40mW Frequency Synthesizer in 45nm CMOS for mm-Wave Communication Applications — 1:30 PM

J. F. Osorio[1], C. S. Vaucher[1], B. Huff[2], E. v.d. Heijden[1], A. de Graauw[1]
[1]NXP Semiconductors, Eindhoven, The Netherlands
[2]NXP Semiconductors, San Diego, CA

A 21.7-to-27.8GHz PLL in 45nm CMOS combines a tuning range of 24.8%, a residual phase noise of 2.57 degrees rms, and power dissipation of 40mW. Combined with a frequency multiplier-by-two and a divider-by-two in a sliding-IF configuration, the PLL supplies the LO frequencies for the 60GHz 802.15.3c standard. Phase noise performance is suitable for higher-order modulation schemes.

16.2 A mm-Wave Quadrature VCO Based on Magnetically Coupled Resonators — 2:00 PM

U. Decanis[1], A. Ghilioni[1], E. Monaco[2,3], A. Mazzanti[1], F. Svelto[1]
[1]University of Pavia, Pavia, Italy
[2]University of Modena e Reggio Emilia, Modena, Italy
[3]Istituto Universitario di Studi Superiori di Pavia, Pavia, Italy

A ring of two magnetically coupled resonators is proposed for low phase noise quadrature generation at mm-Waves. Prototypes in 65nm CMOS show: 56 to 60.3GHz tunable oscillation frequency, a record phase noise FOM of -179dBc/Hz, and 1.5° maximum phase error while consuming 22mW.

16.3 A 6.5mW Inductorless CMOS Frequency Divider by 4 Operating up to 70GHz — 2:15 PM

A. Ghilioni[1], U. Decanis[1], E. Monaco[2,3], A. Mazzanti[1], F. Svelto[1]
[1]University of Pavia, Pavia, Italy
[2]University of Modena e Reggio Emilia, Modena, Italy
[3]Istituto Universitario di Studi Superiori di Pavia, Pavia, Italy

Differential amplifiers working as dynamic CML latches are proposed to realize compact, low power mm-Wave frequency dividers. An inductorless divider by 4 realized in 65nm CMOS technology demonstrates an operating frequency programmable from 20 to 70GHz with a maximum power dissipation of 6.5mW from 1V supply.

16.4 A 60GHz Antenna-Referenced Frequency-Locked Loop in 0.13µm CMOS for Wireless Sensor Networks — 2:30 PM

K-K. Huang, D. D. Wentzloff
University of Michigan, Ann Arbor, MI

A 60GHz frequency locked loop using an on-chip patch antenna as both a radiator and frequency reference is presented. The transmit frequency is locked to the maximum-efficiency point of the antenna with a mean of 59.34GHz and standard deviation of 195MHz. The circuit occupies 2.85mm^2 in 0.13µm CMOS, and consumes 29.6mW.

16.5 A 220-to-275GHz Traveling-Wave Frequency Doubler with -6.6dBm Power at 244GHz in 65nm CMOS — 2:45 PM

O. Momeni, E. Afshari
Cornell University, Ithaca, NY

A traveling-wave frequency doubler that effectively generates and combines the second harmonic from multiple transistors is proposed. The circuit operates from 220 to 275GHz in a 65nm CMOS process. Output power of -6.6dBm and conversion loss of 11.4dB are achieved at 244GHz.

Break 3:00 PM

16.6 Distributed Active Radiation for THz Signal Generation **3:15 PM**

K. Sengupta, A. Hajimiri
California Institute of Technology, Pasadena, CA

A novel concept of distributed active radiator which combines the signal generation, multiplication, filtering, and radiation in a single structure is introduced. An example 2x2 array in 45nm CMOS radiates 80μW of power and EIRP of -1dBm at 300GHz.

16.7 A 120GHz 10Gb/s Phase-Modulating Transmitter in 65nm LP CMOS **3:30 PM**

N. Deferm, P. Reynaert
KU Leuven, Leuven, Belgium

This paper presents a 120GHz fully integrated phase-modulated 65nm LP CMOS differential transmitter that achieves data rates above 10Gb/s. A wideband QPSK/8QAM modulator architecture is implemented. The transmitter occupies an area of 1875×940μm^2, operates from a 1V supply and consumes 200mW.

16.8 A 1.5GHz-Modulation-Range 10ms-Modulation-Period 180kHz$_{rms}$-Frequency-Error 26MHz-Reference Mixed-Mode FMCW Synthesizer for mm-Wave Radar Application **3:45 PM**

H. Sakurai, Y. Kobayashi, T. Mitomo, O. Watanabe, S. Otaka
Toshiba, Kawasaki, Japan

An FMCW synthesizer for mm-Wave radar application is implemented in 65nm CMOS. It achieves 1.5GHz modulation bandwidth, 10ms modulation period, and 180kHz$_{rms}$ frequency error from a 26MHz reference clock by using an analog/digital mixed-mode PLL, which relaxes resolution of the modulator in the analog PLL and the resolution of the DCO in the ADPLL. It occupies 1.7mm^2 and consumes 152mW from a 1.2V supply.

16.9 A Short-Range UWB Impulse-Radio CMOS Sensor for Human Feature Detection **4:15 PM**

T-S. Chu[1,2], J. Roderick[1], S. Chang[1], T. Mercer[1], C. Du[1], H. Hashemi[1]
[1]University of Southern California, Los Angeles, CA
[2]National Tsing Hua University, Hsinchu, Taiwan

A wireless non-contact sensor that enables detection, localization, and monitoring of people along with their specific features such as gait and cardiopulmonary activities is presented. The direct-sampling UWB Impulse Radio radar utilizes time-interleaved and equivalent time sampling, and employs averaging to drastically reduce the power consumption.

16.10 183GHz 13.5mW/Pixel CMOS Regenerative Receiver for mm-Wave Imaging Applications **4:45 PM**

A. Tang, M-C. Chang
University of California, Los Angeles, CA

A 183GHz, 65nm CMOS imaging receiver that uses a digital version of the super-regenerative architecture is realized to achieve 13.5mW/pixel power consumption while occupying only 1.3x104μm^2 of chip area. The receiver is suited to large arrays and offers a digital time-encoded output signal that allows for easy routing and multiplexing within imaging arrays.

Conclusion **5:15 PM**

BIOMEDICAL & DISPLAYS

Session Co-Chair: ***Sam Kavusi,*** *Bosch, Palo Alto, CA*
Session Co-Chair: ***Young-Sun Na,*** *LG Electronics, Seoul, Korea*

17.1 A 160µW 8-Channel Active Electrode System for EEG Monitoring — 1:30 PM

J. Xu[1,2], R. Yazicioglu[3], P. Harpe[1], K. A. Makinwa[2], C. van Hoof[3]
[1]imec - Holst Centre, Eindhoven, The Netherlands
[2]Delft University of Technology, Delft, The Netherlands; [3]imec, Leuven, Belgium

This paper describes an active electrode based on a chopper-stabilized amplifier for gel-free EEG monitoring. Several design techniques, such as back-end CM feedback, input-impedance boosting and digital offset calibration, are employed to achieve 82dB CMRR, a 2GΩ input impedance, rail-to-rail electrode offset rejection and $0.8\mu V_{rms}$ input-referred noise.

17.2 A 0.013mm² 5µW DC-Coupled Neural Signal Acquisition IC with 0.5V Supply — 2:00 PM

R. Muller[1], S. Gambini[1,2], J. M. Rabaey[1]
[1]University of California, Berkeley, CA; [2]Telegent Systems, Sunnyvale, CA

An area-efficient neural signal-acquisition chain replaces AC coupling capacitors and analog filters with a dual loop mixed-signal feedback architecture. The 65nm prototype provides simultaneous Spike and LFP band digitization in 0.013mm² while consuming 5.04µW from a 0.5V supply and achieving $49nV_{rms}/\sqrt{Hz}$ input noise.

17.3 An AC-Powered Optical Receiver Consuming 270µW for Transcutaneous 2Mb/s Data Transfer — 2:15 PM

S. Lange[1], H. Xu[2], C. Lang[1], H. Pless[1], J. Becker[2], H-J. Tiedkte[3], E. Hennig[1], M. Ortmanns[2]
[1]Institute for Microelectronic and Mechatronics Systems, Ilmenau, Germany
[2]Ulm University, Ulm, Germany; [3]Intelligent Medical Implants, Bonn, Germany

A transcutaneous IR data link for implantable systems with no DC terminals is presented. The link features an integrated optical receiver to enable data transfer of 2Mb/s. The chip is AC-powered at 13.56MHz, has a low drop CMOS rectifier and on-chip buffer. The data signal is provided as an AC-output current. The circuit draws $270\mu W_{max}$ from the AC link and consumes 2mm² in 0.35µm CMOS.

17.4 A Neural Stimulator Front-End with Arbitrary Pulse Shape, HV Compliance and Adaptive Supply Requiring 0.05mm² in 0.35µm HVCMOS — 2:30 PM

K. Sooksood, E. Noorsal, J. Becker, M. Ortmanns, Ulm University, Ulm, Germany

A flexible neural stimulator front-end is realized in 0.35µm HVCMOS. It provides arbitrary stimulation waveforms, high output voltage compliance, and supply to load adaption using a compliance monitor. Three types of charge balancers are implemented. The front-end occupies 0.05mm² per electrode, and is intended for a 1024-electrode epiretinal stimulator.

17.5 A Low Noise Current Readout Architecture for Fluorescence Detection in Living Subjects — 2:45 PM

R. T. Heitz[1], D. B. Barkin[2], T. D. O'Sullivan[1], N. Parashurama[1], S. S. Gambhir[1], B. A. Wooley[1]
[1]Stanford University, Stanford, CA; [2]National Semiconductor, Santa Clara, CA

An interface for a fluorescence sensor is realized in 0.18µm CMOS. An incremental ΔΣ modulator is combined with a capacitive TIA to implement a ramp oversampling architecture that achieves noise reduction and DR extension. The system is implanted in live mice, and continuous fluorescence sensing is demonstrated.

Break 3:00 PM

17.6 A Cubic-Millimeter Energy-Autonomous Wireless Intraocular Pressure Monitor **3:15 PM**

G. Chen, H. Ghaed, R.M. Haque, M. Wieckowski, Y. Kim, G. Kim, D. Fick, D. Kim, M. Seok, K. Wise, D. Blaauw, D. Sylvester
University of Michigan, Ann Arbor, MI

A 1mm^3 intraocular pressure monitor (IOPM) is presented for optimal implantation to track glaucoma and prevent blindness. It achieves 0.5mmHg resolution with a MEMS sensor and a ΔΣ capacitance-to-digital converter. The user wirelessly activates the IOPM, which responds by transmitting data using 4.7nJ/b. The 5.3nW IOPM harvests solar energy to recharge its battery at 80.6nW.

17.7 A 160×128 Single-Photon Image Sensor with On-Pixel 55ps 10b Time-to-Digital Converter **3:45 PM**

C. Veerappan[1], J. Richardson[2], R. Walker[2,3], D-U. Li[3], M. W. Fishburn[1], Y. Maruyama[1], D. Stoppa[4], F. Borghetti[4], M. Gersbach[5], R. K. Henderson[3], E. Charbon[1]
[1]Delft University of Technology, Delft, The Netherlands; [2]STMicroelectronics, Edinburgh, United Kingdom
[3]University of Edinburgh, Edinburgh, United Kingdom; [4]Fondazione Bruno Kessler - IRST, Trento, Italy
[5]EPFL, Lausanne, Switzerland

A 160×128 pixel array is presented detecting photons with 55ps time resolution. Each pixel comprises a counter, a time-to-digital converter, and a 10b memory, while a frame is read out every 20μs. The sensor is well suited for applications such as fast fluorescence lifetime imaging, optical rangefinding, and time-correlated single-photon counting.

17.8 Bidirectional OLED Microdisplay: Combining Display and Image Sensor Functionality into a Monolithic CMOS Chip **4:15 PM**

B. Richter, U. Vogel, R. Herold, K. Fehse, S. Brenner, L. Kroker, J. Baumgarten
Fraunhofer Institute for Photonic Microsystems, Dresden, Germany

This paper presents a bidirectional 320×240 monochrome OLED microdisplay with a nested 160×120 image sensor in 0.35μm CMOS for near-to-eye applications with embedded eye-tracking capabilities.

17.9 A 0.014mm^2 9b Switched-Current DAC for AMOLED Mobile Display Drivers **4:45 PM**

H-S. Kim, J-Y. Jeon, S-W. Lee, J-H. Yang, S-T. Ryu, G-H. Cho
KAIST, Daejeon, Korea

An area-efficient switched-current (SI) DAC structure that includes a highly linear current-mode S/H is proposed for current-mode AMOLED mobile display drivers. The designed 9b DAC occupies 0.014mm^2 in 0.35μm CMOS and achieves a 1μs/b conversion rate at a static current of 10μA and a 3.3V supply. The measured INL and DNL are 1.6LSB and 0.8LSB, respectively.

17.10 A 10b Resistor-Resistor-String DAC with Current Compensation for Compact LCD Driver ICs **5:00 PM**

C-W. Lu[1], P-Y. Yin[2], C-M. Hsiao[2], M-C. Chang[3]
[1]National Tsing Hua University, Hsinchu, Taiwan; [2]National Chi Nan University, Puli, Taiwan
[3]University of California, Los Angeles, CA

We propose a 10b RRDAC for compact LCD driver ICs with current compensation to offset the loading effect of parallel-connected resistor strings, eliminating the need for unity-gain buffers. The measured DNL and INL are 0.14 LSB and 0.61 LSB, respectively. The 10b RRDAC occupies 70% of the conventional 8b RDAC area.

Conclusion **5:15 PM**

INDUSTRY DEMONSTRATION SESSION

ISSCC 2011 is introducing a new event, the Industry Demonstration Session (IDS), to be held on Tuesday February 22nd, from 4 to 7 pm, Golden Gate Hall. IDS will feature live demonstrations of selected ICs presented by industry in regular paper sessions. These ICs include wireless communication, high-performance amplifiers, graphics processors, OLED microdisplays, energy harvesters, cellphones, and more. IDS is intended to exemplify the real-life applications made possible by new ICs presented this year. In the Advance Program, papers for which demonstrations are available will be notated by the symbol 

Papers in the regular day program (along with their times of presentation) for which demonstrations will be available on Tuesday, February 22, from 4 to 7 pm in Golden Gate Hall are listed below:

Tuesday February 22nd

7.6	**A MIMO WiMAX SoC in 90nm CMOS for 300km/h Mobility**	**11:15 AM**
7.7	**A 70Mb/s -100.5dBm Sensitivity 65nm LP MIMO Chipset for WiMAX Portable Router**	**11:45 AM**
9.3	**A 60GHz CMOS Phased-Array Transceiver Pair for Multi-Gb/s Wireless Communications**	**9:30 AM**
13.3	**Filterless Integrated Class-D Audio Amplifier Achieving 0.0012% THD+N and 96dB PSRR When Supplying 1.2W**	**2:30 PM**
13.8	**A 3.3V-Supply 120mW Differential ADC Driver Amplifier in 0.18µm SiGe BiCMOS with 108dBc IM3 at 100MHz**	**4:45 PM**
15.2	**An 80Gb/s Dependable Communication SoC with PCI Express I/F and 8 CPUs**	**3:45 PM**
15.4	**A Low-Power Integrated x86-64 and Graphics Processor for Mobile Computing Devices**	**4:15 PM**
17.8	**Bidirectional OLED Microdisplay: Combining Display and Image Sensor Functionality into a Monolithic CMOS Chip**	**4:15 PM**

Wednesday February 23rd

19.2	**An 82µA/MHz Microcontroller with Embedded FeRAM for Energy-Harvesting Applications**	**10:45 AM**
21.1	**A SAW-less GSM/GPRS/EDGE Receiver Embedded in a 65nm CMOS SoC**	**8:30 AM**
24.4	**An EDGE/GSM Quad-Band CMOS Power Amplifier**	**3:15 PM**
25.7	**A 10Gb/s Half-UI IIR-Tap Transmitter in 40nm CMOS**	**4:45 PM**
26.3	**A 2.4GHz ULP OOK Single-Chip Transceiver for Healthcare Applications**	**2:30 PM**

ES5: Gb/s+ Portable Wireless Communications

Organizer: **Didier Belot,** *STMicroelectronics, Crolles, France*
Chair: **George Chien,** *MediaTek, San Jose, CA*

In the last few years, several gigabit-class wireless communication standards have reached commercial status, these are mainly driven by the higher demand of fast data transfer in multimedia applications (e.g. wireless HDMI, video streaming, etc.) At the same time, the number of portable devices has been increasing drastically; in the coming decade, the adoption of gigabit-class wireless communication in these portable devices will become a standard. In order to meet this demand, the electronic industry has to address the limitations of power consumption and form factor in the present solutions.

In this special evening session, we have assembled a group of industrial experts in gigabit wireless communication to speak about their respective technology; and their views on how these standards can achieve lowest power AND highest data rate simultaneously. These standards include WirelessHD, Wireless Gigabit Alliance (802.11ad), 802.11ac etc...

Time	Topic
8:00	**Opportunities for 60GHz Short-Range Link** **Jri Lee,** *National Taiwan University, Taipei, Taiwan*
8:20	**WirelessHD 60 GHz Technology for Multi-Gbps Portable Wireless Applications** **Jeff Gilbert,** *SiBEAM, Sunnyvale, CA*
8:40	**Defining the Future of Multi-Gigabit Wireless Communications** **Ali S. Sadri,** *Intel, Santa Clara,CA*
9:00	**802.11ac Standard Toward Portable Applications** **Rolf De Vegt,** *Qualcomm, Santa Clara, CA*
9:20	**Panel Discussion**

ES6: Technologies for Smart Grid and Smart Meter

Chair/Co-organizer: **Jed Hurwitz,** *Gigle Networks, Edinburgh, United Kingdom*
Co-organizer: **Wing-Hung Ki,** *HKUST, Hong Kong, China*

A Smart Grid is a required infrastructure in the near future to meet the world's energy usage and generation demands. The US government has just injected 4.5B of stimulus into creating Smart Grid technologies, and this has created a huge momentum to implement the infrastructure today.

With a variety of diverse renewable power sources (wind, wave, solar) and new challenging-loads (e.g. electric vehicles), and usage models (e.g. peak shaving), the role of Smart Meters and communications among meters and appliances of your home is becoming increasingly important.

As consumers are becoming more aware of their own economic and environmental responsibilities regarding green power consumption and generation, connecting their appliances in the home to the WWW will also open up new opportunities in Energy 2.0 applications independent of the traditional utility companies.

This special topic session aims at introducing to the audience the market requirements and three of the key candidate technologies for the Smart Grid and Energy 2.0 applications: accurate power metering, powerline communications, and low-power wireless communications for energy management.

Time	Topic
8:00	**Introduction** **Jed Hurwitz,** *Gigle Networks, Edinburgh, United Kingdom*
8:20	**Smart Grid: An Overview** **Martin Manniche,** *GreenWave Reality, Irvine, CA*
8:40	**Metrology - Smart Meter Reading Devices** **Mick Mueck,** *Analog Devices, Wilmington, MA*
9:00	**HomePlug Green PHY** **Keith Findlater,** *Gigle Networks, Edinburgh, United Kingdom*
9:20	**Wireless Communications - Zigbee for Energy Management** **Sang-Gug Lee,** *KAIST, Daejeon, Korea*
9:40	**Open Discussion**

EP2: 20/22nm Technology Options and Design Implications

Organizer/Moderator: Don Draper**,** *True Circuits, Los Altos, CA*

The objective is that the panelists describe technology approaches to reducing local variation and leakage at the 20/22nm node and what the implications are for circuit designers of each. Potential topics include double-patterning and other lithographic methodologies, gate first or last, EUV, channel enhancements, new developments in strain engineering, reducing contact resistance, SOI vs. bulk, mobility enhancement, and new gate metals for Vt control. What will be the design responses to these and how will designers manage variability and leakage? Which of these technology options justify the fabrication cost and design complexity? What new design techniques would be needed to make optimum use of these technologies? The panelists will explore the divergence between manufacturers and the differing needs of IDMs and foundries. How will differing product requirements with respect to power dissipation and manufacturing cost influence how manufacturers balance these constraints?

Panelists:

Mark Bohr, *Intel, Hillsboro, OR*
Min Cao, *TSMC, Hsinchu, Taiwan*
Koichiro Ishibashi, *Renesas Electronics, Tokyo Japan*
Bill Liu, *Global Foundries, Sunnyvale, CA*
Ghavam Shahidi, *IBM, Fishkill, NY*

ORGANIC INNOVATIONS

Session Chair: ***Chris Van Hoof,*** *imec, Leuven, Belgium*
Associate Chair: ***Masaitsu Nakajima,*** *Panasonic, Osaka, Japan*

18.1 An 8b Organic Microprocessor on Plastic Foil — 8:30 AM

K. Myny[1,2], E. van Veenendaal[3], G. H. Gelinck[4], J. Genoe[1,5], W. Dehaene[1,2], P. Heremans[1,2]
[1]imec, Leuven, Belgium
[2]KU Leuven, Leuven, Belgium
[3]Polymer Vision, Eindhoven, The Netherlands
[4]TNO Science and Industry, Eindhoven, The Netherlands
[5]KHLim, Diepenbeek, Belgium

We present an 8b organic microprocessor in a dual-gate, pentacene (p-type only) thin-film transistor technology on a 25µm thin plastic foil. The design comprises a microprocessor foil and an instruction foil, in which a program is hardcoded. A running averager program is executed at clock frequencies up to 6Hz for V_{DD}=10V.

18.2 A 3.3V 6b 100kS/s Current-Steering D/A Converter Using Organic Thin-Film Transistors on Glass — 9:00 AM

T. Zaki[1,2], F. Ante[3], U. Zschieschang[3], J. Butschke[1], F. Letzkus[1], H. Richter[1], H. Klauk[3], J. N. Burghartz[1,2]
[1]Institute for Microelectronics Stuttgart (IMS CHIPS), Stuttgart, Germany
[2]University of Stuttgart, Stuttgart, Germany
[3]Max Planck Institute for Solid State Research, Stuttgart, Germany

A 3.3V 6b binary-weighted current-steering D/A converter using organic p-type thin-film transistors (OTFTs) is presented. The circuit occupies 12mm^2 and is fabricated on a glass substrate using silicon stencil shadow masks. The converter consumes 260µW at an output swing of 2V and has a maximum update rate of 100kS/s. The measured DNL and INL at an update rate of 1kS/s are -0.69LSB and 1.16LSB, respectively. For sinusoids between 31Hz and 3.1kHz, the minimum SFDR is 32dB.

18.3 A 1V Printed Organic DRAM Cell Based on Ion-Gel Gated Transistors with a Sub-10nW-per-Cell Refresh Power — 9:30 AM

W. Zhang[1], M. Ha[1], D. Braga[1], M. J. Renn[2], C. Frisbie[1], C. H. Kim[1]
[1]University of Minnesota, Minneapolis, MN
[2]Optomec, St. Paul, MN

A DRAM array is demonstrated in a printable, flexible and low-voltage ion-gel electrolyte organic TFT technology for the first time. Under an operating voltage of 1V, the retention time of the implemented gain cell array can exceed 1 minute and the refresh power is less than 10nW per cell. Full read and write functionality is verified from an 8×8 printed organic DRAM test-chip.

18.4 Fully Printed Organic CMOS Technology on Plastic Substrates for Digital and Analog Applications — 9:45 AM

A. Daami[1], C. Bory[1], M. Benwadih[1], S. Jacob[1], R. Gwoziecki[1], I. Chartier[1], R. Coppard[1], C. Serbutoviez[1], L. Maddiona[2], E. Fontana[2], A. Scuderi[2]
[1]CEA-LITEN, Grenoble, France
[2]STMicroelectronics, Catania, Italy

A complete fully printed CMOS technology on flexible substrates is presented. We show elementary logic, ring oscillators, and analog circuits such as current mirrors and differential pairs that are fully functional.

Break 10:00 AM

LOW-POWER DIGITAL TECHNIQUES

Session Chair: ***Stephen Kosonocky,*** *AMD, Fort Collins, CO*
Associate Chair: ***Ming-Yang Chao,*** *MediaTek, Hsinchu, Taiwan*

19.1 A Voltage-Scalable Biomedical Signal Processor Running ECG Using 13pJ/cycle at 1MHz and 0.4V — 10:15 AM

M. Ashouei[1], J. Hulzink[1], M. Konijnenburg[1], J. Zhou[1], F. Duarte[1], A. Breeschoten[1], J. Huisken[1], J. Stuyt[1], H. de Groot[1], F. Barat[2], J. David[2], J. Van Ginderdeuren[2]
[1]imec - Holst Centre, Eindhoven, The Netherlands, [2]NXP Semiconductors, Leuven, Belgium

An event-driven system with voltage and frequency range of 0.4-to-1.2V and 1-to-100MHz capable of tuning to application performance needs is presented. Scenario-based configurations keep the power of unused resources low. The system consumes between 13 and 95pJ/cycle running ECG depending on the operating voltage.

19.2 An 82µA/MHz Microcontroller with Embedded FeRAM for Energy-Harvesting Applications — 10:45 AM

M. Zwerg[1], A. Baumann[1], R. Kuhn[1], M. Arnold[1], R. Nerlich[1], M. Herzog[1], R. Ledwa[1], C. Sichert[1], V. Rzehak[1], P. Thanigai[2], B. O. Eversmann[1]
[1]Texas Instruments, Freising, Germany,[2]Texas Instruments, Dallas, TX

A 16b MCU SoC with an embedded 16kB FeRAM reduces active current consumption to 82µA/MHz for code execution from the NVM. The performance of the memory subsystem is based on a 2k×72b FeRAM array with 55ns access time combined with a 2-way 2-line associative cache. A dedicated FeRAM power system with a fast fail detection ensures uninterrupted refresh cycles to the FeRAM.

19.3 Comparison of 65nm LP Bulk and LP PD-SOI with Adaptive Power Gate Body Bias for an LDPC Codec — 11:00 AM

J. Le Coz[1], P. Flatresse[1], S. Engels[1], A. Valentian[2], M. Belleville[2], C. Raynaud[1], D. Croain[1], P. Urard[1]
[1]STMicroelectronics, Crolles, France,[2]CEA-LETI-MINATEC, Grenoble, France

An 802.11n 693Mb/s LDPC codec is implemented in the first available 65nm $3V_t$ 7ML Low-Power Partially Depleted SOI (LP PD-SOI) technology. Low resistivity forward-body-biasing power-switching techniques are introduced in PD-SOI to reduce the leakage current by 52.4% vs. bulk. We also increase frequency by 20% at 1.2V and decrease dynamic power by 30% at 360MHz.

19.4 A 77% Energy-Saving 22-Transistor Single-Phase-Clocking D-Flip-Flop with Adaptive-Coupling Configuration in 40nm CMOS — 11:15 AM

C. Teh, T. Fujita, H. Hara, M. Hamada, Toshiba, Kawasaki, Japan

We present a D flip-flop with 2 fewer transistors, and that is 77% more energy-saving than a transmission-gate flip-flop (TGFF), offering a 24% power reduction for a wireless LAN chip. A configuration with adaptively weakening state-retention coupling during transition, is introduced. It is operable down to 0.75V, with spreads of timing parameters comparable to TGFF, in 40nm CMOS.

19.5 A 62mV 0.13µm CMOS Standard-Cell-Based Design Technique Using Schmitt-Trigger Logic — 11:30 AM

N. Lotze[1,2], Y. Manoli[1,2]
[1]University of Freiburg - IMTEK, Freiburg, Germany, [2]HSG-IMIT, Villingen-Schwenningen, Germany

A leakage-reducing technology employing a Schmitt-trigger-enhanced digital cell library for supply-voltage minimization is tested using 8×8 multipliers. Gate-size scaling is demonstrated to reduce minimum supply up to a subthreshold-slope-limited point, resulting in reliable operation of combinational logic and flip-flops down to 62 to 84mV depending on the area overhead invested in standard 0.13µm bulk CMOS.

19.6 A 0.27V 30MHz 17.7nJ/transform 1024-pt Complex FFT Core with Super-Pipelining — 11:45 AM

M. Seok[1], D. Jeon[1], C. Chakrabarti[2], D. Blaauw[1], D. Sylvester[1]
[1]University of Michigan, Ann Arbor, MI, [2]Arizona State University, Tempe, AZ

This paper proposes circuit and architectural techniques to improve energy efficiency in aggressively voltage-scaled circuits, while also enhancing performance and robustness. The approaches are validated on an FFT core in 65nm CMOS with measured throughput of 234ktransforms/s. The core consumes 17.7nJ per 1024-pt complex FFT operating at 30MHz with V_{dd}=0.27V.

Conclusion **12:00 PM**

HIGH-SPEED TRANSCEIVERS & BUILDING BLOCKS

Session Chair: ***Jae-Yoon Sim,*** *Pohang University of Science and Technology, Pohang, Korea*

Associate Chair: ***Masafumi Nogawa,*** *NTT, Atsugi, Japan*

20.1 A 4-Channel 10.3Gb/s Transceiver with Adaptive Phase Equalizer for 4-to-41dB Loss PCB Channel — 8:30 AM

Y. Hidaka[1], T. Horie[2], Y. Koyanagi[2], T. Miyoshi[2], H. Osone[1], S. Parikh[1], S. Reddy[1], T. Shibuya[1], Y. Umezawa[2], W. W. Walker[1]
[1]Fujitsu Laboratories of America, Sunnyvale, CA
[2]Fujitsu Laboratories, Kawasaki, Japan

An analog linear equalizer, a 1-tap DFE, and a 3-tap pre-emphasis (PE) are adapted to cancel 4.1 to 41.7dB loss at 10.3Gb/s or 4.9 to 34.9dB loss at 12.5Gb/s. PE taps are adapted to cancel phase distortion due to PCB material. Fabricated in 90nm CMOS, TX/RX occupies 0.420mm^2 and consumes 316mW from 1.2V at 10.3Gb/s per channel.

20.2 A 1.0625-to-14.025Gb/s Multimedia Transceiver with Full-rate Source-Series-Terminated Transmit Driver and Floating-Tap Decision-Feedback Equalizer in 40nm CMOS — 9:00 AM

S. Quan, F. Zhong, W. Liu, P. Aziz, T. Jing, J. Dong, C. Desai, H. Gao, M. Garcia, G. Hom, T. Huynh, H. Kimura, R. Kothari, L. Li, C. Liu, S. Lowrie, K. Ling, A. Malipatil, R. Narayan, T. Prokop, C. Palusa, A. Rajashekara, A. Sinha, C. Zhong, E. Zhang
LSI, Milpitas, CA

The transceiver employs on-chip RX AC coupling and equalizes up to 26dB insertion loss at 14.025Gb/s with a linear equalizer, 10-tap DFE, and 4-tap TX FFE in SST driver. Presented techniques enable direct feedback for 1st-tap ISI cancellation, and the positions of four DFE taps to be independently adapted over the range 7 to 38. A prototype in 40nm CMOS passes 16GFC test at 14.025Gb/s.

20.3 Analog-DFE-Based 16Gb/s SerDes in 40nm CMOS That Operates Across 34dB Loss Channels at Nyquist with a Baud Rate CDR and 1.2V$_{pp}$ Voltage-Mode Driver — 9:30 AM

A. K. Joy[1], H. Mair[2], H-C. Lee[3], A. Feldman[3], C. Portmann[3], N. Bulman[1], E. Cordero Crespo[1], P. Hearne[1], P. Huang[3], B. Kerr[1], P. Khandelwal[1], F. Kuhlmann[2], S. Lytollis[1], J. Machado[1], C. Morrison[2], S. Morrison[2], S. Rabii[3], D. Rajapaksha[1], V. Ravinuthula[2], G. Surace[1]
[1]Texas Instruments, Northampton, United Kingdom
[2]Texas Instruments, Dallas, TX
[3]Arda Technologies, Mountain View, CA

A 14-tap DFE and analog-equalizer-based SerDes that achieves a 10^{-17} BER across a 34dB loss channel at 16Gb/s for a power dissipation of 235mW/lane in 40nm CMOS. The SerDes uses an enhanced-swing TX voltage mode driver giving a 1200mV$_{pk-pk}$ differential output and a receiver with a baud-rate CDR lock point that minimizes the number of samplers for adaptation and two-tap speculation.

Break 10:00 AM

20.4 An 8.4mW/Gb/s 4-Lane 48Gb/s Multi-Standard-Compliant Transceiver in 40nm Digital CMOS Technology **10:15 AM**

M. Ramezani, M. Abdalla, A. Shoval, M. Van Ierssel, A. Rezayee, A. McLaren, C. Holdenried, J. Pham, E. So, D. Cassan, S. Sadr
SnowBush-Gennum, Toronto, Canada

This work presents a 4-lane transceiver implemented in 40nm CMOS technology which operates over a wide range of data rates from 1 to 12Gb/s (48Gb/s aggregated) using NRZ coding. The supply voltages are 0.9V and 1.8V. No inductors are used in the design to provide a VCO with a wide tuning range, to reduce area and to improve design portability.

20.5 A Pattern-Guided Adaptive Equalizer in 65nm CMOS **10:45 AM**

S. Shahramian[1], C. Ting[1], A. Sheikholeslami[1], H. Tamura[2], M. Kibune[2]
[1]University of Toronto, Toronto, Canada
[2]Fujitsu Laboratories, Kawasaki, Japan

A digital adaptive engine for an analog equalizer counts the occurrence of 6 out of 16 4-bit patterns in the received data and adjusts the equalizer gains at f_N and $f_N/2$, where f_N is half the bit rate. Measured results at 6Gb/s confirm that the engine opens a closed eye to within 2.6% of optimal vertical opening, while consuming 16.8mW from a 1.2V supply in 65nm CMOS.

20.6 A 6Gb/s Receiver with 32.7dB Adaptive DFE-IIR Equalization **11:15 AM**

Y-C. Huang, S-I. Liu
National Taiwan University, Taipei, Taiwan

A 6Gb/s receiver with 32.7dB adaptive DFE-IIR feedback technique in 90nm CMOS process is presented. The amplitude and RC time constant of an IIR filter is automatically adjusted to compensate large channel loss. The power consumption is 52mW and the area is 0.089mm^2.

20.7 A 5.4Gb/s Adaptive Equalizer Using Asynchronous-Sampling Histograms **11:45 AM**

W-S. Kim, C-K. Seong, W-Y. Choi
Yonsei University, Seoul, Korea

We demonstrate an adaptive equalizer using asynchronous-sampling histograms. The optimal filter condition is selected by finding the histogram having the largest peak value. The prototype chip realized in 0.13µm CMOS technology equalizes 5.4Gb/s data through 40cm, 80cm, and 120cm PCB traces and 3m DisplayPort cable. The chip consumes 35mW and occupies 340×525µm^2 of area.

20.8 A 0.076mm^2 3.5GHz Spread-Spectrum Clock Generator with Memoryless Newton-Raphson Modulation Profile in 0.13µm CMOS **12:00 PM**

S. Hwang, M. Song, Y-H. Kwak, I. Jung, C. Kim
Korea University, Seoul, Korea

A 0.076mm^2 frequency-locked loop based 3.5GHz spread-spectrum clock generator is presented with memoryless nonlinear Newton-Raphson modulation profile in 0.13µm CMOS. The SSCG supports 14 frequency deviations from ±0.5 to 3.5% with Δ=0.5% and 3 modulation frequencies of f_m, $2f_m$ and $3f_m$. It achieves an EMI reduction of 19.14dB with 0.5% down spreading and an f_m of 31kHz.

Conclusion 12:15 PM

CELLULAR

Session Chair: ***Myung-Woon Hwang,*** *FCI, Sungnam, Kyunggi, Korea*
Associate Chair: ***Taizo Yamawaki,*** *Renesas Electronics, Gunma, Japan*

21.1 A SAW-less GSM/GPRS/EDGE Receiver Embedded in a 65nm CMOS SoC 8:30 AM

I.S-C. Lu[1], C-Y. Yu[2], Y-H. Chen[2], L-C. Cho[2], C-H. E. Sun[2], C-C. Tang[2], G. Chien[1]
[1]MediaTek, San Jose, CA; [2]MediaTek, Hsinchu, Taiwan

A 65nm CMOS quad-band RX, embedded in a GSM SoC, complies with the ETSI standard without the need of external SAW filters. By using a Class-AB low noise amplifier and passive mixer with current-mode LPF, the RX achieves sensitivity of <-110 dBm, out-of-band P1dB of > +1dBm, and IIP2/IIP3 of >+44dBm/0dBm respectively. The transceiver consumes 58.9mA in the RX mode and occupies 4.94 mm^2.

21.2 A 9-Band WCDMA/EDGE Transceiver Supporting HSPA Evolution 9:00 AM

M. Nilsson[1], S. Mattisson[2], N. Klemmer[3], M. Anderson[2], T. Arnborg[1], P. Caputa[1], S. Ek[2], L. Fan[1], H. Fredriksson[1], F. Garrigues[3], H. Geis[1], H. Hagberg[1], J. Hedestig[1], H. Huang[3], Y. Kagan[3], N. Karlsson[1], H. Kinzel[1], T. Mattsson[1], T. Mills[3], F. Mu[2], A. Mårtensson[1], L. Nicklasson[1], F. Oredsson[1], U. Ozdemir[1], F. Park[3], T. Pettersson[1], T. Påhlsson[1], M. Pålsson[1], S. Ramon[3], M. Sandgren[1], P. Sandrup[1], A-K. Stenman[1], R. Strandberg[2], L. Sundström[2], F. Tillman[2], T. Tired[1], S. Uppathil[3], J. Walukas[3], E. Westesson[1], X. Zhang[1], P. Andreani[1,4]
[1]ST-Ericsson, Lund, Sweden; [2]Ericsson, Lund, Sweden
[3]Formerly with ST-Ericsson, Raleigh, NC; [4]Lund University, Lund, Sweden

A 90nm RFCMOS cellular transceiver supporting 9 WCDMA/EDGE bands with full RX diversity is presented. All RF ports are single-ended with internal matching.

The 2G RX/TX+LO consume 129mW/126mW, while the 3G TX+RX+LO consume 269mW. The SAW-less 2G/3G RX has an NF of 2.3 to 2.5dB, with an IIP2 of +58dBm and an IIP3 of -6dBm.

The 2G TX EVM is below 1.5% using a polar TX architecture with a two-point PLL, while the 3G TX EVM is below 4%. The RX EVM is below 3%.

The transceiver occupies a die area of 3.8×3.8mm^2 and is currently in production.

21.3 A 65nm CMOS SoC with Embedded HSDPA/EDGE Transceiver, Digital Baseband and Multimedia Processor 9:30 AM

A. Cicalini[1], S. Aniruddhan[1], R. Apte[2], F. Bossu[1], O. Choksi[1], D. Filipovic[1], K. Godbole[1], T-P. Hung[1], C. Komninakis[1], D. Maldonado[1], C. Narathong[1], B. Nejati[1], D. O'Shea[1], X. Quan[1], R. Rangarajan[1], J. Sankaranarayanan[1], A. See[1], R. Sridhara[1], B. Sun[1], W. Su[1], K. van Zalinge[1], G. Zhang[1], K. Sahota[1]
[1]Qualcomm, San Diego, CA; [2]Qualcomm, Santa Clara, CA

A multimode transceiver in 65nm CMOS supports quad-band GSM/EDGE and 3 bands UMTS. The radio occupies 13.4mm^2 of an SoC that integrates mixed-signal, audio, DSP and memory cores. It eliminates UMTS interstage RX SAW while realizing sensitivity of -111dBm. DPLL-based GSM polar transmitter peak battery current is 53mA in LB.

Break 10:00 AM

21.4 A Receiver for WCDMA/EDGE Mobile Phones with Inductorless Front-End in 65nm CMOS **10:15 AM**

F. Beffa[1], T. Sin[1], A. Tanzil[2], D. Ivory[3], B. Tenbroek[1], J. Strange[1], W. Ali-Ahmad[2]
[1]MediaTek, West Malling, United Kingdom; [2]MediaTek, Singapore, Singapore
[3]MediaTek, Cambridge, United Kingdom

A 65nm CMOS eight-channel receiver for WCDMA, TD-SCDMA and EDGE with an inductorless front-end provides an out-of-band IIP3 of -2dBm and an NF below 2.5dB up to 2.2GHz. The receiver is part of a multimode transceiver requiring no interstage SAW filters for 3G operation. The front-end area per channel is 0.11mm^2.

21.5 A Compact SAW-less Multiband WCDMA/GPS Receiver Front-End with Translational Loop for Input Matching **10:45 AM**

X. He, H. Kundur
NXP Semiconductors, Eindhoven, The Netherlands

This paper describes a compact multiband SAW-less receiver design using a translational loop for input matching. It eliminates inductors for input matching without noise penalty, and decouples the optimization of noise and linearity performance from the input matching. The receiver current consumption can be adapted to the wanted input signal levels.

21.6 A Multiband LTE SAW-less Modulator with -160dBc/Hz RX-Band Noise in 40nm LP CMOS **11:00 AM**

V. Giannini[1], M. Ingels[1], T. Sano[2], B. Debaillie[1], J. Borremans[1], J. Craninckx[1]
[1]imec, Leuven, Belgium; [2]Renesas Electronics, Itami, Japan

A 40nm CMOS transmitter combines adaptive out-of-band noise filtering with voltage-sampling up-conversion to achieve RX-band noise down to -162dBc/Hz and OP1dB up to 11dBm in all LTE FDD bands, including the most challenging VII, XI and XII. The Pre-Power Amplifier (PPA) offers 60dB gain tuning range with scalable power consumption. The transmitter operates up to 5.5GHz with up to 40MHz channel bandwidth, achieving EVM better than 3% and LO feedthrough below -40dBc.

21.7 A Fully Digital Multimode Polar Transmitter Employing 17b RF DAC in 3G Mode **11:15 AM**

Z. Boos[1], A. Menkhoff[1], F. Kuttner[2], M. Schimper[1], J. Moreira[1], H. Geltinger[1], T. Gossmann[1], P. Pfann[1], A. Belitzer[1], T. Bauernfeind[3]
[1]Infineon Technologies, Neubiberg, Germany; [2]Infineon Technologies, Villach, Austria
[3]DICE, Linz, Austria

A fully digital multimode, multiband polar transmitter, designed in 65nm CMOS, achieves -160dBc/Hz far-off noise at all 3GPP Rel. 7 specified duplex distances. The transmitter employs 17b and 19b RFDAC in 3G and 2,5G modes respectively. Targeting a true multimode, multiband power amplifier application, the transmitter supports GSM/EDGE/EDGEEvo/WCDMA/HSPA+ modes and consumes 35mA DG09 weighted current in 3G mode.

21.8 A Low-Power Wideband Polar Transmitter for 3G Applications **11:45 AM**

M. Youssef[1,2], A. Zolfaghari[1], H. Darabi[1], A. Abidi[2]
[1]Broadcom, Irvine, CA; [2]University of California, Los Angeles, CA

A low-power, multimode polar transmitter based on a two-point injection PLL with a linearized VCO is implemented in 65nm CMOS. A wideband frequency-locked loop nested inside the PLL linearizes and accurately controls the VCO gain. Differential delay between AM-PM paths is self-calibrated. In WCDMA mode, the transmitter achieves -42dBc ACLR1, -159dBc/Hz noise at 45MHz, and 2.9%EVM at 0dBm. Transmitter current is 40mA and active area is 0.7mm^2.

Conclusion 12:15 PM

DC/DC CONVERTERS

Session Chair: ***Francesco Rezzi,*** *Marvell Semiconductor, Pavia, Italy*
Associate Chair: ***Baher Haroun,*** *Texas Instruments, Dallas, TX*

22.1 A Fully Integrated Power-Management Solution for a 65nm CMOS Cellular Handset Chip — 8:30 AM

A. J. D'Souza[1], R. Singh[1], R. J[1], G. Chowdary[1], A. Seedher[1], S. Somayajula[1], N. R. Nalam[1], L. Cimaz[2], S. Le Coq[2], P. Kallam[3], S. Sundar[3], S. Cheng[3], S. Tumati[3], W. Huang[3]
[1]ST Ericsson, Bangalore, India
[2]ST Ericsson, Rennes, France
[3]ST Ericsson, Austin, TX

This paper presents a 5.5V direct-to-battery PMU integrated as part of a GSM/EDGE single-chip in a 65nm deep-Nwell standard CMOS process, comprising a 20V tolerant battery charger, a regulated -2V charge pump for ground referred headset power amplifier, modular LDOs, a hysteretic buck converter and a programmable series/parallel WLED controller.

22.2 A Digitally Controlled DC-DC Converter for SoC in 28nm CMOS — 9:00 AM

F. Kuttner[1], H. Habibovic[1], T. Hartig[1], M. Fulde[1], G. Babin[1], A. Santner[1], P. Bogner[1], C. Kropf[1], H. Riesslegger[1], U. Hodel[2]
[1]Infineon Technologies, Villach, Austria
[2]Infineon Technologies, Munich, Germany

A digitally controlled DC-DC converter with more than 90% efficiency and input voltages up to 5.5V, with fully integrated driver is realized in Hi-K 28nm CMOS. The regulator makes use of a digital intense control loop and can operate in PFM and PWM DCM/CCM modes achieving a peak efficiency >90% over a wide range of load currents.

22.3 20µA to 100mA DC-DC Converter with 2.8 to 4.2V Battery Supply for Portable Applications in 45nm CMOS — 9:30 AM

S. Bandyopadhyay[1], Y. K. Ramadass[1,2], A. P. Chandrakasan[1]
[1]Massachusetts Institute of Technology, Cambridge, MA
[2]Texas Instruments, Dallas, TX

A 45nm CMOS DC-DC buck converter is designed to supply 20µA-100mA output load from a Li-ion battery (2.8-4.2V). It uses PWM and PFM control modes using an I-C DAC based DPWM with sleep mode. Internal SC converters are used for the control circuit and stacking in the power stage. The converter achieves 87.4% peak efficiency.

Break **10:00 AM**

22.4 A Digitally Controlled DC-DC Buck Converter with Lossless Load-Current Sensing and BIST Functionality — 10:15 AM

T. Liu[1], H. Yeom[1], B. Vermeire[1], P. Adell[2], B. Bakkaloglu[1]
[1]Arizona State University, Tempe, AZ
[2]Jet Propulsion Laboratory, Pasadena, CA

A 1-to-5.5V output range, 1A load current, digitally controlled buck regulator with inductor built-in self-test (BIST) and digital lossless load current sensing scheme using inductor DCR is presented. The BIST module can measure filter inductance in a range from 3.7 to 22.3µH with an average 2.1% error and inductor DCR in the range from 15 to 75mΩ with an average 3.6% error. Load current sensing error is less than 2% for 100 to 750mA range. BIST and current sensing modules occupy less than 6% of the total chip area.

22.5 Zero-Order Control of Boost DC-DC Converter with Transient Enhancement Using Residual Current **10:45 AM**

T-H. Kong, Y-J. Woo, S-W. Wang, S-W. Hong, G-H. Cho
KAIST, Daejeon, Korea

This paper introduces a new zero-order control scheme for a Boost DC-DC converter free from the dynamics of inductor and output capacitor. A robust control method is suggested utilizing phase differences in on/off signals. A Chip is implemented in a 0.35μm BCD process and 88% efficiency is obtained for an 8V output from 3.7V at 480mW output power working with 833kHz.

22.6 Robust and Efficient Synchronous Buck Converter with Near-Optimal Dead-Time Control **11:15 AM**

S. Lee, S. Jung, J. Huh, C. Park, C-T. Rim, G-H. Cho
KAIST, Daejeon, Korea

A near optimum dead-time switching control method for the synchronous buck converter is developed. On/off dead-times are adjusted precisely by error integral control, therefore providing robustness against load variations. Moreover, a dv/dt-induced turn-on prevention scheme is used to lower the switching loss. 90% efficiency at 1MHz switching frequency is achieved when operating at 3.3V input/1.5V output voltage.

22.7 A 90% Peak Efficiency Single-Inductor Dual-Output Buck-Boost Converter with Extended-PWM Control **11:45 AM**

W. Xu[1], Y. Li[1], Z. Hong[1], D. Killat[2]
[1]Fudan University, Shanghai, China
[2]Brandenburg University of Technology, Cottbus, Germany

By using the proposed extended-PWM control, the SIDO buck-boost converter can automatically select operation mode and enable each output step down/up conversion. The converter, implemented in 0.25μm CMOS, maintains a high efficiency over 80% in wide output range with a 2.5W maximum total power and operates from 2.5 to 5V supply.

22.8 Spurious-Noise-Free Buck Regulator for Direct Powering of Analog/RF Loads Using PWM Control with Random Frequency Hopping and Random Phase Chopping **12:15 PM**

C. Tao, A. A. Fayed
Iowa State University, Ames, IA

A PWM-controlled DC-DC buck regulator with random frequency hopping and phase chopping is proposed and implemented in 0.35μm CMOS. The design eliminates all spurs at the output of the converter and maintains a -70dBm noise floor peak with negligible overhead on power and area. The implementation also eliminates duty cycle disturbance and transients associated with it due to hopping.

Conclusion **12:30 PM**

IMAGE SENSORS

Session Chair: ***Tetsuo Nomoto,*** *Sony, Kanagawa, Japan*
Associate Chair: ***Jan Bosiers,*** *DALSA Professional Imaging, Eindhoven, The Netherlands*

23.1 An 80μV$_{rms}$-Temporal-Noise 82dB-Dynamic-Range CMOS Image Sensor with a 13-to-19b Variable-Resolution Column-Parallel Folding-Integration/Cyclic ADC **8:30 AM**

M-W. Seo[1], S. Suh[1], T. Iida[2], H. Watanabe[3], T. Takasawa[1], T. Akahori[2], K. Isobe[2], T. Watanabe[2], S. Itoh[1], S. Kawahito[1,2]
[1]Shizuoka University, Hamamatsu, Japan
[2]Brookman Technology, Hamamatsu, Japan; [3]Sanei Hytechs, Hamamatsu, Japan

A 1Mpixel, 7.5μm pixel pitch, 0.18μm CMOS image sensor with column-parallel folding-integration and cyclic ADCs has 80μV$_{rms}$ (1.2e$^-$) temporal noise, 82dB dynamic range using 64 samplings in the folding-integration ADC mode. Variable gray-scale resolution of 13b through 19b is obtained by changing the number of samplings for pixel outputs.

23.2 A Sub-Electron Readout Noise CMOS Image Sensor with Pixel-Level Open-Loop Voltage Amplification **9:00 AM**

C. Lotto[1,2], P. Seitz[3,4], T. Baechler[2]
[1]Heliotis, Root Längenbold, Switzerland; [2]CSEM, Zurich, Switzerland
[3]CSEM, Landquart, Switzerland; [4]EPFL, Neuchâtel, Switzerland

A 256×256 pixel, 11μm pixel pitch, 0.18μm CMOS image sensor featuring pixel-level open-loop voltage amplification reaches a readout noise of 0.86e$^-$ and a dynamic range of 90dB in a single readout using a low-complexity readout circuit with 60fps. A reset method based on negative feedback allows the use of open-loop amplification while achieving PRNU of 2.5% and a peak linearity error of 1.7%.

23.3 A 320×256 90dB SNR and 25μm-Pixel-Pitch Infrared Image Sensor **9:15 AM**

A. Peizerat[1], F. Guellec[1], M. Tchagaspanian[1], E. De Borniol[1], S. Bisotto[1], P. Maillard[2]
[1]CEA-LETI-MINATEC, Grenoble, France; [2]Sofradir, Chatenay-Malabry, France

A 320×256 pixel, 25μm pixel pitch, 0.18μm CMOS readout IC with a 15b pixel-level ADC for cooled hybrid infrared image sensors is presented. The chip is hybridized with a long wave infrared detector fabricated in HgCdTe via indium bump bonding and yields 90dB SNR at 50fps operation in a snapshot mode.

23.4 A 16 Mfps 165kpixel Backside-Illuminated CCD **9:30 AM**

T. G. Etoh[1], D. H. Nguyen[1], S. V. Dao[1], C. L. Vo[1], M. Tanaka[1], K. Takehara[1], T. Okinaka[1], H. van Kuijk[2], W. Klaassens[2], J. Bosiers[2], M. Lesser[3], D. Ouellette[3], H. Maruyama[4], T. Hayashida[4], T. Arai[4]
[1]Kinki University, Higashi-Osaka, Japan; [2]DALSA PI, Eindhoven, The Netherlands
[3]University of Arizona, Tucson, AZ; [4]NHK Science and Technical Laboratories, Tokyo, Japan

A 362×456, 43.2μm pixel pitch, 16Mfps, backside-illuminated CCD storing 117 consecutive images recorded with charge carrier multiplication achieves image capture capability with less than 9photons/pixel. The full well capacity of 8,000e$^-$ at 16Mfps and 22,000 e$^-$ at 4Mfps is realized.

23.5 A 300mm Wafer-Size CMOS Image Sensor with In-Pixel Voltage-Gain Amplifier and Column-Level Differential Readout Circuitry **9:45 AM**

Y. Yamashita, H. Takahashi, S. Kikuchi, K. Ota, M. Fujita, S. Hirayama, T. Kanou, S. Hashimoto, G. Momma, S. Inoue
Canon, Kawasaki, Japan

A 1.6Mpixel, 202×205mm^2 CMOS image sensor on 300mm wafer consists of pixels of 160μm pitch with a 0-to-24dB variable gain in-pixel voltage amplifier. Reset and integrated signals are simultaneously read out from the pixel through a pair of column lines. It achieves a sensitivity of 25Me$^-$/lux·s, random noise of 13e$^-_{rms}$ and operates at 100fps with global synchronous shutter.

Break 10:00 AM

23.6 A 128×96 Pixel Event-Driven Phase-Domain ΔΣ-Based Fully Digital 3D Camera in 0.13µm CMOS Imaging Technology **10:15 AM**

R. J. Walker[1,2], J. A. Richardson[2], R. K. Henderson[1]
[1]University of Edinburgh, Edinburgh, United Kingdom; [2]STMicroelectronics, Edinburgh, United Kingdom

A 128×96 pixel, 44.65µm pitch, digital 3D camera SOC in 0.13µm CMOS imaging technology is reported. Each pixel comprises a single-photon avalanche diode and phase-domain ΔΣ loop for on-chip computation of distance. 3D images are obtained at 20fps with sub-16cm repeatability error and ±0.5cm linearity over 0.4-to-2.4m at significantly reduced system power and processing cost.

23.7 An Angle-Sensitive CMOS Imager for Single-Sensor 3D Photography **10:45 AM**

A. Wang, P. R. Gill, A. Molnar, Cornell University, Ithaca, NY

A 0.18µm 3D CMOS image sensor composed of angle-sensitive pixels captures both local incident angle and intensity. The 400×384 pixel array has a 7.5µm pitch and local diffraction gratings over each pixel. One such chip, using one lens and ambient light, enables post-capture refocus and range finding accurate to ±1.3cm at 50cm.

23.8 A 1/13-inch 30fps VGA SoC CMOS Image Sensor with Shared Reset and Transfer-Gate Pixel Control **11:15 AM**

R. Johansson[1], A. Storm[1], C. Stephansen[1], S. Eikedal[1], T. Willassen[1], S. Skaug[1], T. Martinussen[1], T. Whittlesea[2], G. Ali[3], J. Ladd[3], X. Li[3], S. Johnson[3], V. Rajasekaran[3], Y. Lee[4], J. Bai[3], M. Flores[3], G. Davies[2], H. Samiy[2], A. Hanvey[2], D. Perks[2]
[1]Aptina Imaging, Oslo, Norway; [2]Aptina Imaging, Bracknell, United Kingdom
[3]Aptina Imaging, San Jose, CA; [4]Aptina Imaging, Corvallis, OR

This paper describes a 1/13-inch VGA SoC CMOS image sensor, with a 1.75µm pixel pitch capable of outputting 30fps at full resolution. The paper focuses on the sensor core, with a size of 1.77mm^2 and a power consumption of 17mW. Thel pixel architecture uses a pixel-sharing scheme that improves low-light performance.

23.9 A 1/2.33-inch 14.6M 1.4µm-Pixel Backside-Illuminated CMOS Image Sensor with Floating Diffusion Boosting **11:30 AM**

S. Lee[1], K. Lee[1], J. Park[1], H. Han[1], Y. Park[1], T. Jung[1], Y. Jang[1], B. Kim[1], Y. Kim[1], S. Hamami[2], U. Hizi[2], M. Bahar[2], C. Moon[1], J. Ahn[1], D. Lee[1], H. Goto[1], Y-T. Lee[1]
[1]Samsung Electronics, Yong-In, Korea; [2]Samsung Semiconductor, Ramat-Gan, Israel

A 1/2.33-inch 14.6Mpixel CIS is developed by employing a 1.4µm BSI pixel with a floating diffusion boosting scheme driven by coupling with additional row-wise metal-line, achieving 30% higher QE than that of an FSI sensor, 87lux for SNR=10, and no image lag, for high-sensitivity and high-speed applications.

23.10 An APS-C Format 14b Digital CMOS Image Sensor with a Dynamic Response Pixel **11:45 AM**

D. Pates[1], J-H. Lyu[1], S. Osawa[2], I. Takayanagi[2], T. Sato[2], T. Bales[3], K. Kawamura[2], E. Pages[2], S. Matsuo[2], T. Kawaguchi[2], T. Sugiki[2], N. Yoshimura[2], J. Nakamura[2], J. Ladd[1], Z. Yin[1], R. Iimura[1], X. Fan[1], S. Johnson[1], A. Rayankula[1], R. Mauritzson[1], G. Agranov[1]
[1]Aptina Imaging, San Jose, CA; [2]Aptina Imaging, Tokyo, Japan; [3]Aptina Imaging, Bracknell, United Kingdom

A 16M APS-C format CMOS image sensor with 14b SAR-ADC and 8-lane LVDS output is fabricated and characterized. A 4.78µm dynamic response pixel with ring gate transistors and no STI provides 62% QE, responsivity of 49.5ke$^-$/lux·s, and dark current of 17e$^-$/s @ 60°C. The readout noise floor is 2.2e$^-$ with column FPN of 0.11e$^-$ in HCG mode.

23.11 A 17.7Mpixel 120fps CMOS Image Sensor with 34.8Gb/s Readout **12:00 PM**

T. Toyama[1], K. Mishina[1], H. Tsuchiya[1], T. Ichikawa[1], H. Iwaki[1], Y. Gendai[1], H. Murakami[1], K. Takamiya[2], H. Shiroshita[1], Y. Muramatsu[1], T. Furusawa[1]
[1]Sony, Kanagawa, Japan; [2]Sony LSI Design, Kanagawa, Japan

A 17.7Mpixel CMOS image sensor with a 27.5mm optical format realizes 120fps at 12b using 90nm CMOS. This sensor achieves 2.75e$^-_{rms}$ random noise at 12b, 120fps with a maximum data rate of 34.8Gb/s. The 16 channels of scalable low-voltage signaling I/F with embedded clock operate at 2.376Gb/s each and the single-slope ADC ramp generator runs at 2.376GHz.

Conclusion **12:15 PM**

TRANSMITTER BLOCKS

Session Chair: ***Francesco Svelto,*** *Universita degli Studi di Pavia, Pavia, Italy*
Associate Chair: **Shoji Otaka,** *Toshiba, Kawasaki, Japan*

24.1 A 40nm Wideband Direct-Conversion Transmitter with Sub-Sampling-Based Output Power, LO Feedthrough and I/Q Imbalance Calibration — 1:30 PM

E. Lopelli, S. Spiridon, J. van der Tang
Broadcom, Bunnik, The Netherlands

A 40nm CMOS auto-calibrated wideband OFDM transmitter is presented. TX image, LO feedthrough and output power are calibrated by sub-sampling the TX output by the RX ADC. The TX attains ACPR>55dBc, and IM3<-64dBc up to 200MHz baseband frequency. Digital-assisted calibration assures IR>55dBc, LO feedthrough>40dBc and an output power level accurate within ±0.6dB over PVT up to 1.6GHz LO.

24.2 A Flip-Chip-Packaged 1.8V 28dBm Class-AB Power Amplifier with Shielded Concentric Transformers in 32nm SoC CMOS — 2:00 PM

Y. Tan, H. Xu, M. A. El-tanani, S. Taylor, H. Lakdawala
Intel, Hillsboro, OR

A flip-chip packaged, class-AB PA with Shielded Concentric Transformers, for a 1.8V supply in 32nm SoC CMOS, is presented. It achieves 28dBm Psat with peak 31.9% PAE, 26.5dBm P1dB, and 21dBm average power with 16% PAE meeting -25dB EVM for OFDM 64QAM without digital pre-distortion linearization.

24.3 A Switched-Capacitor Power Amplifier for EER/Polar Transmitters — 2:30 PM

S-M. Yoo, J. S. Walling, E. Woo, D. J. Allstot
University of Washington, Seattle, WA

A digitally controlled switched-capacitor-based RF power amplifier is implemented in 90nm CMOS. It delivers peak and average output powers of 25.2 and 17.7 dBm respectively, for a 64-QAM OFDM-modulated signal with a measured EVM of 2.9% in the 2.4 GHz band. Peak and average PAE are 55.2% and 32.1% respectively.

Break 3:00 PM

24.4 An EDGE/GSM Quad-Band CMOS Power Amplifier — 3:15 PM

W. Kim, K. Yang, J. Han, J. Chang, C-H. Lee
Samsung Electro-Mechanics, Atlanta, GA

A 0.18µm dual-mode quad-band CMOS PA with an integrated passive device is assembled in a 5x5mm2 QFN package. The linear PA for EDGE mode achieves an average output power of 28.5 dBm, a PAE of 22 %, an ACPR of -57dBc and an EVM-rms of 1.6% for GSM/EGSM bands. The PA as a switching amplifier performs an output power of 34.5dBm with a PAE of 55% for GSM application.

24.5 A Compact 1V 18.6dBm 60GHz Power Amplifier in 65nm CMOS — 3:45 PM

J. Chen, A. M. Niknejad
University of California, Berkeley, CA

A 60GHz PA is demonstrated in 65nm digital CMOS with 1V supply. By using an efficient and compact 4-input transformer power combiner, the PA achieves 18.6dBm P_{SAT}, 15dBm P_{-1dB} and 15.1% PAE while only occupying 0.28 mm^2 silicon area. The PA maintains 17.8dBm P_{SAT} and 12.6% PAE over the IEEE band from 58GHz to 64GHz.

Conclusion 4:00 PM

CDRs & EQUALIZATION TECHNIQUES

Session Chair: ***SeongHwan Cho,*** *KAIST, Daejon, Korea*
Associate Chair: ***Tatsuya Saito,*** *Hitachi, Tokyo, Japan*

25.1 A 5Gb/s Adaptive DFE for 2× Blind ADC-Based CDR in 65nm CMOS — 1:30 PM

B. Abiri[1], A. Sheikholeslami[1], H. Tamura[2], M. Kibune[2]
[1]University of Toronto, Toronto, Canada
[2]Fujitsu Laboratories, Kawasaki, Japan

This paper presents an adaptive DFE for a 2× blind ADC-based receiver. The proposed adaptive engine uses a triangular desired waveform, instead of a fixed desired level, to shape the equalizer output in spite of blind nature of sampling. The measured results confirm the adaptive engine restores a 5Gb/s eye subjected to 13dB of attenuation at Nyquist frequency to an equivalent of 320mV of vertical opening. The digital CDR consumes 78mW from a 1.2V supply.

25.2 A 0.5-to-2.5Gb/s Reference-less Half-Rate Digital CDR with Unlimited Frequency Acquisition Range and Improved Input Duty-Cycle Error Tolerance — 2:00 PM

R. Inti, W. Yin, A. Elshazly, N. Sasidhar, P. Hanumolu
Oregon State University, Corvallis, OR

A reference-less half-rate digital CDR with unlimited frequency acquisition range and improved tolerance to input duty cycle error is presented. Fabricated in 0.13µm CMOS, the CDR consumes 6.1mW at 2Gb/s from a 1.2V supply and operates from 0.5 to 2.5Gb/s.

25.3 A TDC-less 7mW 2.5Gb/s Digital CDR with Linear Loop Dynamics and Offset-Free Data Recovery — 2:30 PM

W. Yin, R. Inti, A. Elshazly, P. Hanumolu
Oregon State University, Corvallis, OR

A digital CDR that combines linear and bang-bang phase detectors to decouple the design tradeoff between jitter generation and jitter transfer is presented. Fabricated in a 0.13µm CMOS, it achieves an operating range of 0.5 to 3.2Gb/s. At 2.5Gb/s, the power is 7mW and the RMS jitter of the recovered clock is 6ps.

Break **3:00 PM**

25.4 A Digital Wideband CDR with ±15.6Kppm Frequency Tracking at 8Gb/s in 40nm CMOS — 3:15 PM

H. Pan[1], M. Valliappan[2], W. Zhang[1], K. Vakilian[1], S-H. Lee[1], H. Hatamkhani[1], M. Caresosa[1], K. Khanoyan[1], H. Tong[1], D. Tran[1], A. Brewster[1], I. Fujimori[1]
[1]Broadcom, Irvine, CA
[2]Broadcom, Austin, TX

A digital CDR using a double-edge triggered shift register to speed up the phase rotation and a latency minimized loop filter to widen the bandwidth achieves ±15.6Kppm tracking range and up to 10MHz tracking bandwidth at 8Gb/s in 40nm CMOS. A mostly digital transceiver is described that utilizes the digital wideband CDR to enable a wide range of applications.

25.5 A 20Gb/s Digitally Adaptive Equalizer/DFE with Blind Sampling **3:45 PM**

Y-M. Ying, S-I. Liu
National Taiwan University, Taipei, Taiwan

An adaptation equalizer using blind sampling is presented. It consists of an analog equalizer and a decision-feedback equalizer. This adaptive equalizer is fabricated in a 65nm CMOS process. It achieves a data rate of 20Gb/s with BER<10^{-12} over a 35cm FR4 board consuming 52mW from a 1.2V supply.

25.6 A 15Gb/s 0.5mW/Gb/s 2-Tap DFE Receiver with Far-End Crosstalk Cancellation **4:15 PM**

M. Honarvar Nazari, A. Emami-Neyestanak
California Institute of Technology, Pasadena, CA

A 2-tap DFE receiver is implemented in a 45nm SOI technology. High data rate and low power dissipation is achieved using a switched-capacitor S/H/summer front-end which enables FEXT cancellation with 33µW/Gb/s/lane power overhead. It equalizes 15Gb/s data over a link with >14dB loss and dissipates 7.5mW from a 1.2V supply.

25.7 A 10Gb/s Half-UI IIR-Tap Transmitter in 40nm CMOS **4:45 PM**

H. Cirit, M. J. Loinaz
Netlogic Microsystems, Santa Clara, CA

A transmit equalizer is designed for 10Gb/s serial communication and features half-UI, IIR and FIR taps. Both SFI transmitter waveform dispersion penalty (TWDPc for direct-attach copper cable) and data-dependent jitter (DDJ) specifications are met with a single transmitter configuration. The circuit, fabricated in 40nm CMOS, dissipates 125mW and occupies 0.22mm^2.

25.8 A 13.8mW 3.0Gb/s Clock-Embedded Video Interface with DLL-Based Data-Recovery Circuit **5:00 PM**

S. Jang, H. Song, S. Ye, D-K. Jeong
Seoul National University, Seoul, Korea

A 3.0Gb/s video-data interface that minimizes the complexity in the receiver is presented. The DLL generates multiphase clocks that sample 8bit data from a data stream with 3bit-wide delimiter of zero-to-one transition. Fabricated in 0.13µm CMOS, the receiver operates from 1.36 to 3.0Gb/s with a BER of <10^{-12} while consuming 13.8mW at 3.0Gb/s and occupying 0.064mm^2.

Conclusion **5:15 PM**

LOW-POWER WIRELESS

Session Chair: ***Jan Crols,*** **AnSem,** *Heverlee, Belgium*
Associate Chair: ***Stefan Heinen,*** *RWTH Aachen University, Aachen, Germany*

26.1 A 7.9μW Remotely Powered Addressed Sensor Node Using EPC HF and UHF RFID Technology with -10.3dBm Sensitivity — 1:30 PM

H. Reinisch[1], M. Wiessflecker[2], S. Gruber[2], H. Unterassinger[1], G. Hofer[2], W. Pribyl[1], G. Holweg[2]
[1]Graz University of Technology, Graz, Austria
[2]Infineon Technologies, Graz, Austria

A fully passive multifrequency EPC-compatible RFID sensor node is fabricated in a 0.13μm CMOS process. The chip operates from 13.56MHz to 2.45GHz. The RF sensitivity is -10.3dBm, and the overall power consumption is 7.9μW. Embedded on-chip temperature sensing, signal monitoring and controlling of off-chip sensors are implemented.

26.2 An Isolator-less CMOS RF Front-End for UHF Mobile RFID Reader — 2:00 PM

E-H. Kim[1], K. Lee[1], J. Ko[2]
[1]KAIST, Daejeon, Korea
[2]PHYCHIPS, Daejeon, Korea

An isolator-less, low-power RF front-end architecture for mobile UHF RFID readers is presented. To eliminate the additive noise from a strong TX leakage, a self-correlation RX aligns the phase of an LO and TX leakage. For a highly efficient system, a polar ASK TX is implemented with envelope feedback linearization, achieving a wide linear DR while offering good PA efficiency.

26.3 A 2.4GHz ULP OOK Single-Chip Transceiver for Healthcare Applications — 2:30 PM

M. Vidojkovic[1], X. Huang[1], P. Harpe[1], S. Rampu[1], C. Zhou[1], L. Huang[1], K. Imamura[2], B. Busze[1], F. Bouwens[1], M. Konijnenburg[1], J. Santana[1], A. Breeschoten[1], J. Huisken[1], G. Dolmans[1], H. de Groot[1]
[1]Holst Centre / imec, Eindhoven, The Netherlands
[2]Panasonic, Osaka, Japan

A ULP OOK single-chip transceiver for WBAN applications in 90nm CMOS is presented, operating in the 2.4GHz medical BAN and ISM bands. The TX outputs pulse-shaped OOK with 0dBm peak power, and consumes 2.53mW with 50% OOK. The RX front-end supports up to 5Mb/s with –75dBm sensitivity. Including the digital part, the RX consumes 715μW at 1Mb/s data rate, oversampled at 3MHz.

Break **3:00 PM**

26.4 A 120μW MICS/ISM-Band FSK Receiver with a 44μW Low-Power Mode Based on Injection-Locking and 9x Frequency Multiplication — 3:15 PM

J. Pandey, J. Shi, B. Otis
University of Washington, Seattle, WA

We report a 120μW MICS/ISM-band receiver for wireless sensing. The low-IF FSK receiver achieves a -90dBm sensitivity at 200kb/s data rate. It has a 44μW low-power mode with -70dBm sensitivity. We use 9x frequency multiplication, allowing a 44.5MHz LO. The injection-locked LO has a settling time of <100nS. The receiver front-end has a noise figure of 13dB and OIP3 of 7.6dBm.

26.5 A GPS/Galileo SoC with Adaptive In-Band Blocker Cancellation in 65nm CMOS — 3:30 PM

C-H. Wu[1], W-C. Tsai[1], C-G. Tan[2], C-N. Chen[1], K-I. Li[1], J-L. Hsu[1], C-L. Lo[1], H-H. Chen[1], S-Y. Su[1], K-T. Chen[1], M. Chen[1], O. Shana'a[2], S-H. Chou[1], G. Chien[3]
[1]MediaTek, Hsinchu, Taiwan
[2]MediaTek, Singapore, Singapore
[3]MediaTek, San Jose, CA

A host-based GPS/Galileo SoC achieves 2.0dB NF, -165dBm chip-in tracking sensitivity, -5dBm out-of-band IIP3, and consumes 18mW (8.6mW for RF portion). The device can sustain out-of-band blockers as high as +16dBm at its antenna port without the need of external LNA and inter-stage SAW filter. By using the proposed scheme of in-band blocker cancellation, this SOC can withstand 12 in-band CW blockers simultaneously. The chip consumes 6.6mm^2 in a 65nm CMOS process.

26.6 A 0.05-to-10GHz 19-to-22GHz and 38-to-44GHz SDR Frequency Synthesizer in 0.13µm CMOS — 3:45 PM

S. Rong, H. Luong
HKUST, Hong Kong, China

An SDR frequency synthesizer covers not only all the wireless standards from 47MHz to 10GHz (including 14-band MB-OFDM UWB) but also the 802.15.3c standard from 57 to 66GHz. Implemented in a 0.13µm CMOS, the prototype occupies an active area of 3mm^2, consumes a total power of 33 to 83mW, and achieves a measured phase noise of -139.6dBc/Hz at 3MHz offset from a 1.7GHz carrier.

26.7 A 4.6GHz MDLL with -46dBc Reference Spur and Aperture Position Tuning — 4:15 PM

T. A. Ali[1,2], A. A. Hafez[1], R. Drost[2], R. Ho[2], C-K. Yang[1]
[1]University of California, Los Angeles, CA
[2]Oracle, Menlo Park, CA

An MDLL with aperture position tuning is presented. A calibration loop slides a phase interpolator and places the aperture in optimal position to minimize period jitter and spurs. A charge pump with static and dynamic mismatch is designed to minimize phase errors. The MDLL is implemented in a 90nm process. It achieves -46dBc of reference spur at 4.6GHz and consumes 6.8mW.

Conclusion **4:30 PM**

OVERSAMPLING CONVERTERS

Session Chair: ***Kong-Pang Pun,*** *Chinese University of Hong Kong, Hong Kong, China*
Associate Chair: ***Lucien Breems,*** *NXP, Eindhoven, The Netherlands*

27.1 A 4GHz CT ΔΣ ADC with 70dB DR and -74dBFS THD in 125MHz BW — 1:30 PM

M. Bolatkale[1], L. Breems[1], R. Rutten[1], K. Makinwa[2]
[1]NXP Semiconductors, Eindhoven, The Netherlands
[2]Delft University of Technology, Delft, The Netherlands

A 4GHz CT ΣΔ ADC is presented with a loop filter topology that absorbs the pole caused by the input capacitance of its 4b quantizer and compensates for the excess delay caused by the quantizer's latency. Implemented in 45nm CMOS, the ADC achieves 70dB DR and -74dBFS THD in a 125MHz BW, while dissipating 256mW and occupying only 0.9mm^2.

27.2 An 8mW 50MS/s CT ΔΣ Modulator with 81dB SFDR and Digital Background DAC Linearization — 2:00 PM

J. G. Kauffman, P. Witte, J. Becker, M. Ortmanns
Ulm University, Ulm, Germany

A 3rd-order single-loop CT ΔΣ modulator with a 4b quantizer is sampled at 500MHz with an OSR of 10. It achieves 63.5dB SNDR and -81dB SFDR in a 25MHz bandwidth without DEM. The DAC nonlinearity is digitally estimated and corrected. All feedback amplifiers are compensated for finite GBW influence. The modulator occupies 0.15mm^2 in 90nm CMOS and achieves an FOM of 125fJ/conversion-step.

27.3 A Third-Order DT ΔΣ Modulator Using Noise-Shaped Bidirectional Single-Slope Quantizer — 2:30 PM

N. Maghari, U-K. Moon
Oregon State University, Corvallis, OR

A single-slope quantizer using modified bidirectional discharging is proposed. This quantizer provides first-order shaping of quantization noise and is used as the quantizer of a second-order delta-sigma loop. The fabricated prototype ADC achieves 78.2dB SNDR at 50MHz sampling speed at OSR of 24 with 2.9mW power consumption.

Break 3:00 PM

27.4 A 250mV 7.5µW 61dB SNDR CMOS SC ΔΣ Modulator Using a Near-Threshold-Voltage-Biased CMOS Inverter Technique **3:15 PM**

F. Michel, M. Steyaert
KU Leuven, Leuven, Belgium

An ultra-low-voltage SC ΔΣ converter using a near-threshold-voltage-biasing technique is reported. This guarantees reliable operation of inverter-based integrators over temperature while running at a supply voltage of 250mV. An SNDR of 61dB is achieved for a BW of 10 kHz with a total power consumption of only 7.5µW.

27.5 A 84dB SNDR 100kHz Bandwidth Low-Power Single Op-Amp Third-Order ΔΣ Modulator Consuming 140µW **3:45 PM**

A. Pena Perez, E. Bonizzoni, F. Maloberti
University of Pavia, Pavia, Italy

A third-order ΔΣ modulator with single operational amplifier achieves 13.6 bits with 100kHz signal bandwidth and consumes 140µW. The time-interleaved two-integrators scheme is a modification of a second-order prototype. A slew-rate boost enables minimum power in a two stages op-amp. The SFDR is 96dB with an FoM of 54fJ/conversion-step.

27.6 A 1.7mW 11b 1-1-1 MASH ΔΣ Time-to-Digital Converter **4:15 PM**

Y. Cao[1,2], P. Leroux[1,3], W. De Cock[2], M. Steyaert[1]
[1]KU Leuven, Leuven, Belgium
[2]SCK-CEN, Mol, Belgium
[3]KH Kempen, Geel, Belgium

The first radiation tolerant third-order ΔΣ TDC is presented. The converter, implemented in 0.13µm CMOS, employs a 1-1-1 MASH architecture. It achieves an ENOB of 11b and a time resolution of 5.6ps, when the OSR is 250. A radiation assessment up to 5MGy proves the TDC's robustness. The TDC core consumes 1.7mW and occupies 0.11mm^2.

27.7 A 120dB-SNR 100dB-THD+N 21.5mW/Channel Multibit CT ΔΣ DAC **4:45 PM**

A. Bandyopadhyay, M. Determan, S. Kim, K. Nguyen
Analog Devices, Wilmington, MA

A continuous-time 8b oversampling DAC architecture is presented, which measures 120dB of SNR and 100dB of THD+N while consuming 21.5mW/channel. This performance is achieved by using a 3-level rotational data-shuffling scheme along with analog low-power techniques. The 1.35mm^2/channel chip is fabricated in 0.35µm DPQM CMOS process.

27.8 A 108dB-DR 120dB-THD and 0.5V_{rms} Output Audio DAC with Inter-Symbol-Interference-Shaping Algorithm in 45nm CMOS **5:15 PM**

L. Risbo[1], R. Hezar[2], B. Kelleci[2], H. Kiper[2], M. Fares[2]
[1]Texas Instruments, Copenhagen, Denmark
[2]Texas Instruments, Dallas, TX

An oversampled audio multi-bit DAC using a mismatch-shaping algorithm designed to shape element mismatch errors concurrently with inter-symbol-interference is presented. It can achieve THD powers better than -120dBFs with spurious tone free operation at low signal levels. It is implemented in 45nm CMOS with 0.16mm^2 area, 0.875mW power, and 0.5V_{rms} output.

Conclusion **5:45 PM**

DRAM & HIGH-SPEED I/O

Session Chair: ***Yasuhiro Takai,*** *Elpida Memory, Sagamihara, Japan*
Associate Chair: ***Heinz Hoenigschmid,*** *Elpida Memory, Munich, Germany*

28.1 An 8.4Gb/s 2.5pJ/b Mobile Memory I/O Interface Using Simultaneous Bidirectional Dual (Base+RF)-Band Signaling **1:30 PM**

G-S. Byun[1], Y. Kim[1], J. Kim[2], S-W. Tam[1], H-H. Hsieh[3], P-Y. Wu[3], C. Jou[3], J. Cong[1], G. Reinman[1], M-C. Chang[1]
[1]University of California, Los Angeles, CA; [2]Hongik University, Seoul, Korea; [3]TSMC, Hsinchu, Taiwan

A dual baseband and RF-band interconnect (DBI) system can support simultaneous bidirectional data communication for mobile memory I/O interface operating at 8.4Gb/s with the energy efficiency of 2.5pJ/bit. The transceiver is fabricated in 65nm 1V CMOS process and the active area is 0.14mm^2.

28.2 A 2.7Gb/s/mm^2 0.9pJ/b/Chip 1Coil/Channel ThruChip Interface with Coupled-Resonator-Based CDR for NAND Flash Memory Stacking **2:00 PM**

N. Miura, Y. Take, M. Saito, Y. Yoshida, T. Kuroda, Keio University, Yokohama, Japan

A 2.7Gb/s/mm^2 0.9pJ/b/chip inductive-coupling interface for 0.18µm NAND Flash memory stacking performs 10× bandwidth (or occupies 0.1× area) and consumes 0.5× energy compared to the latest work. The total number of coils needed to form a channel is reduced from 6 to 1 by a one-coil relayed transmission scheme and coupled-resonator-based CDR.

28.3 A 12Gb/s Non-Contact Interface with Coupled Transmission Lines **2:30 PM**

T. Takeya, L. Nan, S. Nakano, N. Miura, H. Ishikuro, T. Kuroda, Keio University, Yokohama, Japan

The paper describes a high data rate non-contact memory card interface using a single channel. The wideband channel based on differential coupled transmission lines achieves measured coupling level of 16dB and a bandwidth from 2.6 to 9GHz. The system achieves 12Gb/s with BER<10^{-13} at a communication distance of 1mm.

28.4 A 4.8Gb/s Impedance-Matched Bidirectional Multi-Drop Transceiver for High-Capacity Memory Interface **2:45 PM**

W-Y. Shin[1], G-M. Hong[1], H. Lee[1], J-D. Han[1], S. Kim[1], K-S. Park[1], D-H. Lim[1], J-H. Chun[2], D-K. Jeong[1], S. Kim[1]
[1]Seoul National University, Seoul, Korea; [2]Sungkyunkwan University, Suwon, Korea

An impedance-matched bidirectional multi-drop (IMBM) DQ bus and corresponding transceiver architecture effectively eliminates reflective ISI at all the stubs of a 4-slot 8-drop channel. A prototype is designed and fabricated in 0.13µm standard CMOS process. We achieve a data-rate of 4.8Gb/s with a timing margin of 0.61UI in TX mode and 0.73UI in RX mode when the BER threshold is 10^{-9}.

Break 3:00 PM

28.5 A 1.2V 12.8GB/s 2Gb Mobile Wide-I/O DRAM with 4×128 I/Os Using TSV-Based Stacking **3:15 PM**

J-S. Kim, C. Oh, H. Lee, D. Lee, H-R. Hwang, S. Hwang, B. Na, J. Moon, J-G. Kim, H. Park, J-W. Ryu, K. Park, S-K. Kang, S-Y. Kim, H. Kim, J-M. Bang, H. Cho, M. Jang, C. Han, J-B. Lee, K. Kyung, J-S. Choi, Y-H. Jun
Samsung Electronics, Hwasung, Korea

A 1.2V 1Gb mobile SDRAM with 4×128 DQ per each is fabricated. It consumes 330.6mW read power during 4-channel operation, achieving 12.8GB/s data bandwidth. Test correlation techniques to verify functions through microbumps are developed. A stack of 2 dies with 7.5µm diameter TSVs is fabricated and tested, resulting in 76% overall package yield.

28.6 A 40nm 2Gb 7Gb/s/pin GDDR5 SDRAM with a Programmable DQ Ordering Crosstalk Equalizer and Adjustable Clock-Tracking BW **3:45 PM**

S-J. Bae, Y-S. Sohn, T-Y. Oh, S-H. Kim, Y-S. Yang, D-H. Kim, S-H. Kwak, H-S. Seol, C-H. Shin, M-S. Park, G-H. Han, B-C. Kim, Y-K. Cho, H-R. Kim, S-Y. Doo, Y-S. Kim, D-S. Kang, Y-R. Choi, S-Y. Bang, S-Y. Park, Y-J. Shin, G-S. Moon, C-G. Park, W-S. Kim, H-J. Yang, J-D. Lim, K-I. Park, J. Choi, Y-H. Jun

Samsung Electronics, Hwasung, Korea

A 2Gb 7Gb/s/pin GDDR5 SDRAM is implemented in a 40nm DRAM process. 4-DQ group transmitter has a crosstalk equalizer with programmable aggressor capability to match the switchable DQ ordering across board and package designs. Tri-mode clocking is employed for multiple clock jitter filtering bandwidth: PLL off (bypass), LC-PLL (~5MHz) and injection-locked oscillator (~100MHz).

28.7 A 58nm 1.8V 1Gb PRAM with 6.4MB/s Program BW **4:15 PM**

H. Chung, B. Jeong, B. Min, Y. Choi, B-H. Cho, J. Shin, J. Kim, J. Sunwoo, J-M. Park, Q. Wang, Y-J. Lee, S. Cha, D. Kwon, S. Kim, S. Kim, Y. Rho, M-H. Park, J. Kim, I. Song, S. Jun, J. Lee, K. Kim, K-W. Lim, W-R. Chung, C. Choi, H. Cho, I. Shin, W. Jun, S. Hwang, K-W. Song, K. Lee, S-W. Chang, W-Y. Cho, J-H. Yoo, Y-H. Jun

Samsung Electronics, Hwasung, Korea

A PRAM implemented in a 58nm PRAM process with a low-power double-data-rate nonvolatile-memory (LPDDR2-N) interface is presented. To enhance the core-write performance of 6.4MB/s, we design a data-comparison write with inversion flag (DCWI) scheme and a timing controlling method. For the read, a mid-array pre-charge scheme is presented.

28.8 A 1.6V 1.4Gb/s/pin Consumer DRAM with Self-Dynamic Voltage-Scaling Technique in 44nm CMOS Technology **4:45 PM**

H-W. Lee[1,2], K-H. Kim[1], Y-K. Choi[1], J-H. Shon[1], N-K. Park[1], K-W. Kim[1], C. Kim[2], Y-J. Choi[1], B-T. Chung[1]

[1]Hynix Semiconductor, Icheon, Korea; [2]Korea University, Seoul, Korea

A DRAM with self-dynamic voltage scaling (SDVS) technique is fabricated in 44nm CMOS technology. The SDVS technique saves power by changing the internal supply voltage depending on the process skew and the operating frequency. The SDVS reduces the IDD3N current by 12% at 200MHz, 25°C and the DLL consumes 6.25pJ/Hz at 90°C at 1.8V.

28.9 An Embedded DRAM Technology for High-Performance NAND Flash Memories **5:15 PM**

D. Takashima, M. Noguchi, N. Shibata, K. Kanda, H. Sukegawa, S. Fujii, Toshiba, Yokohama, Japan

A 32KB embedded DRAM with 1.5μm^2 cell using a 32nm standard NAND-Flash-memory process realizes 2.4mm^2/Mb density. A ±100mV cell signal is obtained in a 3fF cell by self-boosted cell node to 4V and 60fF bitline capacitance. A 2-step-rise/fall wordline and a-half-of-"1"-data dummy cell result in stable eDRAM operation with 90ns cycle and 15ns burst.

28.10 A 700MHz 2T1C Embedded DRAM Macro in a Generic Logic Process with No Boosted Supplies **5:30 PM**

K. Chun, W. Zhang, P. Jain, C. Kim, University of Minnesota, Minneapolis, MN

A logic-compatible embedded DRAM test macro with no boosted supplies in a 65nm CMOS achieves a 700MHz random access frequency and a 500μs refresh period at 1.1V 85°C. Key features include a 2T1C gain cell for boosted supply-less DRAM operation, a single-ended 7T SRAM redundancy cell integrated with the DRAM array, and a storage voltage monitor for adaptive refresh control.

Conclusion **5:45 PM**

SPICE
40th Anniversary

Please join the Celebration of the 40th Anniversary of the SPICE (Simulation Program with Integrated Circuit Emphasis) circuit simulator. It was born as a UC Berkeley class project and first released in 1971. The Computer History Museum (Mountain View, CA) will host a roundtable discussion among leaders in the creation and world-wide dissemination of this invaluable and universal design tool. Topics will include the origins, evolution, and future of SPICE, and its seminal role as early open-source software.

For more information, and to register please see:
http://www.computerhistory.org/events/

Cellular and Wireless LAN Transceivers: From Systems to Circuit Design

Organizer: **John R. Long,** *Delft University of Technology, Delft, The Netherlands*

Instructors: **Hooman Darabi,** *Broadcom, Irvine, CA*
Frank Op't Eynde, *Audax Technologies, Leuven, Belgium*
Behzad Razavi, *Uiversity of California, Los Angeles, CA*
Bogdan Staszewski, *Technical University of Delft, Delft, The Netherlands*

Overview

RF design has matured to the point where almost any wireless standard (e.g., GSM, WiFi, Bluetooth, etc.) and/or multiple standards operating in different bands can be integrated onto a single chip in deep submicron CMOS. This course is an in-depth tutorial that discusses many of the challenges facing the designer of a single-chip radio, and their solutions.

The topics addressed in the course range from the system right down to the circuit level, including: system requirements and the demands they place on transceiver circuit specs, the design of RF front-ends with >100dB dynamic range at GHz frequencies, direct conversion architectures, autocalibration methods, sub-systems robust to substrate/supply coupling and crosstalk, fast responding PLL synthesizers with low spurious content, and the latest 'more digital than analog' developments.

This course is aimed at circuit designers who are familiar with the basic terminology of RF and mixed-signal/analog circuits and wish to acquire further depth in RF IC design.

System Requirements of RF Transceivers

This lecture offers a system-level analysis of advanced RF transceivers for wireless and mobile applications. An overview of RF standards is then presented, followed by a detailed discussion of various radio transceiver architectures. Key radio requirements are derived and translated to their corresponding circuit specifications, giving an overview of a practical top-down radio design. Several non-idealities and limitations of RF-CMOS are discussed, and architectural and calibration techniques that overcome these limitations are described. Finally, advanced topics such as handset calibration, the evolution to broadband, RF diversity, and next generation mobile standards and their requirements are presented.

Instructor: Hooman Darabi was born in Tehran, Iran in 1972. He received the BS and MS degrees in electrical engineering from Sharif University of Technology, Tehran in 1994 and 1996, respectively. He received the Ph.D. degree in electrical engineering from the University of California, Los Angeles, in 1999. He is currently a senior technical director with Broadcom, Irvine, CA. His interests include analog and RF IC design for wireless communications. Dr. Darabi holds over 60 issued, and 80 pending patents with Broadcom, and has published over 40 IEEE peer-reviewed and conference papers.

Front-end Circuit Design for RF Transceivers

This lecture deals with the transistor-level design of RF front-end circuits, including low-noise amplifiers, downconversion and upconversion mixers, VCOs, and PA drivers. The role of each block in the transceiver is described, and design procedures are offered and carried out in a 65-nm CMOS technology. State-of-the-art examples are also presented.

Instructor: Behzad Razavi received the B.S.E.E. degree from Sharif University of Technology, Tehran, Iran, in 1985 and the M.S.E.E. and Ph.D.E.E. degrees from Stanford University, Stanford, CA, in 1988 and 1992, respectively. He was with AT&T Bell Laboratories and Hewlett-Packard Laboratories until 1996. Since 1996, he has been Associate Professor and subsequently Professor of Electrical Engineering at the University of California, Los Angeles. His current research includes wireless transceivers, frequency synthesizers, phase-locking and clock recovery for high-speed data communications, and data converters. Professor Razavi is a Distinguished Lecturer for the Solid-State Circuits Society and an IEEE Fellow.

Implementation of Direct-Conversion Transceivers

The direct-conversion transceiver principle offers the advantages of a high degree of integration, low overall system cost, and low power consumption. However, the principle is difficult to implement due to practical design limitations such as calibration of static and dynamic offset, and I/Q imbalance. In this lecture, the principle and practical implementation of direct conversion receivers and transmitters are described. Different direct-conversion architectures are compared, and strategies for static and dynamic offset removal and autocalibration methods are presented. Special attention is paid to secondary effects such as crosstalk. Design problems are highlighted and explained by means of real design examples.

Instructor: Frank Op't Eynde received the E.E. and the Ph.D. degrees from the Catholic University of Leuven in 1986 and 1990, respectively. From 1990 to 1994 he was design project leader with Alcatel Mietec in Brussels, Belgium. From 1994 until 1997, he was CTO of Mixed Silicon Structures (Roubaix, France) and a member of the board of Misil Design (Rungis, France). From 1997 to 2001, he was Development Manager for xDSL front-ends and for wireless circuits at Alcatel Microelectronics in Brussels, Belgium and was promoted to Corporate R&D Director. In 2002, he co-founded AsicAhead SRL, a Wireless Product Development company based in Bucharest, Romania and in Genk, Belgium. Since 2007, Dr. Op't Eynde has been self-employed. He has approximately 40 publications and thirteen patents in the field of analog and RFIC design.

Recent Advances in RF Synthesis

Frequency synthesizers are an integral part of digital, mixed-signal, and RF systems-on-chip. As CMOS processes continue to scale, raw transistor performance and power consumption improve dramatically, but difficulties arise when implementing traditional phase-locked loop architectures. This lecture first reviews design challenges such as operation from a 1V supply, gate and off-channel leakage, flicker noise, effect of non-linear device characteristics, and poor isolation from digital logic. Next, well-known workarounds to these problems are presented. Finally, new solutions for RF synthesis that are amenable to nanometer-scale technologies are described.

Instructor: R. Bogdan Staszewski received his B.S.E.E. (summa cum laude), M.S.E.E. and Ph.D. degrees from the University of Texas at Dallas in 1991, 1992 and 2002, respectively. He joined Texas Instruments in Dallas in 1995. In 1999, he co-started the Digital RF Processor (DRPTM) group at TI with a mission to invent digitally intensive approaches to traditional RF functions. Since July 2009, he has been an Associate Professor at Delft University of Technology in the Netherlands. He has co-authored one book, two book chapters, 110 journal and conference publications, and holds 60 issued and 40 pending US patents. Professor Staszewski is an IEEE Fellow.

F3: Towards Personalized Medicine and Monitoring for Healthy Living

Organizer: **Christian Enz,** *CSEM, Neuchâtel, Switzerland*
Co-Organizer: **Andreia Cathelin,** *ST Microelectonics, Crolles, France*

Committee: **Maysam Ghovanloo,** *Georgia Institute of Technology, Atlanta, GA*
Stefan Heinen, *RWTH Aachen University, Aachen, Germany*
Minkyu Je, *Institute of Microelectronics, A*STAR, Singapore*
David Scott, *TSMC, Plano, TX*

The ever-increasing cost of healthcare and the the aging of the population are driving the development of diagnostic tests and drug-delivery systems that determine an individual's therapeutic responsiveness and enable a more efficient therapy, saving healthcare dollars and giving patients better choices. Targeted personalized medicine represents a huge market (estimated at about $232 billion for the US only today) with an annual growth rate of 11% in the coming years. One of the many challenges ahead for this to happen, besides the regulatory, and, new business models that need to be developed, is the development of new technologies that enable the production and realization of the devices required for truly personalized medicine.

This forum will give the opportunity for engineers to better understand the technical issues and challenges faced when designing devices for personalized medicine. It is organized in 3 parts: the first part is focused on the basic components required for sensing and drug delivery. In particular, we will be looking at the basic sensing principles of bio-molecules, the related electronics interface and the miniaturized drug delivery systems using MEMS. The second part is dedicated to health monitoring systems with a particular emphasis on the aspects of wireless communications. Finally, the third part is more focused on cell-inspired electronics and will give some perspectives on the future of personalized medicine.

Forum Agenda

Time	Topic
8:00	Breakfast
8:20	**Introduction** **Christian Enz,** *CSEM, Neuchâtel, Switzerland*
8:30	**Bio-Sensing on Chip** **Carlotta Guiducci,** *EPFL, Lausanne, Switzerland*
9:15	**Electronic Sensing of DNA: CMOS-Based Active Microarrays and Single-Molecule Levels of Detection** **Ken Shepard,** *Columbia University, New York, NY*
10:00	Break
10:15	**Engineering Pain Relief: Microsystems for Intrathecal Drug Delivery** **Yogesh Gianchandani,** *University of Michigan, Ann Arbor, MI*
11:00	**Wearable Body Area Networks: Towards Preemptive and Proactive Healthcare Applications** **Jerald Yoo,** *Masdar Institute of Science and Technology, Abu Dhabi, United Arab Emirates*
11:45	**Miniaturized Wireless CMOS Drug Delivery SoC** **Shey-Shi Lu,** *National Taiwan University, Taipei, Taiwan*
12:30	Lunch
1:30	**Power and Data Telemetry for Implantable Biomimetic Systems** **Wentai Liu,** *University of California, Santa Cruz, CA*
2:15	**Bionic Ear: Hearing Health Care Rehabilitation in the 21st Century** **Stefan Launer,** *Phonak/Sonova, Staefa, Switzerland*
3:00	Break
3:15	**Ultra Low Power Biomedical and Bio-inspired Systems** **Rahul Sarpeshkar,** *MIT, Cambridge, MA*
4:00	**Towards Disposable Healthcare – a Paradigm Shift** **Chris Toumazou,** *Imperial College, London, UK*
4:45	Conclusion

F4: Design of *"Green"* High-Performance Processor Circuits

Organizer: **Tobias Noll,** *RWTH Aachen University, Aachen,Germany*
Co-Organizer: **Raney Southerland,** *ARM, Austin, TX*

Committee: **Sonia Leon,** *Intel, Santa Clara, CA*
Vladimir Stojanovic, *MIT, Cambridge, MA*
Lew Chua-Eoan, *Qualcomm, San Diego, CA*
Alice Wang, *Texas Instruments, Dallas, TX*
Byeong-Gyu Nam, *Samsung Electronics, Yongin, Korea*
Masaya Sumita, *Panasonic, Osaka, Japan*

Energy efficiency is one of the most important design criteria of high-performance processors for practically every application. Whether the chip is a 100W general-purpose processor or a 1W application specific SoC, or whether it is a single- or multi-core architecture, the best practice design techniques applied to maximize performance while minimizing power consumption are essentially the same. . Design targets become more and more challenging with every new technology generation, which shows with increasing variability how to keep energy efficiency high in every mode of operation, i.e. sleep, standby, regular, and peak performance. General techniques being applied here are: gating, adaptivity, and calibration. Finally, in the future, truly successful improvements in energy efficiency will require transitioning from the classical "energy vs. flexibility" trade-off to a new "energy vs. reliability" trade-off due to the increasing rate of transient faults.

The objective of this Forum is to present a comprehensive overview of energy-efficient optimization methodologies for different kinds of processors (general-purpose/application-specific/embedded SoC, single-/multi-core) and to give exemplary examples. While power optimization generally has to be performed at every design level and in all architectural components, including memories, this Forum focuses on microarchitecture, logic and circuits down to the physical implementation level as well as state-of-the-art clocking and supply techniques. The Forum concludes with an outlook on future options, developments, challenges and issures, and possible way-outs will be discussed.

Forum Agenda

Time	Topic
8:00	Breakfast
8:20	**Introduction** **Vladimir Stojanovic,** *MIT, Cambridge, MA*
8:30	**Microarchitectural Features for a Low-Power Multiprocessor System** **Matthias Knoth,** *MIPS, Sunnyvale, CA*
9:15	**Energy-Efficient Computing** **William Dally,** *NVIDIA, Santa Clara, CA*
10:00	Break
10:15	**Power Management in the Wireless Communications Ecosystem** **Anthony Hill,** *Texas Instruments, Dallas, TX*
11:00	**State Retention and Advanced Power Gating Techniques Applied to SoC Subsystems – Design Approaches and Silicon Evaluation** **David Flynn,** *ARM, Cambridge, United Kingdom*
11:45	**An H.264 Full-HD Application Processor with 10GB/s x512b Stacked DRAM and a Power Management System with Multiple Power Domains** **Masafumi Takahashi,** *Toshiba, Kawasaki, Japan*
12:30	Lunch
1:30	**Design and Process Optimization for Complex SoCs** **Ronald Preston,** *Intel, Austin, TX*
2:15	**Near-Threshold Computing: Trade-Offs in Energy Efficiency, Reliability and Adaptivity** **David Blaauw,** *University of Michigan, Ann Arbor, MI*
3:00	Break
3:15	**A 1TFLOPS 100mW Processor** **Sung Bae Park,** *Samsung Electronics, Yongin, Korea*
4:00	Panel Discussion
5:00	Conclusion

F5: Image Sensors for 3D Capture

Organizer: **Johannes Solhusvik,** *Aptina Imaging, Oslo, Norway*

Co-Organizer/Chair: **Albert Theuwissen,** *Harvest Imaging, Bree, Belgium and Delft University of Technology, Delft, The Netherlands*

Committee: **Sam Kavusi,** *Bosch, Palo Alto, CA*
Tetsuo Nomoto, *Sony, Kanagawa, Japan*
Iliana Chen, *Analog Devices, Somerset, NJ*

Low-cost 3D image capture is a popular R&D topic these days, driven by a rapid growth in 3D viewing applications such as gaming and 3D movies. This forum commences with an overview of 3D display technologies and applications. It is followed by a 3D capture technology overview, how each method compares in performance, and its key design challenges to be successful in cost-driven consumer and industrial applications. World experts on image-sensor design will present pixel architectures, devices, circuits and technologies used to build 3D imager chips. Time-of-flight, stereo vision, structured light and multi-aperture imaging will be covered. The forum concludes with a panel discussion providing the opportunity for participants to give feedback and ask questions. The forum is aimed at circuit designers and engineers working in the imaging industry.

Forum Agenda

Time	Topic
8:00	Breakfast
8:30	**Introduction** **Albert Theuwissen,** *Harvest Imaging, Bree, Belgium and Delft University of Technology, Delft, The Netherlands*
8:35	**3D Display Technologies and Applications** **Ian Underwood,** *University of Edinburgh, Edinburgh, Scotland*
9:15	**Review of Optical 3D Ranging Techniques and Key Design Challenges for Required Image Sensors** **Peter Seitz,** *CSEM, Landquart, Switzerland*
9:55	**3D Time-Of-Flight Image Capture with Pulsed Illumination** **Pierre Magnan,** *ISAE, Toulouse, France*
10:35	Break
10:50	**3D TOF Image Capture with Drift Field Pixel Structures** **Bernhard Buettgen,** *MESA Imaging, Zurich, Switzerland*
11:30	**3D Time-Of-Flight Image Capture Based on SPADs** **Edoardo Charbon,** *Delft University of Technology, Delft, The Netherlands*
12:10	Lunch
13:10	**High-Speed 3D Image Capture Using 1D Structured Light** **Shingo Mandai,** *University of Tokyo, Tokyo, Japan*
13:50	**Single-Chip Stereo Vision Cameras** **Ralph Etienne-Cummings,** *Johns Hopkins University, Baltimore, MD*
14:30	**Multi-Aperture Image Sensor for 3D Capture,** **Keith Fife,** *Ubixum, Palo Alto, CA*
15:10	Break
15:30	**Arrays of Angle-Sensitive Pixels in Standard CMOS for 3D Light-Field Capture** **Alyosha Molnar,** *Cornell Univ, USA*
16:10	Panel Discussion
17:00	Closing Remarks

F6: High-Speed Transceivers: Standards, Challenges, and Future

Organizer: **Ali Sheikholeslami,** *University of Toronto, Toronto, Canada*

Committee: **Franz Dielacher,** *Infineon Technologies, Austria*
Miki Moyal, *Intel, Haifa, Israel*
Jafar Savoj, *Xilinx, San Jose, CA*
John Stonick, *Synopsys, Hillsboro, OR*
Takuji Yamamoto, *Fujitsu Laboratories, Kawasaki, Japan*

The goal of this forum is to present the implementation challenges in developing standards-based high-speed transceivers, such as those for USB3, PCIe, SATA, and Ethernet. The forum opens with two presentations on fundamental transceiver design challenges. The third presentation focuses on the challenges of a multistandard PHY supporting Ethernet/PCIe/SATA/USB. Next, a 10Gbase-KR Ethernet PHY will be presented.

The fifth speaker discusses the challenges faced by IP providers arising from the need to proliferate designs across many process geometries and foundries. The final two presentations will focus on transceiver design techniques for increased energy efficiency. The forum concludes with a panel discussion.

Forum Agenda

Time	Topic
8:00	Breakfast
8:20	**Introduction** **Ali Sheikholeslami,** *University of Toronto, Toronto, Canada*
8:30	**Overview of High-Speed Transceiver Techniques and Their Challenges** **Jared Zerbe,** *Rambus, Los Altos, CA*
9:20	**Design Challenges, Latest Achievements and Future Directions of High-Speed I/Os** **Thomas Toifl,** *IBM Research, Zurich, Switzerland*
10:10	Break
10:35	**Ethernet/PCIe/SATA/USB PHY Implementation Challenges and Tradeoffs** **Marcus van Ierssel,** *Snowbush-Gennum, Toronto, Canada*
11:25	**Ethernet Standards and Their Implementation Challenges** **Takeshi Horie,** *Fujitsu Laboratories, Kawasaki, Japan*
12:15	Lunch
1:20	**Standards and Their IP Perspectives** **Daniel Weinlader,** *Synopsys, Allentown, PA*
2:10	**Energy-Efficiency Considerations for High-Speed Transceivers** **Fulvio Spagna,** *Intel, CA*
3:00	Break
3:20	**How Can Standards Provide Low Power Solutions for SoC?** **Anthony Fraser Sanders,** *Lantiq Deutschland, Neubiberg, Germany*
4:10	Panel Discussion
5:00	Conclusion

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Online: This is the fastest, most convenient way to register and will give you immediate email confirmation of your events. To register online (which requires a credit card), go to the ISSCC website at www.isscc.org and select the link to the registration website.

FAX or mail: Use the "2011 IEEE ISSCC Registration Form" which can be downloaded from the registration website. All payments must be made in U.S. Dollars, by credit card or check. Checks must be made payable to "ISSCC 2011". It will take several days before you receive email confirmation when you register using the form. **Registration forms received without full payment will not be processed until payment is received at YesEvents.** Please read the descriptions and instructions on the back of the form carefully.

Onsite: The Onsite Registration and Advance Registration Pickup Desks at ISSCC 2011 will be located in the Yerba Buena Ballroom Foyer at the San Francisco Marriott Marquis. All participants, except as noted below, should register or pick up their registration materials at these desks as soon as possible. **Pre-registered Presenting Authors and all pre-registered members of the ISSCC Program and Executive Committees must go to the Nob Hill Room, Ballroom level, to collect their conference materials.**

REGISTRATION DESK HOURS:

Saturday,	February 19	4:00 pm to 7:00 pm
Sunday,	February 20	6:30 am to 8:00 pm
Monday,	February 21	6:30 am to 3:00 pm
Tuesday,	February 22	8:00 am to 3:00 pm
Wednesday,	February 23	8:00 am to 3:00 pm
Thursday,	February 24	7:00 am to 1:00 pm

Students must present their Student ID at the Registration Desk to receive the student rates. Those registering at the IEEE Member rate must provide their IEEE Membership number.

Deadlines: The deadline for registering at the Early Registration rates is 11:59 pm Pacific Time **Friday January 14, 2011.** After January 14th, and on or before 11:59 pm Pacific Time Sunday January 30, 2011, registrations will be processed **at the Late Registration rates. After January 30th, you must register onsite at the Onsite rates.** You are urged to register early to obtain the lowest rates and ensure your participation in all aspects of ISSCC 2011.

Cancellations/Adjustments/Substitutions: Prior to 11:59 pm Pacific Time **Sunday January 30th, 2011,** conference registration can be cancelled. Fees paid will be refunded (less a processing fee of $75). Registration category or credit card used can also be changed (for a processing fee of $35). Send an email to the registration contractor at ISSCCinfo@yesevents.com to cancel or make other adjustments. **No refunds will be made after 11:59 pm Pacific Time January 30th, 2011.** Paid registrants who do not attend the conference will be sent all relevant conference materials. Transfer of registration to someone else is allowed with **WRITTEN** permission from the original registrant.

Membership saves you on ISSCC registration

Take advantage of reduced ISSCC registration fees by using your IEEE membership number. If you're an IEEE member and have forgotten your member number, simply phone IEEE at 1(800) 678-4333 and ask. IEEE membership staff will take about 2 minutes to look up your number for you. If you come to register onsite without your membership card, you can phone IEEE then, too. Or you can request a membership number look-up by email. Use the online form at: www.ieee.org/web/aboutus/help/member_technical.html

If you're not an IEEE member, consider joining before you register to save on your fees. Join online at www.ieee.org/join at any time and you'll receive your member number by email. If you join at the conference, you can also select a free Society membership. This offer is not available to existing IEEE members.

Upgrade your IEEE membership to Solid-State Circuits Society membership for $28. Free tutorials and short courses online are some of the new programs available to SSCS members in 2011. Students are eligible for new conference travel grants with SSCS membership and an application. Add Society membership at www.sscs.org/join or use the onsite membership registration desk at the hotel to renew or join.

ITEMS INCLUDED IN REGISTRATION

Technical Sessions: Registration includes admission to all technical and evening sessions starting Sunday evening and continuing throughout Monday, Tuesday and Wednesday.
Technical Book Display: A number of technical publishers will have collections of professional books and textbooks for sale during the Conference. The Book Display will be open on Monday from Noon to 8:00 pm; on Tuesday from 10:00 am to 8:00 pm; and on Wednesday from 10:00 am to 3:00 pm.
Poster Session: The recent ISSCC/DAC student contest winners will display their work in poster form. These students will be available to discuss their posters during the Social Hour on Monday evening.
Demo Session: Hardware demonstrations will support selected papers during the Social Hour on Tuesday evening.
Author Interviews: Author Interviews will be held in the Atrium of the hotel, located one level above the lobby, on Monday and Tuesday and Wednesday.
Social Hour: Social Hour refreshments will be available starting at 5:15 pm on Monday and Tuesday in both the Book Display and Author Interview areas.
University Events: Several universities are planning social events during the Conference. Check the University Events display at the conference for the list of universities, locations and times of these events.
ISSCC logo case: A convenient soft briefcase will be provided to all conference registrants to carry their conference materials.

Publications:
Full conference registration includes:
-The **Digest of Technical Papers** in both hard copy and on CD (available onsite beginning on Sunday at 4:00 pm, and during registration hours on Monday through Wednesday).
-The **ISSCC 2011 Conference DVD** that includes the Digest and Visuals Supplement (to be mailed in April). **Student registration does not include the ISSCC 2011 Conference DVD, however it is available for purchase at a reduced fee for students.**

OPTIONAL EVENTS

Educational Events: Many educational events are available at ISSCC 2011 for an additional fee. There are nine 90-minute Tutorials and two all-day Forums on Sunday. There are four additional all-day Forums on Thursday as well as an all-day Short Course. All events include a course handout in color. The all-day events also include breakfast, lunch and break refreshments. See the schedule for details of the topics and times.
Women's Networking Reception: ISSCC will be sponsoring a networking event for women in solid-state circuits on **Monday evening**. It is an opportunity to get to know other women in the profession and discuss a range of topics including leadership, work-life balance, and professional development. By registering and paying a nominal fee for this event, you will receive a ticket to the reception, a chance to build new friendships, and an opportunity to expand your professional network. Please indicate on your ISSCC registration form if you plan to attend this special event, open to women only.

OPTIONAL PUBLICATIONS

ISSCC 2011 Publications: The following ISSCC 2011 publications can be purchased in advance or onsite:
Additional copies of the **Digest of Technical Papers** in book or CD format.
Additional copies of the **ISSCC 2011 Conference DVD (mailed in April).**
ISSCC 2011 Conference DVD at the special student price **(mailed in April).**
2011 Tutorials DVD: All of the 90 minute Tutorials **(mailed in May).**
2011 Short Course DVD: "**Cellular and Wireless LAN Transceivers: from Systems to Circuit Design**" **(mailed in May)**.
Short Course and Tutorial DVDs contain audio and written English transcripts synchronized with the presentation visuals. In addition, the Short Course DVDs contain a pdf file of the presentations suitable for printing, and pdf files of key reference material.
Earlier ISSCC Publications: Selected publications from earlier conferences can be purchased. There are several ways to purchase this material:
-Items listed on the registration form can be purchased with registration and picked up onsite at the conference or mailed to you when available.

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-Visit the ISSCC Publications Desk. This desk is located in the registration area and has the same hours as conference registration. With payment by cash, check or credit card, you can pick up (or order for future delivery) materials at this desk. Tutorial and Short Course DVDs from prior conferences are available. See the order form for titles and prices.
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HOW TO MAKE HOTEL RESERVATIONS

TO ALL ATTENDEES WHO NEED A HOTEL ROOM: We are offering this year a $100 Marriott rebate coupon! If you register for ISSCC 2011 and spend at least three nights at the San Francisco Marriott Marquis, a credit of $100 will be applied to your hotel bill. Enjoy the convenience of staying at the Conference hotel AND save money too! See the hotel reservations site for details.

Online: ISSCC participants are urged to make their hotel reservations at the San Francisco Marriott Marquis online. Go to the conference website at www.isscc.org and click on the Hotel Reservation link to the San Francisco Marriott Marquis. **Conference room rates are $213 for a single/double, $233 for a triple and $253 for a quad** (per night plus tax). In addition, we have negotiated that ISSCC attendees staying at the Marriott Marquis receive **in-room Internet access for free**. All online reservations require the use of a credit card. Online reservations are confirmed immediately. You should print the page containing your confirmation number and reservation details and bring it with you when you travel to ISSCC.
Telephone: Call 888-575-8934 (US) or 415-896-1600 and ask for "Reservations." When making your reservation, identify the group as ISSCC 2011 to get the group rate.
Changes: Once confirmed, your reservation can be changed online or by calling the Marriott Marquis at 415-896-1600 (ask for "Reservations"); or by faxing your change to the Marriott Marquis at 415-486-8153. Have your hotel confirmation number ready.
Hotel Deadline: Reservations must be received at the San Francisco Marriott Marquis no later than January 25, 2011 to obtain the special ISSCC rates. A limited number of rooms are available at these rates. **Once this limit is reached or after January 30th, the group rates will no longer be available and reservation requests will be filled at the best available rate.**

REFERENCE INFORMATION

TAKING PICTURES, VIDEOS OR AUDIO RECORDINGS DURING ANY OF THE SESSIONS IS NOT PERMITTED

Conference Website:	www.isscc.org	
ISSCC Email:	ISSCC@ieee.org	
Hotel Information:	San Francisco Marriott Marquis 55 Fourth Street San Francisco, CA 94103	Phone: 415-896-1600
Press Information:	Kenneth C. Smith University of Toronto Email: lcfujino@cs.com	Phone: 416-418-3034 Fax: 416-971-2286
Registration:	YesEvents P.O. Box 32862 Baltimore, MD 21282 Email: issccinfo@yesevents.com	Phone: 410-559-2200 or 800-937-8728 Fax: 410-559-2217

Hotel Transportation: Visit the ISSCC website "Attendees" page for helpful travel links and to download a document with directions and pictures of how to get from the San Francisco Airport (SFO) to the Marriott Marquis. You can get a map and driving directions from the hotel website at www.marriott.com/hotels/travel/sfodt-san-francisco-marriott-marquis/

Next ISSCC Dates and Location: ISSCC 2012 will be held on February 19-23, 2012 at the San Francisco Marriott Marquis Hotel.

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ISSCC 2011 ADVANCE PROGRAM

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