INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS • UNIVERSITY OF PENNSYLVANIA •

ISSCC®

2010

PRESS KIT

ISSCC PRESS KIT DISCLAIMER

The material presented here is preliminary.
As of November 1, 2009, there is not enough information to guarantee its correctness.
Thus, it must be used with some caution.

ISSCC VISION STATEMENT

The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and use to maintain technical currency, and to network with leading experts.

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ISSCC 2010
Conference Overview

CONFERENCE THEME

SENSING THE FUTURE

The ISSCC 2010 Conference theme is:

"Sensing the Future"

Magnetic, mechanical, chemical, light, temperature, bio and many other sensors are becoming a natural part of the semiconductor business. Sensors already play a key role in electronics for medical and life sciences. Now, sensors are becoming an integral part of digital systems which measure operating conditions and cope with device variability. In the near future, silicon sensors will be everywhere, not only within electronic products and gadgets, but even inside the human body! Contributions are encouraged from researchers and designers demonstrating novel sensing circuit applications and systems, or circuit and system design in subject areas including, but not limited to the following: digital and analog circuits, memory, imagers, wireless, and wireline communication circuits.

EVENTS

TUTORIALS (SUNDAY, FEBRUARY 7, 2010)

- **9** 90-minute Tutorials, each taught twice, by circuit experts from the International Technical Program Committee, serve to meet attendees` needs for introductory material in circuit specialties.

FORUMS (SUNDAY, FEBRUARY 7, 2010)

- Circuit experts exchange information on their current research in an all-day informal environment.

SPECIAL-TOPIC EVENING SESSIONS (SUNDAY – TUESDAY, FEBRUARY 7-9, 2010)

- **5** Special-topic presentations, in which experts provide insight and background on a subject of current importance.
- **Student Research Preview** – short student presentations of work-in-progress at Universities around the world.

EVENING PANELS (MONDAY – TUESDAY, FEBRUARY 8-9, 2010)

- **2** Panels in which industrial and academic experts debate a selected topic and field audience questions in a semi-formal atmosphere.

TECHNICAL SESSIONS (MONDAY – WEDNESDAY, FEBRUARY 8-10, 2010)

- **4 invited talks** presented in the Plenary Session.
- **210 technical papers** presented in **25** Regular Sessions, highlighting the latest circuit developments.

SOCIAL HOURS (MONDAY – TUESDAY, FEBRUARY 8-9, 2010)

- Network with experts in a wide range of circuit specialties; meet colleagues in an informal exchange; browse the technical-book exhibits!

SHORT COURSE (THURSDAY, FEBRUARY 11, 2010)

- Intensive all-day course on a single topic, taught by world-class instructors, can serve to “jump start” a change in an engineer’s circuit specialty.

FORUMS (THURSDAY, FEBRUARY 11, 2010)

- Circuit experts exchange information on their current research in an all-day informal environment.

PAPER STATISTICS

OVERALL:

- **4** papers invited
- **638** papers submitted to ISSCC 2010
- **210** papers accepted
  - **85** papers from North America, including
    - **42** Industry papers
    - **43** University papers
  - **66** papers from the Far East, including
    - **38** Industry papers
    - **28** University papers
  - **59** papers from Europe, including
    - **28** Industry papers
    - **31** University papers
- **27** Sessions, over 3 days

INTERNATIONAL SCOPE:

	2010	2009	2008	2007
Americas:	41 %	38 %	43 %	39 %
Far East:	31 %	35 %	28 %	31 %
Europe:	28 %	27 %	29 %	30%

WIDE COVERAGE:

	2010	2009	2008	2007
Analog:	9 %	11 %	9 %	7 %
Data Converters:	7 %	7 %	10 %	7 %
High-Performance Digital:	10%	4 %	7 %	13%
Imagers, MEMs, Medical, and Displays:	12 %	12 %	11 %	12%
Low-Power Digital:	6 %	6 %	5 %	4%
Memory:	11 %	9 %	12 %	8%
PLL:	6 %	--	--	--
RF:	8 %	11 %	11 %	10%
Technology Directions:	12 %	13 %	12 %	12%
Wireless:	11 %	13 %	11 %	12%
Wireline:	8 %	14 %	11 %	13%

PLENARY SESSION

Paper 1.1:
MEMS for Automotive and Consumer Applications
Jiri Marek, *Senior Vice President, Robert Bosch, Reutlingen, Germany*

- MEMS sensors are increasingly more important and even common place.
- MEMS-assisted electronic systems are making system reactions to human needs more intelligent, and much faster than unaided humans can provide.
- MEMS success has been based on their reducing size, reducing power and reducing cost.
- MEMS development, thus far, has relied on surface micromachining whose development was the breakthrough required for this advance.
- MEMS success relied as well on innovative ASIC design, simulation of electrical and mechanical behaviour, and deep understanding of package and structure over temperature and lifetime.
- Bosh has evolved these capabilities over 20 years and over 1 billion sensors.
- Earliest MEMS successes were in airbag control and gyroscopes for vehicle-dynamics control.
- Now, consumer applications abound: switching the cell-phone from portrait to landscape as the phone orientation changes, avoiding disk damage as the laptop falls, identifying vehicle vertical location in parking and multi-level highway structures through pressure sensing, detecting weather trends, measuring personal altitude, monitoring activity in shoes and sportswear, and providing intuitive controls for games and other interfaces.
- This presentation will consider other applications such as inkjet heads and micromirrors, as well as the challenges to be faced by MEMS-creating technologies.
- Bosh product evolution will be described up to current designs for inertial sensors that are critical to so-called "ESP®-systems".
- Arising new applications, such as energy harvesters and micro-fuel-cells will be discussed.

Paper 1.2:
Harnessing Technology to Advance the Next-Generation Mobile User-Experience
Greg Delagi, *Senior Vice President, Texas Instruments, Dallas, TX*

- The mobile handset market is driven by increased bandwidth, increased processing performance, improved screen technology and reducing power consumption.
- Current 3G/4G handsets are multimedia Internet devices, with big screens, HD video, gaming, HD camcorders, controlled by touch screens in a myriad of social, entertainment, and productivity applications.
- The mobile future portends new modes of social interaction.
- Handsets of the future will be smart autonomous lifestyle devices with a multitude of incorporated sensors, applications and display options, all designed to make life easier and more productive!
- Future displays including 3D imaging, virtual interaction and conferencing will make every call feel like you are right there, providing an experience far beyond today's lesser technologies.

- 3D touch screen with image projection and gesturing will support a new era of intuitive mobile-device applications, interaction, and information sharing.
- True mobile companions will require new compelling services and features to function as well as the office or home computer.
- The massive amounts of data needed by the mobile companion will require immense improvements in system performance, including specialized circuits, highly-parallel architectures, and new packaging design.
- A smart-mobile-companion device will seem to be always-on always-aware in a way that is completely seamless and transparent, by automatically determining the best and most appropriate modem link, whether WiFi, LTE, 5G, or mmWave, based on which will optimize performance, battery life, and costs to deliver the best-possible user experience.
- Future systems will require today's modem technologies, along with new man-machine interfaces and body-area-networks.
- Additional energy supply needed by computational requirements necessitates improved energy efficiency, particularly to deliver all-day operation or two-day always-on standby without a recharge.
- Innovations ranging from low-voltage digital and analog circuits, non-volatile memory, and adaptive power management, to energy harvesting, will be needed to extend battery life to a week or more.
- Increased bandwidth, combined with decreased latency, lower power requirements combined with energy scavenging and harvesting, massive multimedia processing power, and new interface technologies will all work together, will revolutionize how we interact with our smart-companions of the future.
- The implementation challenges will be met with strong collaboration in research and development by universities, government agencies, and corporations, with smart mobile-companion devices likely to be a reality within 10 years!

Paper 1.3:
Challenges of Image Sensor Development
Tomoyuki Suzuki, *Senior Vice President, Sony, Atsugi, Kanagawa, Japan*

- The semiconductor industry has been pushed by successes in digitalization and computerization. And now, is further encouraged by successes in networking.
- Image digitalization has been an important part of these successes.
- Currently, and in the future, image sensors have been, and will remain, key elements in these developments.
- Digital cameras were initiated in 1969 by the invention at Bell Laboratories of CCD image sensors, (for which the Nobel Prize was granted in 2009), and extended by them and others through the mid 1970s, leading to the first video cameras in the mid-1980s.
- Still camera use expanded into the 21st century, with high resolution capability increasingly demonstrated, leading in 2005 to an HD digital video camera which was able to record a 1080i high-definition image using CMOS image sensors!
- As CMOS image sensors achieve higher performance and higher speed, the use of CMOS-equipped D-SLR and cell-phone cameras is expanding.
- Over the past 25 years, camera size has decreased by a factor of 500, as a result of pixel miniaturization, with image-sensor photosensitivity improving by ten-fold per decade.

- These advances were brought about by the use of an n-type substrate to reduce pixel size, and to implement electronic-shutter function, as well as, a Tungsten light shield to reduce the smear signal to −100dB for a pixel size of 3.9μm. Such developments led to the 2M pixel digital still camera in 1999.
- Beginning in 1998, high-speed imaging development at Sony emphasizing increased read-out speed through parallelism, led to the 10M pixel CMOS image sensor providing more than 70dB dynamic range with a high-speed read-out of 576M pixels/s.
- This imager which can also be operated with a 16:9 aspect ratio in a 6M pixel mode at 60 frames/s, utilizes column ADCs, and a back-illuminated structure. This design is currently impacting digital still and video cameras, and will dominate the cell-phone market in the future.
- The presentation will include milestones in the development of the CMOS image sensor such as "3D", "4Kx2K", "global shutter", and describe new materials, new structures, and new processes to be employed.

Paper 1.4:
Nanoelectronics in Retrospect, Prospect, and Principle
James Meindl, *Professor, Georgia Institute of Technology, Atlanta, GA*

- The information revolution has been the paramount economic development of the past five decades.
- Principal driver of the information revolution has been silicon microchip technology, which has advanced in productivity by a factor of approximately one billion and in performance by a factor of nearly one million (for microprocessor chips, for example).
- Productivity has advanced, top-down, through directed assembly with scaling to 25nm, and, bottom-up, through self-assembly nanotechnology to 300mm single-crystal silicon ingots.
- While scaling maintains IGFET dynamic power-delay product, gate-tunneling current, subthreshold channel leakage, manufacturing tolerances, interconnect latency with copper size effects, become problematic.
- Solutions include: Increased chip I/O, improved heat removal, and 3D chip stacking.
- For the perceived saturation of the advance of silicon technology early in the 2020s, a new genre of nanoelectronics is needed.
- The leading candidate is graphene, with its ballistic carrier transport, adjustable energy band gap of nanoribbons, amenabiity to both top-down and bottom-up processes, and the potential for 3D monolithic integration. However, graphene still lacks the equivalent of the "transistor" and of the "integrated circuit".

TECHNICAL HIGHLIGHTS

Analog:

- A completely new type of integrated frequency reference uses silicon thermal time constants to achieve excellent accuracy over the full commercial temperature range. An accuracy of ±0.2% is achieved without trimming! **[4.1]**
- New techniques and meticulous implementations are used to drive down offset and noise in CMOS instrumentation amplifiers. Fully integrated chopper amplifiers achieve 2μV offsets with μW power consumption. **[4.2, 4.4]**
- Audio-driver designs operate in class D and class G using nanometer geometries. With 79% efficiency and 100dB SNR achieved, using 45nm CMOS, even nanometer SoC applications can include high-quality speaker-driver functions. **[4.6, 4.7]**
- Analog control is being replaced by digital signal processing in advanced DC/DC power supplies. Clever control techniques enable several outputs to be generated with a single inductor, reducing external component count and cost. **[10.3, 10.5, 10.6]**
- Nanometer technology makes charge pumps viable for delivering significant power levels. A switched-capacitor converter in 32nm CMOS can deliver over half a Watt per mm^2. **[10.8]**

Data Converters:

- Breaking the 100dB linearity barrier at sample rate of more than 100MS/s enables multi-carrier GSM base-stations. **[16.1, 16.2]**
- The first 45nm CMOS high-performance audio ADC achieves 110dB Signal-to-Noise Ratio (SNR) at only 500μW in 0.04mm^2. **[16.7]**
- Unparalleled speed of a new ADC impacts medical devices. Its 12.5MS/s operation with 18-bit resolution, reduces power and complexity for MRI and digital X-ray.**[21.1]**
- A record breaking 40GS/s sample rate is demonstrated in a mainstream 65nm CMOS process. **[21.7]**

High-Performance Digital:

- The next processor generation reaches unprecedented integration levels using devices comprised of just a handful of atoms. Both Intel and AMD present designs that use Hi-κ metal-gate 32nm manufacturing processes that yield 50% greater integration in the same area with the same power, as the previous generation. **[5.1, 5.6]**
- The amount of computational parallelism integrated in the next generation of server processors has been taken to new extremes. SUN has integrated 128 threads per chip, enabling 128 applications to run simultaneously with a whopping 2.4 Tb/s of I/O bandwidth. This leading edge processor is built in 40nm technology, has 16 cores with 8 threads each, and a 6MB L2 cache. **[5.2]**
- New devices are being integrated to enable the continued performance growth of processor designs. IBM presents a high-end processor that uses embebbed DRAM (eDRAM) memory technology which is over 3 times as dense as the conventional SRAM used in other commercial processors. The 567mm^2 45nm chip includes 32MB of integrated memory, 1.2B transistors, and has 8 cores with 4 threads each which will enable the most demanding high-end server applications. **[5.4]**
- As technology shrinks, small transistors having only a few atoms in critical parts, exhibit large variations, necessitating innovative techniques for reliable integration in the billions. This year, at ISSCC, three presentations address innovations

regarding on-die-aging and path-delay monitoring with extremely fine resolution sensing and adaptation capabilities. **[9.7, 9.8, 9.10]**

Imagers, MEMS, Medical and Displays (IMMD):

- Increased lifetime displays are closer to reality! A new stable RGBW AMOLED display with OLED degradation compensation substantially reduces image sticking and increases the useful lifetime of active OLED displays. **[6.3]**
- A signal processor with the lowest-reported power consumption extracts the heart's rhythm with elegant simplicity. This circuit consumes only 30μW, enabling it to run off a small battery for months, constantly monitoring the state of the patient for the diagnosis of chronic illness. **[6.6]**
- Integrated temperature sensors needing no calibration can be used anywhere and everywhere! Quality is not sacrificed with ±0.2ºC 3σ accuracy from −55ºC to 125ºC. **[17.4]**
- A new Aluminum-Nitride-on-silicon resonator is an important step towards integrating high-Q, low-phase-noise reference oscillators on-chip. The associated transimpedance amplifier has a gain >76dB-Ohm across a bandwidth of 2.5GHz, with a figure-of-merit of 2190GHz·Ω/mW, with a 500fF load. **[17.6]**
- Time-of-flight sensor with the smallest pixel enables the first generation of range-finding sensors for gaming applications. Integrated optical sensors and interfaces provides an 80×60 pixel range-finding image sensor with 10×10 μm^2 lock-in pixels. **[22.7]**
- The first backside-illuminated (BSI) CMOS image sensor with 10Mpixel resolution opens new avenues. A BSI sensor with 1/2.3-inch 10.3 Mpixel image using 1.65×1.65μm^2 pixels, operates up to 50 frames per second and achieves a sensitivity of 9890e-/lux·s. **[22.9]**

Low-Power Digital:

- The first functional 4G silicon chips are described enabling high-speed communication for netbooks, smart phones, and the next generation of mobile devices. ETH Zurich with Advanced Circuit Pursuit and CEA-LETI with T. U. Kaiserslautern describe chips that implement 390 Mb/s turbo code decoding, and a multimode software-defined radio capable of 4G, WIMAX, 802.11n, and cognitive radio. **[15.1, 15.3]**
- Low-power processors break through the gigahertz barrier, enabling a new generation of smart phones with never-before-seen capabilities. ARM and Intel describe new embedded processors with over 1GHz operation at power levels under 50 mW, while Qualcomm describes low-power-design techniques used in their 1.4GHz Snapdragon processor. **[15.5, 15.6, 15.7]**
- The first super-HD and 3D-video decoder is presented. This 90nm chip supports video signals with 4096x2160 resolution or multiview video, consuming only 59mW. **[18.3]**
- A massively parallel processor enables advanced intelligent image processing for surveillance cameras and multimedia phones. With 2048 cores, this chip can be applied to object tracking, face/gesture detection, and other computationally intensive image processing problems. **[18.5]**

Memory:

- Highest density of 64Mb STT-MRAM with smallest perpendicular cell of 0.358μm^2 in 65nm CMOS. The 30ns access time is used a clamped reference with a new adequate-reference-based sensing schemes. **[14.2]**
- Highest density of 64Mb CMOx memory in 0.13μm CMOS in a four-layer 0.17μm^2 cross-point-cell array. Using the multi-layer capability, this memory is scalable to 64Gb capacity. **[14.3]**
- Fastest 12ns 4Mb embedded PCM in 90nm CMOS ever reported! Fast read is achieved by using low-voltage MOS in the hierarchical column decoder. **[14.7]**

- Highest density of 1Gb PCM on 45nm CMOS with 1.8V operation features the fastest-ever read/write performance with 266MB/s and 9MB/s read/write throughputs respectively. **[14.8]**
- First 45nm embedded DRAM (eDRAM) as L3 cache in a high-end server-class microprocessor, the POWER7™. Previously, all microprocessors have used SRAM for L3 cache implementations while this design uses eDRAM to reduce area and cost. **[19.1]**
- First use of margin-improvement techniques at 32nm for enhanced low-voltage operation. A new approach called wordline underdrive (WLUD) has been applied in 32nm High-κ Metal-Gate technology to reduce Vcc_{min} by 130mV. **[19.3]**
- Smallest 32nm SRAM bit cell (0.149μm^2) uses an assist technique to improve low-voltage operation. This new technique improves write margins, reducing cell-failure rate by two orders of magnitude in High-κ Metal-Gate 32nm CMOS. **[19.4]**
- Fastest wide-I/O-mobile SDRAM using micro-bumps achieves a 12.8GB/s data rate at 200MHz. **[24.2]**
- Fastest 200MB/s DDR interface on a 32nm 32Gb NAND flash memory. **[24.6]**
- 32nm 32Gb NAND flash memory with adaptive code selection and floating-gate-coupling cancelation. **[24.8]**

Phase-Locked Loops (PLLs):

- A new MEMS-based oscillator provides an accurate reference frequency with wide programmability. A MEMS resonator, combined with a particularly area-efficient CMOS chip forms a programmable crystal-less 1-to-115MHz clock reference. **[13.1]**
- For the first time, high-quality low-noise frequency synthesizers for wireless-infrastructure applications are demonstrated in a fully-integrated fashion. The chips achieve cellular basestation performance using 0.18μm SiGe BiCMOS technology. **[13.4]**
- A new time-to-digital converter achieves the lowest spur-performance in a wideband all-digital PLL. The new design uses dithering to trade off fractional spur power for a slight increase in in-band noise. **[26.1]**
- For the first time, digital PLLs combine TDC with oscillator functions. This is achieved by re-using the digitally-controlled ring oscillator (DCO) as an intrinsically-tuned phase quantizer, eliminating the calibration required with traditional TDCs. **[26.3, 26.6]**

Radio Frequency (RF):

- First 2x2 beamforming transmitter demonstrator in 65nm CMOS offers robust independent vertical and horizontal scanning of a transmit signal in the 60GHz band. **[2.3]**
- First demonstration of autonomous wireless in-flight recording of a live insect. A passive ultra-low- power RFID system in 0.13μm CMOS consumes only 9.2μA, exhibits a range of 3m, and is so small that it can be mounted on a live moth. **[2.8]**
- Sony and Cal Tech team up to develop the longest-distance inter-chip high-speed/low power communication link. Their millimeter-wave interconnect chips demonstrate 11Gb/s data transmission over a distance of 14mm with an energy consumption of 6.4 pJ/bit. **[23.1]**
- UC Davis demonstrates a 60GHz CMOS power amplifier with the highest-reported RF output.. Use of three on-chip 2-way power combiners maximizes output, providing a record 20dBm (100mW) RF output-power level. **[23.7]**

Technology Directions (TD):

- For the first time, analog circuits and data converters are manufactured using only organic, plastic-like materials. Such circuits will allow the integration of sensors and digital circuits on flexible media embodying intelligent electronics. **[7.1, 7.2]**

- User-Customizable Logic Paper (UCLP) enables the development of integrated circuits with a standard ink-jet printer. This new technology will provide programmability for integrated circuits used in large-area electronics such as smart flexible displays, power transmission sheets, and electronic skin for robots. **[7.3]**
- The first prototype of a commercially-viable cost-effective 3D-stacked IC is demonstrated by IMEC. It is based on a new analysis of methodologies for the use of Through-Silicon Vias (TSVs). **[7.8]**
- For the first time, a implantable CMOS System on Chip (SoC) has been designed to provide low-voltage radio waves that gently heat your back to relieve pain. The SoC is fabricated in a 0.35µm CMOS process and for initial experiments is mounted on a PCB that is connected with a flexible coil antenna mounted in the spinal region. **[12.1]**
- The smallest-ever pressure monitoring device promises new developments in ultra-small medical implants. . This device occupies less than one mm^3, consumes 200,000× less energy than state-of-the-art monitors, will enable promising new techniques for monitoring blood pressure and intraocular pressure. **[12.2]**
- Researchers from Harvard University will present the smallest-ever complete nuclear magnetic resonance (NMR) system that makes possible human cancer screening in a low-cost hand-held platform. Their 0.1-kg 'palm' NMR system is 1200× lighter, 1200× smaller, 1400× cheaper, yet 150× more sensitive than a 120-kg state-of-the-art commercial bench-top NMR system. **[27.2]**
- For the first time, a poultice applied to the chest can help prevent heart failure. Electronics in the poultice ensure that ECG patterns, heart rhythms, thoracic impedance variance (TIV), and heart pumping-power, are evaluated and relayed automatically to your cell phone. **[27.3]**

Wireless:

- Highly robust and reliable cellular transceivers for advanced 3G (HSPA) and 2G (E-EDGE) communications are core enablers for the truly mobile internet. These breakthrough solutions demonstrate the feasibility of enhancing user data rates in all market segments and geographical areas. **[3.1, 3.3]**
- The first wireless receiver that connects the ADC directly to the RF provides a major step towards true software-defined radio (SDR). The resulting linearity improvement of up to +4dBm exceeds previous limits over the receiver spectrum at 900MHz,without major impact on sensitivity. **[3.5]**
- The first CMOS 77GHz Long Range Radar satisfying the 100m range standard requirement is demonstrated. The fully-integrated solution includes clock generation and a complete chip-antenna assembly. **[11.2]**
- The first 16-Element Phased-Array Transmitter for 60GHz WHDMI communications is realized in 0.12µm SiGe BiCMOS technology. The solution uses an antenna-array approach to meet the QoS demanded to enable WHDMI. **[11.3]**
- A 51µW always-on wake-up receiver is demonstrated in 90nm CMOS. This solution paves the way for truly autonomous sensor nodes employing energy scavenging to satisfy their power needs. **[11.5]**
- An IR-UWB architecture enabling robustness against narrowband interferers has been realized in 90nm CMOS. The interference-robust asynchronous energy-detector receiver can tolerate interferers of up to -5dBm. **[11.7]**
- The first reported SoC that combines WLAN, Bluetooth, and FM radios on a single chip. The 16.9mm^2 combo radio is implemented in 65nm CMOS technology, and integrates an on-chip PA with linear output power of 21dBm in the 2.4GHz band. **[25.3]**
- Highest level of integration in multi-standard mobile TV SoCs. Implemented in 65nm CMOS technology, the chips utilizes multiple on-chip LNAs to cover different frequency bands of operation while sharing the rest of the receive chain**. [25.6, 25.7]**

Wireline:

- One half trillion bits communicated in one second! Intel presents an extremely "green" transceiver chip with 47 channels operating at 10 Gb/s while consuming only one tenth of the power/bandwidth of any work reported previously. **[8.1]**
- The most effective CMOS wireline receiver equalizer ever published, is presented. This solution is able to recover "almost-completely-evaporated" data, as demonstrated by its ability to compensate for up to 39dB of loss, which is equivalent to receiving only 1.4% of the data energy originally transmitted! **[8.5]**
- Another nail in the coffin of analog transceivers by digital! An ADC-assisted receiver using digital signal processing operates successfully at 6.875Gb/s under challenging conditions. **[8.6]**
- Low-cost optical receivers are finally a reality. A high responsivity production-quality Ge photodiode (PD) is integrated in 0.13μm SOI-CMOS technology. The PD exhibits a sensitivity of 6μA p-p at a BER of 10^{-12}, while consuming a paltry 15mW when operating at 10Gb/s. **[20.1]**
- The fastest single-chip CMOS Opto-Electronic Integrated Circuit (OEIC) receiver ever reported! The OEIC incorporates an 8.5Gb/s receiver with on-chip silicon photodiode for short-distance optical communications. **[20.2]**
- A huge step forward in green electronics is evident with the most efficient fully-featured 10Gb/s-class transceiver ever reported!. The 12.5Gb/s 65nm CMOS transceiver breaks the mythical 1mW per Gb/s efficiency benchmark with a power consumption of only 12.3mW. **[20.5]**

EDUCATIONAL EVENTS

TUTORIALS

T1: Battery Management for Portable Devices
Francisco Rezzi (Marvell)

T2: SoC Integration of RF Front-end Passives
Hooman Darabi (Broadcom Inc.)

T3: Specifying and Testing ADCs: Where Do I Start and How Do I Know When I'm Finished?
Aaron Buchwald (Mobius Semiconductor)

T4: RF CMOS Power Amplifiers and Linearization Techniques
Domine Leenaerts (NXP Semiconductors)

T5: Design of Energy-efficient On-chip Networks
Vladimir Stojanovic (Massachusetts Institute of Technology)

T6: Design of Smart Sensors
Kofi Makinwa (TU Delft)

T7: High-speed Memory Interfaces
Yasuhiro Takai (Elpida Memory)

T8: Power Gating
Stephen Kosonocky (AMD)

T9: PLL Design in Nanometer CMOS
Kumar Lakshmikumar (Conexant Systems)

FORUMS

F1: Silicon 3D Integration Technology and Systems
Pol Marchal (IMEC), Georg Kimmich (ST-Ericsson), Jean-Luc Jaffard (STMicroelectronics), Ho-Ming Tong (ASE Group), Hiroki Ishikuro (Keio University), Flynn Carson (STATS ChipPACK), Uksung Kang (Samsung), Yoshihisa Iwata (Toshiba), Samuel Naffziger (AMD)

F2: Reconfigurable RF and Data Converters
Kenichi Okada (Tokyo Institute of Technology), Yann Deval (University of Bordeaux), Hooman Darabi (Broadcom), Stephane Boudaud (CSR), Harald Pretl (DICE - Infineon), Robert van Veldhoven (NXP Semiconductors), Jan Craninckx (IMEC)

F3: Transceiver Circuits for Optical Communications

Naim Ben-Hamida (Nortel), Norman Swenson (ClariPhy Communications), Hirotaka Tamura (Fujitsu), Chris Cole (Finisar), Afshin Momtaz (Broadcom), Michiel Steyaert (KU Leuven)

F4: High Speed Image Sensor Technologies

Boyd Fowler (Fairchild Imaging), Jan Bosiers (DALSA), Guy Meynants (CMOSIS), Shoji Kawahito (Shizuoka University), Makoto Ikeda (University of Tokyo), Levy Gerzberg (Zoran), Masatoshi Ishikawa (University of Tokyo), Katsu Nakamura (Analog Devices), Jean Dassonville (Agilent Technologies)

F5: Circuits for Portable Medical Electronic Systems

Tim Denison (Medtronic), Bruno Murari (ST Microelectronics), Akira Matsuzawa (Tokyo Institute of Technology), Manish Goel (Texas Instruments), Brian Otis (University of Washington), Refet Firat Yazicioglu (IMEC), Hoi-Jun Yoo (KAIST), Soon Kwan An (Nurobiosys), Julien Penders (Holst Centre / IMEC)

F6: Signal and Power Integrity for SoC's

Ron Ho (Sun Microsystems), Sam Naffziger (AMD), Makoto Nagata (Kobe University), Marcel Pelgrom (NXP Semiconductors), John Bainbridge (Silistix), Stefan Rusu (Intel)

SHORT COURSE

SC1: CMOS Phase-locked Loops for Frequency Synthesis

John Cowles (Analog Devices), Ian Galton (UCSD), Peter Kinget (Columbia University), Behzad Razavi (UCLA)

EVENING SESSIONS

SPECIAL TOPICS

ES1: Beyond CMOS – Emerging Technologies

Thomas H. Lee (Stanford University), Peter Fromherz (Max Planck Institute), Xiaofeng Li (Harvard University), Takayasu Sakurai (University of Tokyo)

ES2: Student Research Preview

Organizers: Jan Van der Spiegel (University of Pennsylvania), SeongHwan Cho (KAIST)

ES3: Energy-efficient High-speed Interfaces

Subodh Bapat (Sun Microsystems), Brian Leibowitz (Rambus), Ian Young (Intel), Tadahiro Kuroda (Keio University)

ES4: Fusion of MEMS and Circuits

Kazuya Masu (Tokyo Institute of Technology), Jim Hall (Texas Instruments), Kazusuke Maenaka (University of Hyogo), Matton Kamon (Coventor), Fabio Pasolini (STMicroelectronics)

ES5: Can RF SoCs (Self)Test Their Own RF?

R. Bogdan Staszewski (Delft University of Technology), Mani Soma (University of Washington), Donald Y.C. Lie (Texas Tech University), Gernot Hueber (Infineon), Srenik Mehta (Atheros Communications)

ES6: Can We Rebuild Them? Bionics Beyond 2010

Gerald Loeb (University of Southern California), Hugh McDermott (University of Melbourne), Albrecht Rothermel (University of Ulm), Daryl R. Kipke (University of Michigan)

PANELS

EP1: Analog Circuits: Stump the Panel

Bob Blauschild (Consultant), Barrie Gilbert (Analog Devices), Akira Matsuzawa (Tokyo Institute of Technology), Bob Pease (Consultant), Willy Sansen (Katholieke Universitat Leuven), Yannis Tsividis (Columbia University)

EP2: The Semiconductor Industry in 2025

William Holt (Intel), Tadahiro Kuroda (Keio University), Pierre-Yves Lesaicherre (NXP Semiconductors), Sreedhar Natarajan (TSMC), Gary Patton (IBM), Walden Rhines (Mentor Graphics), Charles G. Sodini (MIT)

SUBCOMMITTEE CONTRIBUTIONS

SUBCOMMITTEE	SESSIONS	EVENING SESSIONS	EVENING PANELS	TUTORIALS	FORUMS	SHORT COURSES	PRESS COPY PAGE #'S
ANALOG	4, 10		EP1	T1		SC1	120, 133
DATA CONVERTERS	16, 21			T2			140, 145
HIGH-PERFORMANCE DIGITAL	5, 9			T3	F3		121, 122, 123, 124, 132
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LOW-POWER DIGITAL	15, 18	ES4		T8	F5		139, 142
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ANALOG SUBCOMMITTEE

ISSCC 2010 – ANALOG

Subcommittee Chair: *Bill Redman-White, NXP/Southampton University, Southampton, UK*

OVERVIEW

CONTEXT AND PRESENT STATE OF THE ART

- Conventional device physics has limitations in implementing mainstream frequency-control applications. **[4.1]**
- Sensing the physical world demands ever improving analog interfaces with μV offsets and nV noise levels. **[4.2, 4.4]**
- High performance analog interfaces are essential in nanometer SoCs**. [4.6, 4,7]**
- Efficient DC/DC power conversion is difficult when a fast output response is needed in RF polar modulation**. [10.1]**
- Analog controllers are typically used in high-efficiency multiple-output power supplies. **[10.3, 10.5, 10.6]**
- Fully-integrated supplies for SoC block-level power management traditionally used lossy linear regulators**. [10.8]**

MOST-SIGNIFICANT RESULTS

- A completely new type of integrated frequency reference uses silicon thermal time constants to achieve excellent accuracy over the full commercial temperature range. An accuracy of ±0.2% is achieved without trimming! **[4.1]**
- New techniques and meticulous implementations are used to drive down offset and noise in CMOS instrumentation amplifiers. Fully integrated chopper amplifiers achieve 2μV offsets with μW power consumption. **[4.2, 4.4]**
- Audio-driver designs operate in class D and class G using nanometer geometries. With 79% efficiency and 100dB SNR achieved, using 45nm CMOS, even nanometer SoC applications can include high-quality speaker-driver functions. **[4.6, 4.7]**
- Polar modulation requires that the PA power supply provide the modulation, a limiting factor for high bandwidths. New hybrid power supplies raise the bar with high efficiency and fast tracking up to 4MHz. **[10.1]**
- Analog control is being replaced by digital signal processing in advanced DC/DC power supplies. Clever control techniques enable several outputs to be generated with a single inductor, reducing external component count and cost. **[10.3, 10.5, 10.6]**
- Nanometer technology makes charge pumps viable for delivering significant power levels. A switched-capacitor converter in 32nm CMOS can deliver over half a Watt per mm^2. **[10.8]**

APPLICATIONS AND ECONOMIC IMPACT

- Hot news on frequency references – on-chip silicon thermal time-constants make for accurate fully-integrated frequency references with minimal or no trimming, further reducing system costs. **[4.1]**

- Amplifier offsets get the chop – combining the latest design innovations pushes the performance of micropower instrumentation amplifiers. **[4.2, 4.4]**
- Making a noise in SoC – high-efficiency audio-speaker drivers achieve high efficiency in nanometer CMOS, eliminating the cost of external amplifiers in handheld applications. **[4.6, 4.7]**
- Pushing the envelope in power supplies – advanced hybrid power supplies make polar modulation of RF PAs possible at wide bandwidths, boosting efficiency, and extending battery lifetime in mobile radios. **[10.1]**
- Power conversion goes digital – advanced DSP techniques make complex embedded power-management systems feasible with low external-component count, even in nanometer technologies, enabling higher system integration and reduced system costs. **[10.2, 10.3, 10.4, 10.6]**
- Embedded circuit blocks get vital supplies – switched-capacitor power supplies deliver significant currents in nanometer CMOS, making fine control of supply voltages possible in SoC IP blocks**. [10.8]**

Data Converters Subcommittee

ISSCC 2010 – DATA CONVERTERS

Subcommittee Chair: *Venu Gopinathan, Ayusys, Bangalore, India*

OVERVIEW

CONTEXT AND PRESENT STATE OF THE ART

- In multi-carrier GSM base-stations, blocker channels can mix into the signal band of interest ruining signal fidelity. 100dB SFDR is required to achieve the desired performance.**[16.1, 16.2]**
- Consumer mobile-audio applications demand higher performance, longer battery life, and lower cost. In next generation SoCs, 45nm CMOS will enable embedded audio functions. **[16.7]**
- For medical imaging, converters of 18-bit resolution are needed for high image quality. Higher sample rates are the key to reducing system complexity. **[21.1]**
- 100Gb/s optical networks require that four 40 to 56GS/s 6-bit ADCs be available in mainstream state-of-the-art CMOS, to allow integration with the digital parts of the system. **[21.7]**

MOST-SIGNIFICANT RESULTS

- Breaking the 100dB linearity barrier at sample rate of more than 100MS/s enables multi-carrier GSM base-stations. **[16.1, 16.2]**
- The first 45nm CMOS high-performance audio ADC achieves 110dB Signal-to-Noise Ratio (SNR) at only 500µW in 0.04mm^2. **[16.7]**
- Unparalleled speed of a new ADC impacts medical devices. Its 12.5MS/s operation with 18-bit resolution, reduces power and complexity for MRI and digital X-ray.**[21.1]**
- A record breaking 40GS/s sample rate is demonstrated in a mainstream 65nm CMOS process. **[21.7]**

APPLICATIONS AND ECONOMIC IMPACT

- Important advances in ADCs for cellular and mobile base-stations. **[16.1, 16.2]**
- Unusually high-speed high-resolution converters will reduce the cost and complexity of medical-imaging systems. **[21.1]**
- Pushing the speed of successive-approximation converters higher. **[21.1, 21.2, 21.4, 21.7]**
- 40GS/s CMOS ADC will extend 100Gb/s optical communication. **[21.7]**

High-Performance Digital Subcommittee

ISSCC 2010 – HIGH-PERFORMANCE DIGITAL

Subcommittee Chair: *Sam Naffziger, AMD, Fort Collins, CO*

OVERVIEW

CONTEXT AND PRESENT STATE OF THE ART

- Ever-increasing-integration levels are enabled by the seemingly unstoppable continuation of Moore's-law of scaling, as evidenced this year by two 32nm processor designs from Intel and AMD. **[5.1, 5.6]**
- High-performance processors continue to push performance with large multi-core systems-on-a-chip (SoCs) providing, unprecedented bandwidth, energy-efficiency and core counts, all with the goal of delivering more-power-efficient performance to their respective markets. **[5.2, 5.4, 5.7, 7.4]**
- The miniscule devices that enable today's extreme densities are subject to greater manufacturing and operational variation than the comparatively huge transistors of just a few years ago. Ensuring a high yield of reliably operating billion plus transistor chips in advanced technologies is now an area ripe for innovation and research, as evidenced by the large number of publications surrounding embedded sensors and power-management approaches **[9.7, 9.8, 9.10]**.

MOST-SIGNIFICANT RESULTS

- The next processor generation reaches unprecedented integration levels using devices comprised of just a handful of atoms. Both Intel and AMD present designs that use Hi-κ metal-gate 32nm manufacturing processes that yield 50% greater integration in the same area with the same power, as the previous generation. **[5.1, 5.6]**
- The amount of computational parallelism integrated in the next generation of server processors has been taken to new extremes. SUN has integrated 128 threads per chip, enabling 128 applications to run simultaneously with a whopping 2.4 Tb/s of I/O bandwidth. This leading edge processor is built in 40nm technology, has 16 cores with 8 threads each, and a 6MB L2 cache. **[5.2]**
- New devices are being integrated to enable the continued performance growth of processor designs. IBM presents a high-end processor that uses embebbed DRAM (eDRAM) memory technology which is over 3 times as dense as the conventional SRAM used in other commercial processors. The 567mm^2 45nm chip includes 32MB of integrated memory, 1.2B transistors, and has 8 cores with 4 threads each which will enable the most demanding high-end server applications. **[5.4]**
- As technology shrinks, small transistors having only a few atoms in critical parts, exhibit large variations, necessitating innovative techniques for reliable integration in the billions. This year, at ISSCC, three presentations address innovations regarding on-die-aging and path-delay monitoring with extremely fine resolution sensing and adaptation capabilities. **[9.7, 9.8, 9.10]**

APPLICATIONS AND ECONOMIC IMPACT

- The goal of integrating dozens of cores and billions of transistors on a single die is to feed the insatiable need for computation that the world's ever-expanding IT infrastructure demands. The chips presented in the "Processor" session will power the next generation of high-performance systems through increased levels of integration, high-speed I/O, and greater focus on fine-grained power management with multiple clock/power domains, and low-voltage caches. **[5.1, 5.2, 5.4, 5.5]**
- The exploding core counts and heterogeneous integration enabled by billion plus transistor designs has required fast-paced architectural and circuit innovations in on-chip networks, since integrated components need to move data around at a pace that matches their computational ability. These innovations are enabling significant advances in energy efficiency and application throughput for systems with a large number of cores. **[5.2, 5.7]**
- If all of this computation capability is to be delivered as cheaply and reliably, as it has been in the past, all of the variation and manufacturing issues associated with the miniscule dimensions have to be measured and adapted to, using sophisticated new methods. Hence, a great deal of research is being done with the on-chip delay and aging sensors used in adaptive power-management techniques that are becoming regular features in new processors. **[9.1, 9.7]**

TRENDS IN PROCESSORS PRESENTED AT ISSCC

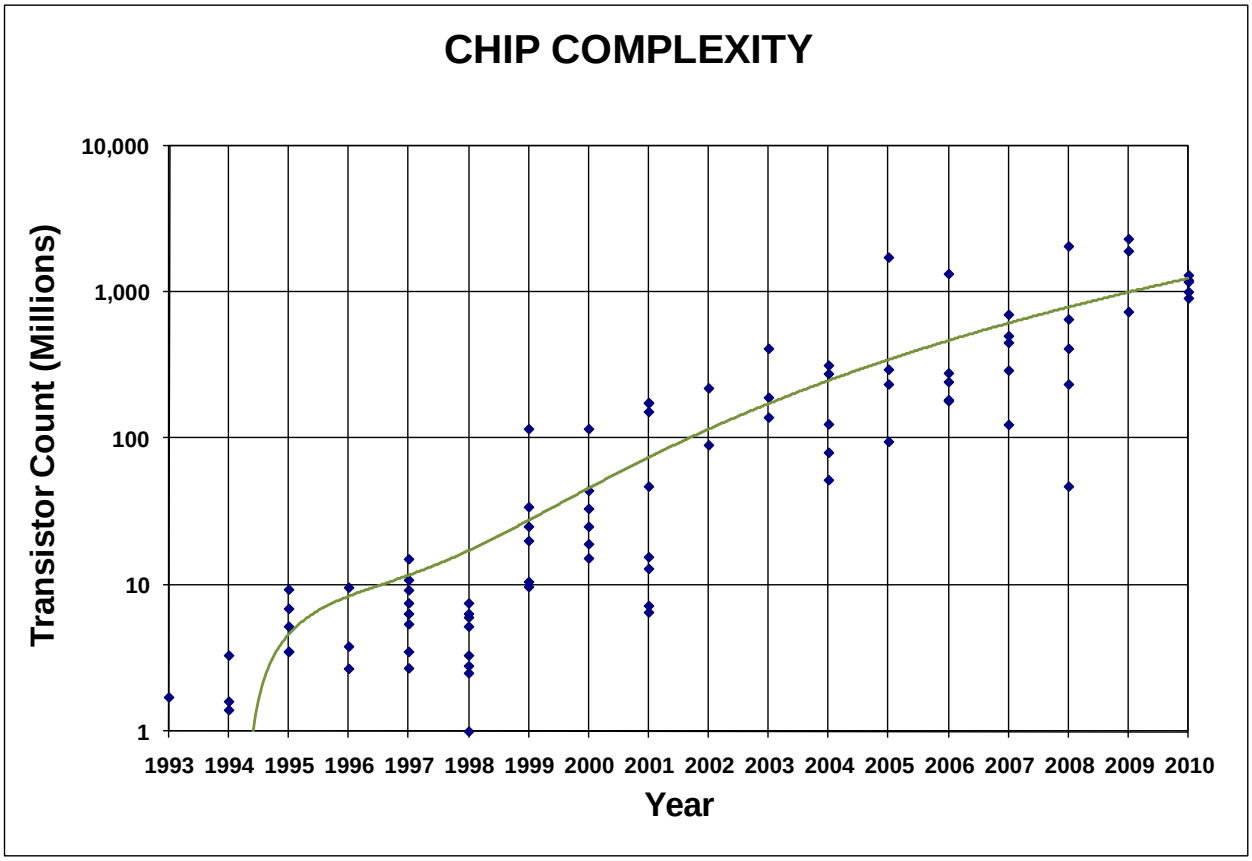
The advances in new materials, device architectures, and processing techniques, have enabled silicon manufacturing technology scaling into the 32 nanometer regime where the transistor channels are comprised of literally just a handful of atoms. The extreme scaled dimensions have enabled massive transistor-integration capacity on commercial silicon chips. The relentless pursuit of performance has driven the utilization of the available transistor capacity and prompted designers to integrate more functions in hardware that push the performance beyond the previously-assumed barriers.

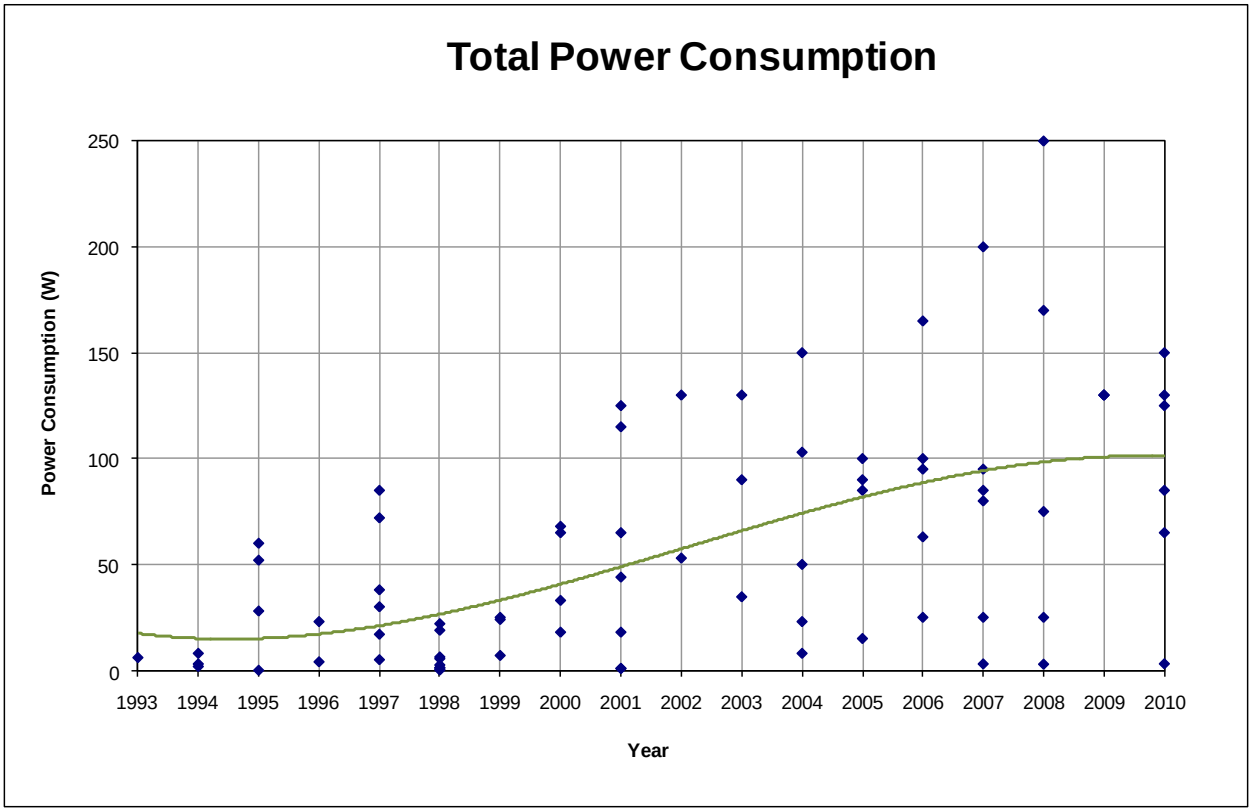
The **chip-complexity chart** shows the trend for the number of transistors integrated in a single silicon chip over the last two decades. Recently, many products have been deployed successfully with more than a billion logic transistors (a staggering four orders of magnitude increase over the earliest microprocessors of the 1980s). At ISSCC 2010, both Intel and AMD will present their latest microprocessors implemented in the leading 32 nanometer technology **[5.1, 5.6]**, while SUN and IBM will show their new generation of large-server-class processors **[5.2, 5.4]**. It should be noted that the massive integration capacity has also enabled very large multi-megabyte on-die caches, exemplified most notably by IBM's whopping 32 megabytes of embedded DRAM cache on a POWER7™ processor chip **[5.4]**.

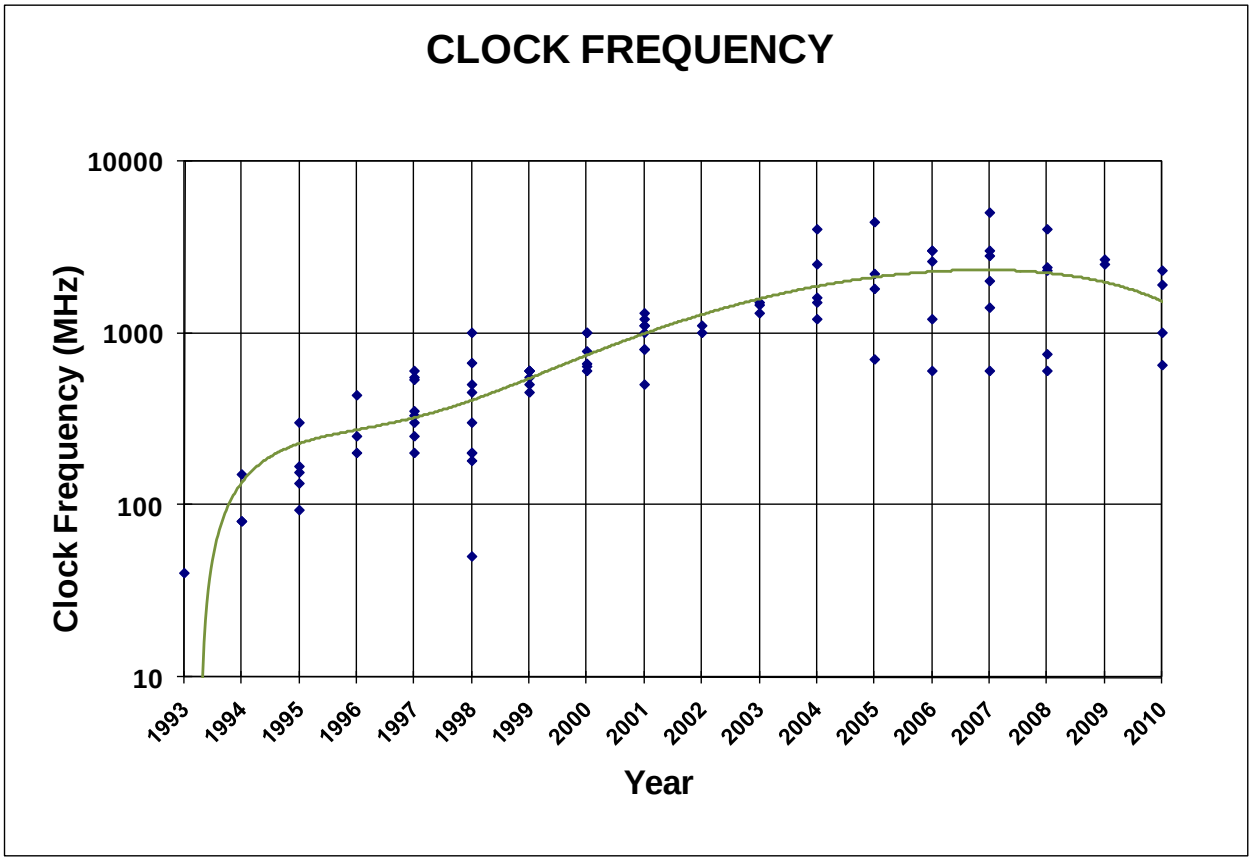
The pursuit of increased hardware-implemented functionality on a single die has hit the well known power wall, a barrier set by power-delivery and thermal limits. This event can easily be seen in the **power trend chart,** where if anything, maximum power consumption is now exhibiting a downward trend driven by the cost burden of the cooling infrastructure. Achieving this power reduction requires innovative heat-removal solutions and sophisticated on-die power management. High-power processors exceeding 200 Watts of power consumption were presented at past ISSCC Conferences; but these are largely relics of the past, as energy efficiency dominates the computer industry.

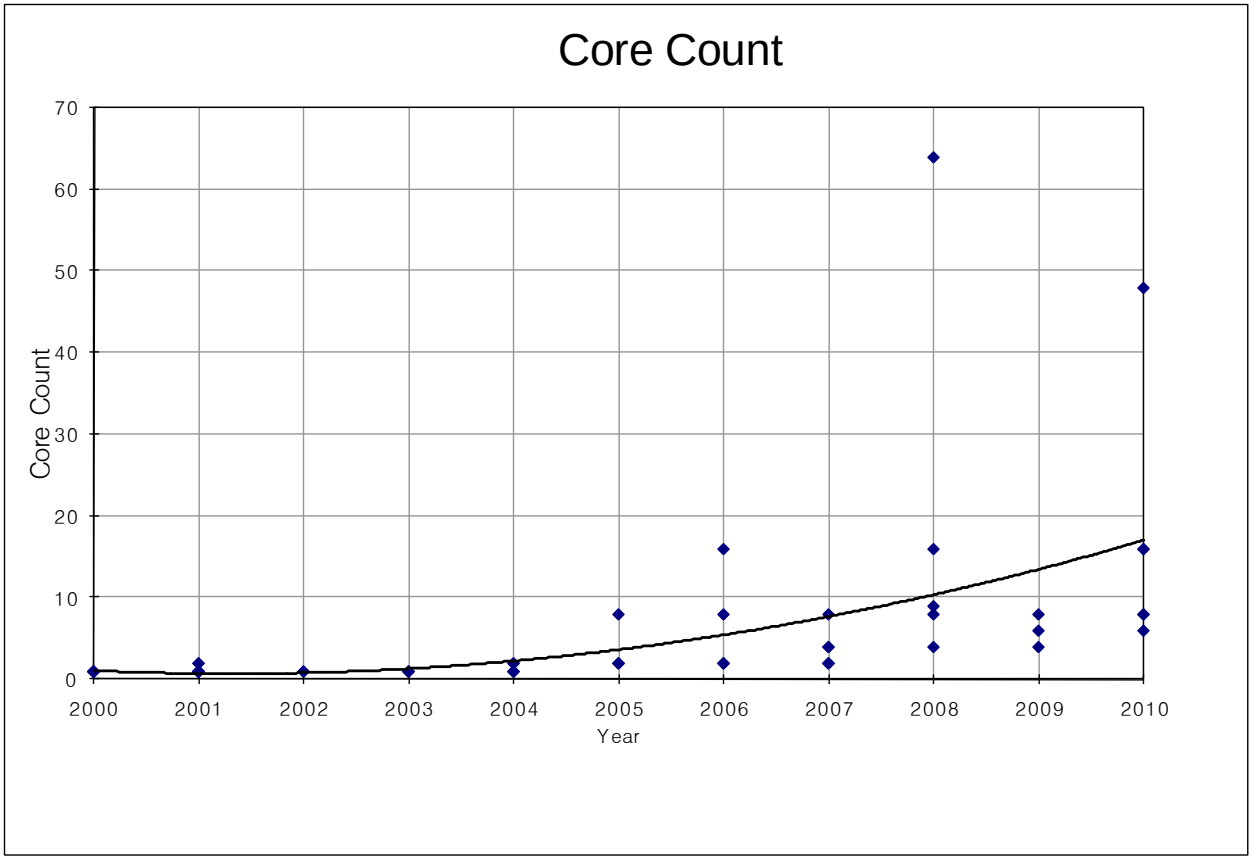
The trend to lowering the power consumption implies constraining the growth of operating frequency to zero or below, as shown in the **frequency chart**. As the usual frequency knob of increased performance is no longer available to architects and designers, the new trend is towards parallelism in the implementation. The best hardware approach to parallelism is to provide parallel execution paths in terms of multiple processor cores on a single chip, or multiple threads running on a single core. At ISSCC 2010, Sun Microsystems will present a 16-core 128-thread server-class processor **[5.2]**, while Intel will present a 48-core research processor **[5.7]**, both of which represent benchmarks in parallelism. This trend of increasing performance through parallelization is well illustrated by the **core count chart** which shows a steady upward trend, and a complete lack this year of single or even dual core processor implementations.

The combination of high transistor counts and low power (resulting in low operating voltages), along with scaled threshold voltages has incited variability and uncertainty in chips' performance and power consumption. Various dynamic variations, such as voltage, temperature, and aging, must be sensed, and the processor adapted to the continuously changing environment. At ISSCC 2010, many interesting papers in the **Digital Circuits & Sensors session** will show how device degradation and delay variations at pico-second resolution can be monitored.









Imagers, MEMS, Medical & Displays Subcommittee

ISSCC 2010 – IMAGERS, MEMS, MEDICAL AND DISPLAY

Subcommittee Chair: *R. Daniel McGrath, Eastman Kodak Co., Rochester, NY*

OVERVIEW

CONTEXT AND PRESENT STATE OF THE ART

- Current display technology degrades over time resulting in short device lifetimes and an abundance of electronic waste. **[6.3]**
- The potential for extensive integration of sensors for medical diagnosis and long-term monitoring is not being utilized. **[6.6]**
- Current temperature sensors are implemented in older CMOS technologies and require very costly trimming operations to establish their accuracy. **[17.4]**
- Typical wireless systems require off-chip crystal oscillators that are expensive and consume precious area on small cell phone circuit boards. **[17.6]**
- The explosion of home gaming has been propelled by the integration of sensors into controllers. Gaming platforms are always searching for better technologies to enable new interface paradigms and more interactive play. **[22.7]**
- Currently, the resolution of mobile-phone cameras suffers from the tradeoffs necessary to satisfy the form factor and cost realities of commodity-electronics design. Further, as pixel size is reduced, front-side illuminated image sensors suffer from reduced sensitivity. **[22.9]**

MOST-SIGNIFICANT RESULTS

- Increased lifetime displays are closer to reality! A new stable RGBW AMOLED display with OLED degradation compensation substantially reduces image sticking and increases the useful lifetime of active OLED displays. **[6.3]**
- A signal processor with the lowest-reported power consumption extracts the heart's rhythm with elegant simplicity. This circuit consumes only 30μW, enabling it to run off a small battery for months, constantly monitoring the state of the patient for the diagnosis of chronic illness. **[6.6]**
- Integrated temperature sensors needing no calibration can be used anywhere and everywhere! Quality is not sacrificed with ±0.2ºC 3σ accuracy from −55ºC to 125ºC. **[17.4]**
- A new Aluminum-Nitride-on-silicon resonator is an important step towards integrating high-Q, low-phase-noise reference oscillators on-chip. The associated transimpedance amplifier has a gain >76dB-Ohm across a bandwidth of 2.5GHz, with a figure-of-merit of 2190GHz·Ω/mW, with a 500fF load. **[17.6]**
- Time-of-flight sensor with the smallest pixel enables the first generation of range-finding sensors for gaming applications. Integrated optical sensors and interfaces provides an 80×60 pixel range-finding image sensor with 10×10 μm^2 lock-in pixels. **[22.7]**

- The first backside-illuminated (BSI) CMOS image sensor with 10Mpixel resolution opens new avenues. A BSI sensor with 1/2.3-inch 10.3 Mpixel image using 1.65×1.65μm^2 pixels, operates up to 50 frames per second and achieves a sensitivity of 9890e-/lux·s. **[22.9]**

APPLICATIONS AND ECONOMIC IMPACT

- As high-resolution displays become ubiquitous, those that last longer with enhanced feature sets will have a "greener" appeal, being more flexibile and durable. **[6.3]**
- Integrated sensors will allow for vastly improved diagnostics and point-of-care health monitoring, enabling new opportunities in the $10B+ USD market. **[6.6, 6.9]**
- Pervasive temperature sensing will enable advanced power management for the next generation of datacenters, and allow smart building-control systems that provide "greener" structures with higher energy efficiencies. **[17.4]**
- Integrating the frequency-reference oscillator on-chip will simplify the next generation of compact low-power mobile-device designs. Eliminating the external crystal oscillator will reduce both the system costs and the form factor of these devices, enabling smaller, lighter, and lower cost cell phones. **[17.6]**
- Range-finding CMOS image sensors will enable a whole new level of interaction in the multi-billion dollar electronic entertainment and video game markets. **[22.7]**
- The next generation of portable multimedia device cameras will require backside illuminated CMOS image sensors to compete in the multi-billion dollar mobile-handset market. **[22.9]**

TRENDS IN SENSORS AND MEMS

- **Cost Reduction and Growth:** The recent advances in design, technology, system integration, packaging of sensors together, and increased product volumes, have dramatically reduced the cost of sensors. Cell phones, game consoles, and other consumer products now integrate several sensors (such as a combination of accelerometers and gyroscopes in a single package), and have spurred-on significant innovation at the application level. The use of multiple sensors, their downscaling in size and the ever higher levels of integration available will lead to further growth in the sensor market.

- **Temperature Sensors:** Temperature sensors have evolved to lower power, lower cost, and elimination of expensive calibration, without sacrificing sensor accuracy. Recent highlights are an ultra-low power sensor with a power consumption of less than 1μW, as well as a device without trimming and an accuracy of better than ±0.2°C over a wide temperature range.

- **MEMS:** Higher frequencies extend the reach of MEMS to new application areas beyond sensors (such as frequency generation and radio tuning).

- **3-D Integration:** 3-D integration of heterogeneous LED and CMOS technologies enables an addressable matrix of high-speed optical sources for biological and medical applications.

TRENDS IN DISPLAYS

- **OLED Displays:** Organic LEDs (OLEDs) represents a revolutionary display technology that promises to displace LCDs. Today it suffers from new-technology teething issues that have consequences such as the degradation of the image quality with use. Traditionally, straightforward solid-state circuits been used to drive conventional displays, but, now, new electronic methods of monitoring and adjusting the signal applied to the OLED can extend the uniformity and lifetime of the display.

- **LCD Backlights:** Ongoing trends for LCDs include the march toward larger, thinner, lower-power, and better quality displays. Structured LED backlights have provided benefits in all of these dimensions. In this technique, solid-state circuits are enabling LED backlight drivers to significantly increase the rate at which LED backlights can operate, and allow extended dynamic range by locally varying brightness. In particular, fast-moving sequences look better on screens that operate at higher frame rates.

- **Mobile Touch Screens:** More and more mobile devices have touch screens. These remove the need for a physical keyboard and allow the display to fill almost the whole size of the device. This allows new simpler user interfaces, and enabling more-natural game play. A new IC combines the display driver and touch-screen controller onto a single chip.

TRENDS IN MEDICAL

- **Evidence-based Medicine:** We are facing enormous pressure to demonstrate the effectiveness of medical treatments for outcome and cost-effectiveness. This will require new sensors and diagnostics for establishing quantitative metrics of success.

- **Cost Control:** Currently, medicine is under enormous cost pressure. At the same time, technical trends in the semiconductor industry are being applied to the health-care field, helping to establish evidence for effective care, and to support the shift from reactive medicine to proactive care.

- **Bench to Bedside is Practical:** The trends in bioelectrical-circuit engineering portend the likelihood that these technologies will transfer soon from "bench" to "bedside" -- moving analysis from the laboratory to the patient. The key enabling features that we are seeing include lower implant power, higher-complexity-algorithm implementation for feature extraction, and faster telemetry for data dissemination and for concurrent implant control. The applications of this technology are also expanding to include heart-rate monitoring, implantable neural tags for research and chronic monitoring, and acute detection of electroencephelograms (EEG) for seizure monitoring and brain-state detection.

- **Power Management:** Another key trend in biomedical devices is enhanced power management. This is critical since the battery or other energy storage unit can dominate the size of the medical device. Inductive links are being prototyped that yield higher efficiency to provide greater flexibility for the supply of energy from external sources.

- **Complex Measurement Circuits for System Simplicity:** Improvements in circuit instrumentation are also transferring into the point-of-care arena. Novel measurement techniques, with a particular focus on complex impedance, are providing label-free methods that lower cost. Other emerging techniques include the combination of magnetic beads for sensing forces and molecular tagging. While these approaches currently do not match state-of-the-art approaches using optical techniques, improvements in sensitivity continue that might provide a disruptive point-of-care approach.

TRENDS IN IMAGE SENSORS

- **Markets and Growth:** The CMOS image sensor business is still one of the fastest growing segments of the semiconductor industry, due to cell phone cameras and other digital-imaging applications. The cell phone camera adoption rate is expected to be approximately 90% for 2009, and the 3G mobile technology is accelerating its utilization of multiple cameras per cell phone. Other digital imaging markets include traditional ones such as DSC and camcorders, and emerging markets including web cameras, security cameras, automotive cameras, digital-cinema cameras, and gaming.

- **Issues to Address:** In order to maintain market growth in this industry, many barriers must be overcome. This includes better image quality, higher sensitivity, higher-sensor resolution, lower cost, higher data-transfer rate, higher system-level integration, lower power consumption, and 3D imaging. The number of technology barriers in each market depends on the target application.

- **Technical Advances:** The resolution and miniaturization races have still not ended, and while the performance requirements stay constant, the pixel size is still scaling down. Moreover, in 2009, CMOS image sensors with 1.4μm^2 pixels became available, and sensors with 1.1μm^2 pixels are expected to be available in 2011. In order to compete in this race, new innovative technologies are being continuously developed. These include advanced sub-100 nanometer CMOS image-sensor fabrication processes, backside illumination, digital optics, and wafer-level cameras. The importance of digital-signal-processing technology in cameras continues to grow. This processing is used to mitigate sensor imperfections and noise, and to compensate for optical limitations. The level of sensor computation is increasing to thousands of operations per pixel, and requires high-performance and low-power digital-signal-processing solutions. There is a parallel trend pushing the industry toward higher levels of integration to reduce system costs.

- **Emerging Markets:** The trends in emerging markets include lower-bandwidth communication for surveillance cameras, wider dynamic range, and optical-communication function for automotive cameras, faster read-out for digital-cinema cameras, and three dimensional imaging for gaming. As the required functionality and performance increase, the technological challenges continue to grow rapidly. The complexity and performance of CMOS image sensors are growing at an exponential rate. This will enable digital cameras to be used in more aspects of our lives within the next few years.

Low-Power Digital Subcommittee

ISSCC 2010 LOW-POWER DIGITAL

Subcommittee Chair: *Tzi-Dar Chiueh, National Taiwan University, Taipei, Taiwan*

OVERVIEW

CONTEXT AND PRESENT STATE OF THE ART

- Current 3G mobile devices can deliver bit rates up to only 10Mb/s and support only a single wireless standard. **[15.1, 15.3]**
- Current embedded processors run at speeds of several hundred MHz and consume hundreds of mW of power. **[15.5, 15.6, 15.7]**
- Most video decoders today are limited to single-view 1920x1080 video signals. **[18.3]**
- Simple intelligent vision processing, such as smile detection and face tracking, is experiencing widespread adoption in commercial applications such as digital cameras. **[18.5]**

MOST-SIGNIFICANT RESULTS

- The first functional 4G silicon chips are described enabling high-speed communication for netbooks, smart phones, and the next generation of mobile devices. ETH Zurich with Advanced Circuit Pursuit and CEA-LETI with T. U. Kaiserslautern describe chips that implement 390 Mb/s turbo code decoding, and a multimode software-defined radio capable of 4G, WIMAX, 802.11n, and cognitive radio. **[15.1, 15.3]**
- Low-power processors break through the gigahertz barrier, enabling a new generation of smart phones with never-before-seen capabilities. ARM and Intel describe new embedded processors with over 1GHz operation at power levels under 50 mW, while Qualcomm describes low-power-design techniques used in their 1.4GHz Snapdragon processor. **[15.5, 15.6, 15.7]**
- The first super-HD and 3D-video decoder is presented. This 90nm chip supports video signals with 4096x2160 resolution or multiview video, consuming only 59mW. **[18.3]**
- A massively parallel processor enables advanced intelligent image processing for surveillance cameras and multimedia phones. With 2048 cores, this chip can be applied to object tracking, face/gesture detection, and other computationally intensive image processing problems. **[18.5]**

APPLICATIONS AND ECONOMIC IMPACT

- 4G mobile high-speed networking can bring HD video and other internet content to smartphones, netbooks, and mobile devices, enabling the next-generation user experience. **[15.1, 15.3]**

- With higher computational power and lower power consumption, high-performance cores make next-generation smart phones even more powerful, with longer battery lifetime. **[15.5, 15.6, 15.7]**
- Advanced video decoders enable the next generation of super high-definition displays and the emerging market of 3D TV. **[18.3]**
- Smart cameras that can recognize your smile/face/gesture and track interesting objects are possible thanks to this massively-parallel image-processor chip. This will result in new and innovative applications that were previously thought to be impossible due to computational limitations in the current generation of image processors. **[18.5]**

MEMORY SUBCOMMITTEE

ISSCC 2010 – MEMORY

Subcommittee Chair: *Hideto Hidaka, Renesas Technology, Itami, Japan*

OVERVIEW

CONTEXT AND PRESENT STATE OF THE ART

- 16Mb Spin-Torque Transfer Magnetic RAM (STT-MRAM) has been demonstrated. **[14.2]**
- Conductive-Metal-Oxide (CMOx) memory has been prototyped in kilo-bit chips. **[14.3]**
- Phase-Change Memory (PCM) has achieved a limited capacity of 512Mb in 90nm CMOS. **[14.8]**
- Microprocessors currently use SRAM for on-chip L3 caches. **[19.1]**
- 32nm SRAMs are limited by low-voltage operation. **[19.3]**
- DRAMs for mobile applications have used a low power LDDR2 (LPDDR2) interface for higher bandwidth. **[24.2]**
- Higher interface speed is a cricital requirement for memory systems, as NAND capacity increases. **[24.6]**

MOST-SIGNIFICANT RESULTS

- Highest density of 64Mb STT-MRAM with smallest perpendicular cell of 0.358μm^2 in 65nm CMOS. The 30ns access time is used a clamped reference with a new adequate-reference-based sensing schemes. **[14.2]**
- Highest density of 64Mb CMOx memory in 0.13μm CMOS in a four-layer 0.17μm^2 cross-point-cell array. Using the multi-layer capability, this memory is scalable to 64Gb capacity. **[14.3]**
- Fastest 12ns 4Mb embedded PCM in 90nm CMOS ever reported! Fast read is achieved by using low-voltage MOS in the hierarchical column decoder. **[14.7]**
- Highest density of 1Gb PCM on 45nm CMOS with 1.8V operation features the fastest-ever read/write performance with 266MB/s and 9MB/s read/write throughputs respectively. **[14.8]**
- First 45nm embedded DRAM (eDRAM) as L3 cache in a high-end server-class microprocessor, the POWER7™. Previously, all microprocessors have used SRAM for L3 cache implementations while this design uses eDRAM to reduce area and cost. **[19.1]**
- First use of margin-improvement techniques at 32nm for enhanced low-voltage operation. A new approach called wordline underdrive (WLUD) has been applied in 32nm High-κ Metal-Gate technology to reduce Vcc_{min} by 130mV. **[19.3]**
- Smallest 32nm SRAM bit cell (0.149μm^2) uses an assist technique to improve low-voltage operation. This new technique improves write margins, reducing cell-failure rate by two orders of magnitude in High-κ Metal-Gate 32nm CMOS. **[19.4]**
- Fastest wide-I/O-mobile SDRAM using micro-bumps achieves a 12.8GB/s data rate at 200MHz. **[24.2]**
- Fastest 200MB/s DDR interface on a 32nm 32Gb NAND flash memory. **[24.6]**

- 32nm 32Gb NAND flash memory with adaptive code selection and floating-gate-coupling cancelation. **[24.8]**

APPLICATIONS AND ECONOMIC IMPACT

- The 64Mb MRAM can potentially replace current flash technology with almost unlimited read and write cycles. **[14.2]**
- The 64Mb Conductive-Metal-Oxide (CMOx) memory with multi-layer capability can potentially reach 64Gb single-chip capacity to drive down the cost of current NAND flash technologies, enabling, extremely low-power and low-cost applications. **[14.3]**
- New PCM technologies may unseat traditional SRAM and flash technologies as the embedded memory of choice for SoCs, providing very-high capacity non-volatile memory at low costs making PCM ideally suited for cost-sensitive embedded applications. **[14.7, 14.8]**
- New eDRAM technology enables never-before-seen levels of memory integration for server processors, improving performance while lowering both power and cost. **[19.1]**
- Improved SRAM designs with reduced power consumption, and improved reliability and robustness at low supply voltages, enable dependable operation in the migration to deep submicron 32nm CMOS. **[19.3]**
- Novel System-in-Package (SiP) technology, enabling the integration of sophisticated memory controllers and DRAMs, will increase performance while reducing costs by allowing for smaller form-factors in future designs. **[24.2]**
- NAND-flash costs are further reduced by foregoing more complicated 3b/cell multi-level cell technologies in favor of further extending the limits of lithography to improve the cost per bit. This will result in increased capacities, faster read/write times, and faster adoption of NAND technologies in new markets such as solid-state drives (SSDs). **[24.6, 24.8]**

TRENDS IN MEMORY

Memory design has seen a number of trends over the years: process technology has steadily reduced its minimum feature size, a wide variety of techniques have been developed to improve packing-density, and a myriad of technology/circuit/system optimizations have been created to improve performance and reduce power dissipation. In addition, emerging technologies such as 3D chip stacking and new physical memory mechanisms are pushing the memory R&D frontier even-further forward. At ISSCC2010, a plethora of descriptors is needed to capture t memory developments:

- 32nm 32Gb MLC NAND flash memory
- 8Gb/s-GDDR5 DRAM with 1Gb capacity
- 32nm SRAM using 7/8/10/12T cells for excellent margins at low-voltage low-power designs
- 3D integration includes revolutionary interface techniques (such as, 8Tb/s/1pJ/b inductive interfaces)
- Emerging memory technologies to realize non-volatile RAM, abounds: 45nm 1Gb PCRAM (Phase-Change Memory), FeRAM (Ferrolectric RAM), ReRAM (Resistive RAM), MRAM (Magnetic RAM), and so on.

In particular, NAND flash memory has seen significant developments in the past few years, with the advent of high-density technology to meet the low-power and low-cost storage demands for replacing hard-disk storage in the form of solid-state disks (SSDs). The figure below shows the observed trend in NAND flash capacities presented at ISSCC in the past 12 years. Note that in 2010, the reduction in process feature sizes, coupled with advanced multi-level cell (MLC) techniques have yielded a 32Gb/chip capacity in a 32nm technology with 2b/cell operation.

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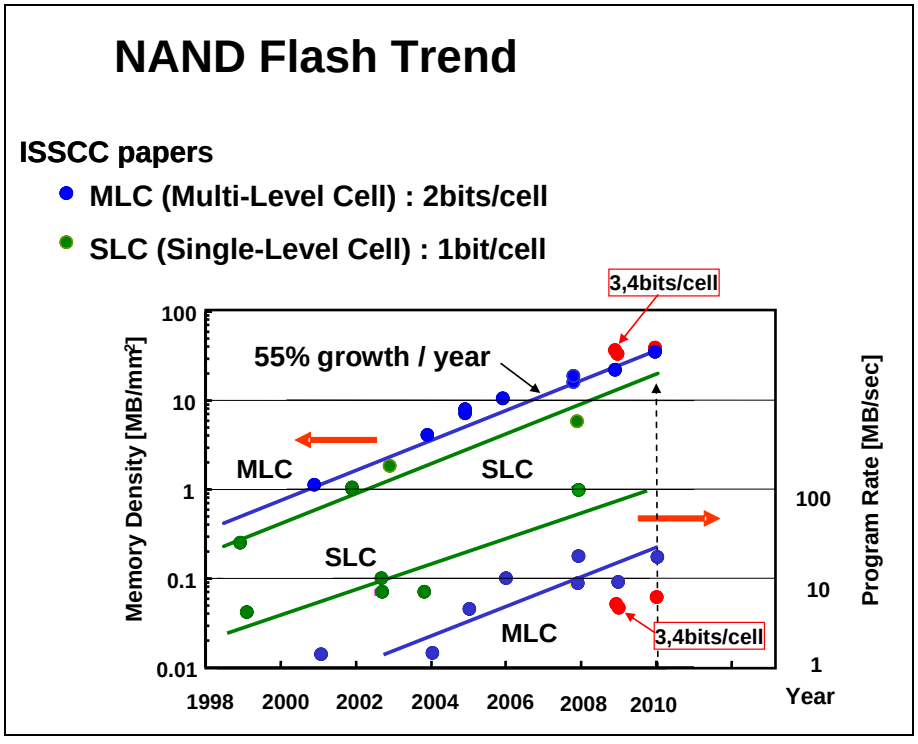


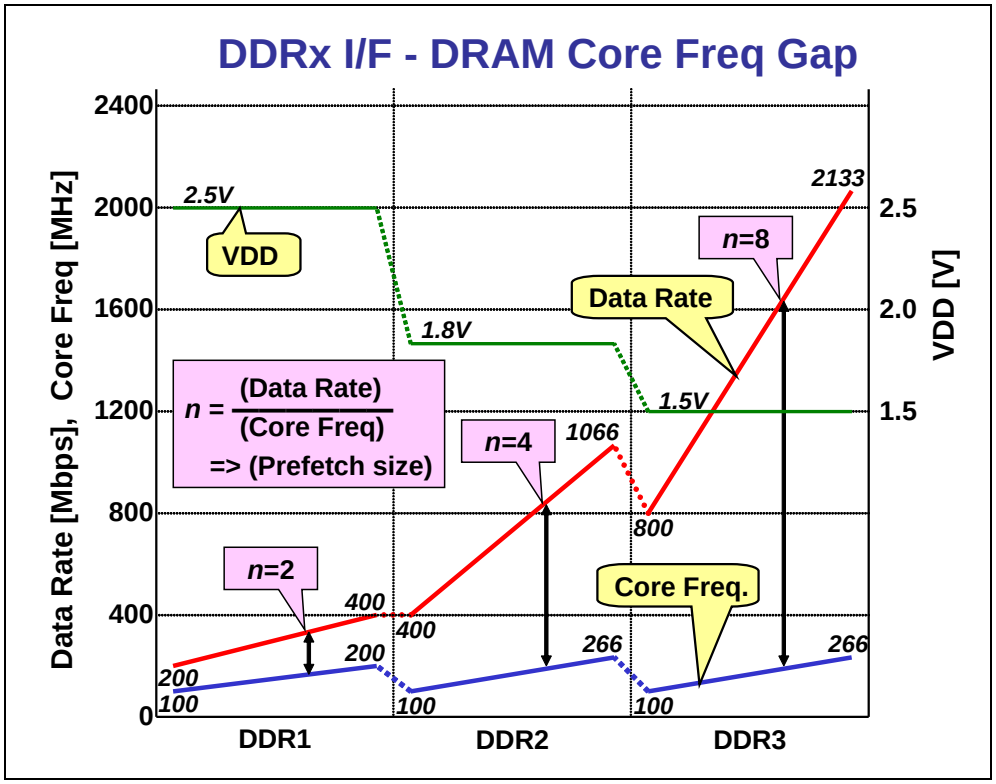
SOLID-STATE DISKS (SSDS)

The aforementioned SSD technology has recently begun to take off as integration density and bit-cost reduction have made SSDs feasible replacements for conventional hard disk drives (HDDs) in niche applications where the higher costs are tolerable (such as, high-end ultra-portable laptops). Continued optimization of both density and cost will enable SSDs to become more price-competitive, increasing their adoption rate in more mainstream applications, and introducing new requirements for the SSD environment, such as:

- High-bandwidth NAND flash operations
- Optimized organization for SSD systems with 3D chip-stack structures
- Wireless interface schemes for 3D chip-stacks
- Defect control
- High-voltage power supplies for NAND flash memory cell operations

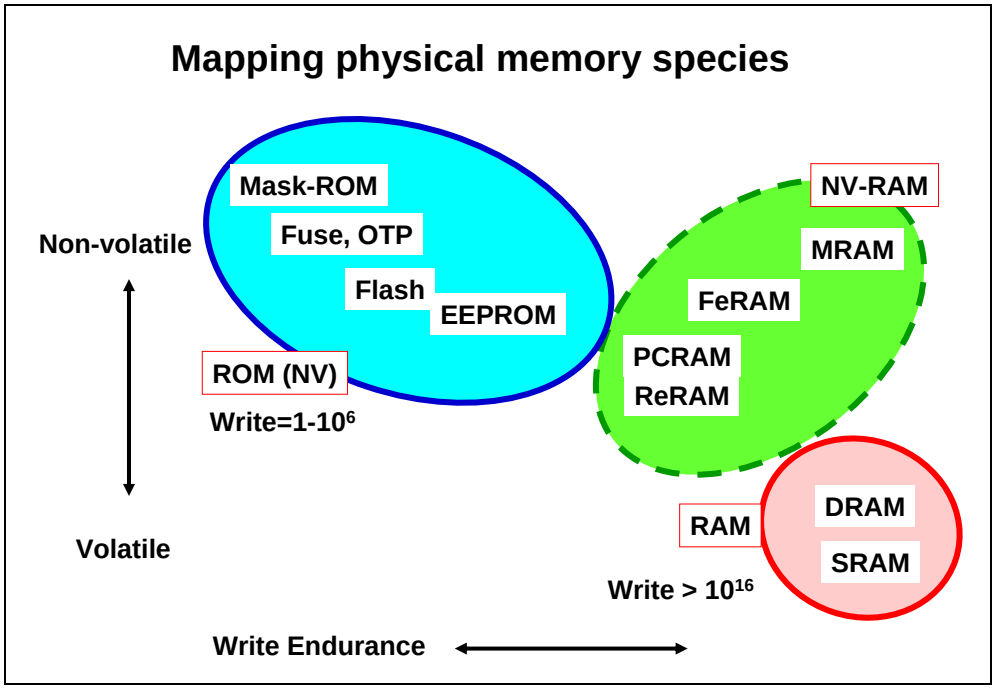
INTERFACES

Unfortunately, the gap between memory-core frequency and external-data rate continues to increase as conventional high-speed wired interface schemes such as DDRx and GDDRx for DRAM and NAND flash memory continue to evolve (see figure below). This leads to the need for a larger prefetch size, which is emerging as a major problem in modern memory systems. However, alternatives which accommodate high data rates through the use of wider or differential interfaces will face the problem of increased pin-counts, and enlarged silicon areas. Combined with 3D integration of memory and memory/logic in near-future commercial products, new interface technologies will yield more memory stacking, along with lower-power and higher-bandwidth interfaces. A recent experimental inductive coupling interface demonstration has achieved a 128 NAND chip stack for SSD use, with an 8Tb/s interface for a DRAM/GPU stack.



NON-VOLATILE MEMORY

New breeds of non-volatile memory technologies aiming at persistent, non-volatile-RAM (NV-RAM) has evolved over time, with ISSCC faithfully tracking these developments over the years. ISSCC 2010 will feature a new level of ReRAM (Resistance RAM) integration and circuit design, presenting a new opportunity for extending the memory technology spectrum, together with existing FeRAM/MRAM/PCRAM technologies, as shown in the figure below. Commercial uses of these new breeds of NV-RAM have been very slow to appear because of the rapid reduction of per-bit costs of conventional flash memory technologies already in the market. However, these new technologies are sure to capture some specific markets for lower-power or zero stand-by system implementation in the coming age of green technology!



PLL Subcommittee

ISSCC 2010 – PHASE-LOCKED LOOPS (PLLs)

Subcommittee Chair: *Nikolaus Klemmer, ST-Ericsson, Research Triangle Park, NC*

OVERVIEW

CONTEXT AND PRESENT STATE OF THE ART

- In essentially all electronic devices at least one off-chip crystal resonator provides a reference time base or clock. Unfortunately, crystals are bulky and non-configurable in their resonance frequency. MEMS resonators are emerging as viable alternatives to traditional crystal resonators for accurate frequency references. A variety of different reference frequencies may be needed, depending on the application or communications system. **[13.1]**
- Transmitters and receivers for wireless-infrastructure applications require higher-performance, and lower-noise frequency sources than their mobile counterparts. To achieve these demanding requirements, such systems currently require discrete bulky and power-hungry implementations of their PLLs and oscillators. **[13.4]**
- Digital PLLs require the detection and digitization of small timing errors on the order of picoseconds. Various implementations have been reported over the past years but typically manufacturing tolerances and device mismatches lead to periodic disturbances of their digital output, generating spurious tones in the PLL output signal. **[26.1]**
- To date, digitization of timing errors in digital PLLs was achieved via a time-to-digital converter (TDC) block. But, manufacturing tolerances in unitary time delays in these converters lead to a need for calibrating their time base relative to a known reference. **[26.3, 26.6]**

MOST-SIGNIFICANT RESULTS

- A new MEMS-based oscillator provides an accurate reference frequency with wide programmability. A MEMS resonator, combined with a particularly area-efficient CMOS chip forms a programmable crystal-less 1-to-115MHz clock reference. **[13.1]**
- For the first time, high-quality low-noise frequency synthesizers for wireless-infrastructure applications are demonstrated in a fully-integrated fashion. The chips achieve cellular basestation performance using 0.18μm SiGe BiCMOS technology. **[13.4]**
- A new time-to-digital converter achieves the lowest spur-performance in a wideband all-digital PLL. The new design uses dithering to trade off fractional spur power for a slight increase in in-band noise. **[26.1]**
- For the first time, digital PLLs combine TDC with oscillator functions. This is achieved by re-using the digitally-controlled ring oscillator (DCO) as an intrinsically-tuned phase quantizer, eliminating the calibration required with traditional TDCs. **[26.3, 26.6]**

APPLICATIONS AND ECONOMIC IMPACT

- Advances in analog PLLs, using new design techniques and high-performance silicon technologies, show a further increase in noise performance and integration level, allowing smaller lower-power implementations of wireless-infrastructure devices, and higher-fidelity transmitters and receivers. These developments will pave the way to reducing the cost of high-performance wireless networks that will extend connectivity around the globe. **[13.4, 26.4]**
- Advances in digital PLLs are essential to further increases in the development speed of System-on-Chip (SoC) implementations of otherwise-complex and power-hungry systems. Digital clock-generation macros are showing performance metrics previously achievable only using analog techniques, which are time consuming in implementation, and difficult to migrate to new technologies. **[26.1]**
- Digital implementations are paving the way to fully-synthesized-clocking cores that allow straightforward process scaling and shortened design cycles, which will ultimately drive down development costs. **[26.3, 26.6]**

RF Subcommittee

ISSCC 2010 – RADIO FREQUENCY (RF)

Subcommittee Chair: *John R. Long, Delft University of Technology, Delft, The Netherlands*

OVERVIEW

CONTEXT AND PRESENT STATE OF THE ART

- Practical implementations of 60GHz indoor communication links require beamforming for high-data rate applications. **[2.1, 2.2, 2.3]**
- Voltage-controlled oscillators currently limit integration of truly portable all-digital phase-locked loops in CMOS. **[2.6, 2.7]**
- Passive RFID technology is presently limited by activated power consumption, size, and weight in sensing applications. **[2.8]**
- Power amplifiers are beginning to perform well into the millimeter-wave frequency range. **[23.6, 23.7, 23.8]**
- Millimeter-wave transceivers are beginning to offer the promise of wireless communication at Gb/s rates. **[23.1]**
- 60GHz CMOS power amplifiers are currently capable of operating with a +10 to 13dBm output- power level. **[23.7, 23.8]**

MOST-SIGNIFICANT RESULTS

- First 2x2 beamforming transmitter demonstrator in 65nm CMOS offers robust independent vertical and horizontal scanning of a transmit signal in the 60GHz band. **[2.3]**
- The unrelenting quest for power-consumption reduction and performance improvement in GHz transceivers is showcased by voltage-controlled oscillators with outstanding tunability precision **[2.6],** and ultra-low-phase-noise performance **[2.7]**.
- First demonstration of autonomous wireless in-flight recording of a live insect. A passive ultra-low- power RFID system in 0.13µm CMOS consumes only 9.2µA, exhibits a range of 3m, and is so small that it can be mounted on a live moth. **[2.8]**
- Sony and Cal Tech team up to develop the longest-distance inter-chip high-speed/low power communication link. Their millimeter-wave interconnect chips demonstrate 11Gb/s data transmission over a distance of 14mm with an energy consumption of 6.4 pJ/bit. **[23.1]**
- UC Davis demonstrates a 60 GHz CMOS power amplifier with the highest-reported RF output.. Use of three on-chip 2-way power combiners maximizes output, providing a record 20dBm (100mW) RF output-power level. **[23.7]**

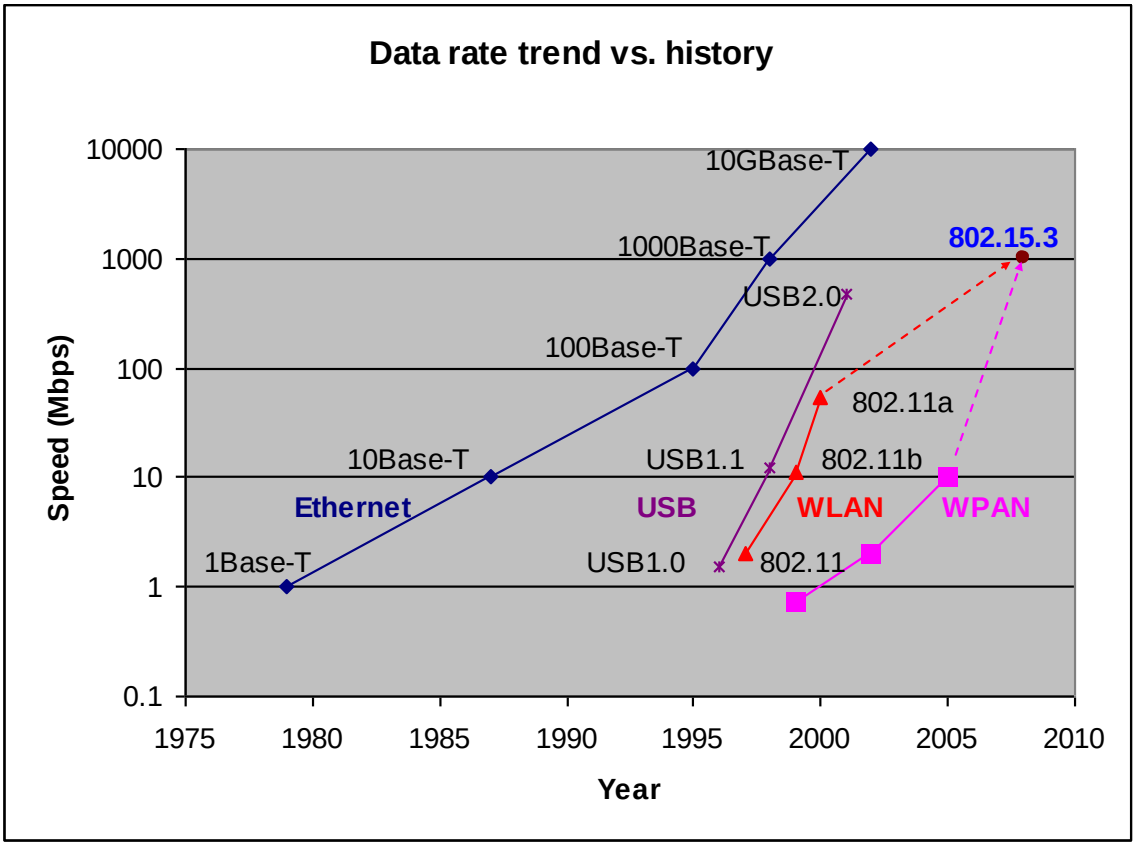
APPLICATIONS AND ECONOMIC IMPACT

- High-throughput systems for wireless video streaming and kiosk downloads enabled by beamforming with antenna arrays in the millimeter-wave band. **[2.1, 2.2, 2.3]**

- Power-efficient and process-insensitive voltage-controlled oscillators amenable to digital integration dramatically decrease silicon area and enable fully-digital phase-locked loops, while reducing the complexity of technology migration. **[2.6, 2.7]**
- Low-power miniaturized RFID techniques advance biomedical research and open the door to unobtrusive human-health monitoring. **[2.8]**
- Millimeter-wave inter-chip communications lead to smaller and cheaper consumer devices operating at Gb/s data rates. **[23.1]**
- Millimeter-wave circuits continue to advance high performance imaging systems for scientific, medical, space, and industrial markets. **[23.2, 23.3, 23.4, 23.5, 23.6, 23.7, 23.8, 23.9]**
- New power amplifier (PA) designs usher in Gigabit data-rates to wireless-communication applications. **[23.6, 23.7, 23.8]**

TRENDS IN DATACOM TECHNOLOGIES

As communication needs increase in our ever technological society, there is an increasing need for higher and higher data-communication (datacom) rates. The data rate trend chart, shown below, projects the capabilities of wireless and wireline datacom technologies using current standards. Note that the graph indicates that millimeter-wave frequency bands (for example, 60GHz) provide a potentially-disruptive technology, enabling gigabit/s data rates over a short-range wireless link at speeds well over 1,000Mbits/s (1Gb/s) (for example, 802.15.3 shown below).



TRENDS IN MM-WAVE IMAGING

As silicon IC technology advances to higher and higher frequencies, millimeter-Wave (mm-Wave) and TerHertz (THz) technology is enabling fine resolution imaging for biomedical, logistics, and security applications. The two images shown below – one optical and the other taken using a 94GHz radio imager – reveal that a concealed weapon is easily detected using very-high-frequency radio imaging techniques.

man concealing a weapon

mm-wave image

Images courtesy of TNO-FEL, The Netherlands

Technology Directions Subcommittee

ISSCC 2010 – TECHNOLOGY DIRECTIONS (TD)

Subcommittee Chair: *Siva Narendra, Tyfone,, Portland, OR*

OVERVIEW

CONTEXT AND PRESENT STATE OF THE ART

- Transistors made with organic, plastic-like materials are emerging to enable low-cost electronics that can be manufactured using conventional printing techniques **[7.1, 7.2, 7.3, 7.4, 7.5]**
- The technologiy of 3D integration with Through-Silicon Vias (TSVs) is maturing, but for designers it is still a daunting task to partition circuit functions to fully exploit 3D freedoms **[7.8]**
- Current medical devices like blood pressure monitors and spinal-cord stimulators to combat severe pain are sizeable boxes **[12.1, 12.2]**
- Nuclear Magnetic Resonance (NMR) has a broad spectrum of powerful applications, such as biomolecule sensing and medical imaging, but NMR instruments are bulky and expensive, and thus remain as specialized equipment in hospitals and laboratories **[27.2]**
- Monitoring heart health to prevent failures involves many visits to the hospital to undergo specific medical tests **[27.3]**

MOST-SIGNIFICANT RESULTS

- For the first time, analog circuits and data converters are manufactured using only organic, plastic-like materials. Such circuits will allow the integration of sensors and digital circuits on flexible media embodying intelligent electronics. **[7.1, 7.2]**
- User-Customizable Logic Paper (UCLP) enables the development of integrated circuits with a standard ink-jet printer. This new technology will provide programmability for integrated circuits used in large-area electronics such as smart flexible displays, power transmission sheets, and electronic skin for robots. **[7.3]**
- The first prototype of a commercially-viable cost-effective 3D-stacked IC is demonstrated by IMEC. It is based on a new analysis of methodologies for the use of Through-Silicon Vias (TSVs). **[7.8]**
- For the first time, a implantable CMOS System on Chip (SoC) has been designed to provide low-voltage radio waves that gently heat your back to relieve pain. The SoC is fabricated in a 0.35µm CMOS process and for initial experiments is mounted on a PCB that is connected with a flexible coil antenna mounted in the spinal region. **[12.1]**
- The smallest-ever pressure monitoring device promises new developments in ultra-small medical implants. . This device occupies less than one mm^3, consumes 200,000× less energy than state-of-the-art monitors, will enable promising new techniques for monitoring blood pressure and intraocular pressure. **[12.2]**
- Researchers from Harvard University will present the smallest-ever complete nuclear magnetic resonance (NMR) system that makes possible human cancer screening in a low-cost hand-held platform. Their 0.1-kg 'palm' NMR system is 1200× lighter, 1200× smaller, 1400× cheaper, yet 150× more sensitive than a 120-kg state-of-the-art commercial bench-top NMR system. **[27.2]**

- For the first time, a poultice applied to the chest can help prevent heart failure. Electronics in the poultice ensure that ECG patterns, heart rhythms, thoracic impedance variance (TIV), and heart pumping-power, are evaluated and relayed automatically to your cell phone. **[27.3]**

APPLICATIONS AND ECONOMIC IMPACT

- Organic transistors and printed electronics are evolving to extend the integration of sensors and logic. Organic intelligent sensors can be distributed on large surfaces or be produced at extremely low cost to enable applications such as artificial skin and freshness-monitoring devices embedded in food wrapping. **[7.1, 7.2, 7.3, 7.4, 7.5]**
- 3D integration is essential for future integrated systems and is rapidly becoming a workhorse of the semiconductor industry. **[7.8]**
- Integrated electronics enable complex medical monitoring and therapy systems, as well as laboratory measurement equipment like NMR, in unprecedented small form-factors. Exploiting such innovative devices, prevention, diagnosis, cure, and recovery, will move more and more outside the hospital, and provide patients with a greatly improved quality of life. **[12.1, 12.2, 27.2, 27.3]**

Wireless Subcommittee

ISSCC 2010 – WIRELESS

Subcommittee Chair: *Trudy Stetzler, Texas Instruments Inc., Stafford, TX*

OVERVIEW

CONTEXT AND PRESENT STATE OF THE ART

- Internet multimedia data, on-line social networking, and virtual worlds are driving wireless-communications engineers towards new challenges as intensively as they are changing human behavior in everyday life. Enhanced user interfaces are making Web usage ubiquitous among both fixed and mobile devices, and remote data processing is becoming more prevalent with the adoption of "cloud computing". This mandates substantial improvements in connection speed, capacity, mobility, and reliability in wireless wide-area networks. Cellular techniques leading towards wideband software-defined radios provide one way to allow these services for everyone around the world. **[3.1, 3.3, 3.5]**
- Silicon circuits for Automotive Radar at 24GHz and 77GHz have appeared in the past four years. Initially they were implemented in BiCMOS technology and demonstrated the feasibility of implementing such applications in silicon. Last year the first pure CMOS 77GHz circuits appeared, but they did not fully meet the ranging requirements for today's automotive radars. **[11.2]**
- Circuits for 60GHz multi-Gb/s short range communications in BiCMOS and CMOS technologies have proven the feasibility of implementing such applications in silicon. The main challenges beyond the 60GHz band are the wide bandwidth and high data rate required. In addition, multiple antenna arrays will be needed to maintain the necessary Quality of Service (QoS) for Wireless High-Definition-Medium Interface (WHDMI) over a 10 meter range. **[11.3]**.
- One of the main challenges to making long life wireless sensor networks a reality is to reduce the power consumption of the wireless receivers as much as possible. Ultra-low-power wake-up receivers reduce sensor power even further as they activate the whole sensor only when needed. At the same time, Impulse-Radio Ultra-Wide-Band (IR-UWB) offers another solution for reducing power consumption using a special modulation scheme, allowing ranging possibilities and wireless communications. **[11.5, 11.7]**
- Advanced mobile devices, such as cell phones, no longer provide a single function. Instead, in order to improve the end-user experience, they are required to support as many standards as possible, such as WLAN, Bluetooth, FM, mobile TV, and GPS, to name a few. Providing these functions while enabling a low-cost solution requires a high degree of silicon integration. **[25.3, 25.6, 25.7]**

MOST-SIGNIFICANT RESULTS

- Highly robust and reliable cellular transceivers for advanced 3G (HSPA) and 2G (E-EDGE) communications are core enablers for the truly mobile internet. These breakthrough solutions demonstrate the feasibility of enhancing user data rates in all market segments and geographical areas. **[3.1, 3.3]**

- The first wireless receiver that connects the ADC directly to the RF provides a major step towards true software-defined radio (SDR). The resulting linearity improvement of up to +4dBm exceeds previous limits over the receiver spectrum at 900MHz,without major impact on sensitivity. **[3.5]**
- The first CMOS 77GHz Long Range Radar satisfying the 100m range standard requirement is demonstrated. The fully-integrated solution includes clock generation and a complete chip-antenna assembly. **[11.2]**
- The first 16-Element Phased-Array Transmitter for 60GHz WHDMI communications is realized in 0.12µm SiGe BiCMOS technology. The solution uses an antenna-array approach to meet the QoS demanded to enable WHDMI. **[11.3]**
- A 51µW always-on wake-up receiver is demonstrated in 90nm CMOS. This solution paves the way for truly autonomous sensor nodes employing energy scavenging to satisfy their power needs. **[11.5]**
- An IR-UWB architecture enabling robustness against narrowband interferers has been realized in 90nm CMOS. The interference-robust asynchronous energy-detector receiver can tolerate interferers of up to -5dBm. **[11.7]**
- The first reported SoC that combines WLAN, Bluetooth, and FM radios on a single chip. The 16.9mm^2 combo radio is implemented in 65nm CMOS technology, and integrates an on-chip PA with linear output power of 21dBm in the 2.4GHz band. **[25.3]**
- Highest level of integration in multi-standard mobile TV SoCs. Implemented in 65nm CMOS technology, the chips utilizes multiple on-chip LNAs to cover different frequency bands of operation while sharing the rest of the receive chain**. [25.6, 25.7]**

APPLICATIONS AND ECONOMIC IMPACT

- The first internet access in emerging countries will be based on cellular systems. This will quickly facilitate local business and everyday life using recent affordable advances in GSM/EDGE. **[3.1]**
- The 'always on' internet will be available for the first time via broadband cellular access using extremely high performance low cost low-power digital signal processing. Novel techniques merging RF and digital processing using RF ADCs will pave the way towards very small-form-factor software-defined radios. **[3.5]**
- Cruise-control radar crash-avoidance features will markedly increase the safety of future vehicles. Advanced silicon technologies will reduce the cost while improving the performance of these applications, spurring widespread adoption. **[11.2]**
- The consumer market is driving the demand for wireless connectivity between BluRay DVD players and High Definition Video Screens, thereby avoiding the clutter, expense, and wiring complexity of cables. **[11.3]**
- Battery-less wireless sensor networks for health and environment monitoring benefit from ultra-low-power transceivers. Ranging capabilities will allow multiple identical sensors distributed over an area while identifying each sensor individually. **[11.5, 11.7]**
- SoC integration of multiple radios will enable faster adoption in mobile platforms while opening up new market opportunities. **[25.3]**
- Multi-standard mobile-TV chips will enable faster penetration into the cell phone market while lowering the overall solution cost. **[25.6, 25.7]**

TRENDS IN WIRELESS COMMUNICATIONS

Approximately four years ago, the first wireless LAN System-on-Chip (SoC) implementation was presented for a single-mode WLAN solution. Now, in just four short years, SoC solutions for WLAN have become multi-band and multi-standard, heralding a truly astonishing evolution! In the past three to four years, the celluar-handset world has evolved from simple radio transceivers to complete SoC solutions that include both the RF transceiver and baseband processor. Currently, 65nm CMOS SoCs are common place for these applications, with the expectation of 45nm CMOS solutions in the very near future! Unfortunately, the number of solutions in these areas is limited to a few companies who have the capabilities and can afford the access to advanced technologies; however, occasional disruptions occur when talented start-up companies with revolutionary ideas appear.

As well. another emerging trend in the wireless area focuses on millimeter-wave radio transceivers, first in SiGe, and now in conventional nanoscale CMOS technologies. Recent wireless sessions at ISSCC have included university groups and companies who have introduced 60GHz high-speed short-range data links. There has also been an evolving trend toward the use of 65nm CMOS in low-cost 77GHz automotive radar solutions that enable these systems to move beyond high-end luxury vehicles to more economical market segments.

Currently, as well, research activities in both academia and industry are focusing on all aspects of wireless sensor networks. Today's research efforts are exploring various circuit techniques and radio architectures to achieve the lowest possible power consumption, while enabling battery-less operation via energy scavenging from the surrounding environment. These new architectures encourage the highest level of integration in nanoscale CMOS, including the integration of antennas. Such combined efforts are slated to drive low-cost medical devices, inventory tracking, and new ways of interpersonal networking that will lead to ubiquitous wireless communications, continuing to improve (hopefully!) everyone's quality-of-life!

Wireline Subcommittee

ISSCC 2010 – WIRELINE

Subcommittee Chair: *Franz Dielacher, Infineon Technologies, Villach, Austria*

OVERVIEW

CONTEXT AND PRESENT STATE OF THE ART

- A roadblock to increasing the data rate in many systems is the power efficiency of the transceivers employed. The significance of this challenge grows as more and more backplane and chip-to-chip bandwidth requirements are measured in the Tb/s range. **[8.1, 20.5]**
- Higher data rates will only be enabled when power-efficient sophisticated equalization techniques are realized in silicon processes. **[8.5, 8.6]**
- The cost of optical systems is presently prohibitive because optics have not yet been integrated into CMOS processes. **[20.1, 20.2]**

MOST-SIGNIFICANT RESULTS

- One half trillion bits communicated in one second! Intel presents an extremely "green" transceiver chip with 47 channels operating at 10 Gb/s while consuming only one tenth of the power/bandwidth of any work reported previously. **[8.1]**
- The most effective CMOS wireline receiver equalizer ever published, is presented. This solution is able to recover "almost-completely-evaporated" data, as demonstrated by its ability to compensate for up to 39dB of loss, which is equivalent to receiving only 1.4% of the data energy originally transmitted! **[8.5]**
- Another nail in the coffin of analog transceivers by digital! An ADC-assisted receiver using digital signal processing operates successfully at 6.875Gb/s under challenging conditions. **[8.6]**
- Low-cost optical receivers are finally a reality. A high responsivity production-quality Ge photodiode (PD) is integrated in 0.13μm SOI-CMOS technology. The PD exhibits a sensitivity of 6μA p-p at a BER of 10^{-12}, while consuming a paltry 15mW when operating at 10Gb/s. **[20.1]**
- The fastest single-chip CMOS Opto-Electronic Integrated Circuit (OEIC) receiver ever reported! The OEIC incorporates an 8.5Gb/s receiver with on-chip silicon photodiode for short-distance optical communications. **[20.2]**
- A huge step forward in green electronics is evident with the most efficient fully-featured 10Gb/s-class transceiver ever reported!. The 12.5Gb/s 65nm CMOS transceiver breaks the mythical 1mW per Gb/s efficiency benchmark with a power consumption of only 12.3mW. **[20.5]**

APPLICATIONS AND ECONOMIC IMPACT

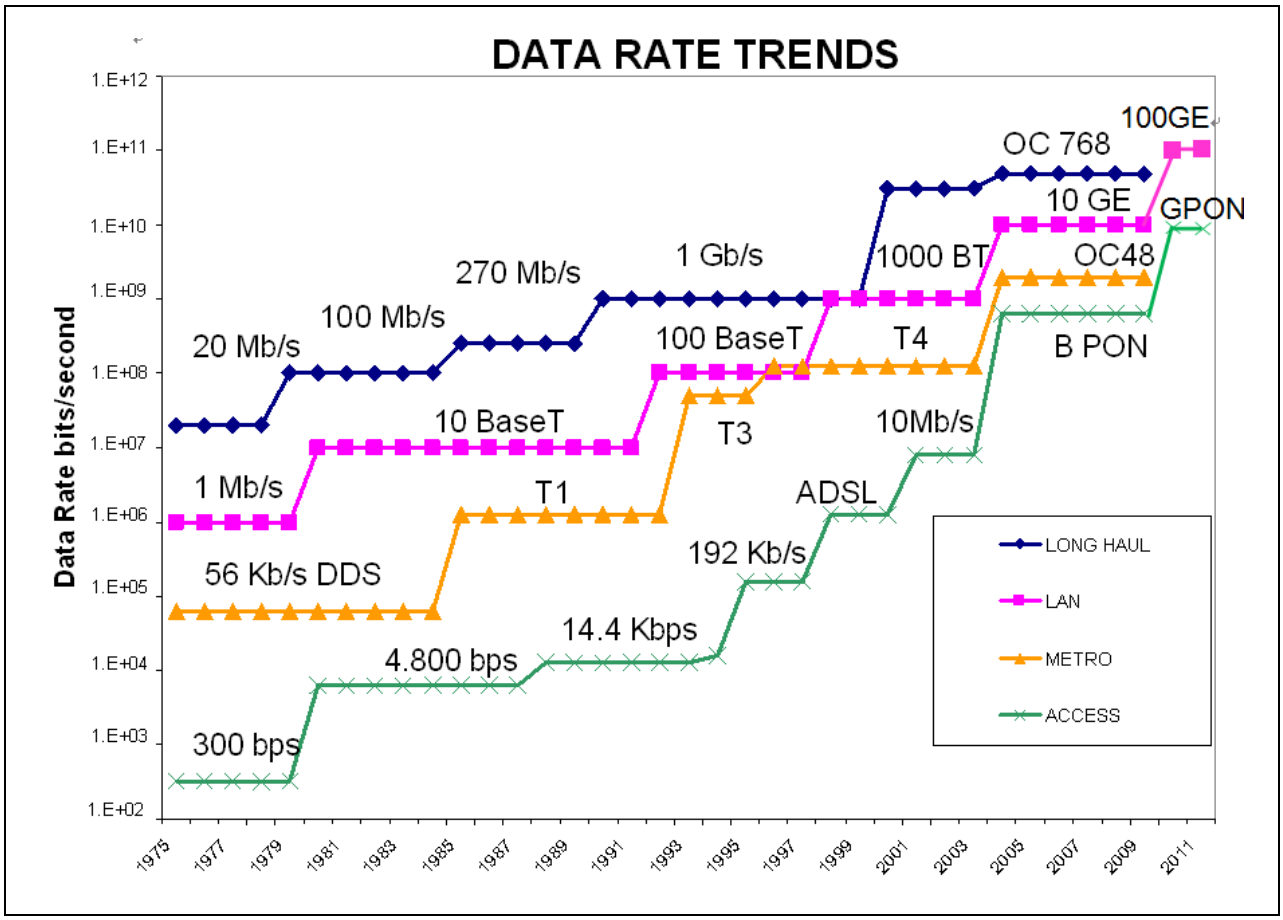
- The trend in electronics to "greener" pastures is evident with the presentation of the most efficient wireline transceivers ever reported. **[8.1, 20.5]**
- System costs can now be lowered through the use of lower-priced lower-quality materials due to recent advances in realizing sophisticated power-efficient equalization techniques in silicon processes. **[8.5, 8.6]**
- Optical connectivity everywhere, from backbone networks all the way down to chip-to-chip communications, took a giant step forward with the demonstration of the integration of production quality optics in a CMOS process. This represents a major step for driving down the price of optical communication systems, removing yet another barrier to their widespread deployment. **[20.1, 20.2]**
- 100Gb/s Ethernet is now one step closer to becoming a reality with the first successful demonstration of a 2x25Gb/s CMOS demux chip. **[20.8]**

TRENDS IN WIRELINE COMMUNICATIONS

Greener yet-faster wireline communications is everyone's dream. It is driven by an ever-increasing demand for more high-bandwidth services such as YouTube, IP video, and cloud computing. This demand can be fulfilled by exploiting the scaling of CMOS processes, innovative energy-efficient yet high-performance circuit techniques, and overall system architectures. At ISSCC 2010, two sessions **[Session 8, Session 20]** will describe a number of results that address these trends.

New applications are emerging such as Internet multi-player gaming, network-based computing/data-storage, transaction-intensive Web 2.0 applications, and high-definition home-entertainment networks. The enabling technologies for these applications are OC-768 (40Gb/s) and 100G Ethernet, high-speed green serial links for data centers, and the deployment of gigabit passive optical networks (GPON), which will provide home-access data rates up to 10 Gb/s, and beyond, in the near future. PON technology reduces system cost by sharing fiber between multiple customers, but challenges transceiver designers by requiring burst-mode operation of amplifiers, and clock recovery with low latency at gigabit data rates. We expect continuing innovation in this area for the foreseeable future.

As shown in the figure below, up to 100 Gb/s data rates are now readily available, using CMOS chips. An entire high-definition movie can be transferred at this rate in less than a second. To achieve such a high data rate with reasonable power consumption, advanced energy-efficient clock-and-data recovery and equalizing techniques are necessary to conquer transmission-channel impairments and speed limitations of low-cost CMOS. ISSCC 2010 will present a large selection of techniques in various CMOS nodes, down to 32 nm, with impressive sub-milliwatt power consumption per Gb/s achieved for a complete transceiver.



ISSCC 2010
Session Overview
Press-Release Material

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PREAMBLE

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FOOTNOTE

- From ISSCC's point of view, the phraseology included in the box below captures what we at ISSCC would like your readership to know about this, the 57th appearance of ISSCC, on February 7th to the 11th, in San Francisco.

This and other related topics will be discussed at length at ISSCC 2010, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 7-11, 2010, at the San Francisco Marriott Marquis Hotel.

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As of November 1, 2009, there is not enough information to guarantee its correctness.
Thus, it must be used with some caution.

Session 2 Overview / RF

mm-Wave Beamforming & RF Building Blocks

Session Chair: *Bud Taddiken, Garland, TX*
Session Co-Chair: *Andreas Kaiser, IEMN-ISEN, Lille, France*

Several thematic areas are covered in this session. Advances in integrated phased arrays for millimeter-waves are described in the first part, followed by circuit techniques for mobile communications, and finally an ultra low-power RF-ID for sensor applications is presented.

Fully integrated phased arrays at millimeter wave frequencies are expected to be system enablers for wireless high data-rate short-range communications, automotive radars as well as for millimeter-wave imagers. Full integration of antenna phased arrays on silicon allows performing on-chip signal processing without the need to go off-chip. This provides a substantial improvement in system reliability, cost and size. Papers in the first part of this session present significant advances of the state of the art in the trend toward higher system integration.

In paper 2.1, researchers from the University of Southern California describe an original approach to beam-forming entirely based on true time delays. Seven evenly spaced beams are formed from six antennas with each beam having a dedicated output. No further processing for beam-separation is required, and very wide bandwidth from 30 to 40 GHz is achieved without any group-delay variation. Paper 2.2 from IMEC proposes a programmable 4-path baseband receiver / beam former in 40nm, developed according to ECMA 387 AV-OFDM mode. Phase shift resolution is better than 20° and experiments show performance is adequate for two bonded channels of 0.88GHz each. In paper 2.3, Delft University of Technology in the Netherlands and IBM teamed up to design a 4-way transmitter with continuous 2D beam steering in a 65nm CMOS technology. This work uses an original power-efficient approach to LO generation and phase shifting in a zero-IF architecture. The total power consumption of the circuit is only 590mW while producing four 11dBm output signals.

In the second part of the session various new techniques for RF circuits for mobile communications are presented. In paper 2.4, researchers from Caltech present a broadband power amplifier of interest for various distinct applications: from high data rate links to software defined radio and smart antenna systems. In the paper, they describe a technique enabling the output network to track the optimum load impedance over a broad bandwidth. Prototypes, realized in 90nm CMOS, achieve a -3dB bandwidth of 7.8GHz, around 9.1GHz, demonstrating a peak Pout of 25.2dBm at a PAE of 21.6%. Paper 2.5 presents an improved passive-mixer first receiver architecture allowing for tuning of the RF input match through baseband circuitry. The circuit designed at Cornell University achieves an impressive 28dBm IIP3 with a total receiver gain of over 70dB. In paper 2.6, researchers from the University of Pavia in Italy present a way of digitally tuning a VCO in very fine steps. This will allow direct digital control of the VCO in a digital PLL without the use of delta-sigma modulators. In paper 2.7, another Italian group from the Politecnico di Milano presents a VCO with very low close-in phase noise. By adding only 4 resistors to the conventional circuit, the 1/f noise contribution responsible for phase noise close to the carrier can be largely suppressed. The 65nm CMOS 3.3GHz oscillator exhibits à phase noise of only 44dBc/Hz at 1kHz offset for a sub-milliwatt power consumption.

This session concludes with an RFID tag realized for biomedical research and human health monitoring. Paper 2.8 presented by researchers from University of Washington describe a passive RFID sensor, realized in 0.13m CMOS. The tag is remotely powered through the communication link within a 3m range and has been deployed to perform in-flight recording of a moth.

Session 3 Overview / Wireless
Cellular Techniques

Session Chair: *Aarno Pärssinen, Nokia Research Center, Helsinki, Finland*
Session Co-Chair: *George Chien, Media Tek, San Jose, CA*

In most parts of the world the cellular mobile terminal market is dominated by GSM/EDGE standards. However, a key enabler for the popular smart phones, netbooks and other mobile devices is the high data rate provided by 3G standards as WCDMA/HSPA. Another evolving standard based on GSM/EDGE is the Evolved EDGE (E-EDGE) aiming to quintuple the peak data rate of EDGE. The first three papers in this session will address CMOS transceiver solutions for these standards.

Paper 3.1 [Advanced Circuit Pursuit] presents the first single chip to support Evolved-EDGE (E-EDGE) with downlink dual carrier (DLDC). E-EDGE aims at a peak data rate of 1.2Mb/s. The dual carrier aspect requires that two synthesizers operate simultaneously at carrier frequencies very close to each other. The presented transceiver shows to be capable of DLDC multi slot class 39 as the synthesizers are pulling resistant. The E-EDGE transceiver with complete on-chip power management has been realized in 0.13μm CMOS and housed in a TFBGA package.

A small-signal polar EDGE transmitter, as part of a 65nm CMOS SoC will be presented in paper 3.2 by [TI]. The transmitter incorporates the first fully digital implementation for the amplitude path. Various RF impairments in the AM circuitry are digitally compensated, resulting in a 2.5% EVM and meeting the emission mask without a SAW filter. The TX consumes 105mA at 1.2V.

Paper 3.3 [Advanced Circuit Pursuit] addresses a SAW-less WCDAM/HSPA transceiver with integrated DC-DC converter. The receiver has an enhanced IIP2 technique utilizing DC feedback resulting in an IIP2 of +55dBm without any production calibration. The receiver consumes 40mA and the transmitter 65mA in full sensitivity test condition while implemented in 0.13μm CMOS.

The remaining 5 papers in this session address more specific techniques to improve the overall performance of cellular transceivers.

Paper 3.4 [NXP Semiconductors] proposes direct quadrature voltage mixing combined with a 32x over-sampled digital front-end to realize a SAW-less transmitter for WCDMA. Realized in a 45nm CMOS process, the transmitter achieves 2% EVM with a noise floor at -158dBc/Hz at 240MHz offset. At +1 dBm output power the transmitter consumes 30mW.

A direct conversion ΔΣ receiver architecture that can improve out-of-band linearity with an RF feedback loop is proposed in paper 3.5 [ST-Ericsson, Nokia]. The second integrator of the 4th order continuous-time ΔΣ modulator using 1 bit quantization includes the down converting mixing stages. The 900-MHz direct conversion receiver achieves a NF of 2.3dB in conventional and 6.2dB in delta-sigma mode respectively and an out-of-band IIP3 up to +4dBm. Realized in a 65nm CMOS process the chip consumes 80mW from a 1.2-V supply.

Paper 3.6 [Toshiba] presents a wide bandwidth Cartesian loop transmitter for off-chip PA linearization. Applying a feed forward technique in the base band, the RF delay can be compensated. The technique improves the ACLR to 38.4dB and the EVM to 1.6% for a 10MHz 64QAM 802.16e signal at 15dBm PA output power. The transmitter has been implemented in 0.13μm CMOS and consumes 225mW including the PA.

Paper 3.7 [Samsung] demonstrates a GPS with robust interferer rejection, intended for mobile applications. An LC-tuned structure has been used to implement a narrow band pass filter for rejecting large interferer signals. The 65nm CMOS radio chip has a -15dBm blocker ICP1dB at 1710MHz while operating in the L1 band. The switching mode power supply enables low power consumption of only 23mW.

The last paper in this session, paper 3.8 [Columbia University], discusses a robust background self calibration technique to improve the receiver IIP2. The digitally assisted self-calibration loop maintains the IIP2 better than 60dB. The front-end operates at 1.8GHz and has a conversion gain of 38.5dB and a NF of 2.6dB while consuming 15mA at 1.5V supply. The chip has been realized in 0.13μm CMOS.

Highly integrated, CMOS based cellular RF solutions presented in this session demonstrated advances in robustness, reduced power consumption, digitalization and performance required to facilitate next generation systems.

Session 4 Overview / Analog

Analog Techniques

Session Chair: *Doug Smith, SMSC, Austin, TX*
Session Co-Chair: *Chris Mangelsdorf, Analog Devices, Tokyo, Japan*

This year's session on Analog Techniques presents the output of the global research community in amplifiers, references, filters, and codecs, the core topics in linear analog circuit design. The applications are varied. The performance achievements are impressive.

Our session begins with Paper 4.1 from the Delft University of Technology that exploits the thermal rather than electrical properties of silicon to produce a stable frequency reference. The absolute accuracy is +/-0.1% and a temperature coefficient of +/-11.2ppm/ºC over the wide temperature range of -55 ºC to 125 ºC.

Paper 4.2 from the University of Pavia shows how chopper correlated double sampling techniques are applied to an amplifier design to achieve an impressive offset drift of 0.03uV/ºC, while drawing only 12.8μA.

Paper 4.3 from NXP Semiconductors and Delft University of Technology presents a single-trim bandgap voltage reference with a 3-σ inaccuracy of +/-0.15%, a number which is comparable with values in other published references where multiple trims are normally used.

Paper 4 4 from Delft presents another design for a chopper-stabilized current-feedback instrumentation amplifier that extends the state of the art technique of ripple reduction.

From Broadcom we have Paper 4.5 which presents a complete audio codec in 0.13um CMOS using just 10mW of power dissipation. The codec system includes both a microphone PGA and a class-AB audio driver along with the high resolution data conversion functions.

Although class-G audio amplifiers are not brand new, Paper 4.6 from the University of Pavia demonstrates a design that smoothes the transition between the two power supplies in a class-G audio driver. With an output power of 16mW into 32Ω, the THD+N specification is better than -80dB.

The design provided from Texas Instruments in Paper 4.7 is a class-D direct battery connected amplifier in 45nm CMOS which achieves an impressive efficiency of 79% while delivering more than half a watt into 8 Ω.

Paper 4.8 from KAIST introduces a 500MHz, -3dB bandwidth amplifier in 65nm CMOS intended for use in transmitter PA polar modulation systems. The design uses a clever positive and negative feedback scheme to increase the voltage gain, as well as switched capacitor biasing of the class-AB output stage, and achieves 0.1Ω output impedance at 5MHz.

ST Microelectronics presents Paper 4.9 on the design of a 3.2GHz sample rate, 800MHz bandwidth charge based analog FIR filter in 45nm CMOS. The filter is fully reconfigurable through the use of an integrated high speed DAC.

Paper 4.10 is our final paper in the session comes from Delft University and presents a practical instantaneous companding filter technique applied to the design of a 5th order Chebyshev low pass for WLAN receiver applications. Analog non-linearities are avoided in this technique to achieve excellent intermodulation performance.

Session 5 Overview / High-Performance Digital *Processors*

Session Chair: *Stefan Rusu, Intel, Santa Clara, CA*
Session Co-Chair: *Sonia Leon, Sun Microsystems, Santa Clara, CA*

Processors have long been the leading edge of integration and process technology, and this year's papers emphatically demonstrate that this is still the case. This year's crop of processors exhibit astounding increases in chip integration levels with more cores, special function units and huge increases in the bandwidth of both on and off-die interconnect. Emerging new markets combine the attributes of network processors (many threaded low power cores) and server processors (large cores with virtualization and RAS). Higher levels of memory integration are achieved by using Embedded DRAM in these large processors to support the higher bandwidth demands on throughput computing. The challenges of managing the dramatic growth in dynamic power and leakage (if all integrated components were allowed to activate simultaneously) are addressed with a variety of innovative power management methods such as on-die gating and multiple voltage and frequency domains. Moore's law continues as the first 32nm processors from Intel and AMD are described, together with the latest architectures of the POWER and SPARC architectures.

The first paper (5.1) describes a family of 32nm microprocessors from Intel, including a dual-core configuration for client applications and a 6-core implementation for servers. Both processors implement power gates for cores, as well as a large L3 cache and global queues. The paper also presents the implementation of the first low-voltage DDR3 buffers and enhancements to the Quick Path Interconnect (QPI) buffers for the 32nm generation.

Paper 5.2 presents the next generation of CMT SPARC processors from Sun Microsystems. A 16-core SoC is implemented in 40nm enabling up to (an unprecedented) 512 threads in a 4-way glueless system, to deliver double the throughput performance in the same power envelope. The processor uses six clock and four voltage domains together with power management and circuit techniques to optimize performance, power, variability and yield across the 377mm2 die. The unified 6MB L2 cache delivers a peak bandwidth of 461GB/s. The high speed SerDes provides a remarkable bandwidth of 2.4Tb/s.

Paper 5.3 is a 648MHz 153.8mm2 CMOS SoC that integrates eight general-purpose CPU cores, four dynamically reconfigurable processors, two 1024-way matrix-processors, peripherals and external interfaces in a 45nm process. This SoC achieves 37.3GOPS/W at 1.15 V, the highest reported among comparable processors excluding special-purpose codecs. Key power reduction techniques include DDR3 latency reduction and clock buffer deactivation.

Paper 5.4 describes the POWER7TM processor from IBM. The 8 core chip supports 32 threads and is implemented in 45nm, 11M CMOS SOI technology. The 32MB of shared L3 is implemented using eDRAM, the first time this dense memory technology has been implemented in a volume commercial processor. To aid in power management, each core can run at a separate frequency appropriate to its operating mode. The processor is designed in a modular fashion with multiple voltage and clock domains controllable according to workload requirements.

New emerging markets merge networks and servers attributes to minimize power at the same performance levels. A 45nm 2.3GHz 64 thread Wire Speed Power processor (paper 5.5) provides a high level of integration combining 16 cores, accelerators, network interfaces and DDR3 I/O taking advantage of multiple power savings techniques and eDRAM caches to achieve high throughput at low power.

Paper 5.6 describes AMD's next generation implementation of an x86-64 core in 32nm technology. Key improvements with this design are related to power management and reduction, including an integrated power gate that provides an essentially zero power off state, and a digital power monitor that tracks power with 2% accuracy for use in chip level power management functions.

Continuing the trend on increasing number of cores, paper 5.7 integrates 48 IA-32 cores and 4 DDR3 channels in a 6x4 2D-mesh network. A total of 8 voltage and 28 frequency domains facilitate independent DVFS of the cores and mesh for fine grain power management. The 567mm2 processor in 45nm dissipates between 25W and 125W depending on the voltage and frequency operating point.

The last paper (5.8) introduces a 45nm high throughput 8x8 2D-mesh multi-core circuit-switched network improving power-efficiency to 1.51 Tbps/W through advanced architecture and circuit techniques such as circuit-switched transmission, circuit-switched channel queue and dual power supply providing a streaming performance of an impressive 6.43Tbps.

In summary, it's evident that any reduction in the pace of innovation, integration and capability for microprocessors is still somewhere off in the distant future. High-performance processors continue to push performance with large multi-core Systems on Chip (SoCs) providing unprecedented bandwidth, energy efficiency and core counts all with the goal to deliver more power efficient performance to their respective markets. Judging by the number of significant breakthroughs in bandwidth, threads, on-die cache integration and power management techniques present in these papers, the technological progress is only accelerating.

Session 6 Overview / IMMD

Displays and Medical Devices

Session Chair: *Iliana Fujimori-Chen, Analog Devices, Wilmington, MA*
Session Co-Chair: *Roland Thewes, TU Berlin, Berlin, Germany*

Advances in capacitive touch sensor technology, LED dimming controller for LCD backlight applications and an electronic compensation method to minimize OLED degradation are highlighted in the first three papers of this session.

The integration of display and touch sensing functions on a single panel paves the way for low-cost systems and challenges design engineers to sense small changes in capacitance in the presence of noisy display signals. Paper 6.1 [Samsung Electronics] presents a display driver with an embedded capacitive touch sensor controller using a readout compensation method to minimize the signal loss due to parasitic capacitances.

LEDs present a low-power alternative to fluorescent lamps for LCD backlight units, but their transient response is limited by the boost converter in the driver IC. Paper 6.2 [Hanyang University and Silicon Mitus] proposes a driving architecture with a double-loop control method for an LED backlight providing a 50kHz PWM dimming frequency and 8b dimming resolution.

Active-matrix OLED (AMOLED) is a leading technology for next generation displays with superior image quality and wider viewing angles compared with LCD. Some teething issues, such as image sticking and reduced lifetime, motivate the need for driving techniques to mitigate image degradation. Paper 6.3 [Ignis Innovation, London Center for Nanotechnology and Eastman Kodak] demonstrates a 32-inch HDTV AMOLED display with an electronic compensation method to minimize OLED degradation.

In the second part of this session, medical devices for neural tissue interfacing purposes and biomolecule detection are presented. A major direction in the area of neural signal recording is the trend to decrease power while maintaining signal integrity and increasing the amount of information received from such systems.

Paper 6.4 [Georgia Institute of Technology] discusses a wireless recording SoC with 32 channels for interfacing with the central nervous system. Closed-loop power control stabilizes the received power despite movements of live animals. In Paper 6.5 [University of Florida] a neural recording tag utilizing a supply current modulated analog front end is proposed. It operates at 915MHz and consumes 20μW.

Paper 6.6 [IMEC and KU Leuven] proposes a portable analog signal processor for biopotential signal monitoring. Low power consumption of 30μW is achieved by specifically adapted data-rate-reduction techniques. A 22μW implantable chip with 32 channels for EEG recording is suggested in Paper 6.7 [National University of Singapore]. System design is motivated by neurosurgical requests for epilepsy patients.

The last two publications demonstrate that a thorough system understanding allows us to optimize analog circuits for their biomedical target applications.

Paper 6.8 [Alfred Mann Foundation] considers an AC-DC converter specifically shaped for biomedical implants powered by external magnetic sources. The nominal output power is 4mW.

Finally, in Paper 6.9 [University of Texas at Austin] a comprehensive discussion concerning a CMOS array for impedance-based biomolecule detection is presented. A sensitivity of 1nA/V at 90dB dynamic range is obtained.

Session 7 Overview / Technology Directions

Designing In Emerging Technologies

Session Chair: *Satoshi Shigematsu, NTT Electronics, Yokohama, Japan*
Session Co-Chair: *Shekhar Borkar, Intel, Hillsboro, OR*

This session highlights circuit techniques for designing in new and emerging technologies such as fully depleted SOI, micro-mechanical switches, organic semiconductors, and 3D integration. Organic semiconductors are getting very popular for large area electronics due to much lower cost; however, they pose circuit design challenges. 3D integration technology with through-silicon vias is getting a lot of attention to further Moore's law, but would need careful design considerations. Researchers have proposed bold technologies such as micro-mechanical switches to replace semiconductor devices, and designing with them could be a totally different paradigm. This session presents 10 exciting papers covering design challenges to harness benefits of these emerging technologies.

Papers 7.1 and 7.2 (Stanford U, K. U. Leuven) propose the first analog-to-digital converters for mixed-signal processing implemented in organic electronics on glass and plastic substrates, respectively. The design described in Paper 7.1 uses an auto-zeroed, inverter-based comparator and on-chip calibration to achieve 6b precision in the presence of large component variations, and paper 7.2 presents a design that achieves 26.5dB precision at 500Hz, consuming only 100μA at 15V. Paper 7.3 (U Tokyo) takes economics of organic electronics to the extreme, with ink-jet printing based patterning for quick turn-around for prototyping, and especially for educational purposes. It presents the concept of user customizable logic paper (UCLP) with sea-of-transmission-gates (SOTG) of organic CMOS transistors to fabricate custom integrated circuits by printing 200μm wide interconnects with ink-jet printers.

Paper 7.4 (IMEC) addresses the biggest challenges of organic electronics, such as variability in performance, by dual-gate technology using back-gate control. It presents a comprehensive study of dual-gate organic thin-film transistors targeting robustness. It compares two logic styles: zero-Vgs-load and diode-load logic, and proposes an optimized design demonstrated with 99-stage ring oscillators and a 64b RFID transponder chips yielding data rates of 4.3kb/s. Paper 7.5 (MIT) proposes a novel temperature sensing circuit array to compensate for temperature variations in organic electronics. The array outputs an average responsivity of 6.8mV/ºC, which is 22x more responsive than the MOSFET implementation while dissipating only 90nW/cell. Highly linear outputs enable two-point calibrations to remove the effects of cell-to-cell variations.

Paper 7.6 (ASET) and 7.7 (Toshiba) take advances in organics beyond electronics into membranes and innovative packaging. They highlight capacitively coupled probing using membrane-based probe cards, and wafer-level integration of heterogeneous technologies for pseudo-SoC. Paper 7.6 presents a capacitively-coupled prober with a novel de-skewer, a low-pass filter and a weak feedback receiver to realize a membrane-based wafer-level simultaneous testing scheme, which is robust and provides more than 300K pins. Paper 7.7 presents a flexible pseudo-SoC with a new packaging technology, integrating electrostatic MEMS based grating light valves and a 40V high-speed PWM driver CMOS chip, demonstrating a wafer-level system integration technology.

Paper 7.8 (IMEC) addresses important design issues for 3D integration, such as variability, ESD, and noise, and proposes design considerations. The paper investigates key design issues of a low-cost 3D Cu-TSV technology: impact of TSV on MOS devices and interconnects, reliability, thermal hot spots, ESD, signal integrity, and circuit performance. It presents experimental verification, proposes solutions and changes to current design practices. Paper 7.9 (MIT) presents novel micro-electro-mechanical switches for analog and digital electronics. The test chip was fabricated with monolithic integration of micro-electro-mechanical (MEM) switch circuit building blocks for logic, timing, I/O and memory functions. It demonstrates experimental results with functionality for an inverter, XOR, carry generation block, oscillator, DAC, latch, and 10-cell DRAM.

Paper 7.10 (IBM) describes the benefits and challenges of fully depleted SOI for circuit design. It claims that fully depleted SOI is a viable candidate for 22nm CMOS node and beyond. It presents circuit design aspects and demonstrates that analog, I/O, and passive circuits can be fabricated in the thin silicon layer. It shows excellent device matching, gm/gds scaling to small gate length, good RF performance, and absence of history effect as the main highlights.

In summary, the session is packed with exciting papers providing valuable insights into the emerging technologies to help circuit designers.

Session 8 Overview / Wireline

High-Speed Wireline Transceivers

Session Chair: *Ali Sheikholeslami, University of Toronto, Toronto, ON, Canada*
Session Co-Chair: *Tatsuya Saito, Hitachi, Tokyo, Japan*

The demand for higher bandwidth in chip-to-chip and backplane communication is driven by the video transmission over the internet. This demand has driven the data rates to 10Gb/s and beyond. Currently, there are two approaches to address the increasing bandwidth requirement for high-speed transceivers: one is to increase the number of parallel lines while maintaining the line rate and the other is to increase the data rate per line while maintaining the number of parallel lines. The former eases the requirement for clock and data recovery, as the clock can be forwarded with small overhead. This is applicable to cases where the channel is short and linear equalization is sufficient to compensate for the channel loss. The latter reduces the number of pins on the chips and reduces the board area at the expense of more complicated equalization scheme and techniques for clock and data recovery (CDR). This is applicable to cases where the channel is long and linear equalization is no longer sufficient.

Papers 8.1 to 8.3 take advantage of feed-forward clocking so as to share this clock among all the parallel links and thereby reduce the power and area of the transceivers. Paper 8.1 from Intel presents a 47x10Gbps parallel interface that increases the power efficiency to 1.4mW/Gbps by sharing the forwarded clock among up to 28 lanes. These lanes are further grouped to share the same phase-alignment circuits. Paper 8.2 from University of Toronto uses sub-rate forwarded clock for low jitter amplification. In addition, this paper takes advantage of low power Injection Locked Oscillators (ILO) to multiply the common clock frequency and align the clock phase for each lane. Paper 8.3 from IBM Research implements a pulsed CDR with a programmable bandwidth to save power.

Multi-tap DFE is a key building block for equalizing the high frequency loss of long channels. However, for data rates above 10Gb/s, the first tap of DFE becomes the speed bottleneck. The following three papers address this problem in different ways. Paper 8.4 from NEC uses a T/H based one-tap FFE to cancel the first post-cursor ISI and relies on a three-tap DFE to remove the residue post-cursor ISIs. Paper 8.5 from STMicroelectronics uses a limiter to speed up the first tap feedback and adjusts the limiter delay to maximize the horizontal eye opening. Paper 8.8 from UCLA circumvents the first-tap timing issue with a half-rate speculative one-tap DFE.

Finally, Paper 8.6 and 8.7, jointly submitted by University of Toronto and Fujitsu Laboratories of Japan, attempt to address the equalization issues in purely digital domain. Paper 8.6 presents a fractional-sampling-rate CDR that enables ADC front-end to run at less than 2x the baud rate and thereby saving power. Paper 8.7 presents a CDR and an FFE with the ADC running at 2x the baud rate.

Overall, the papers in this session provide important steps towards satisfying the demand for higher aggregate bandwidth and higher power efficiency.

Session 9 Overview / High-Performance Digital *Digital Circuits and Sensors*

Session Chair: *Shannon Morton, Icera Inc., Bristol, UK*
Session Co-Chair: *Joshua Friedrich, IBM Austin, TX*

No one is safe from the laws of physics. State-of-the-art process scaling is creating panic in the industry, with ever increasing degrees of variability and aging effects becoming more and more of a concern. No company can risk shipping products which fail in the field, and filtering out such devices during manufacturing costs money. Investors – relax. Help is at hand. In line with the conference theme of "Sensing the Future", this session focuses on a suite of sensors and circuit techniques to extract the highest performance from deep sub-micron technologies. Armed with these circuits, designers have implemented new and innovative methods of keeping device alive in the field, and operating at their maximum performance. Furthermore, the number of processor cores integrated on silicon has risen rapidly. How best to manage them? How can they communicate effectively and at high speed? There is a need for greater intelligence and clever communication, and once again, ISSCC leads the way in unveiling breakthrough solutions, with papers from Intel, IBM, Rambus, and the University of Michigan.

Paper 9.1 addresses the time-changing performance of multi-core processors by shifting threads between Dynamic Voltage and Frequency Scaling (DVFS)-enabled cores according to their speed and leakage. As these factors vary across cores, across die, and as devices age, a (constantly changing) optimum operating point can be maintained to maximize power efficiency.

High speed processors demand low clock skew to achieve their performance/power goals. In this pursuit, resonant LC tanks have been proposed to generate low skew standing wave oscillations on wire loops. Paper 9.2 extends this LC tank approach to DLLs, generating negative delay to enable a promising approach to low-skew phase locking across multiple serialized clock domains.

Paper 9.3 presents a modular and reconfigurable clock gating design is introduced which enables both pulsed (highest performance) and master/slave (simplest) configurations to be driven, as well as tuning of the pulsed performance across process and as devices age. Furthermore, a simple design for increased flop resilience to SER is introduced for SOI technology which targets another aspect of advanced process scaling: susceptibility to high energy particle strikes.

Just like car designers (and purchasers) who never have enough horsepower in the engine, processor designers never have enough high bandwidth, low latency system interconnect. Paper 9.4 from Intel describes a massively high bandwidth ring interconnect for on-die communication between cores. Paper 9.5 from the University of Michigan further describes a repeater-less design for wire transmission using adaptive pre-emphasis and clock-less receivers which promises the ability to deliver this bandwidth at reduced power levels.

Embedded sensors in high-performance digital systems are another key area of digital circuit innovation. These sensors allow designers to better characterize and respond to deep-sub micron process effects such as oxide-wearout, NBTI, and random Vt variability. Adapting the operating point at run-time to mitigate these affects in addition to temperature and voltage changes can enable much better efficiency. Papers from the University of Michigan, NEC, Cypress, and Intel expand the state of the art in this all-important field.

Paper 9.6 showcases a manufacturable scheme for managing PVT variations and controlling the speed and power consumption of an SRAM by utilizing an on-chip microcontroller and a temperature sensor. The system varies body bias and power supplies of the memory core and periphery logic independently while occupying only a fraction of the total area.

Paper 9.7 proposes a low voltage, high sensitivity random process variations sensor utilizing an on-chip calibration circuit for improved accuracy. The proposed sensor features a replica biasing circuit which compensates global PVT variations and maintains sensitivity for robust operation. The result is very useful in fast characterization of random process variations for rapid process optimization and early yield improvement.

Paper 9.8 presents a minimally-invasive, in-situ delay slack monitor that directly measures the timing margins on critical timing signals. By operating such a sensor during runtime, margins due to both global and local variations can be observed and adapted to.

Paper 9.9 introduces a novel, in-situ approach to detecting the initial onset of oxide breakdown in large-scale circuits using the characteristic change in resistive behavior of the oxide from non-linear to linear. Measured results show robustness under temperature variation and the ability to capture the onset of failure after just 0.5% delay increase. Two 65nm test chips show that this technique has promise for detecting and managing wearout.

Finally, Paper 9.10 describes an on-chip aging monitor which has the advantages of the small area of a ring-oscillator monitor and the quick measurement time of a delay-line monitor. It offers a 10x improvement in measurement speed over prior art, allowing it to measure degradation prior to any recovery effects. At the same time, it retains a small area and strong VDD noise immunity.

The breadth of innovation presented here pursuing the goal of maintaining the pace of processor performance improvements is impressive. The huge challenges associated with implementing billion-plus transistor processors in the face of the variations and wearout issues of nanometer scale technologies are being actively worked on. The application of these key innovations will enable the trend of increased performance and efficiency to continue despite the rising challenges that process scaling presents.

Session 10 Overview / Analog
DC/DC Power Conversion

Session Chair: *Philip K.T. Mok, Hong Kong University of Science and Technology, Kowloon, Hong Kong*
Session Co-Chair: *Yoshihisa Fujimoto, SHARP, Abenu-ku, Japan*

Nowadays, power management is an essential part of the overall system design of modern highly integrated applications. Not only are strict demands placed on overall power consumption, but sophisticated control of supplies is essential for power dissipation in individual blocks. The design of dc-dc converters in these advanced power management systems is very challenging and is critical to achieving optimal operating performance as well as the overall power efficiency of the systems. These dc-dc converters are not only needed to provide a constant regulated voltage to power up individual building blocks, they also need to provide, in some cases, multiple output voltages for the complex systems or adaptive output voltages for efficiency and performance improvement. All of these goals need to be met with minimum system cost and external components. This session presents different approaches to address these issues.

There is an also increasing trend toward using digital control in DC-DC power converters for power management, as they can offer a number of potential advantages over their conventional analog-control counterparts. Two papers in this session demonstrate the robustness of these digitally-controlled dc-dc power converters. Due to the strong motivation to fully integrate the voltage conversion on chip, a fully integrated switch-capacitor dc-dc converter is an excellent alternative for low power applications. Two papers in this session demonstrate a fully-integrated switched-capacitor dc-dc power converter in 45nm and 32nm technologies.

The session starts with Paper 10.1 [HKUST] that describes a two-phase switching hybrid supply modulator for W-CDMA polar transmitters. Inherent ripple cancellation together with the on-chip feed-forward bandpass filtering technique boosts the static efficiency by 9% and dynamic efficiency by 8-12%.

Paper 10.2 [TSMC] demonstrates a fully integrated digital control DC-DC converter in 40nm CMOS. By replacing a classical analog loop with a robust digital control loop, the converter achieves a power efficiency of 90% with maximum supply current of 1A at an output voltage of 3.3V.

Paper 10.3 [KAIST] introduces a new modified bang-bang controlling technique for a single-inductor multiple-output converter. The PLL applied at the last output enables the converter to operate at a constant switching frequency with high stability.

Paper 10.4 [Qualcom, Arizona State Univ.] presents a digitally controlled DC-DC buck converter with a Analog-to-Digital Converter. By developing a highly linear frequency-domain ADC technique with a digital PWM controller, the converter achieves maximum efficiency of 94% and a regulated output voltage accuracy of 1%.

Paper 10.5 [Univ. of Arizona] introduces a highly power efficient control scheme for a high switching frequency non-inverting flyback converter. With a highly reconfigurable power stage, the converter achieves more than 80% efficiency over a wide output power range with a fast transient response.

Paper 10.6 [Univ. of Florida] demonstrates two high frequency DCM boost converters with integrated Schottky diodes in a standard CMOS process. With the digitally assisted multi-phase synchronization loop, the converters achieve higher step-up ratios and higher peak efficiencies.

Paper 10.7 [MIT] presents a completely on-chip switched-capacitor DC-DC converter in 45nm CMOS for modern wireless SoCs. By properly controlling a Digital Capacitance Modulation and a Pulse Frequency Modulation, a fast transient regulation is achieved with more than 60% efficiency.

Paper 10.8 [UC Berkeley] demonstrates a fully-integrated switched-capacitor (SC) DC-DC converter in 32nm SOI CMOS. The converter has multiple SC unit cells and is reconfigurable for optimum efficiency and high output power density.

Session 11 Overview / Wireless

Radar, mm-Wave & Low-Power Transceivers

Session Chair: *Yorgos Palaskas, Intel, Hillsboro, OR*
Session Co-Chair: *Mark Ingels, IMEC, Leuven, Belgium*

Advanced silicon technologies enable low-cost systems for emerging mm-wave applications, such as multi-Gb/s wireless communications at 60GHz, and automotive radar systems in 24 to 26 or 77GHz bands.

Paper 11.1 [Columbia University, University of Southern California], describes an emerging radar system that simultaneously transmits multiple beams with different coding, and uses correlation at the receiver to capture direct and multipath reflections from the target. A chip demonstrating this idea has been fabricated in 90nm CMOS and uses 4 channels, 4 beams in the 24 to 26GHz band.

Paper 11.2 [National Taiwan University] describes a 77GHz FMCW radar transceiver for automotive radar applications. The 65nm CMOS chip includes a 77GHz fractional-N synthesizer to generate the FMCW frequency ramp. The 1mm2 chip has been tested with external horn antennas and achieves a measured radar range of more than 100 meters.

On the multi-Gb/s communications side, Paper 11.3 [IBM, MediaTek] describes a 16-element beamformer transmitter. The single element of the transmitter delivers a P1dB of 9dBm, with an estimated EIPR of 33dBm accounting for beam-former gain. The 44mm2 chip is fabricated in 0.[illegible]m SiGe BiCMOS and consumes 3.8W.

60GHz communications requires more than 10GHz bandwidth to cover the available channels over PVT. Paper 11.4 [University of Pavia] presents a receiver integrating an LNA, VCO and two-step sliding-IF down-converter. The design uses capacitive and inductive coupling to achieve a measured bandwidth of more than 13GHz. The receiver occupies 2.4mm2 in 65nm CMOS, dissipates 75mW, and achieves a NF of 6.5dB.

Advanced CMOS processes also enable low-power transceivers for wireless sensor networks and impulse-based UWB systems for low-power communication and localization.

Paper 11.5 [Holst Centre/IMEC] presents a 90nm CMOS wake-up receiver using double-sampling envelope detection to suppress 1/f noise and offset. The resulting flat noise floor of the wake-up receiver makes it possible to trade data-rate for sensitivity while still consuming only 51μW.

Paper 11.6 [NXP, University of Twente, Delft University of Technology] describes a receiver that can be used with low-accuracy crystal-less frequency references by combining non-coherent detection with a broadband-IF and using a PPM modulation scheme. Implemented in 65nm CMOS, the circuit features burst mode LO generation employing a DCO to reduce the overall power consumption while avoiding frequency drift of a traditional VCO.

Paper 11.7 [Columbia University] presents a transceiver chip-set that includes self-synchronized OOK pulse modulation for low-complexity and low-power (200pJ/b) data detection. Three interference reduction design techniques are introduced in the receiver to achieve up to -5dBm interference robustness without external filtering.

Paper 11.8 [Purdue University, ETRI] shows a fully integrated UWB transceiver compliant with the 802.15.4a standard in 0.13μm CMOS. The transceiver uses a coherent IQ demodulator and is accompanied by a back-end IC that includes the digital baseband and AD/DA converters. The paper demonstrates a line-of-sight air channel link up to 20m with better than 18cm ranging accuracy.

Finally, Paper 11.9 [Institute of Microelectronics, Singapore] describes a 0.18μm CMOS IR-UWB SoC incorporating RF section and baseband PHY. The transmitter generates ternary coded and BPSK UWB pulses in 3 to 5GHz while the receiver employs a non-coherent demodulation scheme. The system is both for communication and localization with 15cm accuracy.

The papers in this session show the continuing increase in performance and integration for radar, high data rate, and low power wireless systems which drive low cost consumer applications.

Session 12 Overview / Technology Directions

Emerging Medical Applications

Session Chair: *Alison Burdett, Toumaz Technology, Abingdon, Oxfordshire, UK*
Session Co-Chair: *Ken Shepard, Columbia University, New York, NY*

Advances in system integration, whereby diverse technologies including sensors, actuators, signal processing and wireless connectivity are combined within millimetre-scale packaging, are enabling a new generation of medical devices for both therapeutic and diagnostic applications. This session focuses on emerging medical applications which are made possible through innovative system design and integration techniques.

The session opens with paper 12.1 (National Taiwan University), which describes the implementation and in-vivo testing of an implantable and remote-powered (battery-less) CMOS SoC for controlling back pain through low-voltage pulsed radiofrequency stimulation of the lumbar nerve. The high level of integration, combined with advanced biocompatible packaging techniques, enables implantation in rats for system verification.

Paper 12.2 (Purdue University and Texas Instruments) presents the integration of a miniaturised, low power, wireless pressure monitor for application in the diagnosis and treatment of glaucoma and cardiac disease. The system is based around a CMOS SoC which integrates wireless telemetry and powering with a MEMS sensor interface and on-chip FeRAM for data storage. The use of low-leakage FeRAM combined with low-power design techniques and duty-cycled operation leads to an average power consumption over 200,000 times less than similar state-of-the art implantable pressure monitoring systems.

A prototype implantable system for therapeutic optical nerve stimulation is demonstrated in paper 12.3 (Medtronic). The miniature system incorporates ICs for optical stimulation as well as power management and telemetry, and has the advantage over electrical stimulation systems of enhanced MRI and EMI compatibility. The optical stimulation IC is capable of delivering optical intensities and modulation patterns suitable for the treatment of chronic movement disorders such as Parkinson's disease.

Paper 12.4 (ETH) stays on the theme of nerve stimulation, describing the implementation a CMOS SoC for the stimulation and recording of neuronal networks via high density microelectrode arrays. The stimulation channels are based around a novel reconfigurable buffer architecture which can be programmed to deliver either current or voltage stimulation waveforms as appropriate. This SoC enables bidirectional access (stimulation and recording) to neuron cultures, enabling the design of closed-loop experiments which give insight into neural network structures.

The papers within this session demonstrate how CMOS scaling, combined with advances in integration and packaging technologies, is enabling a new wave of advanced medical devices for research as well as for diagnostic and therapeutic applications. These engineering advances are enabling medical researchers to gain new insights into biological systems, processes and disease.

Session 13 Overview / PLL

Frequency & Clock Synthesis

Session Chair: *Ivan Bietti, STMicroelectronics, Grenoble, France*
Session Co-Chair: *Mike Keaveney, Analog Devices Inc., Limerick, Ireland*

High-performance phase locked loops (PLLs) for local oscillator and clock synthesis are essential to all modern electronic communication systems. Advances in silicon technology, relentless market pressures to increase integration and reduce bill-of-material cost without sacrificing performance, and emerging market opportunities for increased functionality are continuing to fuel PLL research. The papers in this session represent a collection of innovations that address these issues.

The first two papers in the session present high-performance clock generators. Paper 13.1 demonstrates a fully-integrated temperature-compensated clock generator based on a bonded-on-chip MEMS resonator (in place of an off-chip crystal), corrected by a very compact fractional-N PLL. The clock generator contains new innovations that maintain stable oscillator performance over temperature, and enable very low PLL area with an on-chip loop filter. Paper 13.2 presents a highly-integrated clock generator for multi-protocol digital I/O including PCI-Express, DisplayPort, and TMDS. The work demonstrates outstanding performance based on techniques to mitigate the challenges presented by a 45nm SOI CMOS process.

The last three papers in the session present PLLs for local oscillator generation in wireless communication systems. Paper 13.3 presents a fractional-N PLL with fref/7 tuning resolution for mobile digital TV. It introduces a technique to achieve a high bandwidth-to-fref ratio by avoiding the use of delta-sigma modulation. Paper 13.4 presents a very low-noise frequency synthesizer for infrastructure applications that achieves high integration without sacrificing performance. Paper 13.5 presents a fully-integrated millimeter-wave PLL for wireless HD video transmission.

Session 14 Overview / Memory

Non-Volatile Memory

Session Chair: *Hideaki Kurata ,Hitachi,Ltd., Tokyo, Japan*
Session Co-Chair: *Roberto Gastaldi, Numonyx, Agrate Brianza, Italy*

Historically flash memory has been the dominate choice in most applications that require solid-state non-volatile memory. As applications grow, flash memory may not be the best fit from many perspectives such random access time, bit alterability, and ease of use. For example, in computer applications, improved system performance and cost can be realized by combining non-volatility, byte alterability and high performance in the same memory technology. Traditionally, slower flash memory in conjunction with DRAM has been used. In addition, flash memory is not well suited as an embedded non-volatile memory in SOC platforms due to the technology complexity and additional cost. Up to now a more expensive flash technology has been integrated into logic technologies to be used in embedded and portable applications. As a result of these needs, industry engineers and university researchers are putting increased focused in alternative non-volatile memory research, development and manufacturing. In addition to the quest for new memories, interfacing to large memory-subsystems is becoming problematic from performance and power perspectives. This drives the need for applying non-conventional design techniques to memory interfaces.

This year Non-Volatile Memory session reports on eight designs that use alternative non-volatile memories technologies in range of topics will be covered: Read Only Memory, CMOS compatible memories, and monolithic memories. Two papers in this session report on such advancements. Another paper will report on advancements in FeRAM design. To address chip interface power and performance issues, a paper will cover a wireless interface chip to address the problem. A low voltage ROM using a NAND-type array will be presented followed by two Phase Change Memory (PCM) papers. One will cover PCM implemented in a standard CMOS process and the last paper in the session will report on a monolithic PCM device that achieves the smallest cell size and highest density ever reported.

The session starts with Paper 14.1 that reports on two negative-resistance schemes for read and write in an STT-MRAM that guarantee non-destructive read by design, a fast random read/write access time and a reduced write power consumption. Advancements in circuit design applied to Spin-Torque-Transfer Magnetorestive Random-Access Memory (STT-MRAM) have resulted in faster access times, better read margin and smaller cell sizes.

Paper 14.2 describes design techniques to overcome lower currents and cell variability for higher density MRAM. An array architecture with a new reference scheme and sense amplifier design will be discussed, which improves read margin compared to the traditional approaches.

A cross-point memory array using a Conductive Metal Oxide technology is presented in the third Paper 14.3.

This work demonstrates four layers of memory fabricated above the standard CMOS layers. A select device is not needed to access a cell in the array, rather, decode bias voltage techniques are developed for both read and write.

Paper 14.4 reports on a ferroelectric capacitor overdrive technique that enables a larger read voltage on the memory capacitor without increasing stress on unselected cells in the array. This achieves a larger read signal without read disturbance. Signal-to-Noise degradation in scaling is mitigated using this technique to reduce cell size.

Paper 14.5 is a short paper presenting a wireless interface on a flash memory card. Circuit techniques are described to achieve a high speed and low power data transmission between the memory card and the host system.

Paper 14.6 is another short paper proposing a NAND- ROM based on metal programming during fabrication. 52% cycle time reduction and 55% power improvement are achieved compared to the conventional implant programmable.

Paper 14.7 reports a phase change memory built on standard CMOS process using just three additional masks. An NMOS transistor is used as the select device and the memory element is fabricated with the lower metal layers. Adequate disturbance margin allows for high read current resulting in fast random access time of 12ns. Random write throughput is 1MB/s and can be increased to 4MB/s using an alternate write mode.

The final Paper 14.8 in this session reports on 45nm 1Gb phase change memory, the highest density and the smallest cells size reported to date. The resulting die size is only 37.5mm2. A small cell size is achieved using a bipolar select device. To realize fast program and read times, the array is organized in 4Mb tiles. 16 tiles are concurrently accessed to sense 256b to achieve 85ns random access time. The write circuit is designed to force a voltage or inject a current for a write throughput of 9MB/s. The array architecture is capable of simultaneous read and write operation.

Session 15 Overview / Low-Power Digital

Low Power Processors and Communication

Session Chair: *Kees van Berkel, ST-Ericsson, Eindhoven, The Netherlands*
Session Co-Chair: *Lew Chua-Eoan, Qualcomm, San Diego, CA*

Tomorrow's smart phones will need to support multiple GHz instruction rates for their application processing, and well over 100Mb/s data rate on their cellular communication links. For all the digital processing involved, only about 1W of battery power is available. In this session we'll highlight a number of milestones towards these challenging goals.

The LTE standard specifies a maximum downlink data rate of 326.4Mb/s. In Paper 15.1 ETH Zurich describes a 0.13μm CMOS Turbo Decoder achieving 390Mb/s. At 100Mb/s it consumes only 69mW, requiring as few as 553k gates.

In Paper 15.2 ETH Zurich describes a digital baseband receiver ASIC that supports the Evolved Edge standard, requiring 32QAM demodulation and Turbo decoding. The 0.13μm CMOS baseband receiver takes only 184k gates. With a clock frequency of only 40MHz, the power consumption at 1.2V is only 20mW.

CEA-LETI from Grenoble presents a heterogeneous 3x5-core NoC-based 65nm chip (Paper 15.3) that can be run-time configured for the baseband processing for a variety of standards. They demonstrate a 4x2MIMO LTE receiver decoding 10.8Mb/s at 370mW at 1.2V.

Multi Gb/s network processors are making it into the home. In Paper 15.4 NTT describes a 90nm CMOS network processor comprising two CPUs and an IPsec offload for Residential Gateways. At 2Gb/s the IPsec function consumes only 24mW.

In Paper 15.5 Intel presents a research microprocessor in 45nm CMOS. Applying error-detection and error-recovery circuits in their RISC processor eliminates margins in supply voltage, thus achieving 22% throughput gains at 0.8V.

ARM Inc. and the University of Michigan apply the Razor technology (timing-error detecting circuits + error recovery mechanisms + voltage-frequency tuning) in an ARM-ISA processor. In Paper 15.6 they demonstrate a 52% power reduction for 1GHz operation in 65nm CMOS.

Paper 15.7 highlights a key component of the 1.4GHz dual-issue superscalar ARMv7 implementation (45nm LP-CMOS) of Qualcomm: a 13-port 64-word 41-bit fully associative content-addressable register file.

Finally, in Paper 15.8 the University of Michigan demonstrates a sensor system comprising an ARM Cortex-M3 core, two 1mm2 solar cells, a thin-film Li-ion battery, and a PMU. The self-contained 8.75mm3 system (2.1μW active, 100pW standby) achieves near-perpetual operation.

Session 16 Overview / Data Converters

High-Performance Data Converters

Session Chair: *Gabriele Manganaro, National Semiconductor, Unterhaching, Germany*
Session Co-Chair: *Kong-Pang Pun, Chinese University of Hong Kong, Hong Kong*

Recent advancements in communication systems, multimedia, consumer, medical and other applications continue driving the demand for increasingly higher-performance data converters.

Emerging communication standards enabling higher data rates and multiple services, together with the recent progress in digital signal processing, heighten the need for data converters with increasingly high dynamic range and bandwidth. This performance often comes at the expense of higher power dissipation. On the other hand, the increased sophistication of portable devices and the associated demand for longer battery life drive innovation toward ever more power-efficient data converters.

This session presents recent advancements on both of these two distinct yet broad categories of data converters.

The first two papers in this session are examples of the former category. Both are BiCMOS 16b pipeline ADCs for communication applications and feature sample rates in excess of 160MS/s. A combination of innovative circuit design techniques, enabled by advanced process technologies, delivers very high dynamic range for wideband input signals.

Paper 16.1 introduces a background calibration scheme to compensate for residue amplifier gain errors and integrates an analog input buffer. Paper 16.2 describes innovative circuit techniques including compensation for harmonic distortion otherwise introduced by the track and hold.

The next four papers focus on minimizing the energy per conversion step. Various techniques have been presented that target widely different resolutions and sample rates.

Paper 16.3 describes a novel 6b pipelined ADC with dynamic amplifiers and comparators with no quiescent current, consuming only 2.6mW at 2.2GS/s.

Paper 16.4 introduces a new delta-sigma ADC architecture using almost exclusively digital circuit elements, making it more amenable to technology scaling.

Paper 16.5 reports a low-power pipelined ADC that uses only one shared amplifier for all its three stages.

In paper 16.6 correlated level shifting and zero-crossing-comparator-based switched capacitor circuits are combined. This results in a hybrid ADC enabling high accuracy at very low power consumption.

The session ends with Paper 16.7, which describes a high-precision DAC for audio applications in a 45nm CMOS process using a cascaded digital delta-sigma modulator.

The outstanding contributions from the papers in this session clearly show how real world applications drive innovation and performance advancement in data converters to quite different directions.

Session 17 Overview / IMMD

Sensors and MEMS

Session Chair: *Makoto Ikeda, University of Tokyo, Tokyo, Japan*
Session Co-Chair: *Christoph Hagleitner, IBM Research, Ruschlikon, Switzerland*

This year's Sensors and MEMS session is closely aligned with the conference theme: "Sensing the future." Sensors are everywhere and play an increasing role in our lives. The availability of small, reliable and inexpensive sensor systems is a key component for many future information technologies that we envision today. The main challenges for such systems are: miniaturization, system integration, cost and power consumption.

This session highlights recent developments in sensors and MEMS that advance the state-of-the-art. It includes temperature sensors that set new benchmarks in terms of power and accuracy as well as removing the need for calibration. Such sensors enable smart RFID tags and facilitate the temperature compensation of inexpensive crystal oscillators. High-Q MEMS devices are emerging and the session discusses interface circuits to enable oscillators with low phase noise and accelerometers that can co-exist with vacuum-packaged gyroscopes.

The session begins with five papers on temperature sensors and their applications. Paper 17.1 [Hong Kong UST] and 17.2 [Delft U] both describe ultra-low-power temperature sensors, which achieve order-of-magnitude improvements in energy efficiency. The temperature sensor in Paper 17.1 is part of a larger SoC that realizes a single-chip passive RFID tag. Paper 17.3 [NXP, Delft U] presents the first precision temperature sensor in nanometer CMOS technology; its inaccuracy (0.2C) represents a significant improvement compared to existing designs. Paper 17.4 [Delft U] describes a temperature sensor that achieves 0.2°C inaccuracy without trimming. This will enable low-cost temperature sensing in SoCs without the extra cost of trimming. In another development, Paper 17.5 [Carnegie Mellon U] describes the use of an embedded temperature sensor to enhance the stability of crystal oscillators.

MEMS-based devices have been a key enabling factor for the realization of a wide range of silicon pressure sensors, inertial sensors and resonators. Recent research is focused on extending the frequency range of MEMS resonator based oscillators from the MHz to the GHz range, and achieving higher integration while further lowering cost. The MEMS oscillators described in Paper 17.6 [Georgia Tech] have phase noise, which begins to approach the performance of crystal oscillators. Combining MEMS accelerometers and gyroscopes in one package creates new challenges, which are met by a new interface architecture described in Paper 17.7 [Helsinki U].

Another sensing domain is addressed by Paper 17.8 [U Edinburgh]; their 3-D integration of heterogeneous LED and CMOS technologies enables an addressable matrix of high-speed optical sources for bio and medical applications.

Session 18 Overview / Low-Power Digital
Power Efficient Media Processing

Session Chair: *Raney Southerland, ARM, Austin, TX*
Session Co-Chair: *Vasantha Erraguntla, Intel, Bangalore, India*

Multi-media applications are expanding in capabilities and new application processors are required to be reconfigurable. Multi-processor capabilities increasingly include support for multiple standards, new integrations for lower power applications, and next generation video. Combining graphics and video processing are becoming state of the art and require new innovations for memory use and optimization. Portability of devices that can address video intensive applications is emerging as suitable solutions for home and industry. Use of graphics applications demonstrating HD1080p resolutions for home video systems that are driven from portable solutions is becoming mainstream. Increased usage of video in mobile applications is driving screen resolutions and video playback/record to the latest standards.

Highlighted this year are papers that combine new levels of integration along with innovations in memory use and optimization. From Toshiba we see an application processor with stacked memory that is highly integrated performing HD video decoding along with a video/audio multiprocessor. Reconfiguration fabric for DSP and media acceleration in 32nm CMOS is shown with a high level of power efficiency by Intel. The next generation MX2 from Renasas and Hiroshima University demonstrates a scalable parallel processor that has further optimizations in power and performance and has processing elements ranging from 256 to 2048.

Paper 18.1 from Toshiba demonstrates a hardware-software solution to realizing a wide range of multimedia applications in 40nm CMOS. The memory requirements are addressed by including new technologies such as a x512b Stacked DRAM.

An ultra low-voltage operation of a media accelerator achieving a maximum energy efficiency of 2.6 TOPS/W in 32nm CMOS is reported in Paper 18.2 from Intel. PVT-tolerant register file circuits are measured at 7.5 Ghz and Vcc-min improvements circuits allow for a wide dynamic voltage operating range between 320mV-1.2V.

The lowest power, scalable, advanced multi-standard video decoder with high throughput efficiency is discussed in Paper 18.3 from National Taiwan University. This is the first reported SVC/MVC/H.264 multi-standard video decoder achieving 3.4x higher throughput and 47% power improvement over earlier reported work.

Paper 18.4 from KAIST, Korea demonstrates a heterogeneous multi-core object recognition SoC with high accuracy and lowest power dissipated (345mW). It integrates a mixed-mode neuro-fuzzy logic element for visual attention and 8 SIMD and 32 MIMD processors to achieve real-time object recognition on cluttered scenes with a power efficiency of 545GOPS/W at 0.65V/50Mhz.

A highly parallel and scalable real time image processor SoC with peak power efficiency of 310GOPS/W is discussed in Paper 18.5 from Renesas. This 65nm custom implemented design achieves the smallest area and power performing object tracking in 22ms/f consuming 450mW. This is over 20X faster than a sub-CPU executing this function in software.

Paper 18.6 from KAIST, Korea discusses the first integration of a graphics and vision processor using reconfigurable elements for the two modes. Inclusion of a dedicated pose estimation engine helped achieve a 30% energy efficiency improvement over reported state-of-the-art while the pose estimation alone had a 23.8% performance improvement.

The first Semantic Analysis SoC (SASoC) that achieves 76.8Gpixels/s for video processing and 51.2Gdimensions for machine learning is reported in Paper 18.7 from National Taiwan University. The integration of video processing and machine learning as well as using power-aware frequency scaling techniques enables 1.6X - 5.9X power efficiency when compared to prior art.

Session 19 Overview / Memory

High Performance Embedded Memory

Session Chair: *Harold Pilo, IBM Systems and Technology Group, Essex Junction, VT*
Session Co-Chair: *Kevin Zhang, Intel, Hillsboro, OR*

Among all integrated circuits, embedded memory has truly become pervasive and plays an essential role in all of today's VLSI applications such as high-performance computing, low-power and ubiquitous consumer electronics. The rapid reduction of technology feature size has made it possible for integrating larger and higher performance on-die memories for various logic applications. Technology scaling also creates growing challenges for the embedded memory designer. It has become increasingly difficult to achieve aggressive density or area scaling while maintaining adequate cell margins for robust read and write operations. The degradation of intrinsic cell design margins, induced by growing device variations, has led to many innovative design solutions to overcome these challenges. Among them, advanced peripheral circuit techniques to improve read and write margins have been explored extensively with focus on more intelligent use of power supplies. On-die adaptive design techniques that automatically compensate Process-Voltage-Temperature (PVT) variations are also emerging to further improve the design robustness for high-volume manufacturing requirements. While improving and optimizing the transistor characteristics in SRAMs, 1T1C based DRAM technology (eDRAM) has made significant progress in recent years and it is successfully integrated into leading logic processes. After years of speculation, an eDRAM-based large on-die cache now has finally arrived in a high-performance microprocessor.

The first two papers from IBM describe two key embedded memory blocks for the POWER7TM cache subsystem in 45nm SOI. Paper 19.1 discloses the first on-chip eDRAM L3-cache for a Server-class processor. This 32MB eDRAM is an alternate solution to existing large 6T SRAM L3-caches. The 32MB memory is capable of operating at a 1.7ns random cycle, closing the gap to existing 6T SRAM solutions at a much reduced area. This work describes enhancements to the micro (SA) architecture that was disclosed at ISSCC in 2007. The eDRAM solution eliminates delay, area and power from the off-chip interface. The second paper features a 32kB L1 data cache with a novel scheme to provide a 2-Read, 1-Write simultaneous operation using a 6T SRAM cell. The Read/Write collision is intercepted inside the array with a write-over-read priority. An array-specific power supply enhances stability and performance while reducing the logic voltage; this is enabled with a novel level-shifting scheme.

The next paper 19.3 from Intel describes a solution to improve SRAM Vccmin using a 32nm High-K metal-gate technology. This 3.4Mb SRAM macro features a built-in stability sensor for adapting the Word-Line Up level. The sensor uses SRAM mimic cells to track PVT variations of each die. The silicon results show an improvement of 130mV of Vccmin margin and a yield improvement of 9% at a target frequency. The autonomous solution is projected to reduce test time up to 40% by eliminating die-by-die Word-Line Up level programming.

The next SRAM paper 19.4 by Toshiba features a configurable SRAM in a 32nm High-K metal-gate CMOS with a 0.149um2 cell. In order to improve write margins, a novel constant negative-level write-assist scheme is introduced. The scheme adjusts the negative bit-line level during a write operation automatically across many bit-line configurations. The measurement results have demonstrated that the cell failure rate improves by two orders of magnitude at 0.5V.

The next two papers present improvements and advancements to 8T SRAM arrays. Paper 19.5 from MIT discloses a 512Kb macro that operates down to 0.57V with a novel single-ended AC-capacitively-coupled Sense Amplifier and an embedded data retention voltage sensor in a 45nm SOI technology. The timing variations associated with low voltage operations are addressed with the AC-coupled sense-amplifier scheme. Furthermore, this scheme improves area efficiency by enabling an increase on number of cells on a bit-line compared to traditional 8T SRAM designs. Finally, the paper discloses a data retention voltage sensor that was developed to predict the mismatch-limited minimum standby voltage without corrupting the memory contents. The measurement data shows 1.2V to 0.57V operation with access times of 400ps to 3.4ns, respectively. Paper 19.6 from Intel features a 16KB 8T register-file macro in 45nm CMOS that uses on-die PVT-adaptive schemes to boost read and write word-lines for minimizing Vccmin. The adaptive schemes enables bit-cell scaling without increasing device sizes. Hardware results indicate a 6-27% reduction in power using a single supply solution.

Paper 19.6 introduces a novel method to characterize SRAM read and write margin distributions using tunable bit-cell-based ring oscillators. A 45nm test chip demonstrates ring-oscillator frequency that can be correlated to static current noise margin, cell read current, and write-ability.

The final paper 19.8 from Renesas discloses a 0.5V 6T SRAM in 90nm PD-SOI that features asymmetric Pass-Gate NMOS devices to enhance the read and write margins. The design further adopts a forward-bias technique to the body of the bit-cell and peripheral circuits. This is enabled by a low area-overhead body-contact feature in this SOI technology. The measured minimum operating voltage of this proposed SRAM is 0.45V, a 100mV improvement compared to the conventional approach.

Area, performance and power scaling of high performance embedded memory will continue into the nano-technology regime. Innovations in autonomous and PVT-adaptive assist features as well as novel sensing techniques will enable the scaling. The use of multi-power supply memory domains will also continue to enable high-performance memory scaling.

Session 20 Overview / Wireline

Next-Generation Optical and Electrical Interfaces

Session Chair: *Michael Green, UC-Irvine, Irvine, CA*
Session Co-Chair: *Daniel Friedman, IBM, Yorktown Heights, NY*

Extending performance in applications from networking to storage to traditional computing increasingly demands advances in communication interface design. In order to meet these demands, tighter integration of optical and electrical components, dramatically improved electrical link power efficiency, and increased serial data rates all play critical roles.

A key challenge for future backplane interconnect continues to be delivering high data rates over increasingly difficult channels under stringent power constraints. With efficient electrical-optical conversion, integrated silicon photonics offers a path to dramatic channel improvement via the replacement of electrical with optical interconnect, potentially enabling future optical backplanes. As I/O requirements begin to be measured in Tb/s for electrical backplane and chip-to-chip applications, improving area- and power-efficiency is an absolute necessity. Looking ahead, enabling 100 Gb/s links is a key milestone for future wireline systems.

This session presents papers describing advances in integrated optical communication, link power efficiency, and link throughput. The optics-related papers describe two approaches to realizing integrated photodetectors and associated amplifier chains. Power efficient approaches for burst-mode CDRs, backplane transceivers, and chip-to-chip I/O are also presented, including a design achieving power efficiency better than 1mW/Gbps. Finally, a realization of a high speed deserializer, a key element of future ultra-high data rate systems, is described.

The session starts with paper 20.1, from Luxtera, which describes a low power optical receiver realized using an integrated germanium photodiode within an SOI CMOS process and circuit techniques including hybrid peaked amplification stages. The receiver consumes 15 mW, achieving a sensitivity of 6 μA p-p at a BER of 1e-12 and low jitter.

An alternative approach to integrated optical receiver design is explored in Yonsei University's paper 20.2. In this paper, the bandwidth limitations of a photodiode realized in a standard CMOS process are compensated using a compact, adaptive equalization filter, enabling 8.5 Gb/s operation.

Paper 20.3, from Sony, describes a significant advancement in burst-mode CDR performance, achieved through the use of a novel dual-edge injection locked oscillator. This design achieves wide range continuous-rate capability (1.296-5.184 Gb/s), locking within 20 bits, all at a power efficiency of 2.4 mW/Gbps.

Paper 20.4, from Intel, describes the most advanced 32nm CMOS backplane equalizer reported to date. This power efficient design includes transmit equalization, receive linear and decision feedback equalization, and a baud-rate CDR, and successfully recovers data to 11.8 Gb/s transmitted over channels with 25dB of loss at half-baud.

Hitachi's paper 20.5 reports, for the first time, a transceiver for chip to chip interconnect with power efficiency better than 1mW/Gbps. Key techniques used in this 12.5 Gb/s transceiver enabling achievement of this efficiency milestone include an edge-rate enhanced low-swing transmitter, resonant clock distribution, and a symbol-rate CDR.

A flexible, power efficient (4.32 mW/Gbps) source series terminated (SST) transmitter design operating to 7.4 Gb/s is presented in paper 20.6 from Rambus. By introducing a digitally controlled shunt path across the output, a significant reduction in transmitter complexity as compared to state-of-the art SST designs is achieved, simultaneously enabling multi-protocol support, swing control, and fine-grain equalization control.

Reconfigurability is taken to new heights in Intel's paper 20.7, which reports a multi-application 5-25 Gb/s, 1.6-3.8 mW/Gbps transceiver. Supported operating modes range from single-ended 2/3/4 PAM signaling, intended for on-package channels, to differential voltage or current-mode signaling, for more difficult backplane channels.

Finally, paper 20.8, from National Taiwan University, explores ways to realize a high-speed deserializer, a component relevant to future 100 Gb/s transmission systems. This design takes as inputs two 25 Gb/s data streams and produces five 10 Gb/s outputs.
This session presents work ranging from paving the way to integrated photonics to breaking the 1mW/Gbps power efficiency barrier, as well as extraordinary advances in reconfigurability for backplane and chip to chip applications. The advances reported here will be crucial to realizing a broad range of high performance systems of the future.

Session 21 Overview / Data Converters

Successive-Approximation ADCs

Session Chair: *Un-Ku Moon, Oregon State University, Corvallis, OR*
Session Co-Chair: *Tatsuji Matsuura, Renesas Technology, Takasaki, Japan*

For many years, successive-approximation ADCs have been the standard architecture for very-low-power and low-speed applications. For moderate-to-high speed applications, other ADC structures such as flash and pipeline have been traditionally the architecture of choice. However, in the recent past, the increasing speed of devices in scaled CMOS technologies has enabled successive-approximation ADCs to penetrate the medium-to-high-speed application domains. Additionally, the lower intrinsic gain of transistors and opamps in scaled CMOS has made the successive-approximation structures more appealing, because in most such implementations an opamp is often not required. Therefore, much recent research activity has been invested in this type of ADCs. In this session, newest advancements in SAR ADCs that push resolution, FoM, and/or speed to the next level are presented.

The session includes 7 papers. The first paper presents a high-performance ADC in terms of resolution. In this paper (Paper 21.1), designers from Analog Devices present a SAR ADC that achieves a benchmark performance of 18b at 12.5MS/s.

The next 5 papers present a variety of state-of-the-art best-in-class FoM implementations of SAR-based ADC structures. In paper 21.2, researchers from University of Illinois at Urbana-Champaign present a SAR ADC that incorporates a perturbation-based digital calibration technique to achieve an ENOB of close to 12b. Paper 21.3 from Toshiba demonstrates a 40MS/s 10b SAR ADC in 65nm CMOS that is intended for WLAN applications. The ADC achieves an ENOB of 8.9b while consuming 1.21mW from a 1.1V supply. Paper 21.4 from Fujitsu Laboratories presents a 10b 50MS/s SAR ADC that incorporates on-chip calibration techniques to achieve an excellent FoM of 30fJ/conversion-step. In Paper 21.5 researchers from National Cheng-Kung University and Himax Technologies describe a 10b 100MS/s SAR ADC that achieves an outstanding FoM of 15.5fJ/conversion-step while stepping well into the domain that was previously dominated by pipelined ADCs. Paper 21.6 from IMEC presents an 8b variable sampling rate SAR ADC that has the unique feature of maintaining its excellent FoM approximately constant (~30fJ/conversion-step) over 3 decades of operating sampling frequency, namely from 10kS/s to 10MS/s.

Finally, Paper 21.7 from Nortel concludes the session by presenting yet another impressive performance in terms of speed. This paper describes an interleaved 6b SAR ADC architecture that achieves 40GS/s performance, a speed that was previously considered mainly the domain of flash ADCs.

Session 22 Overview / IMMD

Image Sensors

Session Chair: *Shoji Kawahito, Shizuoka University, Hamamatsu, Japan*
Session Co-Chair: *JungChak Ahn, Samsung Electronics, Yongin, Korea*

The imaging area is one of the most exciting and dynamic areas of the electronics industry, the pervasion of imaging into society was boosted significantly when it was included inside most mobile phones and although this a huge driver of the industry, there are still new applications that arrive to continue to push the growth and innovation of the technology. This session highlights advances in Image Sensors in several areas, including readout circuitry, pixels, and applications.

The opening paper (22.1) shows the first fully-integrated column-parallel delta-sigma analog-to-digital converter (ADC) for high-speed high-definition CMOS imagers. The 2.1Mpixel 120frames/s CMOS imager with column level second order delta-sigma modulators and decimation filters achieves a read noise of 1.9 e- while dissipating only 180mW. Paper 22.2 presents a column-parallel processing technique for reducing read noise in high-definition CMOS imagers. The noise reduction technique uses multiple-sampling and digital averaging to reduce the sensor noise to 1.1e- without additional circuitry.

Paper 22.3 presents a low-noise CMOS image sensor with true global shutter. Dual-shutter and single-shutter modes are supported by including a pinned storage diode next to a pinned photodiode. High transfer efficiency is achieved by using two different doping layers in the storage and photodiodes respectively. The 7.5 x 7.5μm2 pixels have 25% fill factor. In dual-shutter mode, a dynamic range of 93dB is achieved. In single shutter mode a read noise of 2.7e- is achieved with high shutter efficiency of 99.7% and a dynamic range of 57dB.

Paper 22.4 introduces a QVGA CMOS image sensor array of asynchronous autonomous 30 x 30μm2 pixels with 30% fill factor. Each pixel individually detects changes in illumination and outputs new gray-levels only after a change is detected. This redundancy suppression results in efficient loss-less video compression. The concepts supports correlated double sampling. An intra-scene dynamic range of 125dB at 30fps was achieved.

Paper 22.5 describes a CMOS image sensor that simultaneously captures imagery and optical data. The sensor consists of an array of 642x480 7.5 x 7.5μm2 pixels. Half of the array is used to capture imagery and the other half is used to receive optical data, where the imaging and communication pixels are interleaved between odd and even columns. At 70 meters the communication channel can operate at up to 10Mbits per second.

Papers 22.6 and 22.7 describe CMOS image sensors that collect 3 dimensional range maps. Paper 22.6 uses a light selection method to measure range and can capture 14k range maps per second using an array of 256 x 256 12 x 12μm2 pixels. This work represents a 10 times higher 3D map rate than pervious work with a modest increase in pixel area. Paper 22.7 demonstrates an optical time of flight sensor using a lock-in pixel that measures the phase difference between the transmitted and received illumination. The sensor uses a 0.18μm CMOS process to reduce the pixel size to 10 x 10μm2 and increases the lock-in frequency to 50MHz.

Decreasing pixel sizes continuously requires innovations in pixel design, technology and system concepts. Paper 22.8 introduces an 8Mpixel 2.2/3-inch RGGB color image sensor that supports a dual resolution and exposure technique. In low-light conditions, the sensor can switch from full-resolution progressive scan readout to a high-sensitivity mode where the green pixels are read out only once every four frames. This functionality is introduced by using two sets of transfer gates in the pixel array. In the high-sensitivity mode, the off-chip image processing uses the motion information from the red and the blue pixels to minimize the impact on resolution and motion blur. Paper 22.9 presents a backside-illuminated 1/2.3-inch 10.3Mpixel 50 frames/s CMOS image sensor. The 1.65 x 1.65 μm2 pixels use a 4-shared-pixel floating diffusion boost circuit. The backside approach maintains 85% response at 15 degrees off normal. A deep p-implant is used as an isolation barrier to improve the pixel separation. A sensitivity of 9890 e-/lux.s is reported. The sensor includes a 10b/12b ADC, an internal PLL and a 10b serial LVDS interface to enable a data-rate up to 576MHz.

Session 23 Overview / RF

mm-Wave Tranceivers, Power Amplifiers and Sources

Session Chair: *Michael Zybura, RF Micro Devices, San Jose Design Center, San Jose, CA*
Session Co-Chair: *Santoshi Tanaka, Renesas Technology Corp., Komoro, Japan*

The last several years have witnessed a dramatic increase in silicon-based IC system implementation at millimeter- and sub-millimeter-wave frequencies (e.g., 24GHz-3THz). There are numerous opportunities and challenges for applications such as gigabit wireless communications, sensing, ranging, and imaging in this regime. This session explores the most recent developments in mm-wave applications of silicon and offers a broad set of solutions for communications, radar, imaging, and security in this quickly-emerging and exciting area of integrated circuit design.

Continued demand for ever increasing bandwidth has stimulated advancements in mm-wave communications. These systems can be employed across a variety of applications including short-range distribution of broadband audio-video, high speed networking, and even intra-platform, inter-chip communications. Ever smaller geometry CMOS facilitates a merging of electromagnetic techniques with high speed transistors to create new methods for transmission and detection. IC designers are leveraging the inherent speed of scaled CMOS while overcoming the inherent problems associated with advanced processes, such as low breakdown voltage, small intrinsic gain, limited output power capability, and higher parasitic resistance. This year W-band (60-110GHz) power levels have surmounted water molecule absorption to meet the requirements of automotive forward looking radar applications.

The session begins with paper 23.1 from the Sony in collaboration with Caltech. A 56GHz architecture is described to enable inter-chip communications at greater than 10Gbps. The system employs a self-locking receive sections which attains 6.4pJ/bit efficiencies in 40nm CMOS.

A 160GHz quadrature transmitter and receiver chipset from the University of Wuppertal in Germany, is demonstrated next in paper 23.2. The transmitter chip achieves 5dBm of output power from an integrated VCO, prescaler, tripler and amplifier chain, while the receiver yields a system NF of 11-14dB.

Paper 23.3 is a W-band transmitter from the Helsinki University of Technology. The transmitter chain realizes the highest 95GHz CMOS-based output power, widest RF, LO and IF bandwidths yet reported.

From UC Berkeley, the University of Padova and STMicroelectronics, a fully integrated 90GHz carrier pulsed transmitter with integrated antenna is demonstrated in paper 23.4. The benefits of hybrid PA/antenna switching are explored to achieve greater than 30GHz of bandwidth. The transmitter generates variable carrier-modulated pulses with a minimum pulse width of 35ps.

Paper 23.5 shows a 115GHz frequency multiplier based on an injection-locked Pierce oscillator from the Universities of Modena and Pavia in collaboration with STMicroelectronics. The 65nm CMOS source exhibits an outstanding 13% tuning range with phase noise of -107dBc/Hz at a 10MHz offset using only 12mW.

A novel 65nm CMOS differential power combiner is demonstrated in paper 23.6. A MediaTek and IBM cooperation, this 1V PA provides a P1dB of 15.4dBm of power at 61.5GHz with a power added efficiency of 11.7%.

In Paper 23.7 from UC Davis, a 60GHz 90nm CMOS power amplifier is presented which achieves 20dB of gain, and a P1dB of 18dBm from a 1.2V supply. The design employs three two-way Wilkinson power splitters for amplification and an adjoining three two-way Wilkinson structure for power combination.

STMicroelectronics, ST-Ericsson and CEA/LETI-MINATEC present a 53-68GHz power amplifier in paper 23.8. An eight-way power splitter and combiner achieves 18dBm of power from a 1.2V supply in standard 65nm CMOS.

A striking example of what is achievable in the THz regime is shown in paper 23.9. From the University of Wuppertal, a 650GHz SiGe-based imaging receiver is presented. An integrated LO driver, sub-harmonic mixer and antenna provide a 30GHz bandwidth, -13dBi of conversion gain and a 42dB NF.

Session 24 Overview / Memory
DRAM and Flash Memories

Session Chair: *Ken Takeuchi, University of Tokyo, Tokyo, Japan*
Session Co-Chair: *Nicky C. C. Ku, Etron Technology, Inc., Hsinchu, Taiwan*

This session combines DRAM and NAND Flash memory papers which are the two working horses of the memory industry. Some of the exciting advances that have allowed the adoption of these advanced memory technologies in a variety of consumer electronics will be revealed in this session. More and more of these systems are using both DRAM and NAND in their memory sub-systems and in many cases require close coordination between the interface designs of the two memory types.

Previously published DRAM full chips emphasized high capacities up to 4Gb, fast performance at 7Gb/s for a 1Gb GDDR5 chip, and low power below 8.7mW/Gb/s for a 1Gb LPDDR2 chip. Instead, this year the two DRAM chips presented first were designed more specifically for application needs with emphases on both enhancing system performance and power saving for customers. Both chips are generating new records in performance for different applications such as game consoles and mobile phones.

In Paper 24.1, by improving the bank-to-bank active time to 2.5ns and allowing consecutive accesses to the banks in a bank group the flexibility of memory access for the GPU was significantly improved. The graphic system performance is boosted resulting in higher 3D resolution and more lively gaming action.

The fast growing mobile system applications demand DRAMs with extremely low power consumption as well as high bandwidth, which may not be achieved by using conventional approaches such as mobile DDR and LPDDR2. Paper 24.2 presents a 1Gb Mobile DRAM with very wide I/O up to 512 bits to achieve a 12.8GB/s data rate at 200MHz, which is 4× faster than LPDDR2 at 400MHz, but still consumes similar power.

In graphic applications such as video cards and game consoles, the required bandwidth between GPU and DRAM is increasing 10× every 5 years. Instead of conventional wire connections, Paper 24.3 demonstrates an inductive-coupling interface technology, improving bandwidth, energy consumption, and layout area.

As DRAM cells are further scaled down, the signal-to-noise ratio will be degraded. Paper 24.4 proposes a new sensing scheme to compensate the array noise by 85%. The techniques can be extended for use in denser cell structures.

NAND memory papers presented this year are all based on 30nm technology. They are all 32Gb densities, two of which are 2b/cell while one is 3b/cell. As cost determines the success or lack thereof in this industry, there is fierce competition for most innovative products that provide value to the consumers at the lowest cost; that translates into highest density at the most advanced lithography node.

Paper 24.5 discusses stacking of 128 NAND memory chip dies on top of each other in a staircase topology and uses an inductively coupled technology that allows the memory controller to communicate with random NAND chips in the stack. With the advent of SSDs and the use of large numbers of NAND chips, using this scheme allows for a lot more condensed packing of NAND devices, a lot fewer bonding wires as well as lower power consumption.

Paper 24.6 discloses a 32Gb, 32nm 2b/cell chip using all-bitline technology. The NAND chip optimizes die size by placing the Page Buffer and X-decoder on one side of the array. To reduce the floating-gate coupling, the chip uses a dual-pulse program algorithm. A high performance of 200MB/s is achieved using a DDR interface.

Paper 24.7 reveals a 126mm2, 3b/cell, 32Gb NAND device using 34nm technology operating at 6MB/s. The device is dynamically configurable to 2b/cell, which can operate at 13MB/sc using a Quad-Plane Architecture. The chip utilizes a high-resolution analog system as well as a RISC processor with dedicated NAND instruction set for advanced algorithms.

Paper 24.8 discloses another 32nm, 32Gb NAND device at 146mm2. This paper introduces innovative algorithms for the floating-gate-to-floating-gate interference cancellation and the moving read reference voltage scheme for successful program operations and improved retention. Reduction of power consumption is achieved by use of adaptive coding of the input data.

Session 25 Overview / Wireless

Wireless Connectivity

Session Chair: *Arya Behzad, Broadcom, San Diego, CA*
Session Co-Chair: *Masoud Zargari, Atheros, Irvine, CA*

Portable devices of the future are required to integrate an ever-increasing number of wireless functions in a constantly shrinking area and with continually decreasing power consumption budgets. In order to accommodate this goal, wireless communication platforms will be required to support multiple functionalities as well as multiple standards for each function. While advanced CMOS processes allow for higher levels of integration by providing significant area scaling to digital circuits they impose certain challenges on the radio design. Innovations at the circuit level as well as radio architecture are needed to address these challenges.

A variety of different wireless radios that cover multiple standards are presented in Session 25 including WLAN, WiMAX, Mobile TV, Bluetooth and FM. In addition several novel ideas that allow for more robust and area efficient transceivers are introduced.

The session begins with a highly digital receiver frontend in 40nm CMOS technology. Paper 25.1 [Audax Technologies] places two A/D converters immediately after the mixer. All other receiver functions including filtering, offset compensation and VGAs are implemented in the digital domain. The proposed receiver occupies only 0.07mm2.

Paper 25.2 [Broadcom] presents a 65nm CMOS PA with distributed LC power combining and improved linearity. The PA produces a saturated output power of 31.5dBm and has a peak PAE of 25% while running from a 3.3V supply. Multiple linearization techniques has allowed for an EVM of -25dB at 25.5dBm output power for the 2.4GHz band.

Paper 25.3 [Broadcom] pushes the state-of-the-art level of integration to a new level by combining WLAN, Bluetooth (BT) and FM radios on a single SoC in 65nm CMOS. The receivers of WLAN, BT and FM achieve sensitivities better than -76dBm (54Mbps/2.4GHz), -91dBm and 1μVrms respectively. The WLAN and BT transmitters achieve linear output powers of 21dBm and 10dBm respectively.

Paper 25.4 [Toshiba] describes a fully integrated 2x1 dual-band direct-conversion transceiver for a mobile WiMAX SoC in 65nm CMOS. Inductor-less LO distribution by compact dual-mode fractional dividers are introduced. A 3.8dB NF is achieved by utilizing a novel noise-shaping trans-impedance amplifier. It consumes 214.8mW while transmitting a 1dBm output power and 214.1mW while receiving on both receivers.

Paper 25.5 [IMEC] presents a 5mm2 digital CMOS multi-standard transceiver in 40nm CMOS. The 0.1 to 6GHz receiver features 4 LNAs, 25% passive mixers with IIP3 calibration, 5th order baseband filtering and a 50fJ/conversion step ADC while the 0.1 to 6GHz transmitter integrates baseband filter, voltage sampled mixer and PA driver.

Paper 25.6 [Analog Devices] covers a 65nm multi-standard, multi-band mobile broadcasting receiver that integrates DAB/T-DMB, ISDB-T 1seg and FM. The SoC consists of analog front-end, power management and demodulator. It has a power consumption of 35mW and a die size of 2.9x2.9mm2.

Paper 25.7 [Samsung] introduces a multi-standard, multi-band mobile TV SoC which integrates RF tuner, demodulator, FEC, hardwired MPE-FEC, ARM CPU and SRAM. Implemented in 65nm CMOS it occupies 23.2 mm2 of silicon.

Finally, Paper 25.8 [CSEM] integrates a 150mA/MHz DSP with two MAC per cycle instructions and a configurable 863-928MHz RF transceiver in 018□m CMOS. The chip consumes 3.5mW in continuous reception, 40mW while transmitting 10dBm output and 1uA in sleep mode while running on a 32KHz RTC.

As it is apparent from the papers presented in this session, we are well on our way towards the future of wireless connectivity!

Session 26 Overview / PLL

High Performance & Digital PLLs

Session Chair: *SeongHwan Cho, KAIST, Daejon, Korea*
Session Co-Chair: *K.R. (Kumar) Lakshmikumar, Ikanos Communications, Red Bank, NJ*

Phase-locked loop (PLL) is an essential component in many wireline and wireless applications for clocking and frequency synthesis. The relentless increase in system complexity coupled with process scaling calls for novel techniques for low-noise and low-spur performance. This session presents eight papers that explore innovations in all-digital and sub-sampling PLLs. A common theme in all digital PLLs is to improve the linearity and resolution of the time-to-digital converter (TDC). Seven of the eight papers in this session address this issue.

Paper 26.1 [Columbia University, STMicroelectronics, Univesita degli Studi di Pavia] describes a wide-bandwidth fractional-N PLL with low noise and spur. The effect of TDC non-linearity is significantly reduced with dithering technique in conjunction with feedforward calibration that ensures that the in-band noise is minimally affected.

A low-power low-noise all-digital PLL with 2-step TDC is presented in Paper 26.2 [NEC]. Power consumption is reduced by employing a time-windowed single-shot pulse controlling scheme that minimizes the signal transitions in the TDC.

Paper 26.3 [Atheros] demonstrates an all-digital fractional-N PLL that exploits the multi-phase output of the ring-DCO for enhanced time-resolution without requiring any calibration techniques.

Paper 26.4 [University of Twente] describes a spur-reduction technique for a low-noise sub-sampling PLL. It employs a DLL/PLL dual loop architecture that aligns the reference edges to the zero crossings of the VCO to significantly reduce the reference spur.

A TDC with linearization along with a mismatch cancelled phase-interpolator is described in Paper 26.5 [Politecnico di Milano] to realize a wide loop bandwidth and yet low in-band fractional spurs.

Paper 26.6 [Infineon Technologies] addresses the TDC linearity issue by using the multiphase output of a digitally controlled ring oscillator. When in lock the phase quantization error is a deterministic fraction of the clock period across PVT corners.

A digitally intensive design is reported in Paper 26.7 [IMEC]. A 2-step background calibration enables a TDC with 5ps resolution. The PLL in 40nm CMOS can cover a wide frequency range from 86MHz to 12GHz.

The sub-exponent TDC reported in Paper 26.8 [POSTECH] is based on a self-calibrated chain of time amplifiers. A resolution of 1.25ps in 0.18□m CMOS is achieved.

The architectures and circuit innovations presented in this session will encourage researchers and engineers to invent newer techniques to enable much higher performance PLLs that exploit advancements in CMOS process technology.

Session 27 Overview / Technology Directions

Directions in Health, Energy & RF

Session Chair: *Hélène Lhermet, CEA-Léti, Grenoble, France*
Session Co-Chair: *Bill Bidermann, BK Associates, San Diego, CA*

Improvements in semiconductors translate quickly into improvements in human health care, energy conservation, and high frequency communication. The reduction in size and power of diagnostic and health monitoring equipment demonstrates the impact of these trends. Efficiency improvements in electronics and harvesting of ambient energy in many forms increasingly allow ubiquitous electronic monitoring. Networked communication across the world, across the room or across the human body; all these are offshoots of increased awareness of power use coupled with novel communication methods.

The first half of this session describes contributions to human health and increasingly efficient use of ambient energy. The first paper, 27.1, describes a system capable of producing 10-100 microwatts of regulated 1.8V power. The power is harvested from human body heat in a chip implemented in a 0.35µm CMOS process. Following the trend of efficiency and miniaturization, paper 27.2 chronicles an NMR system more than 1000X smaller than and 150X more sensitive than existing commercial systems. The paper describes a single chip NRM system that detects hCG cancer markers and bladder cancer cells. Paper 27.3 describes an SoC that concurrently monitors two cardiac functions, ECG and Thoracic Impedance Variance, a proxy for blood flow and volume. Consuming only 3.9mW, the configurable system with flexible battery can be applied as a poultice-like plaster. The theme of medical advances continues in paper 27.4 that describes an all-electrical approach for fast genetic testing. A standard CMOS process SoC is paired with a microfluidic cartridge to allow multiple genetic letter to be identified. This system delivers a result within 3 minutes. The last paper before the break, 27.5, describes a system that harvests energy from all available sources. Utilizing an external piezoelectric source, the 2um BiCMOS energy scavenger circuit produces up to 30uW with a loaded efficiency in the 40-50% range.

The second half of this session comprises five papers that cover a range of topics in communication and RF. Paper 27.6 describes a transceiver used in a 1meter fabric link. Consuming only 110uW, the transceiver utilizes a supply-rail-coupled differential signaling scheme for communication in a body area network at 10Mb/s. Utilizing 0.18µm CMOS, paper 27.7 describes a 2.4GHz transmitter architecture that exploits the use of a SSB up-converter mixer, power amplifier and bulk acoustic wave resonators to achieve spectrally clean output power of 5.4dBm. The chip consumes 42mW from a 1.2V supply. This is followed by a description of the first fully integrated electrical mode-locked oscillator in paper 27.8. An on-chip transmission line and a lumped amplifier lock the different harmonics to produce a pulse train of 42ps pulses at 8.6GHz. The oscillator is fabricated in 0.13µm SiGe BiCMOS. The penultimate paper, 27.9, uses a 90nm digital CMOS process to perform clock and data recovery using ambient optical energy. Utilizing a sub .5volt supply, the chip contains integrated photodiodes and diffraction gratings at 4600lux to power data recovery at 50kbps using ~300nW of harvested power. Paper 27.10 that concludes this session returns to the energy harvesting arena, describing the harvesting and accumulation of energy from for vibration sensing. The 2mm x 2mm chip both harvests energy and senses vibration utilizing circuit techniques requiring less than 1nW of power.

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RFID Gets All the "Buzz"

Researchers in both the health- and life-science communities continue to seek new methods for monitoring subjects in a wide variety of applications from research on global warming, to studies involving the behavior patterns of animals, to the real-time observation of ambulatory human patients. The common theme of developments in this area is ultra-low power communications, allowing long-life autonomous operation using either batteries with multiyear lifetimes, or energy-scavenged sources of power, such as solar cells. Moreover, these monitoring applications demand exceptionally-small form-factors, and minimal weight, to allow use in unobtrusive life-science studies on subjects as small as an insect.

ISSCC 2010 will showcase an exciting application of a highly-integrated ultra-low power 900MHz RFID transceiver used for research in the biological community. A 0.13µm CMOS transceiver, implemented by engineers at the University of Washington, illustrates the use of small-form-factor transceivers in the study of Manduca Sexta (Hawkmoth) **[2.8]**. This state-of-the-art wireless chip dissipates 9.2 µW of power and realizes a novel on-chip self-calibrating 260nA temperature-compensated frequency reference, sub-threshold digital logic, a 1.2µA fully differential low-noise chopper-stabilized amplifier/ADC for sensor interfacing,, and a unique chip-ID generator. Two orders of magnitude reduction in power is obtained with respect to existing state-of-the-art RFID tags.

The low weight of the complete sensor system, which weighs only 0.35 grams, enables researchers to mount the entire system on the posterior side of a Hawkmoth, allowing the remote recording its in-flight core body temperature. Since the Hawkmoth is quite small (with a 3 to 5" wing span), this experiment may serve as a watershed achievement in the area of biological- and medical-sciences directed toward research in diverse areas, ranging from animal behavioral-pattern studies, to real-time health monitoring of human outpatients.

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CMOS Reaching the Impossible in Wireless

Modern mobile smart phones allow the user to be connected to the internet at all times using the high data rate provided by 3G standards, especially those capable of HSPA (high-speed packet access) and beyond. As 3G makes its way to the largest mobile markets, lower-cost radio chips are required. This can be achieved by implementing the required radios in advanced low-cost CMOS technologies with very-high levels of integration.

At ISSCC 2010, a session on "Cellular Techniques" will demonstrate the advancement of radio implementations in CMOS technologies. In one area, the aggressive push to drive down the cost of high-speed standards, such as Evolved-EDGE and 3G, is evident with the highly-integrated CMOS transceivers being demonstrated by engineers from Advanced Circuit Pursuit, Switzerland. These devices remove the need for external SAW (surface acoustic wave) filters, and integrate the DC-DC switching regulator to allow direct connection to the battery **[3.1, 3.3]**. To further reduce the cost of devices using the 2.5G GSM/EDGE cellular standard, Texas Instruments will describe an all-digital transceiver with a very-small die area that is integrated with the digital baseband and multi-media processor in 65nm CMOS **[3.2]**. In another area, advances in cellular-phone techniques allow additional cost reductions of CMOS transceivers for future applications: Engineers from Nokia and ST-Ericsson reveal an innovative Δ-Σ ADC capable of directly digitizing radio-frequency signals, targeting more-programmable radios implemented in advanced CMOS technologies **[3.5]**.

The adoption of these innovative cellular-phone techniques in conventional low-cost CMOS technologies will ensure future advanced wireless devices will cost less than ever before, enabling their continued widespread adoption around the world.

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The Dead Have Risen – Analog Marches On!

Two basic problems confront the analog world as we move on to more advanced nanometer process technologies: First, while tiny CMOS transistors (which form the backbone of digital electronics) are easy to integrate in large numbers and are very fast, they are not well suited for precision-measurement operations. Moreover, compared to their older bipolar cousins, MOSFETs are subject to random offsets and large amounts of low-frequency noise that only gets worse as the process scales to smaller geometries. Second, the tiny, ever-shrinking geometries of the modern transistor make them quite weak and unable to handle high voltages. How, then, can we drive real world loads like speakers, displays, and cell phone antennas?

At ISSCC 2010, an entire session on Analog Techniques **[Session 4]** will present some dramatic advances on both of these basic fronts: First, high-speed MOSFETS are made to do precision work by using a switching technique called "chopping". Periodic reversal of the signal polarity causes all of the low-frequency imperfections of the circuitry to appear as high-frequency errors that can be filtered out. While this simple chopping idea is not new, it has been taken to remarkable new levels of sophistication in the latest research. Errors that formerly would have been as high as 10mV are driven down to the 1μV level, 10,000 times smaller! This enables a whole new level of precision measurement and control to be conducted on low-cost highly-integrated ICs, as demonstrated by researchers from the University of Pavia **[4.2]**, and Delft University of Technology [**4.4]**.

The second major area of advance at ISSCC 2010 is power handling. In one example, engineers from Texas Instruments, India, will describe a speaker driver capable of delivering half a watt of power into a standard 8Ω load, using 45nm CMOS **[4.7]**. Another example is provided by a collaboration between researchers from the University of Pavia and Marvell, Italy, who present a sophisticated class-G driver for headphones in 65nm technology, which consumes only one third of the power of previous amplifiers **[4.6]**.

Behind these breakthroughs is the implication that the real-world functionality of analog-circuit techniques – sensing, signal processing, and driving – can now be accomplished in the same dense ultra-small technologies that are "under-the-hood" of the latest digital processors. This opens the way for advanced on-chip analog functions that previously were thought to be out of the question. For the consumer, this will ultimately mean more functionality, longer battery life, and lower cost, particularly in portable devices.

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Processors Push The Edge!

In the unrelenting drive for more performance at lower cost, the migration to more-advanced processes provides higher density and smaller die sizes, with an increase in performance and reduced power dissipation. However, these new processes present significant technological hurdles, which result in a reduced gain in transistor density below that which simple process scaling would predict.The most recent migration from 45nm to 32nm illustrates these aspects.

At ISSCC 2010, the first processors fabricated in 32nm CMOS technology will be presented. Intel's "Westmere" family of processors implements six-cores at higher clock frequencies in the same power envelope as the four-core 45nm "Nehalem" **[5.1]**. The Westmere chip contains 1.17B transistors and a 12MB shared L3 cache in approximately the same die area as Nehalem which had 731M transistors. The 50% increase in transistor density, less than observed in previous generations, illustrates the constraints of the 32nm process. Other integration features include an anti-resonance feature for the Quickpath I/O supply and an on-package LC power filter that reduces the DDR clock drivers' jitter. Dynamic voltage – frequency scaling is used to minimize power, as in previous generations.

Engineers from AMD will describe a 3+ GHz, 32nm Silicon-on-Insulator (SOI) x86-64-processor core with power controllable in a 2.5W to 25W range **[5.6]**. Regular-V_t nFET technology with a total width of 1.38m is used to construct the power gating ring by taking advantage of the isolated substrates inherent in SOI technology. This enables a lower voltage drop during operation, and a low-impedance virtual ground layer using a package-metal layer. The L1 cache uses 8T cells for a lower minimum voltage enabling scalability to lower supply voltages for reduced power dissipation. Power-monitor circuitry calculates the dynamic power dissipation with respect to the thermal design limits, enabling the system controls to enact power reduction by methods such as voltage – frequency scaling.

IBM's POWER7™ processor integrates eight quad-threaded cores in a 567mm^2 45nm SOI die size **[5.4]**. New integration features include the use of embedded DRAM for a 32MB L3 cache utilizing deep-trench technology for at 0.065μm^2 cell size. The deep trench is also used for very high density 100fF/μm^2 on-chip supply decoupling capacitors.

Using general-purpose processors for specialized functions results in lower performance than can be attained with special-purpose hardware. This is especially true in data centers which must combine networking capability with server functions: Engineers from IBM will describe a "wire-speed" processor with network and server attributes that integrates special accelerators for cryptographic applications, compression, pattern matching, and web servicing/security **[5.5]**. Similarly, digital TV processors feature high-performance requirements combined with special processing features that cannot be satisfied with a multi-core processor using homogeneous general-purpose cores. A team led by Renesas will describe a multi-core processor using heterogeneous cores. The chip is implemented using both special-purpose processors such as video accelerators, audio processors, and two 1024-way matrix processors, and dynamically reconfigurable cores to provide image recognition and database search **[5.3]**

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Keeping Up With the Joneses: Can Many-Core Processors Realize Their Potential?

Modern microprocessors have heavily embraced parallelism as a way to continue scaling up their performance while maintaining an increased focus on energy-efficiency. As the core count within the processor chip increases, so do the demands placed on both on-chip and off-chip communication fabrics that enable the data flows necessary to provide the cores with required information. On-chip networks must be designed with a high-degree of flexibility to accommodate the wide variety of application loads inherent in general-purpose computing to ensure that application performance can scale with increasing core count. All this, while overcoming the energy-efficiency challenges in switching and routing imposed by the increasingly miniscule metal filaments used for on-chip interconnects, several million of which fit within a single inch.

This year, at ISSCC 2010, innovations in networks-on-chip feature solutions spanning both the architectural and circuit levels which improve computing performance by taking energy-efficiency and throughput to unprecedented levels. The multi-stage crossbar in SUN's 128 thread Rainbow Falls "data-center-on-a-chip" enables core-to-L2 communication at an impressive 461GB/s **[5.2]**. The first of Intel's many contributions this year proposes an alternative approach, utilizing a ring interconnect bus to deliver an eye-popping 1.2TB/s of communication bandwidth among the 8 on-chip Xeon cores **[9.2]**. As well, Intel describes a message passing scheme using on-die shared memory in a 48-core system with a 6x4 virtual cut-through network enabling a 256GB/s bisectional bandwidth. Dynamic voltage and frequency scaling in 8 voltage and 28 frequency domains yield an impressive network efficiency of approximately 0.2Tb/s/W **[5.7]**. Intel will also describe an experimental circuit-switched streaming network protocol that is applied to a 64-node on-chip mesh network. Router energy-efficiency is significantly improved using circuit-switching and dual-supply channels, and network throughput is increased using back-to-back streaming, achieving an aggregate throughput of 2.6Tb/s at energy efficiencies on the order of 0.66 to 2.0pJ/b (that is, 0.5Tb/s/W to 1.5Tb/s/W) **[5.8]**. Lastly, Intel describes their experiments on the interaction of dynamic voltage – frequency scaling with the application-level impact on core mapping and thread hopping, achieving improvements of 20% to 60% in both throughput and energy-efficiency of many-core processors **[9.1]**.

As core counts increase towards hundreds-per-chip in the very near future, it is becoming nearly impossible to predict the sustained performance of a network architecture or application-mapping protocols using conventional simulation-based analysis. Hence, the insights gained by fabricating various network-on-chip hardware implementation prototypes are proving to be an essential basis for understanding and advancing the sustained application performance of future many-core processor chips.

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Embedded DRAM Dramatically Increases Processor Performance

Today's computers have become more computationally powerful than ever seemed possible, even just a few years ago! The latest generation of microprocessors process data at rates of trillions of operations per second using multi-Gigahertz clock speeds. This means that they complete a processing loop in a few hundred picoseconds, or trillionths of a second! To make matters worse, complex tasks such as server-class work, high-resolution graphics, financial analysis, and weather prediction, need to be processed in real time, failure-free. Hence, the CPU needs to reliably fetch the application program and data at extremely high speeds from wherever they are stored in the system.

Today's computing platforms typically store data in mass media, such as hard disks or solid-state arrays, when it is not needed, and loading it into a nearby dynamic RAM (DRAM) for faster access once the processor requires it. Unfortunately, the dramatic increase in computational power has far outstripped the bandwidth of accessing these external DRAMs, resulting in a sub-optimal user experience, as the high-performance processor sits idle waiting for data from memory. The solution to this problem is to embed additional memory within the processor chip to hold data for possible repeated use, where it can be accessed much more quickly than off-chip memory. This points to the need for a high-density low-voltage on-processor cache memory. Regrettably, standard static RAM (SRAM) technology is not providing enough density and power reduction in on-chip caches as process technology continues to scale. This year, at ISSCC 2010, IBM will present an embedded DRAM (eDRAM) cell built using DRAM-style capacitors and a single transistor, instead of the 6 transistors required for an SRAM cell. IBM manages to embed an impressive total of 32MB of eDRAM inside their new POWER7™ processor **[5.4]**, three times more cache than in any other world-class server microprocessor. This is the first presentation of an eDRAM implemented in a 45 nanometer Silicon-on-Insulator (SOI) process.

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Europe's High Performance Processor Contribution

Europe's contribution to the world of high-performance computing will be recognized at ISSCC 2010, with the detailed unveiling of IBM's POWER7™ processor for high-end servers **[5.4]**. This highly-parallel and scalable processor contains 8 cores supporting 4 threads per core in a 45nm Silicon-on-Insulator (SOI) technology. An amazing 32MB of embedded DRAM, implementing level-3 caches, allows large workloads to be processed rapidly, reducing the impact of external memory latency. Flexible voltage and clock domains allow performance and power consumption to be optimally traded for any given application. This POWER7 ™ processor will presented at ISSCC 2010 by engineers from Boeblingen, Germany, in collaboration with their counterparts worldwide.

In addition, the same European team has contributed to the design of an SRAM cache, integrated in the same processor, which emphasizes the entirely different goals of speed and access bandwidth rather than sheer density **[19.2]**. These diverse memory designs are an important enabler for the breakthrough performance of this new POWER7™ server chip.

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Who Will Watch the Watchmen? (and for how long?)

Traditionally, displays have been a one-way interface in which information is conveyed to the person watching the display. However, the recent boom in smart phones and tablet PCs has resulted in an explosion of two-way display devices that are also collecting information from the environment around them via capacitive touch screens or integrated sensor technologies.

At ISSCC 2010, engineers from Samsung Electronics will describe an embedded-display controller which features an integrated capacitive touch screen controller system **[6.1]**. Displays are not just putting information out these days; they are also taking it in! Information that can be extracted is not just an image, but includes capacitive sensors that monitor your motions and allow you to interact with the display and device. This new level of integration in a low-cost form-factor will open up new avenues of interface-design exploration, and continued cost reductions in the next generation of smart phones.

An often forgotten aspect of display design, but one which is becoming increasingly important as the "green" revolution continues to take hold, is developing ways to extend the lifetimes of next-generation displays. By utilizing innovative electronics, engineers at Ignis Innovation have teamed-up with their colleagues from the London Center for Nanotechnology and Eastman Kodak to develop techniques for reducing the effects of image deterioration in active- matrix organic LED displays **[6.3]**. Their success will have important implications on the entire display industry, since it will help to reduce electronic waste that is currently raising environmental alarms around the world.

Thus, we see that displays, while observed, observe the observers, while they, themselves are being scrutinized for environmental impact!

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Silicon-Based Second Opinions?!

Improvements in integrated-circuit instrumentation are beginning to migrate into the medical-diagnostic measurement and point-of-care (PoC) fields. Previously, the exclusive domain of trained health-care and biomedical experts, these areas are beginning to be augmented by innovative silicon-based solutions that attempt to automate and improve the services being provided to the end-user patient, using complex signal processing and high levels of integration.

At ISSCC 2010, a variety of revolutionary solutions within this fast growing field will be described:

- Non-invasive induction-based signaling and power-delivery systems will be described by engineers from the Georgia Institute of Technology **[6.4]** and the University of Florida **[6.5]**. These solutions are key to the development of extremely-compact and ultimately-embeddable medical solutions that can provide critical continuous real-time diagnostic information.

- Advancements in IC design also include feature-extraction algorithms that provide the key physiological data needed by physicians to make complex diagnoses. Engineers from IMEC with KU Leuven **[6.6]** and the National University of Singapore **[6.7]** will describe power-efficient architectures that allow for small devices with extended measurement lifetimes.

- Researchers from the University of Texas will describe novel measurement techniques, with a particular focus on complex impedance, to provide label-free methods for biomolecular detection at lower analysis cost, by avoiding expensive optical systems **[6.9]**.

The continuing improvement in bioelectrical-circuit engineering increases the likelihood that these technologies will transfer soon from inside the lab to out on the front lines, servicing the patient and health-care infrastructure, in a "bench-to-bedside" technology transfer. In a time of dynamic health-care initiatives and changes brought about by evidence-based medicine, these quantitative diagnostic systems will grow dramatically in importance.

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Organic Smart Sensors are well on the Way!

Organic thin-film transistors (OTFT) present a new approach to building electronics that are flexible, span over large areas, can be inkjet printed, and can be integrated with plastic materials. Potential applications include flexible displays, biochemical sensors, and artificial skin. In many sensor applications, OTFTs act as the interface to the physical realm. However, a key missing component is the analog-to-digital converters (ADCs) allowing for the signal processing to be done digitally. Because of the large process variations in OTFT fabrication – often orders of magnitude higher than those in silicon processes – analog OTFT circuits have only been sparsely reported. In particular, ADCs, which strongly rely on component matching for accuracy, have not been demonstrated in an OTFT process until now.

Cooperation between researchers from Stanford University and from the Max Planck Institute for Solid-State Research **[7.1]**, has led to the first ADC ever reported built in a CMOS organic thin-film process. A successive approximation register (SAR) data converter architecture, whose accuracy largely depends on capacitor matching, is used to take advantage of capacitor matching that is an order of magnitude better than the OTFTs in this organic process. The ADC uses a capacitor C2C ladder and an organic comparator combined with external FPGA logic to achieve the highest resolution reported in an organic process, while operating from a 3-V supply, which is a very low voltage for organic devices.

An alternative organic ADC proposed by researchers from the Katholic University of Leuven **[7.2]** utilizes a first-order continuous-time delta-sigma converter with an oversampling ratio of 16. This architecture is well suited to organic processes as it uses feedback to overcome small variations in process parameters, and doesn't require calibration. The circuit is implemented in a p-type transistor only thin-film organic process requiring dedicated circuit techniques, and operates from a 15-V supply.

These breakthrough achievements are a very important step towards the full integration of sensors, analog, and digital circuits in an organic process. They will enable a whole new range of sensor applications such as ultra-light and ultra-thin, flexible, easy-to-wear, reusable, and disposable sensor devices for health monitoring. Roll-to-roll production processes, comparable to what's now being used in the paper printing industry, will enable these devices to be manufactured in large sizes, high quantities, and at low cost.

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Fabricating IC's in Your Family Room!

Have you ever dreamed of manufacturing your own integrated circuits at home? A collaboration between researchers from the University of Tokyo, Mitsubishi Paper Mills, and the Max Planck Institute has led to the invention of User Customizable Logic Paper (UCLP) which enables integrated circuits to be generated with a standard ink-jet printer at home **[7.3]**.

Basic logic blocks are pre-fabricated using 2V CMOS organic transistors on a thin plastic film. The film is covered with a paper on which interconnects are drawn by a standard ink-jet printer using a newly developed nanoparticle-based ink that is conductive at room temperature, to connect the organic circuit blocks. By using a new Sea of Transmission Gates architecture, the gate array area is reduced by 11-85% compared with the conventional gate array architectures.

By utilizing conventional ink-jet printer available in most homes and classrooms today, UCLP has the potential to be used for educational purposes to allow a letter-sized paper sheet to act as an electronic building block accessible by children and new comers to integrated circuit design. In the future, this type of technology will provide ways to add programmability for integrated circuits used in large-area electronics such as smart flexible displays, power transmission sheets, and electronics skin for robots. In fact, you may soon be printing entire integrated circuits in a family room near you!

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3D-TSV Technologies Coming Of Age

Engineers from IMEC, Panasonic, Qualcomm and K.U.Leuven are paving the road to design in low-cost 3D Integration technologies that will enable the extension of Moore's law into the next decade **[7.8]**. 3D Integration technologies with Through-Silicon Vias (TSV) promise increased system integration at lower cost and reduced footprint. Low cost 3D TSV technology has the potential to revolutionize the IC industry, creating a new wave of handset, wireless, and computing applications.

3D TSV stacked DRAM-on-Logic is expected to reach the market by 2011, followed quickly by Logic-on-Logic and RF-on-Logic. Market forecasts put the production of 3D integrated wafers as high as 10 million units by 2012. However, key technology challenges remain in terms of the realization of a commercially-viable and yielding high-density TSV-based 3D stacking process. The presence of a sea of TSVs in a CMOS wafer will have a significant impact on MOS devices, back-end-of-line, reliability, ESD, signal integrity, thermal hot spots, and therefore overall circuit performance.

An equally formidable challenge is the creation of a 3D design environment to make optimal use of the 3D stacking technology. "Real 3D" will become a reality only when 3D-aware design libraries and tools that result in better methods to partition and design stackable IC units become available.

Researchers from IMEC tackle 3D design considerations starting from a commercially-viable cost-effective 3D stacked-IC process with high-density TSVs. Based on extensive measurements they determined that the thermal and TSV proximity impact on MOS transistors are the key challenges that will have to be included in the 3D design cycle. Other anticipated issues, such as ESD and 3D TSV reliability in contrast do not presently constitute a roadblock to the successful implementation of 3D systems. They have validate that 3D integration shows clear opportunities, such as improved noise isolation for mixed-signal systems, and that a standard-cell logic design style is compatible with cost-effective 3D stacked-IC technology.

These research results indicate that major roadblocks for the acceptance of a cost-effective 3D stacked-IC technology with high-density TSVs are being overcome, and the deployment of a DRAM-on-Logic application is on track for 2011.

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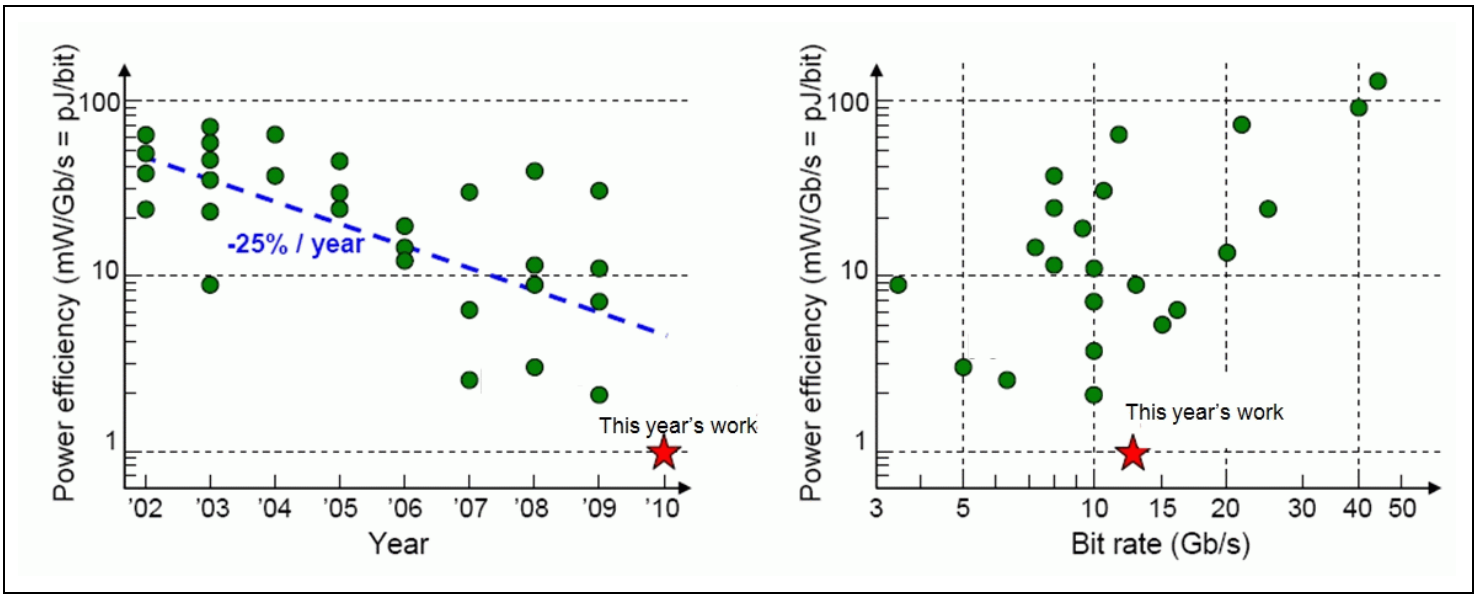
Elegant Transceivers Slash Power!

The magnitude of the quantity of data we share and process has grown exponentially, as our expanding digital lifestyles continue to fuel our appetite for instant access to information, through complex user interfaces. Convenience of access comes with a cost, though; huge amounts of energy are consumed to push bits across continents, within data centers, and even between chips!

Several of the results to be presented at ISSCC 2010 will help to address the problem of shuffling bits between chips in an energy-efficient manner: Researchers from Intel will report new extremes for ultra-low power, combined with ultra-high bandwidth, in the form of a chip-to-chip transceiver interface in 45nm CMOS that delivers almost 0.5Tb/s, all for less than 2/3 of a Watt **[8.1]**. This performance is over 10X more efficient than the current state-of-the-art, paving the way for lower power microprocessors and connectivity.

Engineers from Hitachi Central Research Laboratory will demonstrate there is always room for improvement, as they break the elusive power barrier of 1mW per Gb/s with a 12.5 Gb/s transceiver in 65nm CMOS using only 12.3mW **[20.5]**! The significance of this result is illustrated in the figures below, which indicate its performance relative to a number of previous implementations. Imagine what may be achieved with a 45nm process!



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ADC-Based Receivers: The Great Equalizer

Bottlenecks abound in data links, but gradual improvements in transceiver design have enabled pushing more data through the same "thin pipes". Analog-to-digital converters (ADCs) promise to squeeze every last bit of performance out of tomorrow's links. While ADCs yield the most capable and flexible equalizers, they are also plagued with a reputation for high power consumption, and still have not delivered on the promise of fully digital receivers.

ISSCC 2010 will feature two approaches to tackling these problems. First, engineers from the University of Toronto with Fujitsu Laboratories of Japan will describe an approach where they have eliminated most of the imprecise sensitive analog circuits **[8.6]**. They use a fully-digital engine downstream from the ADC to implement a 6.875Gb/s receiver using only a 1.45X oversampling ratio, compared to typical designs using 2X oversampling. As well, Fujitsu Laboratories will describe an ADC-based front-end where phase tracking of the input signal and the data decisions are performed entirely in the digital domain **[8.7]**.

These ADC-based receivers continue to deliver the promise of maximizing performance while minimizing power!

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Darwinian Semiconductors: Adapting to Survive

Today's high-performance digital systems are facing unprecedented levels of deep sub-micron processing negative effects as geometries continue to shrink, and the level of integration increases. Designers are having to deal with issues such as oxide-wearout, device-threshold variation, and aging effects, on top of the usual suspects (temperature and voltage changes). As a result, it is becoming a Herculean challenge to implement GHz-class billion-plus transistor processors that maintain the traditional trends of increased performance and efficiency. Hence, designers are turning to embedded digital sensors that enable a continuous characterization of (and timely correction for) these effects, to maintain the trends.

ISSCC 2010 will highlight several innovations in the development of these embedded sensors and their applications. Cypress Semiconductor utilizes an on-chip microcontroller and a temperature sensor to manage PVT (Power Voltage Temperature) variations, and thereby control the speed and power consumption of an SRAM **[9.6]**. Engineers from Intel with Purdue University address another important aspect of variation, implementing a random-process-variation sensor to help compensate global PVT variations **[9.7]**. Combined with an on-chip calibration circuit, it enables rapid process optimization and early yield improvement. Engineers from the University of Michigan propose a minimally-invasive in-situ delay-slack monitor that directly measures the timing margins, with 5ps resolution on critical timing signals, enabling the chip to adapt to the performance margins caused by both global and local variations **[9.8]**. They also address another aspect of variation called NBTI (Negative-Bias Temperature Instability) using a "wearout" monitor to detect the initial onset of oxide breakdown in large-scale circuits by utilizing the subtle characteristic change in the resistive behavior of oxides **[9.9]**. Finally, NEC reports an aging monitor that offers a ten times improvement in measurement speed over prior techniques, allowing it to measure degradation prior to any recovery effects **[9.10]**.

Today's high-performance-processor marketplace really is a case of adapt or perish! Those companies that are able to tame the vagaries inherent in the advanced technology processes required to fulfill today's power and performance requirements, will continue to capture more and more of the marketplace; while those that cannot, will fall further and further behind, until they are ultimately forced to leave! Through it all, designers will continue to develop new and innovative methods for keeping their devices alive in the field, and operating at their maximum performance level. Darwin would be proud!

This and other related topics will be discussed at length at ISSCC 2010, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 7-11, 2010, at the San Francisco Marriott Marquis Hotel.

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Power Conversion Where it Matters!

Power conversion is of vital importance in the modern energy-conscious world where everything is portable. Thus, the energy that resides in a battery must be voltage-level-converted into a form that can be used by system ICs without too much waste. Currently, as well, more than half the energy in your cell phone's battery is wasted by the power amplifier which drives the antenna. Hence, for this reason, the battery you carry around is about twice as bulky and heavy as it needs to be. So, it is no surprise that improving the efficiency of power amplifiers for radio frequency transmitters is a key focus of research and development. Accordingly, at ISSCC 2010, a variety of techniques for improving the conversion efficiencies of power supplies and amplifiers will be revealed.

Polar power amplifiers consider the radio-frequency (RF) signal to be composed of two parts – an amplitude and phase – like a polar graph (hence the name), treating these two components separately. Counterintuitively, perhaps, this allows much greater efficiencies than simple linear amplifiers, which attempt to amplify the entire signal at once. In fact, polar amplifiers reduce losses by adopting both a high-efficiency constant-amplitude amplifier to modulate the phase, and a high-efficiency supply modulator that tracks the signal envelope to modulate the amplitude. However, difficulty lies in the implementation details. At ISSCC, researchers from the Hong Kong University of Science and Technology will describe how an advanced supply modulator can deliver envelope power to the amplifier with high efficiency, while achieving the bandwidth required for modern radio systems **[10.1]**. A hybrid stage using a two-phase class D amplifier cuts the power losses to half that of using conventional linear techniques.

Traditionally, analog control techniques are used for high-efficiency power conversion. However, as technology scales down, making digital logic readily available, digital control techniques become increasingly attractive as an alternative control method. The accuracy and flexibility of digital control provides a simple way to compensate control loops, and opens up a whole new world of possibilities in terms of programmability and reconfigurability. To demonstrate this fact, researchers from TSMC **[10.2]**, KAIST with JDA Technology **[10.3]**, Qualcomm with Arizona State University **[10.4]**, and the University of Florida with Intel **[10.6]**, will present a range of developments adopting digital controllers to perform high-efficiency DC-DC conversion. While it is clear, that the research in this area is still quite new, for the first time a clear direction is established where the performance of digitally-controlled power converters match or exceed those using traditional analog control techniques.

The world of power conversion and power management is clearly changing, as we attempt to improve our ability to get the most out of our existing energy-storage devices. Thus, an increasing amount of sophistication is being brought to bear on some very-old problems with very-impressive results. Thanks to these efforts a greener more-efficient world — not to mention a lighter cell phone — is on the horizon.

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Silicon Improving (and Safeguarding!) Lives

Transistor scaling, with superior speed and integration capabilities, will enable new applications such as automotive radar, mm-wave communications, and ultra-low-power communication systems that will continue to improve our quality of life and safety!

Automotive radars will increase driving safety by assisting the driver in avoiding collisions. At ISSCC 2010, researchers from National Taiwan University will present a fully-integrated CMOS automotive-radar system enabling a lower cost solution for today's car manufacturers **[11.2]**. Reducing the cost and improving the performance of such systems is essential for widespread adoption of the technology, ensuring a significant reduction of car accidents and resulting human injuries/fatalities.

As important, but less mobile, wireless sensor networks can be used for environmental monitoring, such as in air-quality measurement and medical applications. Such systems can only be successful if their sensor components require no battery replacement during their operational lifetime. Engineers from Holst Centre/IMEC **[11.5]** and Columbia University **[11.7]** will present techniques to reduce power dissipation by putting such systems into sleep mode between transmissions. These approaches will enable operation either from a single battery over many years, or by scavenging energy from the environment to meet peak power needs.

Currently, stylish, wall-mounted high-definition TVs are burdened by the unsightly bunch of cables needed to connect them to modern home entertainment systems and cable/satellite receivers. Wireless HDMI is an emerging standard that seeks to eliminate the need for cabling by enabling wireless high definition video streaming over high speed 60GHz wireless communication links. Robust performance of these 60GHz links is achieved by focusing the wireless signal of the transmitter towards the receiver, much like the beam of a searchlight: At ISSCC 2010, engineers from MediaTek and IBM will present a phased-array system to implement this beam-forming technique **[11.3]**. Their proposed methods will also have applications in future high-speed communication systems, enabling the continued untethering of electronic devices.

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A Phone Call a Day to Keep the Doctor Away!

Many people suffer from chronic back pain and want to avoid a lifetime of drug dependency for the simple pleasure of sitting in a chair. One alternative is to use heat to damage the nerves and thus limit the pain. However, this technique is destructive and not permanent as the nerves regenerate over time, forcing repeated visits to the doctor for repeated surgeries, and can have severe side effects such as hyper-sensitivity to pain. At ISSCC 2010, this cycle of repeated operations promises to be broken using the same technology upon which mobile phones are based.

For the first time a CMOS System-on-Chip (SoC) has been built by researchers from Taiwan to provide low voltage radio waves that gently heat your back to help relieve the chronic back pain experienced by so many today **[12.1]**. Radio waves are also used to convey power to the SoC, eliminating the need for additional surgeries to replace expired batteries. Laboratory experiments with rats have demonstrated the SoC's effectiveness: rats with an implanted SoC, demonstrate increased tolerance to back pain compared to rats with no SoC.

The SoC is fabricated in a cost-effective 0.35µm CMOS process, mounted on a PCB that is connected with a flexible coil antenna that is wrapped around the spine. The use of integrated circuit technologies reduces the form factor of the complete stimulator module to the size of a US quarter, allowing for easy implantation. It is powered and controlled externally by a transmitter that is outside the body, allowing the doctor to essentially dial your back and give it a radio frequency massage whenever the pain flares up. Perhaps one day we will be able to extend this capability to have a phone number for every part of our body, introducing the new adage "A Call A Day to Keep the Doctor Away!" to the lexicon!

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Ultra-Small Medical Implants Forecast a New Generation of Medical Solutions

In the past silicon nanoelectronics have fueled the communications and computation revolution. Today they are enabling a new generation of ever-smaller and lower-power medical devices. In a study by engineers at Texas Instruments and Purdue University **[12.2]**, implantable pressure monitors have been developed that occupy less than one mm3 volume. Mounted on stents, these monitors allow blood pressure to be measured within the heart itself, facilitating more accurate diagnostics. Packaged in yet another configuration, these devices allow monitoring of intraocular pressure in glaucoma patients.

In addition to their extremely compact size, these remarkable devices have an average system power consumption that is 200,000× lower than state-of-the-art pressure monitors. The system can be powered by free-space radio frequency waves, which are also used to communicate with the device, eliminating the need for wires piercing the skin and opening up avenues for contamination and infection. The system exploits conventional CMOS technology, as well as microelectromechanical (MEMS) and ferroelectric-based memory (FeRAM) in order to achieve these extraordinary gains in size and power reduction.

This work by Texas Instruments and Purdue University provides a window into the new advances in biomedical devices that are enabled by nanoelectronic technology and the augmentation of conventional CMOS with MEMS and FeRAM. These new opportunities will continue to fuel semiconductor technology research into the 21st century, while bringing new advances in improving human health that will benefit society in the years to come.

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Timing is Everything!

Nothing happens in modern communications and computing systems without a clock signal! The clock is the heartbeat of every computing system, and the performance of the system is only as good as the quality of its clock signal. In communication systems, particularly wireless, the frequency and stability of the clock signal determines the transmission band, the amount of information that can be transmitted per second, and the robustness of communication in congested wireless environments. In all such systems, noisy clock signals plagued by timing jitter lead to poor system performance and/or failure of the communications link. For example, in a typical cellular telephone, the clock period is about half a billionth of a second (that is, 0.5ns), and the required accuracy of the clock signal is often better than 0.1% of a period (that is, 0.5ps). Moreover, we expect our phones to work equally well on a ski slope as they do on the dashboard of a hot car, requiring that they must be able to adapt to wide ranges of temperature.

To make things even harder, extreme market pressure dictates that these extraordinarily accurate systems be integrated together with numerous other functions on a single integrated circuit. Such functions include large digital circuits such as microprocessors with billions of switching transistors that generate noise and interference which can easily corrupt timing accuracy. Each year, the continued scaling of CMOS technology, also known as Moore's Law, makes it possible to cram more computing power onto each chip, both in terms of computational complexity and speed. Unfortunately, there is a dark side to Moore's Law; it makes life increasingly difficult for clock-circuit designers. As transistors shrink to nanometer sizes, trade-offs are made which require the use of progressively-lower power-supply voltages on the order of 1V and below. This makes it very hard to maintain accuracy and low jitter in analog blocks such as timing circuits. However, the abundant availability of logic gates in these technologies enables the increasing use of digital enhancement and calibration techniques to improve clock and frequency-synthesizer performance. In addition, the increasing speed of digital circuits allows digital solutions to traditionally-analog problems in high-performance clocking.

At ISSCC 2010, engineers from several companies (NEC **[26.2]**, Atheros **[26.3]**, Infineon **[26.6]**, and IMEC **[26.7]**) and universities (Columbia University **[26.1]**, University of Twente **[26.4]**, Politecnico di Milano **[26.5]**, and Pohang University **[26.8]**) are showing significant advances in minimizing and simultaneously improving the accuracy of frequency synthesizers using mainstream digital technologies and design techniques. Analog-circuit techniques are also well represented by novel implementations of clocking systems, as demonstrated by engineers at SiTime **[13.1]**, AMD **[13.2]**, Fujitsu **[13.3]**, RF Micro Devices **[13.4]** and ST Microelectronics **[13.5]**.

And so, in these session at ISSCC, timing is everything!

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Emerging Non-Volatile-Memories Take the Stage!

At ISSCC 2010, a record number of emerging nonvolatile memory technologies including Phase-Change Memory (PCM), Magnetoresistive RAM (MRAM), and Resistive Ram (RRAM), will be reported. Historically, such emerging technologies have been considered exotic ideas found only in academic research labs, and were not optimized for speed, density, or power efficiency. However, at ISSCC 2010, a number of leading semiconductor companies will present their commercialized versions, demonstrating unprecedented levels of speed, density, and power efficiency, all-the-while using state-of-art mainstream CMOS technologies.

Engineers from Numonyx will describe a 1Gb PCM developed in 45nm CMOS with a 37.5mm^2 die size, and a 266MB/s read throughput that is well suited for an execute-in-place architecture **[14.8]**. An industrial collaboration between STMicroelectronics and Numonyx will present a 4Mb embedded PCM developed in 90nm CMOS that delivers a 12ns read time that approaches the speed of conventional embedded DRAM and SRAM **[14.7]**. This high-performance memory has the potential for widespread adoption in SoC applications requiring nonvolatile capabilities.

Toshiba will describe their development of a 64Mb MRAM that utilizes perpendicular tunnel-junction cells with the fastest-reported read time of 30ns, using a novel sensing scheme and architecture that allows almost unlimited read/write cycling **[14.2]**. Toshiba will also describe a novel solution to achieve larger signal-to-noise ratios in chain FeRAM (Ferroelectric RAM) that will lead to higher memory capacity and increased speeds, allowing it to be used as cache memory in SSD (Solid-State Drives) applications **[14.4]**.

Engineers from Unity Semiconductor will describe a lesser known Conductive-Metal-Oxide (CMOx) memory that reaches a never-before-seen capacity of 64Mb in 0.13µm CMOS. This technology can be pushed into the 64Gb regime in 45nm CMOS, using a multi-layer technique.that they propose,,providing extremely low-cost and low-power solutions for storage applications **[14.3]**.

And thus, this year at ISSCC 2010, we see an unusual advance of exotic memory technologies into commercial production!

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Future Smart Phones are Here!

Smart phones and netbooks have seen explosive growth over the past few years, and will soon become a leading driver of semiconductor sales (see Figure 1 below, from IEEE CS Pervasive Computing, April-June 2009). Next-generation chips will enable new mobile applications that take advantage of high-speed data connections, high-performance application- processing capabilities, and long battery lifetime, for an enhanced multimedia experience.

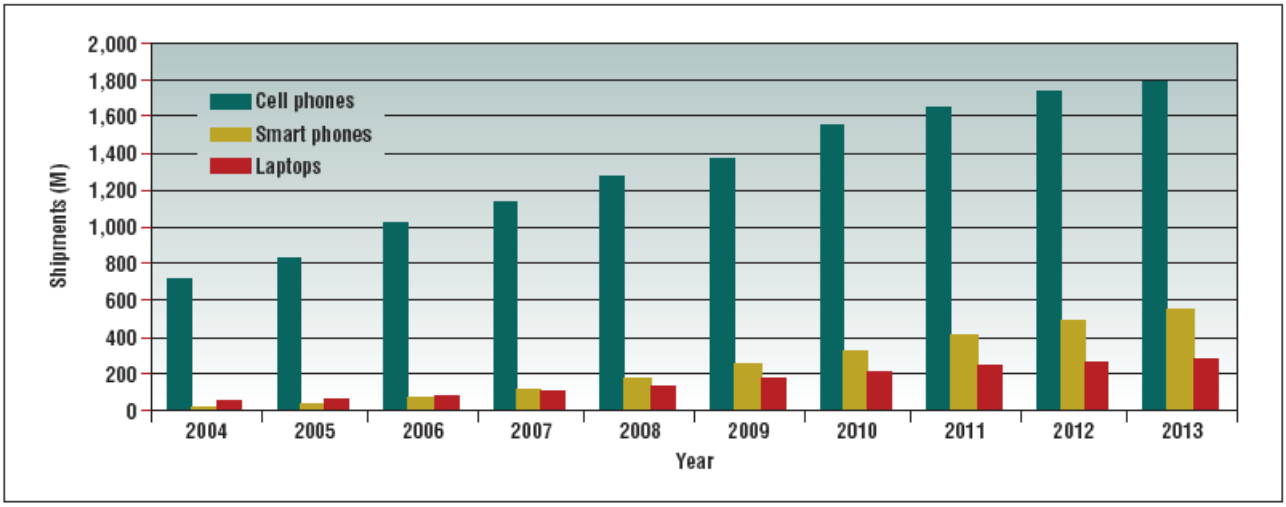

Figure 1. Cell phone, smart phone, and laptop shipments worldwide (M) 2004-2008, forecast 2008-2013. Source: Intel Library

ISSCC 2010 will feature the first functional 4G silicon chip for high-speed communication. This collaboration between researchers from ETH Zurich and Advanced Circuit Pursuit implements full-rate Turbo decoders achieving the maximum LTE throughput data rates **[15.1]**. In addition, researchers from CEA-LETI will describe a reconfigurable chip that can implement multiple wireless standards including 4G, WIMAX, 802.11n, and Cognitive Radio **[15.3]**. Their solution provides the necessary flexibility required to interconnect to a variety of networks using many different standards.

ISSCC 2010 will also unveil several low-power embedded processors that break through the 1 GHz barrier, enabling the next generation of smart phones and netbooks that are fast approaching PC operating speeds. Intel **[15.5]** and ARM **[15.6]** will describe new circuits for dynamic detection and correction of timing errors to squeeze voltage margins for reliable low- power operation over 1.5GHz, while Qualcomm describes low-power-design techniques used in their upcoming 1.4GHz Snapdragon processor core **[15.7]**.

These innovations in both cellular/wireless standard support and low-power, high-performance embedded processors will be the building blocks for the next-generation mobile devices, bringing as-yet-unseen levels of functionality and performance to the masses!

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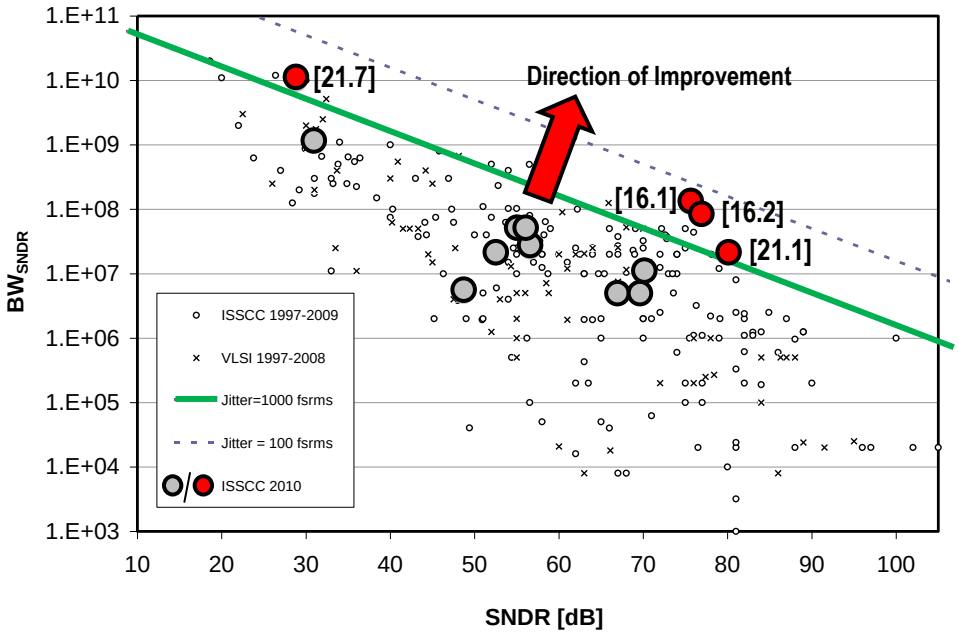
ADCs Push the Limits!

Data converter technology plays a key role in interfacing between the digital processing domain and the inherently analog world around us. Unfortunately, the limits of what we can do with our digital processing wizardry are ultimately limited by the accuracy of the data that we extract from the environment. Hence, devising high-fidelity data converters is crucial to our continued digital evolution.

The bandwidth (BW) and the signal-to-noise-and-distortion ratio (SNDR) are two key performance metrics for an ADC. During the design of a data converter, there is an inherent tradeoff that can be made between those two parameters. This tradeoff is theoretically bounded by the amount of jitter that is present in the ADC sampling clock. Thus, an ADC with a given bandwidth cannot have a SNDR exceeding a theoretical maximum for a given amount of jitter. In the figure below, this limitation is represented by two straight lines, one corresponding to 1000fs, and the other to 100fs, of RMS jitter in the sampling clock of the data converter.

At ISSCC 2010, designers from Analog Devices **[16.1, 21.1]**, Texas Instruments **[16.2]**, and Nortel Networks **[21.7]**, will show how they have utilized innovative design techniques, including background calibration schemes that compensates for amplifier residual errors in a pipelined converter **[16.1]**, and a new input track and hold that minimizes distortion **[16.2]**, to dramatically improve performance. As the figure below shows, these new designs are pushing the boundary in data converter design, moving beyond the $1000fs_{RMS}$ barrier and approaching the $100fs_{RMS}$ boundary. These new techniques are taking the state-of-the-art in data conversion to a whole new level, one that will ensure our continued progress along the long path of digital evolution!



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Temperature Sensors, Everywhere!

Temperature sensors are becoming far more pervasive than their classic applications in electronic thermometers and building control would imply. They are now used in large volume for power-management of microprocessors, and to compensate for temperature effects of many other systems, ranging from quartz oscillators to chemical sensors. This wide range of applications requires continuing advances in the state-of-the-art in terms of temperature range, power consumption, and accuracy.

ISSCC 2010 will feature breakthroughs on several fronts in the field of temperature sensing. Engineers from Hong Kong University of Science & Technology (HKUST) **[17.1]** and TU Delft **[17.2]** will describe ultra-low-power temperature sensors that achieve orders of magnitude improvements in energy efficiency, while demonstrating their utility in applications such as a single-chip passive RFID tag.

Another key metric for temperature sensors is their accuracy over a wide range of temperatures. A collaboration between NXP Semiconductors, TU Delft, and the University of Twente, has yielded the first precision temperature sensor in nanometer CMOS technology **[17.3]**, delivering significantly improved accuracy (±0.2ºC) over a wide temperature range (−70ºC to +125ºC). Engineers from TU Delft will also describe their achievements in the design of high-accuracy (±0.2ºC over the range −55ºC to +125ºC) temperature sensors that require no expensive trimming operations **[17.4]**. Lastly, engineers from Carnegie Mellon University will describe their use of an embedded temperature sensor to enhance the stability of crystal oscillators **[17.5]**.

All of these improvements in power and accuracy, together with the elimination of the need for trimming, will result in significantly reduced total system costs. This reduction will lead to even more pervasive integration of temperature sensing in the next generation of electronic and physical systems. This integration will result in a wealth of real-time environmental information that system operators can use to devise more-cost-effective efficient and innovative solutions in the coming years!

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More Cores, Less Power!

The next generation of advanced multimedia features in mobile systems will require computational capabilities that have historically been the domain of only carefully-crafted systems more at home on the desktop, or in a lab, than in a portable device. However, recent advances in massively-parallel multi-core highly-reconfigurable signal-processing architectures are looking to resolve all that, with their incorporation into future mobile devices. Smart and efficient power-management techniques are essential to enable these processors in power-sensitive applications such as smart phones, mobile internet devices and digital video/still cameras.

ISSCC 2010 will see the demonstration of several multi-core solutions tailored to meet the demands of the next generation of mobile devices. Toshiba will present its 14-core mobile application processor which incorporates H.264 full-HD decoding capability in a 40nm CMOS technology **[18.1]**. Their solution utilizes a power-efficient triple-die "stacked chip-on-chip" technology to achieve high memory bandwidth with low power dissipation. Intel will introduce a highly reconfigurable array of hardware accelerators and logic which provides on-chip acceleration of media-signal-processing algorithms for power-constrained mobile microprocessors **[18.2]**. Engineers from Renesas, together with the research team at Hiroshima University, will unveil a scalable massively-parallel processor for real-time image processing **[18.5]**. Their 2048-core solution achieves remarkable power efficiency with its ability to object track in real-time motion pictures.

These power efficient multi-core based solutions will deliver never-before-seen levels of computational capability in a portable mobile form factor. In the hands of innovative application developers, these new capabilities have the potential to enable a whole new world of intelligent multimedia applications, many of which may have been never thought possible – until now, that is!

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Diversity Advances Embedded Memory!

High-performance embedded dynamic and static RAMs (DRAM/SRAM) are continuing to diversify, making inroads into multiple high-performance and low-power applications, unseating more traditional solutions.

At ISSCC 2010, engineers from IBM will describe the first 45nm embedded DRAM (eDRAM) used as L3 cache memory in a high-end server-class microprocessor, the POWER7™. Previously, all microprocessors used SRAM for L3 cache implementations. The memory latency of embedded RAM is greatly reduced compared to that of a traditional off-chip cache implementation, and both cost and power are also reduced, while improving the robustness to Soft-Error Rate **[19.1]**.

Not to be out done, engineers from Intel will report the first application of margin improvement on 32nm SRAM for enhanced low-voltage operation. They employ a new technique called wordline underdrive (WLUD), along with PVT compensation, to reduce Vcc_{min} by 130mV in a 32nm High-κ Metal-Gate technology. Such techniques will enable lower power for advanced applications and lower cost in the most-advanced CMOS technology available **[19.3]**.

Researchers from Toshiba will describe a new technique that improves the write-margin component of the cell failure rate by two orders-of-magnitude for the smallest bit-cell yet reported in 32nm High-κ Metal-Gate CMOS [19.4]. Consequently, the smallest bit-cell with 32nm technology and new assist technique allows very-low-voltage operation with reduced power consumption.

Just as in military conflict, embedding increases the information flow!

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Integrated Optics: Shining Light on Communications

Society has been changed by the explosive growth of optical communication, as evidenced by the award of the 2009 Nobel Prize in Physics to Dr. Charles Kao, a pioneer in the field of fiber optics. Once relegated to a handful of expensive links delivering data between continents, high-speed optical communication has reached the home and is creeping toward the conquest of the last few inches of chip-to-chip communication.

At ISSCC 2010, engineers from Luxtera will describe a fully-integrated optical receiver suitable for such medium-distance links that dramatically reduces the costs of an optical coupling without sacrificing performance **[20.1]**. They utilize a high-responsivity production-quality Germanium (Ge) photodiode integrated onto a 0.13μm silicon-on-insulator (SOI) CMOS technology. An alternative approach will be presented by researches from Yonsei University for tackling short-distance optical links **[20.2]**. Their solution features a fully-integrated optical receiver using only conventional CMOS technology.

The migration to integrated optics in both conventional CMOS and SOI-CMOS is a breakthrough that will help pave the way to all-optical interconnects in the next generation of communication systems. These efforts show that the future for optical communication is, indeed, bright!

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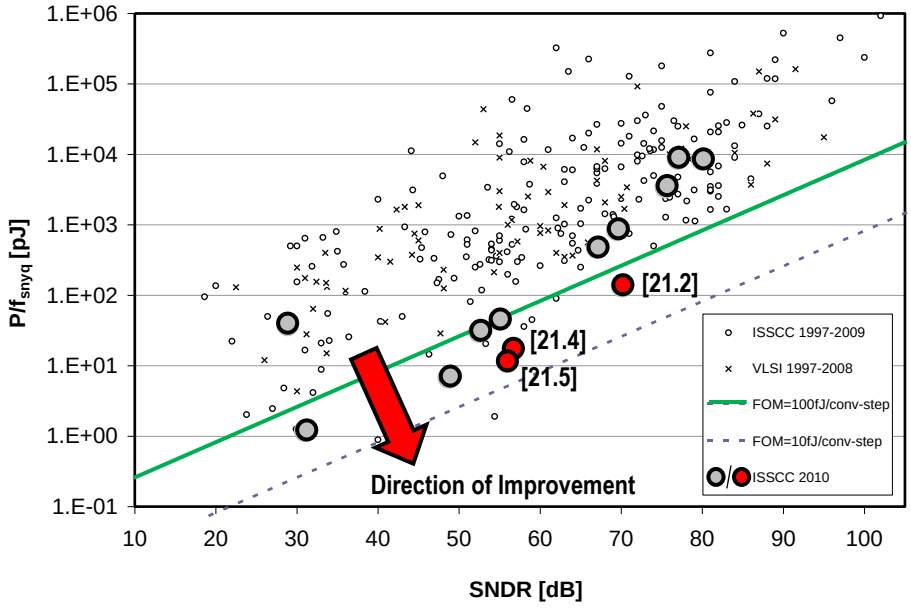
Crossing the Analog-to-Digital Divide…

One way of benchmarking the power efficiency of an ADC is to measure the energy it consumes per conversion step. Over the years, this measure of efficiency has steadily improved thanks to the diligence of engineers and researchers who have focused their attention on improving all aspects of data-converter design. Not surprisingly though, there exists a trade-off between the power efficiency and the accuracy of the conversion (measured as signal-to-noise-and-distortion-ratio, or SNDR). Delivering a higher SNDR for a given conversion rate typically demands higher power dissipation, resulting in lower energy efficiency. The figure below illustrates this situation by plotting the power consumption per conversion as a function of the SNDR for numerous data converters presented in the recent history of the ISSCC and VLSI conferences. Note that there is an obvious trend towards increased power consumption as the SNDR is increased. Within the figure, two lines benchmark the energy dissipation per conversion figure-of-merit (FOM) for 100fJ/conversion-step and 10fJ/conversion-step. These parametric limits help delineate the progress that is being made in the field of data converters as new designs continue to push towards greater energy efficiency. Several contributions to this trend will be presented at ISSCC 2010

At ISSCC 2010, engineers from the University of Illinois at Urbana-Champaign **[21.2]** will describe how they have extended the state-of-the-art using an SAR (Successive-Approximation Register) ADC that is digitally calibrated using a perturbation technique. As well, researchers from Fujitsu Laboratories **[21.4]** will describe how they achieved a FOM of 30fJ/conversion-step for a 10b 50MS/s SAR ADC. Not to be outdone, collaborators from the National Cheng-Kung University with Himax Technologies **[21.5]** will describe their methods for achieving a FOM of just 15.5fJ/conversion-step in a 10b 100MS/s SAR ADC!

This continued push toward the improvement of energy efficiency will enable the development of very-high-fidelity embedded data converters, ones that can be used in a variety of sensing applications, allowing us to digitize more and more of the world around us! Once we cross that analog-to-digital divide, we can apply our dizzying array of digital-signal-processing techniques to create new and exciting applications that will continue to push along our digital evolution!



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Eyes in the Back of Their Head – Seriously!

Conventional consumer-electronics image-sensor design places the pixels that collect the light which makes up the image on the front-side of the sensor's signal-processing-circuit structure. Unfortunately, the light being collected first has to pass by a number of obstacles, such as higher-layer metal and dielectric layers, which corrupt the captured image, and reduce the quality of the result. In an inspired bit of thinking, one that literally turns the problem on its head, researchers have discovered that they can put the pixels on the backside of the sensor-circuit structure where there are no obstructions. This has resulted in improved image quality, but at a much higher cost due to the intricacies of connecting the image sensor's eyes on the "back of its head"!

At ISSCC 2010, engineers from Sony will describe the first commercial instance of a backside CMOS image sensor with 10Mpixel resolution **[22.9]**. Using backside illumination (BSI), they have delivered an imager with high performance 1.65×1.65μm^2 pixels, wide angular response, and a very-low noise floor to ensure high-fidelity image capture. The design incorporates a high-speed on-chip analog-to-digital converter with a high-speed LVDS interface capable of operating at over 550MHz to support high-resolution still-picture imaging during video imaging and slow-motion-video capture.

Unsubstantiated rumours have indicated that teacher groups everywhere are marshalling research funds to see if the technology can be leveraged for bionic implantation, and commercialized for classroom use, but you did not hear this from us! On a more serious note, the commercialization and widespread adoption of BSI technology in the consumer-electronics image-sensor market will result in higher-fidelity images and video-capture solutions in more-compact form factors. To the end user, this means ever-smaller and lower-cost integrated camcorders and digital cameras, with unmatched levels of quality!

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To 100GHz…. and Beyond!

Silicon scaling through Moore's Law continues to present exciting opportunities for research and design engineers to push the fundamental limits of speed in deep-submicron silicon technologies. The silicon-IC implementation of systems at millimeter-wave frequencies (for example, 24GHz, 60GHz, 77GHz, 100GHz and beyond) is now realizable. The smaller wavelengths of mm-waves make it possible to use a fusion of antenna techniques with virtually an unlimited number of transistors in silicon, to create new methods for modulation and encoding of the data, to allow for secure communications and concurrent transmission of independent data sequences in different spatial directions. It is also possible to use the silicon CMOS technology in very large scale phased arrays as a low-cost integrated solution to create scalable tunable multi-band multi-beam phased arrays for a variety of applications.

Presentations at ISSCC 2010 will explore the most recent advances in mm-wave applications of silicon, and offer a broad set of solutions for communications, radar, imaging, and high-speed I/O for chip-to-chip communication. Researchers from Delft University of Technology will describe a two-dimensional 60GHz 2x2 phased-array transmitter in 65nm bulk CMOS **[2.3]**. This device demonstrates that advanced architectures are now being realized in the mm-wave bands. Specifically, this chip utilizes a novel two-local-oscillator (2-LO) phase-tuning system to allow beam steering on both the horizontal and vertical axes. Other notable advances include the realization by Sony with Cal Tech of a millimeter-wave CMOS transceiver for wireless chip-to-chip communication which enables an 11Gb/s intra-connect solution using a 60GHz carrier frequency, with an energy efficiency of 6.4pJ/bit **[23.1]**. This chip, which demonstrates an alternative approach to high-speed I/O interfaces, uses a clever method for injection-locking in the receive-signal path. The fundamental limits to speed in silicon devices is again illustrated with a pair of presentations from the University of Wuppertal, Germany, the first of which is a 160GHz SiGe transceiver with the potential to allow high-speed communication **[23.2]**. The second demonstration by the same research group is of a 650GHz imaging receiver **[23.9]** also implemented in a SiGe process. Finally, record power output for mm-wave CMOS power amplifiers will be presented: A 90nm CMOS PA operates in the 60GHz band **[23.7]** with a power gain of 20dB and a maximum saturated output power of +20dBm.

This year, ISSCC 2010 will mark a pivotal moment in the development of high-speed low-cost communication systems.

This and other related topics will be discussed at length at ISSCC 2010, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 7-11, 2010, at the San Francisco Marriott Marquis Hotel.

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NAND Continues Its Push!

Mainstream NAND flash memory is being implemented in 32nm technology with chip capacities of 32Gb. Such capacity, along with new techniques addressing performance limitations, will enhance the feasibility of solid-state disk (SSD) applications. Such developments will speed the adoption of SSD technology into the mainstream, eliminating the need for conventional hard-disk drives (HDDs), and removing their limitations from the mobile-computing landscape.

Engineers from Samsung will present a 159mm^2 32Gb, 32nm 2bit/cell chip using a novel bitline technology **[24.6]**. Their solution optimizes die size by placing the page buffer and X-decoder on one side of the array. They utilize a dual-pulse-program algorithm to reduce floating gate coupling, and a high-performance DDR interface that achieves 200MB/s throughput.

Hynix will disclose another 32Gb, 32nm NAND device that is 146mm^2 **[24.8]**.They have developed a number of innovative techniques and algorithms to address issues such as: floating-gate-to-floating-gate interference, read-tracking reference programming, and improved data retention. As well, an adaptive coding scheme is applied to the input data in order to reduce power consumption.

Researchers form Micron Technology, Italy, will describe a collaboration with Intel that has resulted in a 126mm^2, 3b/cell, 32Gb NAND device using 34nm technology operating at 6MB/s [24.7]. The device is dynamically configurable to 2b/cell in order to increase performance to 13MB/s using a quad plane architecture. The chip utilizes a high-resolution analog system along with a RISC processor, employing an optimized NAND instruction set, to perform the advanced algorithms required for 3b/cell operation.

And, so we see, that NAND flash continues to push the frontiers of high-density non-volatility!

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Multiple Radios on a Chip – Why Not?

In recent years, the overall trend in the wireless semiconductor industry has been towards increasing levels of integration by adding more radios and radio-related functions within a single chip. From the market's point of view this makes a lot of sense as it enables the integration of more features into the same piece of silicon, lowering the overall solution cost, allowing for smaller footprints, and potentially reducing power dissipation. However, while advanced CMOS processes enable significant scaling in the digital world, they pose certain challenges to analog radio designers including reduced chip supply-voltages, more pronounced parasitic coupling effects, and highly nonlinear transistor characteristics. Innovations in both the radio architecture and the underlying circuits will be required to address these challenges, and at ISSCC 2010 a number of innovative solutions to these challenges will be introduced.

Engineers from Broadcom push the state-of-the-art level-of-integration to a new plateau by combining entire WLAN, Bluetooth (BT), and FM radios, on a single 65nm CMOS SoC, while overcoming the coexistence issues associated with these wireless connectivity functions **[25.3]**. Simply hook it up to an antenna and a battery, and you are ready to go!

Engineers at Analog Devices **[25.6]** and Samsung **[25.7]** will introduce multi-standard fully-integrated mobile-TV SoCs which bring broadcast TV onto your cell phone. Adopting a multi-standard approach is the key to improving the end-user experience by allowing for ubiquitous reception around the world… Just in time for World Cup 2010!

Utilizing these, as well as other solutions to be presented at ISSCC 2010, wireless system providers will continue to redefine what is possible on future wireless devices,while doing so at ever-more attractive price points. We are well on our way to complete wireless connectivity!

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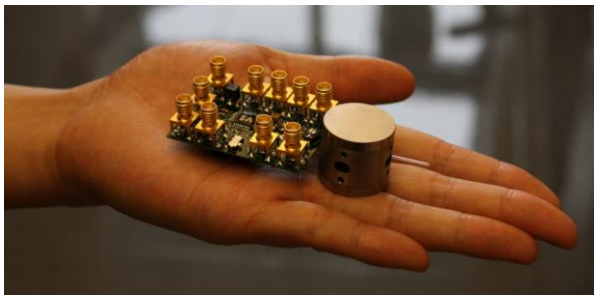
Palm NMR for Human Cancer Screening

By nature, atomic nuclei are tiny bar magnets. These tiny nuclear magnets can swap energy back and forth with radio-frequency (RF) magnetic fields. This phenomenon, known as nuclear magnetic resonance (NMR) whose discovery was awarded the 1952 Nobel Prize, has a broad array of powerful applications, including biomolecular sensing for disease screening, medical imaging, and oil detection. NMR instruments, however, are bulky, heavy, and expensive, and remain as specialized equipment in hospitals, industry, and laboratories. For instance, a state-of-the-art commercial bench-top NMR system weighs 120kg and costs about $70,000 US dollars. The bulky size is due to the large external magnet used to yield a strong NMR signal, which is an essential component in conventional NMR systems. Small, low cost NMR instruments would bring benefits of NMR closer to everyday life. For instance, a miniature NMR biomolecular sensor may enable cancer screening in a doctor's office, local pharmacy, or even a patient's home, at an affordable price.

At ISSCC 2010, researchers from Harvard University will present a 0.1kg 'palm' NMR system, which represents orders-of-magnitude size and cost reduction **[27.2]**. This smallest-ever complete NMR system is 1200× lighter and 1200× smaller, but still 150× more spin-mass sensitive than a 120kg state-of-the-art commercial NMR system. Costs are also drastically reduced by an estimated factor of 1400× due to the use of a small external magnet, only the size of a ping-pong ball, and the design of a high-performance CMOS RF transceiver IC capable of detecting the significantly reduced NMR signal.

The NMR system is also capable of lab-on-a-chip operation by directly interfacing an NMR sample with the CMOS RF transceiver chip, enabling its use as a disposable one-time diagnostic test capable of on-chip disease screening. Indeed, the Harvard researchers will present biomolecular sensing relevant to disease screening, detecting human chorionic gonadotropin (hCG) protein, an important cancer marker for cancers such as choriocarcinoma, germ cell tumors, and islet cell tumor, and detecting human bladder cancer cells.

This multi-faceted work combining the silicon RF IC with the physics of NMR opens new exciting paths not only for NMR miniaturization efforts, but also for circuit designers and biotechnologies. From the circuit design point of view, this work showcases how silicon RF chips can be used not only for wireless RF applications, but also for biosensing. From the biotechnology point-of-view, the work promises a low-cost, hand-held biomolecular sensor aimed at human disease screening, whose detection modality differs from traditional optical biosensing. From the general NMR viewpoint, the NMR system may enable not only biomolecular sensing, but also practical quantum computing and oil detection on silicon chips.



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Cardiologist-on-a-Chip!

Heart disease remains one of the leading causes of death within the modern world. Being diagnosed with heart problems typically constrains you to a regular regimen of costly hospital appointments with your cardiologist. In the hospital technicians place cold metallic electrodes on your chest to monitor your heart rhythm (ECG signals) and a bulky TIV measurement system is used to measure the pumping capability of your heart.

At ISSCC 2010, engineers from KAIST will propose a new technology that enables you to break the cycle, eliminating the need for both hospital visits and bulky equipment that requires a technician to operate **[27.3]**. This extremely low power (3.9mW) healthcare System-on-Chip (SoC) can measure both ECG and TIV signals in a form factor that allows it to be integrated with a thin flexible battery into a plaster-like poultice which allows for anytime anywhere heart-related healthcare. The system automatically reconfigures itself in-situ to optimize its ability to monitor ECG and TIV on an individual-by-individual basis, eliminating the need for expert knowledge in its placement, and allowing the patient to self-administer the test. This cardiologist-on-a-chip can continuously monitor the change of aortic blood volume and velocity of each cardiac cycle and provide important hemodynamic information such as stroke volume and cardiac output. The detected data is then transmitted through the body to a cell phone via body-channel-communication (BCC) with duty cycle modulation. The entire system can be controlled remotely using inductively coupled control transmitted via a cell phone, allowing it to be enabled/disabled by a physician over the phone.

By combining extremely low power consumption, very small form factor, flexible battery technology, and conductive-ink printing-on-fabric technology, KAIST engineers are endeavoring to deliver a low-cost healthcare solution that provides continuous heart monitoring. Hopefully this will allow early detection of abnormal heart conditions, enabling preventative measures to help reduce the risk of hypertension and heart failure, thereby addressing one of the leading health concerns of the modern world!

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