IEEE SOLID-STATE CIRCUITS SOCIETY

ADVANCE PROGRAM

2009 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE

FEBRUARY 8, 9, 10, 11, 12

CONFERENCE THEME:

Adaptive Circuits and Systems

SAN FRANCISCO MARRIOTT HOTEL

REPLAY ON DEMAND
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5-DAY PROGRAM

SUNDAY ALL-DAY: 4 FORUMS: SSD MEMORY; MEDICAL IMAGING; 4G RF FRONTENDS; ULTRA-LOW-VOLTAGE DESIGN — **10 TUTORIALS**
2 SPECIAL-TOPIC SESSIONS: RADIOS HEALTHCARE; FABLESS MEMS

THURSDAY ALL-DAY: 4 FORUMS: HIGH-SPEED INTERFACES; MULTI-DOMAIN PROCESSORS; CLOCK DESIGN; NEURAL INTERFACES
SHORT-COURSE: LOW-VOLTAGE & MIXED-SIGNAL DESIGN

ISSCC VISION STATEMENT

The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and application to maintain technical currency and to network with leading experts.

CONFERENCE HIGHLIGHTS

On **Sunday, February 8th**, the day before the official opening of the Conference, ISSCC 2009 offers:

- A choice of up to 4 of a total of 10 Tutorials
- Four ISSCC Advanced-Circuits-Design Forums:
  - SSD: Memory Subsystem Innovation
  - Medical Image Sensors
  - GIRAFE : 4G RF Frontends
  - Ultra-Low-Voltage Circuit Design
- A Student Forum featuring 5-minute presentations by selected student researchers

The 90-minute tutorials offer background information and a review of the basics in specific circuit design topics. In the all-day Advanced-Circuit-Design Forums, leading experts present state-of-the-art design strategies in a workshop-like format. The Forums are targeted at designers experienced in the technical field.

On Sunday evening, two Special-Topic Evening Sessions addressing next-generation circuit-design challenges will be offered starting at 7:30PM:

- "Healthy Radios": Radio and Microwave Devices for the Health Sciences
- Is Fabless MEMS Fabulous?

The Special-Topic Evening Sessions are open to all ISSCC attendees.

On **Monday, February 9th**, ISSCC 2009 offers four plenary papers followed by six parallel technical sessions. A Social Hour open to all ISSCC attendees will follow the afternoon session. The Social Hour will feature posters from the winners of the joint DAC/ISSCC Student Design Contest. Monday evening features a panel discussion, "Forewarned is Four-Armed: Classic Analog Misteakes to Avoid" and three Special-Topic Evening Sessions:

- Will ADCs Overtake Binary Frontends in Backplane Signaling?
- Highlights of IEDM 2008
- Things All RFIC Designers Should Know (But Were Afraid to Ask)

On **Tuesday, February 10th**, ISSCC 2009 offers morning and afternoon technical sessions. Tuesday evening sessions include, an evening panel; "MID-"Scaled Down" PC of "Souped-Up" Handheld?" and two Special-Topic Evening Sessions

- Interleaving ADCs-Exploiting the Parallelism
- Next-Generation Energy-Scavenging System

Wednesday, February 11th features morning and afternoon technical sessions.

On **Thursday, February 12th**, ISSCC 2009 offers a choice of five events:

- An ISSCC Short Course: "Low-Voltage Analog and Mixed-Signal CMOS Circuit Design". Two sessions of the Short Course will be offered, with staggered starting times.
- Four ISSCC Advanced-Circuits-Design Forums:
  - ATAC: High-Speed Interfaces
  - Multi-Domain Processors
  - Clock Synthesis Design
  - Integrated Neural Interfaces

Registration for educational events will be filled on a first-come, first-served basis. Use of the ISSCC web-registration site (www.isscc.org) is strongly encouraged. You will be provided with immediate confirmation on registration for Tutorials, Advanced-Circuit-Design Forums and the Short Course.

This year, attendees will be able to register for unlimited on-demand web access to multi-media replay of ISSCC technical papers. Attendees will be able to listen to papers they could not attend or to re-play a paper they attended for better understanding.

CONFERENCE INFORMATION

Celebrate IEEE's 125th Anniversary

Tracing its roots to the formation of the American Institute of Electrical Engineers in 1884 by such pioneers as Thomas Alva Edison and Alexander Graham Bell, today's global IEEE is celebrating its 125th anniversary in 2009. Join with us as we commemorate 125 years of ingenuity and innovation in engineering and technology with activities that support the anniversary theme, "Celebrating 125 Years of Engineering the Future."

The year-long IEEE celebration honors the past and focuses on the future with special events at major conferences such as ISSCC. Other anniversary activities around the world include: member and customer events in major world cities; the first student World Congress; the Inaugural IEEE Presidents' "Change the World Competition" for university students; a media roundtable and global webcast featuring emerging, world-changing technologies; IEEE "Engineering the Future Day", on 13 May 2009, the official anniversary date; an IEEE History Center conference and gala; and much more.

All ISSCC attendees are encouraged to take an active role during this milestone anniversary to honor the countless contributions our members and the technology professions have made that have helped change the world. Celebrate with IEEE as we champion the development of future technologies that will benefit humanity.

For more information on the IEEE 125th Anniversary, or to participate online, visit http://www.ieee125.org.

T1: Continuous-Time Filters
Filters are used everywhere in integrated systems. While it is true that precision filtering at low-to-moderate frequencies is best done in the digital domain, the need for continuous-time analog filters has not gone away. Anti-aliasing and reconstruction is always present even for moderate frequency signals, and at high frequencies, analog filters still offer advantages in power. With pressure on the curriculum in all universities, there is less coverage of filter techniques in EE courses, and engineers must pick up the tools on the job. This tutorial aims to lay out the groundwork theory and illustrate the mainstream strategies for integrated continuous-time filters. Topics to be covered include:

- Filter applications and system demands
- Filter specifications and approximations
- Filter realizations and topologies: single-amplifier, biquad, leapfrog
- Integrated implementations: opamp-RC, gm-C
- Tuning strategies: variable elements, digital tuning

Instructor: Bill Redman-White is currently a fellow with NXP Semiconductors UK. He has also worked in France and California on optical storage, cellular radio, WLAN, digital audio, TV, and satellite baseband. He was previously with Motorola Geneva, GEC Marconi, and British Telecom, UK. Concurrently with NXP, he is also a Professor at Southampton University undertaking teaching and research in analog, RF, and SOI CMOS.

T2: Adaptive Power Management Techniques
As highlighted by the conference theme of Adaptive Circuits and Systems, increasingly adaptive techniques are used to manage power dissipation of SoCs. These SoCs are integrating more transistors per die, facing worsening leakage dissipation with each process node and are operating at ever-higher processor frequencies. State-of-the-art adaptive power management techniques such as adaptive voltage scaling, body bias, power gating, dynamic voltage-frequency scaling and sleep modes are discussed both in theory and through examples of implementations found in practice.

Instructor: Alice Wang is currently Senior Member of Technical Staff at Texas Instruments in Dallas, Texas. She is involved in the design of SoCs in the Wireless Terminal Business Unit for application in digital baseband and application processors in cellular phones, focusing on low-power techniques and enhancing battery lifetimes. She received her PhD from the Electrical Engineering department at Massachusetts Institute of Technology, in 2004. Part of her PhD thesis work demonstrated the first-ever 180mV sub-threshold FFT processor.

T3: Turning Bits into Pictures
Electronic displays are deployed in a variety of applications, each of which priorities particular performance criteria (e.g., image quality, size, definition and brightness) whilst imposing its own constraints (e.g., cost, power consumption, robustness). The performance criteria must be met by innovations in electro-optic technology (e.g. LCD, OLED), electronic technology (e.g. LTPS, a-Si) and electronic design. Attendees should leave this tutorial with an understanding of the electronic architectures and circuits that contribute to meeting user expectations in modern display systems.

Instructor: Ian Underwood carried out pioneering R&D in LC microdisplays between 1983 and 1999 when he co-founded MicroEmissive Displays Ltd (MED) as co-inventor of its P-OLED microdisplay technology.. He was a Fulbright Fellow (1991) at the University of Colorado, Photonics Spectra Circle of Excellence designer (1994), British Telecom Fellow (1997), Ben Sturgeon Award winner (1999), Ernst & Young Emerging Entrepreneur of the Year (2003), Fellow of the Royal Society of Edinburgh (2004), Gannochy Medal winner (2004), Fellow of the Institute of Physics (2008) and Fellow of the Royal Academy of Engineering (2008). He is a Professor of Electronic Displays at the University of Edinburgh, Associate Editor of JSID, and a member of the program committees of ISSCC 2009, SID Displays Week 2009 and Eurodisplay/IDRC 2009. He is co-author of the book Introduction to Microdisplays (2006) and is recognized worldwide as an authority on microdisplay technology, systems and applications.

T4: Fundamentals of Digitally-Assisted RF
RF circuits, when implemented in nanoscale CMOS and, especially, when integrated in an SoC, suffer from numerous issues, such as poor linearity, device mismatch, low V_{dd} headroom, high leakage, high flicker and substrate noise, etc. At the same time, the digital gates and memory are 'free' and powerful, so the logical step is to use digital means to mitigate the RF circuit imperfections so that their adjusted performance can match or exceed that of traditional RF circuits. This tutorial first examines opportunities for digital assistance of RF and then presents case studies of calibration due to process spread, compensation due to environmental changes, performance tuning, automatic reconfigurability, and built-in self-test.

Instructor: Robert Bogdan Staszewski received his PhD from the University of Texas at Dallas in 2002 for his research on RF frequency synthesis in digital deep-submicron CMOS. From 1991 to 1995, he worked at Alcatel Network Systems in Richardson, TX. He joined Texas Instruments in Dallas, TX, in 1995 where he holds an elected title of Distinguished Member of Technical Staff for his pioneering work on Digital RF Processor (DRP™) architecture. He is currently a Chief Technical Officer (CTO) of the DRP system and design development group. He has authored and co-authored 80 journal and conference publications and holds 40 issued and 60 pending US patents.

T5: Display and RFID-Tag Design Using Organic Transistors
Electronics based on organic semiconductors has demonstrated its potential to enable printing of complex electronics functions on large-area, paper-like, flexible surfaces. Using high-speed throughput printing instead of the conventional lithography-based manufacturing technology should also enable low-cost products. Typical organic electronics applications are flexible displays, solar cells, light-emitting surfaces, RFIDs and physical, chemical or bio sensors.

This tutorial presents basic modeling of thin-film transistors manufactured with organic semiconductors (OTFTs) and state-of-the-art techniques to design, using organic TFTs, display backplanes, digital electronics and RFID radios.

Instructor: E. Cantatore received his PhD in Electrical Engineering from Politecnico di Bari, Italy in 1998. After a postdoc at CERN, Geneva, Switzerland, where he worked on radiation-hard electronics for particle sensors, he joined Philips Research, Eindhoven, The Netherlands. At Philips he designed some of the first displays based on organic transistor backplanes and strongly contributed to the development of organic RFIDs. His research interests cover as well ultra-low-power analog CMOS design and biomedical applications. In 2007, he joined the Electrical Engineering department of the Eindhoven University of Technology. He has published more than 70 papers in international conferences and journals, holds 10 patents and patent applications and gave invited talks on organic electronics at ESSDERC, DATE, ESSCIRC, BCTM and E-MRS. He serves on the ITPC of ESSDERC and ISSCC, which granted him, in 2006, the Beatrice Winner Award for a paper on organic RFIDs.

T6: SAR ADCs
Technology scaling is offering MOS transistors with higher-frequency capabilities but lower inherent analog gain.

In this scenario, ADC designers must account for the performance sensitivity of their converters to decreasing opamp gain. Thus, alternative ADC topologies that can trade higher operation speed with lower opamp-gain sensitivity have to be developed. Successive-approximation register (SAR) structures are one of the candidate topologies that have experienced a resurgence in recent years.

In this tutorial the basic concepts underlying SAR ADCs will be presented. The most popular implementations will be discussed (charge redistribution, resistive DACs, charge sharing), and recent developments that have allowed SAR ADCs to become the record holders in terms of ADC figure-of-merit will be introduced (redundancy, comparator noise tolerance).

Instructor: Andrea Baschirotto is an Associate Professor at the University of Milano-Bicocca. His main research interests are in the design of mixed-analog/digital integrated circuits, in particular for low-power and/or high-speed signal processing. He has authored or co-authored more than 190 papers in international journals and presentations at international conferences, 1 book, 6 book chapters, and holds 29 USA patents. He has been Associate Editor for the IEEE Transactions on Circuits Systems: Parts I and II. He was the Technical Program Committee Chairman for ESSCIRC 2002. He has collaborated with several companies on the design of mixed-signal ASICs. He participates in several research collaborations, also funded by national and European projects.

T7: Managing Variations Through Adaptive Design Techniques
CMOS technology scaling has given rise to increased sensitivity of design to process, voltage and temperature (PVT) variations as well as to aging effects. These uncertainties have led to ever-larger design margins intended to ensure correct operation under all conditions which result in substantial performance and power losses. In this context, a new trend in adaptive design techniques has emerged where circuits are dynamically adjusted at runtime to compensate for PVT and aging effects. This Tutorial reviews the sources of uncertainty and their classification, and describes techniques for dynamic compensation and adaptive control. Particular emphasis is given to so-called canary circuits, PVT monitors, and adaptive voltage and frequency synthesis. The discussion examines current industrial practice as well as highlighting future trends coming from industrial and academic research.

Instructor: David Blaauw received his BS in Computer Science and Physics from Duke University and his Ph.D. in Computer Science from the University of Illinois, Urbana-Champaign. He worked for Motorola for 8 years as a manager in the Advanced Design Technology group. Since 2001, he has been on the faculty at the University of Michigan, Ann Arbor. His research interests include low-power and high-performance design. He has authored over 250 papers and holds 25 patents. He is a member of the ISSCC Technical Program Committee and has served as chair of the International Symposium on Low Power Electronic Design (ISLPED) and as an executive committee member of the Design Automation Conference.

T8: Variation-Tolerant SRAM Circuit Designs
This Tutorial begins with a discussion of a basic understanding of SRAMs and then describes the challenges and some of the key circuits required for a robust design. Threshold-voltage variation is a critical factor in designing memories at 45nm and below, due to process variation. Various circuit techniques that enable continued area and voltage scaling are shared in this Tutorial. Comparison of the circuit techniques presented at leading conferences for design of 65nm and beyond are discussed, and an overview is presented.

Statistical design methods along with circuit-based design-margin assist techniques and their effect on process, voltage, and temperature variations are discussed in detail.

- Overview of SRAM applications and scaling
- Operating voltage and area scaling trends and key challenges
  - Static-noise margin (SNM)
  - Write margin (WRM)
  - Cell-current margin (I_{CELL})
- Statistical-margin analysis methods
- Circuit-design techniques
- Discussion of the scalability of circuit techniques

Instructor: Hiroyuki Yamauchi is a Professor at the Fukuoka Institute of Technology in Fukuoka, Japan. Previously, he worked for Panasonic in Japan for 20 years, having responsibility as a general manager for developing embedded SRAM, DRAM, and nonvolatile memories. He has invented and developed various SRAM and DRAM circuit design techniques, such as charge-recycling data-bus architecture and a control scheme for elevating SRAM source line potential for leakage reduction and variability tolerance. He holds 87 US patents and has published over 40 papers in the area of memory design. He received his PhD in Engineering in 1997 from the University of Kyushu in Fukuoka, Japan.

T9: Managing Linearity in Radio Front-Ends
Radio front-end linearity requirements can pose a major challenge in the design of receivers for several commercial wireless systems. In this presentation, we will explore circuit techniques and architectures that address this issue, with an emphasis on approaches that reduce the requirement for off-chip passive filters. Basic concepts related to front-end dynamic range, including noise performance and mechanisms for non-linearity-induced performance degradation will be introduced. Design approaches that are useful for improving receiver linearity, such as feedback and feedforward; the use of on-chip filters and frequency-selective terminations; and approaches that utilize multiple receiver paths will be presented, along with relevant examples from practical wireless systems. The impact of these techniques on dynamic range will be considered.

Instructor: Ranjit Gharpurey is an Associate Professor in the Department of Electrical and Computer Engineering at the University of Texas at Austin. His primary research interests are in the areas of high-frequency and high-speed circuit design with emphasis on RFIC design for wireless applications, and parasitic noise sources in integrated circuits. He received his Ph. D. from the University of California at Berkeley in 1995 and his B. Tech (Bachelor of Technology) from the Indian Institute of Technology, Kharagpur, India in 1990.

T10: CMOS Circuit Techniques for High-Speed Wireline Transceivers
This tutorial covers the modern CMOS design techniques for high-speed wireline communications operating at tens of Gb/s. Starting from the architecture-level illustration which explains the necessity and applications of the high-speed blocks, this talk conveys popular design skills and typical considerations on voltage-controlled oscillators, frequency dividers, and broadband amplifiers. Design methodology will be included to investigate the circuit optimization, and case study will be given in the end to introduce the state-of-the-art.

Instructor: Jri Lee received the M.S. and Ph.D. degrees in electrical engineering from the University of California, Los Angeles (UCLA), both in 2003. He joined National Taiwan University (NTU) since 2004, where he is currently Associate Professor of electrical engineering. He is now serving in the Technical Program Committees of the ISSCC, Symposium on VLSI Circuits, and A-SSCC. Prof. Lee received the Beatrice Winner Award for Editorial Excellence at the 2007 ISSCC, the Takuo Sugano Award for Outstanding Far-East Paper at the 2008 ISSCC, and NTU Outstanding Teaching Award in 2007 and 2008.

F1: SSD Memory Subsystem Innovation

Organizer & Session Chair: **Ken Takeuchi,** *University of Tokyo, Tokyo, Japan*

Organizing Committee:
Hideto Hidaka, *Renesas Technology, Itami, Japan*
Frankie Roohparvar, *Micron, San Jose, CA*
Kevin Zhang, *Intel, Hillsboro, OR*
Mark Bauer, *Numonyx, Folsom, CA*
Roberto Gastaldi, *Numonyx, Brianza, Italy*
Joo Sun Choi, *Samsung Electronics, Gyeonggi, Korea*
Dae Seok Byeon, *Samsung Electronics, Gyeonggi, Korea*
Daisaburo Takashima, *Toshiba, Yokohama, Japan*

This Forum addresses a broad range of key technical challenges facing designers of today's VLSI memory systems. The Forum starts with an overview of microprocessor memory architectures. It explores the challenges, implications and options available to remove traditional memory bottlenecks such as memory latency, memory bandwidth, and off-package bandwidth in the Moore's-Law-driven multi- and many-core systems. Next, system-level memory architecture is addressed. The widespread use of NAND Flash memories in SSDs and caches has opened new avenues of innovation for the enterprise- and client-computing segments. System-wide architectural changes are required to make full use of the advantages of SSDs in terms of performance, reliability and power. Circuit design and reliability challenges of NAND-Flash-memory-based SSDs are also discussed. In emerging multimedia applications, a higher bandwidth and therefore a faster-random-access memory is required. NAND flash memory is also playing a more important role because write-performance improvement improves user experience of high-speed wireless downloads. This Forum also discusses fusion memory where innovative memory designs provide flexibility to handset manufacturers allowing them to better balance cost and performance of many types of multimedia handset designs. In addition, in the Forum, three key emerging nonvolatile memories (PCRAM, FeRAM, and MRAM) and their memory systems are examined. Nonvolatile random-access memory is becoming a viable alternative to commonly used volatile and nonvolatile memories in the marketplace. Being bit-alterable like DRAM, nonvolatile like Flash, and CMOS-process compatible, nonvolatile random-access memory has the potential to revolutionize many aspects of computing-platform architectures. Further, the Forum also discusses leading-edge emerging memories and their application to computing and storage architectures. The Forum also provides an excellent opportunity for the attendees to interactively engage with the speakers on any key technical issues they may face in their product development.

Forum Agenda

Time	Topics
8:00	Breakfast
8:20	**Introduction** **Ken Takeuchi,** *University of Tokyo, Tokyo, Japan*
8:30	**Microprocessor Memory Architecture** **Konrad Lai**, *Intel, Hillsboro, OR*
9:20	**System-level Memory Architecture** **Amber Huffman,***Intel, Hillsboro, OR*
10:10	Break
10:25	**NAND Flash Memory Circuit** **Daisaburo Takashima,** *Toshiba, Yokohama, Japan*
11:15	**NAND Flash Memory Reliability** **Seiichi Aritome,** *Powerchip, Hsinchu, Taiwan*
12:05	Lunch
1:00	**SSD** **Dean Klein,** *Micron, Boise, Boise, ID*
1:50	**Fusion Memory and Memory System,** **Tony Kim,** *Samsung, San Jose, CA*
2:40	Break
2:55	**PCRAM and Memory System,** **Sean Eilert,** *Numonyx, Santa Clara, CA*
3:45	**FeRAM and Memory System,** **Hiromitsu Kimura,** *Rohm, Kyoto, Japan*
4:35	**MRAM and Memory System,** **Tadahiko Sugibayashi,** *NEC, Sagamihara, Japan*
5:25	Conclusion

F2: Medical Image Sensors

Organizer: **Boyd Fowler,** *Fairchild Imaging, Milpitas, CA*

Committee:
Makoto Ikeda, *University of Tokyo, Tokyo, Japan*
Hirofumi Sumi, *Sony, Kanagawa, Japan*
Jan Bosiers, *Dalsa Professional Imaging, Eindhoven, Netherlands*
Johannes Solhusvik, *Aptina Imaging, Oslo, Norway*
Daniel McGrath, *Eastman Kodak, Rochester, NY*

Although image sensors in medical and biotech applications are ubiquitous, new technologies and applications are being developed every year. CCD, CMOS, and TFT image sensor technologies are fueling these applications and enabling lower-cost and higher-performance systems. This forum is focused on presenting the newest image-sensor technologies and applications for the medical and biotech markets. The speakers at this forum are experts in their fields. They are invited to present the latest material on the various topics. The goal of this forum is to give engineers and their management an in-depth view of these technologies and their future directions.

Forum Agenda:

Time	Topic
8:00	Breakfast
8:15	**Introduction** **Boyd Fowler,** *Fairchild Imaging, CA*
8:30	**Medical Image Sensor Technology Overview** **Keishi Kitamura,** *Shimadzu Medical Systems Division, Kyoto, Japan*
9:30	**Dental Radiography** **Chiao Liu**, *Fairchild Imaging, Milpitas, CA*
10:30	Break
11:00	**Medical Radiography** **Tim Tredwell**, *Carestream Health, Rochester, NY*
12:00	Lunch
1:00	**Endoscopy** **Jeffrey Adair,** *Micro-Imaging Solutions, San Clemente, CA*
2:00	**Luminescence and Fluorescence Imaging** **Mark Schnitzer**, *Stanford University, Stanford, CA*
3:00	Break
3:30	**Retinal Implants** **Jun Ohta**, *Nara Institute of Science & Technology, Nara, Japan*
4:30	Panel Discussion and Conclusions

F3: GIRAFE: 4G RF Frontends

Organizer: **Stefan Heinen,** *RWTH Aachen University, Aachen, Germany*

Co-Organizer: **Domine Leenaerts,** *NXP, Eindhoven, Netherlands*

Committee: **Tony Montalvo,** *Analog Devices, Raleigh, NC*
Satoshi Tanaka, *Renesas, Komoro, Japan*
Domine Leenaerts, *NXP, Eindhoven, Netherlands*
Aarno Pärssinen, *Nokia Corporation, Helsinki, Finland*
Didier Belot, *ST Microelectronics, Crolles, France*
Marc Tiebout, *Infineon Technologies, Villach, Austria*

Digital cellular standards have emerged over the last 20 years. Today, 2G systems like GSM/EDGE are providing worldwide coverage for voice and basic data services. The increasing demand of true mobile users for high-speed data services has forced the development of 3G toward HSPA. The next step in this evolution is the adoption of OFDM for cellular applications in systems like WiMAX and LTE. The user equipment should be compatible with all standards from 2G up to 4G in order to provide the best possible experience to the end user.

Therefore, the integration of RF transceivers must cope with multiple frequency bands, and multiple modulation schemes as well as MIMO techniques. Nanoscale CMOS provides the flexibility to integrate reconfigurable circuits, which are enhanced or assisted by elaborate digital techniques like calibration, predistortion and $\Delta\Sigma$ modulation.

Moreover, the speed of nanoscale CMOS will open the opportunity for new “Digital RF” techniques.

Last but not least the RF transceiver must address the issue of an increasing number of frequency bands in order to keep the form factor of the phone constant. The elimination of bulky front-end filters and the reduction of the number of required power amplifiers will be a future challenge.

The forum will conclude with a panel discussion addressing the question “4G Introduction: Revolution or Evolution?” where the attendees have the opportunity to ask questions and to share their views.

Attendance is limited and pre-registration is required. This all-day forum encourages open information exchange.

The targeted participants are circuit designers and concept engineers working on wireless systems, who want to learn about the impact of nanoscale technologies in circuit and system design.

Forum Agenda

Time	Topic
8:00	Breakfast
8:15	**Introduction** **Stefan Heinen,** *RWTH Aachen University, Aachen, Germany*
8:30	**Next Generation Mobile Access Network —Super 3G and beyond—** **Atsushi Murase,** *NTT DOCOMO, Japan*
9:15	**RF Challenges for 3G, 4G and Beyond.** **Stefan Heinen,** *RWTH Aachen University, Aachen, Germany*
10:00	Break
10:30	**Wireless Communications ICs: Trends for 3G and LTE** **Sven Mattisson,** *Ericsson, Lund, Sweden*
11:15	**RF Transceivers from 3.x Toward 4G/OFDM-Based Systems** **Christopher Hull,** *Intel, Hillsboro, OR*
12:00	Lunch
1:00	**Reconfigurable RF Front-Ends for 3.9G and 4G** **Pasi Tikka,** *EPCOS, Munich, Germany*
1:45	**Reconfigurable ADCs for 3.xG and 4G** **Yiannos Manoli,** *IMTEK, Freiburg, Germany*
2:30	Break
3:15	**SDR RF Front-Ends** **Asad Abidi,** *University of California, Los Angeles, CA*
4:00	**Application of SDR Softransceivers to 4G Markets** **Geoff Dawe,** *BitWave Semiconductor, Lowell, MA*
4:45	Panel Discussion
5:15	Conclusion

F4: Ultra-Low-Voltage Circuit Design

Organizer: **Rajeevan Amirtharajah,** *University of California, Davis, CA*

Committee: **Tzi-Dar Chiueh,** *National Taiwan University, Taipei, Taiwan*
Ram Krishnamurthy, *Intel, Hillsboro, OR*
Jos Huisken, *IMEC, Eindhoven, Netherlands*
Siva Narendra, *Tyfone, Portland, OR*
Steffen Paul, *Universität Bremen, Bremen, Germany*
Pascal Urard, *STMicroelectronics, Crolles, France*
Alice Wang, *Texas Instruments, Dallas, TX*

Low-power CMOS design has relied heavily on V_{DD} scaling, in the past, to exploit the quadratic dependence of dynamic power and the exponential dependence of leakage power on voltage. Today, leading-edge low-voltage designs are pushing FET operation into the weak inversion and subthreshold regimes. Investigators around the world are reporting circuits at voltages between 180mV and 700mV that offer performance that could support a range of applications in wireless sensors, mobile phones, biomedical devices, and ultra-mobile PC's. However, these circuits are highly sensitive to variations in temperature and process. Ultra-low-voltage circuits will be increasingly challenging to design as feature sizes shrink. Current trends indicate nominal supply voltages are unlikely to be reduced much below 1V, transistor threshold voltages will likely remain between 0.3 and 0.4V to manage subthreshold leakage, and effects such as random dopant fluctuation will increase the spread in transistor parameters, all of which create difficulties in designing robust circuits at low V_{DD}. This forum brings together leading experts to describe future challenges in ultra-low-voltage design, to explore ultra-low-voltage circuit techniques, and to stimulate thinking about prospects for future ultra-low-voltage high-volume products.

Forum Agenda

Time	Topic
8:00	Breakfast
8:20	**Introduction** **Raj Amirtharajah,** *University of California, Davis, CA*
8:30	**Motivation for Ultra-low Voltage / Low Power Designs** **Christian Piguet,** *CSEM, Neuchatel, Switzerland*
9:10	**Technology Scaling and Challenges for Ultra-low Voltage Design** **Kaushik Roy,** *Purdue University, West Lafayette, IN*
9:50	Break
10:10	**Device Sizing for Variability in Energy Constrained Systems** **Dennis Sylvester,** *University of Michigan, Ann Arbor, MI*
10:50	**Variability and Ultra-low Voltage Logic Design** **Takayasu Sakurai,** *University of Tokyo, Tokyo, Japan*
11:30	**Ultra-low Voltage Microprocessor Design: Challenges and Solutions** **Ram Krishnamurthy,** *Intel, Hillsboro, OR*
12:10	Lunch
1:00	**Challenges and Opportunities for Scaled Low Voltage SRAM** **Ben Calhoun,** *University of Virginia, Charlottesville, VA*
1:40	**Ultra-low Voltage Analog Circuit Design** **Christian Enz,** *EPFL, Lausanne, Switzerland*
2:20	**Probabilistic CMOS (PCMOS) Logic for Nanoscale Circuit Design** **Krishna Palem,** *Rice University, Houston, TX*
3:00	Break
3:20	Panel Discussion: Future Prospects for Ultra-low Voltage Design in Commercial Products
4:10	Conclusion

SE1: Healthy Radios: Radio & Microwave Devices for the Health Sciences

Organizer: **Jacques C. Rudell,** *University of Washington, Seattle, WA*
Ali Hajimiri, *Caltech, Pasadena, CA*

Chair: **Jacques C. Rudell,** *University of Washington, Seattle, WA*

More than a century ago, Guglielmo Marconi made the first transatlantic radio transmission which forever changed the way people exchange information with one another. Scientists and engineers have spent the better part of the last century developing more efficient radio circuits, systems and software for wireless communication. Recently, the scientific community has begun exploring the use of radio-frequency circuits for biomedical applications. These "Healthy Radios" can be categorized into two sub-topics. The first is the use of radios to communicate sensed information from the human body to the outside world. The second is the use of traditional radio circuits for medical analysis. The first two speakers in the "Healthy Radio" session explore the use of radio circuits for biomedical sensing and diagnosis, such as early cancer detection or Protein and DNA analysis. The next two speakers describe current work on communication with radios links for body area networks (BAN) and implantable devices. The session concludes with an overview of the state-of-the-art in CMOS medical imaging.

Time	Topic
8:00	**CMOS RF Biosensor Utilizing Nuclear Spin Resonance – An RF Designer's Approach to Early Cancer Detection** **Donhee Ham,** *Harvard University, Cambridge, MA*
8:20	**Integrated Radio-Frequency Biosensors for POC Applications** **Ali Hajimiri,** *Caltech, Pasadena, CA*
8:40	**BANning Low Power Radio Design** **Brian P. Otis,** *University of Washignton, Seattle*
9:00	**Wireless Telemetry Plays a Significant Role in Orchestrated Care: Concerto™/Virtuoso™ with MICS Frequency Band** **Javaid Masoud,** *Medtronic, Minneapolis, MN*
9:20	**Medical Imaging: RF Radio Design to the Rescue** **Kris Iniewski,** *CMOS Emerging Technologies, Vancouver, Canada*

SE2: Is Fabless MEMS Fabulous?

Organizer: **Farrokh Ayazi,** *Georgia Institute of Technology, Atlanta, GA*

Moderator: **Christoph Hagleitner**, *IBM, Rüschlikon, Switzerland*

Recent years have witnessed the maturity of MEMS in automotive safety applications and their penetration into cost-sensitive consumer markets. With the emergence of consumer applications for sensors and reconfigurable radio, the MEMS industry is at a growth inflection point. Many start-ups are trying to bring low-cost devices to market using a fab-less or a fab-lite business model. Despite this, successful commercialization stories are sparse among MEMS start-ups and are mostly related to the larger and more established companies that have commercialized MEMS after many years of costly internal research and development for high-price margin applications. When it comes to MEMS, is fabless fabulous? Or are in-house fabs invaluable? Are today's MEMS low-cost enough to compete and survive in consumer markets?

Panelists:

Janusz Brizek, *LV Sensors, Emeryville, CA*
Kaigham J. Gabriel, *Akustika, Pittsburgh, PA*
Michael Judy, *Analog Devices, Cambridge, MA*
Edvard Kälvesten, *Silex Microsystems, Järfälla, Sweden*
Arthur S. Morris, *wiSpry, Irvine, CA*

PLENARY SESSION - INVITED PAPERS

Chair: **Timothy Tredwell**, *Carestream Health, Rochester, NY*
ISSCC Executive-Committee Chair

Associate Chair: **William Bowhill**, *Intel, Hudson, MA*
ISSCC Program-Committee Chair

FORMAL OPENING OF THE CONFERENCE **8:15AM**

1.1 Leaner and Greener: Adapting to a Changing Climate of Innovation 8:30AM

René Penning de Vries, *CTO, NXP Semiconductors, Eindoven, Netherlands*

The semiconductor industry has been the enabling technology that has driven many huge changes in everyday life. Personal computing, mobile communications, Internet, and broadband technology, are obvious examples. Now, a new challenge is facing the industry – energy and power management – but not simply the concern for longer mobile battery life!

A new vision is needed for the semiconductor industry; how can our technologies help to improve everyone's use of energy to meet the challenges of climate change and limited supplies? Firstly, we need a vision of what can be achieved, in terms of how the semiconductor industry can make significant changes to the energy needs of different application sectors. Obvious targets are the sectors where large energy consumption is common, such as consumer-appliance, lighting, and automotive, and where there are large amounts of electronics, such as PCs and TVs, running continuously. Improved efficiency due to semiconductor technology can make a real difference. For every 1% saved in the world's electricity consumption, roughly 40 fewer power stations are required!

At the same time, we need a technological vision of how semiconductor technology must advance and evolve for more improvements to be realised. Device technologies, such as high voltage and high power, need to be combined with new sensors and control, while operating over extended temperature ranges to provide energy-conserving control and management of systems previously not economic to address. This plenary presentation will explore how the semiconductor industry can go beyond traditional approaches and make bigger reductions in the energy demands of the modern world.

1.2 Adaptive Circuits for the 0.5-V Nanoscale CMOS Era 9:10AM

Kiyoo Itoh, *Fellow, Hitachi Tokyo, Japan*

Low-voltage scaling limitations are one of the major problems in the nanoscale era – they bring evermore-serious power crises with device scaling. The problems stem from the existence of two unscalable device parameters: The first is the high value of the lowest necessary threshold voltage (V_{t0}) of MOSFETs needed to keep the subthreshold leakage low; The second is the variation in threshold (ΔV_t) that has increased in the nanoscale era. Due to these two inherent features of V_{t0} and ΔV_t, the minimum usable power supply (V_{DD}), namely, V_{min} increases with device scaling. The actual operating voltage V_{DD} is thus facing the 1-V wall in the 45-nm generation and is expected to rapidly increase with further scaling of poly-Si bulk MOSFETs.

Another problem in the nanoscale era, that is, the ever-higher interconnect resistance, is also closely related to the voltage-limitation problem at the chip and subsystem levels: It further increases the actual operating voltage, since, while it degrades the speed of ever-larger chips, it reduces power-supply integrity by increasing power-supply droop and noise in power-supply lines. For the ULSI industry to continue to proliferate, the voltage-scaling-limitation problem must be solved in the 32-nm generation and beyond. This requires a multidisciplinary approach, since it covers various fields, such as, devices, circuits (digital and analog), and subsystems.

This Plenary talk will address issues related to adaptive circuits and relevant technologies intended to reduce V_{min} and ensure power-supply integrity. V_{min} reduction is described in the first half. After comparing V_{min} values for several blocks, namely, logic, SRAM and DRAM, state-of-the-art SRAM circuits which tackle the issue are reviewed. Then, devices and circuits to reduce the values of V_{min} to the sub-1-V region, such as ΔV_t-scalable FinFETs and low-V_{t0} low-leakage circuits utilizing the gate-source back-biasing scheme, are discussed. In the second half, the power-supply integrity issues are described. In addition to new architectures such as multi-core MPUs, and 3-D thermally conscious chip integration for compact subsystems, drastic reduction in memory-array area of small cores and chips is particularly vital to ensure integrity, since the array dominates their area. Thus, a logic-process-compatible FinFET DRAM cell, achieved using a unique cell and array selection scheme, is proposed. Finally, a scenario for achieving sub-0.5-V supply in nanoscale CMOS is presented.

ISSCC, SSCS, JSSCC, & IEEE AWARD PRESENTATIONS 9:50AM

BREAK 10:20AM

1.3 The New Era of Scaling in an SoC World 10:35AM

Mark Bohr, *Senior Fellow, Intel, Hillsboro, OR*

Traditional MOSFET scaling served our industry well for about 30 years, until limits posed by leakage and total chip power were reached earlier in this decade. To overcome these limits we have entered a new era of scaling, where innovations in device materials and transistor structure are just as important as simple scaling of dimensions for achieving continued improvements in density and performance. Examples of these types of innovations began with the introduction of copper and low-resistivity interconnects, followed by strained-silicon transistors, and more recently, high-κ dielectrics along with metal-gate transistors.

Circuit layout has also faced severe challenges in meeting high density and low variability as minimum feature sizes have scaled below the wavelength of light used for patterning. Lithography-enhancement techniques such as optical- proximity correction, phase-shift masks and gridded layout have kept us on track for feature-size scaling. Although traditional MOSFET scaling techniques have not been good for analog circuits due to degraded transistor gain g_m/g_{ds}, reduced dynamic range, and worse, transistor mismatch, modern microprocessors have successfully incorporated a larger number, and a wider range, of high-performance analog circuits than in the past due to circuit innovations.

Adaptive circuits have been employed to a greater degree to overcome device-variability limitations and to more finely tune performance and power characteristics. Some of the process and design techniques employed on new microprocessor products will be described along with research options being explored for the 22nm generation and beyond. The goal of these research efforts will be increasingly focused on SoC products that integrate a diverse set of device types, adapting to meet a broader range of product functions and applications than those that are available today!

1.4 Kids Today! Engineers Tomorrow? 11:15AM

John Cohn, *Fellow, IBM Systems and Technology Group, Essex Junction, VT*

Imagine the next generation of engineers. What will they be like? Will there be enough of them worldwide? What will motivate them to join us in the profession we love?

This Plenary presentation will take a look at engineering-enrolment trends worldwide, and try to make sense of the numbers. We will explore the so called “engineering crisis”, and understand what is going on. Is this a world issue, or “only” an issue in the West? Why are kids in certain parts of the world not joining our field? What are they doing instead? Does the answer lie in how society views and portrays our professions? If so, what can we, as practitioners, do to change those perceptions?

In this plenary presentation we will try to understand the real story behind these questions, from a worldwide perspective, and what they mean to the future of our industry. We will look at what motivates kids these days and explore how this resonates with the messages kids are hearing about engineering careers today. We will look at how we can help change the conversation around the engineering profession using a new set of messages and a new set of “Grand Challenges” based on world issues such as energy, climate and global sustainability.

Messages alone are not going to change the future! The only thing that will shape the future of our industry is you the engineer. We will take a look at how each of us has the opportunity to pass on our love and passion of our field to the next generation. We will look at outreach activities that you and your colleagues can start now to pass that passion along and to recharge your own batteries in the process. We will look at specific things you can begin doing to do in your own homes, schools, communities and nations and in the mass media and the Internet. We will also look at ways that you the engineer can use your influence in your own companies, universities and professional societies to magnify your efforts. We will include a few “shocking” demonstrations to drive these points home. Please come and begin helping us shape a better world by helping build the next generation of engineers. It is an important job….. , and we are the only ones who can do it!

Conclusion 11:55AM

IMAGERS

Session Chair: Jan Bosiers, DALSA Professional Imaging, Eindhoven, Netherlands
Associate Chair: Makoto Ikeda, University of Tokyo, Tokyo, Japan

2.1 A 4-Side Tileable Back-Illuminated 3D-Integrated Mpixel CMOS Image Sensor

1:30 PM

V. Suntharalingam[1], R. Berger[1], S. Clark[2], J. Knecht[1], A. Messier[1], K. Newcomb[1], D. Rathman[1], R. Slattery[1], A. Soares[1], C. Stevenson[1], K. Warner[1], D. Young[1], L. Ang[3], B. Mansoorian[3], D. Shaver[1]
[1]MIT Lincoln Laboratory, Lexington, MA
[2]Irvine Sensors, Costa Mesa, CA
[3]Forza Silicon, Pasadena, CA

A 3D-integrated back-illuminated 1Mpixel CMOS image sensor tile includes a stack of 2×32-channel vertically integrated ADC chips, and requires 13.4µm of silicon perimeter to the pixel array. The tile and system connector design supports 4-side abuttability and burst data rates of 1Mpixel in 1ms.

2.2 A Gamma, X-Ray and High-Energy-Proton Radiation-Tolerant CIS for Space Applications

2:00 PM

L. Carrara[1], C. Niclass[1], N. Scheidegger[1], H. Shea[1], E. Charbon[1,2]
[1]EPFL, Lausanne, Switzerland
[2]Delft University of Technology, Delft, Netherlands

This paper presents a 0.35µm CIS that is tolerant to gamma, X-ray and 11MeV/60MeV proton radiation. Its core is an array of 32×32 pixels each containing a static memory and a single-photon detector. A 2-gray-level frame is transfered in 1.2µs. The chip tolerates 1Mrad of gamma, 40krad of proton, and 1mGy of X-ray radiation. The dark-count-rate degradation is contained or negligible.

2.3 A 4-Channel 20-to-300Mpixel/s Analog Front-End with Sampled Thermal Noise Below kT/C for Digital SLR Cameras

2:30 PM

R. Kapusta[1], E. Ibaragi[2], K. Ni[3], R. Wang[3], H. Shinozaki[2], L. Singer[1], K. Nakamura[1]
[1]Analog Devices, Wilmington, MA
[2]Analog Devices, Tokyo, Japan
[3]Analog Devices, Beijing, China

A 0.18µm CMOS 4-channel AFE for digital SLR cameras is reported that is optimized for clock rates of 5 to 75MS/s/channel and that uses nonlinear adaptive biasing based on clock frequency. Optimization techniques for a multi-channel system achieve -85dB crosstalk and 0.01% channel mismatch. Sub-kT/C sampling achieves 80dB DR and uses capacitors that are 60% smaller than normal.

Break 3:00 PM

2.4 A 1/2.5-inch 8Mpixel CMOS Image Sensor with a Staggered Shared-Pixel Architecture and an FD-Boost Operation

3:15 PM

N. Tanaka, J. Naruse, A. Mori, R. Okamoto, H. Yamashita, M. Monoi
Toshiba Semiconductor, Yokohama, Japan

A 1/2.5-inch 8Mpixel CMOS image sensor employs a staggered shared-pixel architecture to suppress Gr/Gb sensitivity imbalance. It also employs an FD-boost operation using the C_{GS} and C_{GD} of amplifier transistors to yield large FD capability and low dark random noise. It achieves a Gr/Gb sensitivity ratio of 99.7%, random noise of 2.6e^-_{rms} and a pixel capacity of 7.7ke^-.

2.5 An SoC Combining a 132dB QVGA Pixel Array and a 32b DSP/MCU Processor for Vision Applications

3:45 PM

P-F. Rüedi, P. Heim, S. Gyger, F. Kaess, C. Arm, R. Caseiro, J-L. Nagel, S. Todeschini
CSEM, Neuchâtel, Switzerland

An SoC combining a QVGA time-domain logarithmic pixel array, a 50MHz 32b DSP/MCU processor and a 128KB SRAM achieves a 132dB intra-scene DR encoded in 10b, representing 149 steps per decade. Computation of contrast magnitude and direction in the readout path allows for visual scene analysis. The SoC achieves an FPN of 0.51 LSB, power consumption of 80mW and a 44mm^2 area in 0.18µm CMOS.

2.6 A 1/3.2-inch 3.3Mpixel CMOS Image Sensor with a Column-Signal-Addition Method Using a PMOS Column Amplifier

4:15 PM

H. Takahashi, T. Itano, T. Watanabe, K. Iwata, H. Akabori, S. Takimoto, R. Mishima, I. Ueno, K. Sakurai, T. Ichikawa, G. Momma, S. Inoue
Canon, Ayase, Japan

A 1/3.2-inch 3.3Mpixel CMOS image sensor is fabricated in a 0.15µm 1P3M CMOS process. A deep-photodiode-isolation pixel and PMOS column amplifier achieves 96µV/e^- conversion gain, 7.2e^-/s dark current at 60°C, and 2.5e^-_{rms} random noise. The sensor has a column-level signal-addition mode that realizes 15500e^-/lx·s sensitivity (green pixel) and interlace scan.

2.7 A Charge-Multiplication CMOS Image Sensor Suitable for Low-Light-Level Imaging

4:30 PM

R. Shimizu, M. Arimoto, H. Nakashima, K. Misawa, K. Suzuki, T. Ohno, Y. Nose, K. Watanabe, T. Ohyama, K. Tani
Sanyo Electric, Anpachi, Japan

A CIF-format charge-multiplication 0.35µm 2P4M CMOS image sensor with 10µm pixel pitch is presented. It can execute charge multiplication using impact ionization of photo-generated signals within each pixel. For a significant increase in SNR at low light levels, up to 60× charge multiplication is achieved at a readout speed of 100µs/frame.

2.8 A Dual-Conversion-Gain Video Sensor with Dewarping and Overlay on a Single Chip

4:45 PM

A. R. Huggett[1], C. Silsby[2], S. Cami[1], J. Beck[2]
[1]Aptina Imaging, Bracknell, United Kingdom; [2]Aptina Imaging, Corvallis, OR

A 47mm^2 video sensor SoC comprises a 60fps 640×480 array of dual-conversion-gain 5.6µm pixels with >80dB DR, noise floor of <1e^-_{rms} and switchable sensitivities of 2.5V/lx·s or 11.9V/lx·s and corresponding PRNUs of 0.57% or 0.68%, a video processor for correcting optical warp of up to 96 lines together with perspective adjustment, and a video overlay circuit.

Conclusion 5:15 PM

MICROPROCESSOR TECHNOLOGIES

Session Chair: Sonia Leon, Sun Microsystems, Santa Clara, CA
Associate Chair: Fabio Campi, STMicroelectronics, Agrate Brianza, Italy

3.1 A 45nm 8-Core Enterprise Xeon® Processor

1:30 PM

S. Rusu, S. Tam, H. Muljono, J. Stinson, D. Ayers, J. Chang, R. Varada, M. Ratta, S. Kottapalli
Intel, Santa Clara, CA

An 8-core 16-thread enterprise Xeon® processor has 2.3B transistors in 9M 45nm CMOS. The I/O links use per-lane TX and RX compensation to enable operation up to 6.4GT/s. Vertical and horizontal spines keep the uncore clock skew under 19ps before engaging the compensation. Core and cache shut-off techniques are used to minimize leakage.

3.2 A Family of 45nm IA Processors

2:00 PM

R. Kumar, G. Hinton
Intel, Hillsboro, OR

A family of next-generation IA processors with up to 8 cores, enhanced Core™ microarchitecture, 3-level caches and 2-way SMT is implemented in 45nm high-κ metal-gate CMOS. The family has a coherent point-to-point link and integrates memory controller, power-management microcontroller and power-gate transistors and scales from sub-10 to 130W in mobile, desktop and server applications.

3.3 A Chip-Stacked Memory for On-Chip SRAM-Rich SoCs and Processors

2:30 PM

H. Saito, M. Nakajima, T. Okamoto, Y. Yamada, A. Ohuchi, N. Iguchi, T. Sakamoto, K. Yamaguchi, M. Mizuno
NEC, Kanagawa, Japan

A dynamically reconfigurable memory chip with 3D integration is fabricated, in which on-chip memories of an SoC chip are moved to the memory chip to increase the efficiency of memory usage. Area overhead of network interconnects for the memory chip is reduced by 63% and the latency overhead by 43%. Signal lines between the two chips are directly connected by 10μm-pitch inter-chip electrodes.

Break 3:00 PM

3.4 Dynamic Frequency-Switching Clock System on A Quad-Core Itanium® Processor

3:15 PM

A. Allen, J. Desai, D. Mulvihill, F. Verdico, F. Anderson
Intel, Fort Collins, CO

The clock system for a 700mm^2 65nm quad-core Itanium® processor has a cascaded PLL architecture and enables dynamic frequency switching with a single-cycle switch penalty and minimal di/dt impact, which minimizes power-supply disturbance. This allows frequency-power optimization without stopping the clock.

3.5 Secure AES Engine with A Local Switched-Capacitor Current Equalizer

3:45 PM

C. Tokunaga, D. Blaauw
University of Michigan, Ann Arbor, MI

A 0.13µm CMOS AES engine uses a switched-capacitor current equalizer to reduce leakage of side-channel information through the power supply, improving security against secret-key attacks, such as DPA. The design has 7.2% area, 33% power and 2× performance overheads compared to differential logic and noise addition, which have 3× area, 4× power, and 4× performance penalties.

3.6 A 4Gb/s/ch 356fJ/b 10mm Equalized On-chip Interconnect with Nonlinear Charge-Injecting Transmit Filter and Transimpedance Receiver in 90nm CMOS

4:15 PM

B. Kim, V. M. Stojanovic
Massachusetts Institute of Technology, Cambridge, MA

A link with 3-tap pre-distorted charge-injection transmit filter and transimpedance receiver in 90nm CMOS achieves 4Gb/s/ch intra-chip communication over 10mm-long global wires at 2µm link pitch, 356fJ/b energy cost, and transceiver area of 1760µm^2. The *in situ* measured eye is 98mV and 50% UI at 4Gb/s.

3.7 Dual-DLL-Based CMOS All-Digital Temperature Sensor for Microprocessor Thermal Monitoring

4:30 PM

K. Woo[1], S. Meninger[2], T. Xanthopoulos[2], E. Crain[2], D. Ham[1]
[1]Harvard University, Cambridge, MA
[2]Cavium Networks, Marlborough, MA

A CMOS all-digital temperature sensor for microprocessor thermal monitoring works by measuring temperature-dependent delays of CMOS inverters. It uses two fine-precision DLLs, occupies 0.12mm^2, and has a 5kS/s bandwidth at 7b resolution, dissipating 1.2mW. Measured errors for a 0.13µm CMOS implementation are -1.8 to 2.3°C across 0 to 100°C.

3.8 Over One Million TPCC with a 45nm 6-Core Xeon® CPU

4:45 PM

R. Kuppuswamy[1], S. R. Sawant[1], S. Balasubramanian[1], P. Kaushik[1], N. Natarajan[1], J. D. Gilbert[2]
[1]Intel, Bangalore, India
[2]Intel, Portland, OR

A monolithic 6-core Xeon® processor has 1.9B transistors in 9M 45nm CMOS with a 9MB L2 and 16MB L3 cache and exceeds 1M transactions/minute TPCC in 8-socket configuration. The FSB I/O circuits are implemented in the center of the die to reduce I/O latency. A low-leakage process variant with cache-sleep and shut-off modes enables low-power 6-core 65W and 4-core 50W variants.

Conclusion 5:15 PM

HIGH-SPEED DATA CONVERTERS

Session Chair: Boris Murmann, Stanford University, Stanford, CA
Associate Chair: Dieter Draxelmayr, Infineon Techologies, Villach, Austria

4.1 A 12b 2.9GS/s DAC with IM3 <-60dBc Beyond 1GHz in 65nm CMOS

1:30 PM

C-H. Lin[1], F. van der Goes[2], J. Westra[2], J. Mulder[2], Y. Lin[2], E. Arslan[2], E. Ayranci[2], X. Liu[2], K. Bult[2]
[1]Broadcom, Irvine, CA
[2]Broadcom, Bunnik, Netherlands

A 12b 2.9GS/s current-steering DAC implemented in 65nm CMOS is presented, with an IM3 <-60dBc beyond 1GHz, while driving a 50Ω load with an output swing of $2.5V_{pp\text{-}diff}$ and dissipating 188mW. The SFDR measured at 2.9GS/s is better than 60dB beyond 340MHz, while the SFDR measured at 1.6GS/s is greater than 60dB beyond 440MHz.

4.2 A 1.1V 50mW 2.5GS/s 7b Time-Interleaved C-2C SAR ADC in 45nm LP Digital CMOS

2:00 PM

E. Alpman[1,2], H. Lakdawala[1], R. Carley[2], K. Soumyanath[1]
[1]Intel, Hillsboro, OR
[2]Carnegie Mellon University, Pittsburgh, PA

A 7b 2.5GS/s Nyquist ADC is implemented in digital 45nm LP-CMOS by time-interleaving 16 C-2C SAR ADCs with radix, offset, gain and timing calibration. The ADC achieves >6.1 ENOB and <-49dBc SFDR for a single SAR, and >5.4 ENOB and <-43dBc SFDR for the time-interleaving SAR up to the Nyquist frequency. The ADC consumes 50mW on a 1.1V supply and achieves an FOM of 480fJ/conversion-step.

4.3 A 1.8V 1.0GS/s 10b Self-Calibrating Unified-Folding-Interpolating ADC with 9.1 ENOB at Nyquist Frequency

2:30 PM

R. C. Taft[1], P. A. Francese[1], M. R. Tursi[1], O. Hidri[1], A. MacKenzie[2], T. Hoehn[1], P. Schmitz[1], H. Werker[1], A. Glenny[3]
[1]National Semiconductor, Unterhaching, Germany
[2]National Semiconductor, Greenock, United Kingdom
[3]National Semiconductor, Santa Clara, CA

A 0.18µm CMOS folding-interpolating ADC that eliminates the separate coarse channel is presented. The single unified channel consists of cascaded folding stages with embedded comparators in which each stage acts as the coarse channel for the following one. The dual 1.8V 1.0GS/s 10b ADC yields ±0.2 LSB DNL and 9.1 ENOB at Nyquist.

Break 3:00 PM

4.4 A 5b 800MS/s 2mW Asynchronous Binary-Search ADC in 65nm CMOS

3:15 PM

Y-Z. Lin, S-J. Chang, Y-T. Liu, C-C. Liu, G-Y. Huang
National Cheng-Kung University, Tainan, Taiwan

A 5b asynchronous binary-search ADC with reference range prediction uses 2n-1 rather than 2^n-1 comparators. It also includes a passive THA, a reference ladder, 56 switches and static logic. The active area is 120×150µm^2 in 65nm CMOS. The ADC consumes 1.97mW from a 1V supply. At 800MS/s the ENOB is 4.45b and the ERBW is 500MHz. The FOM is 113fJ/conversion-step.

4.5 A 600MS/s 30mW 0.13µm CMOS ADC Array Achieving Over 60dB SFDR with Adaptive Digital Equalization

3:45 PM

W. Liu[1], Y. Chang[1,2], S-K. Hsien[1,3], B-W. Chen[3], Y-P. Lee[3], W-T. Chen[3], T-Y. Yang[3], G-K. Ma[3], Y. Chiu[1]
[1]University of Illinois, Urbana-Champaign, IL
[2]Jilin University, Changchun, China
[3]Industrial Technology Research Institute, Hsinchu, Taiwan

A 600MS/s 10-way time-interleaved SAR ADC array is fabricated in 0.13µm CMOS. Digital background equalization adaptively corrects the gain, offset, and linearity mismatch in the array, assisted by an algorithmic ADC. The prototype achieves 47.3dB peak SNDR and 65.2dB peak SFDR, while dissipating 30mW from a 1.2V supply.

4.6 A 10b 500MHz 55mW 90nm CMOS ADC

4:15 PM

A. Verma, B. Razavi
University of California, Los Angeles, CA

A pipelined ADC consisting of 14 stages calibrates capacitor mismatch, and nonlinearity and gain error of opamps using an RDAC with 11b linearity. Employing a 2-stage opamp with a BW of 10GHz and a gain of 25, the 90nm digital CMOS ADC achieves a DNL of 0.4 LSB, an INL of 1 LSB and an SNDR of 53dB for a 233MHz input, while drawing 55mW from a 1.2V supply. The FOM is 0.3pJ/conversion-step.

4.7 A 16b 125MS/s 385mW 78.7dB SNR CMOS Pipelined ADC

4:45 PM

S. Devarajan, L. Singer, D. Kelly, S. Decker, A. Kamath, P. Wilkins
Analog Devices, Wilmington, MA

A 16b 125MS/s pipelined ADC implemented in a 0.18µm CMOS process achieves an SNR of 78.7dB, an SNDR of 78.6dB and an SFDR of 96dB with a 30MHz input, while maintaining SNR >76dB and SFDR >80dB up to 150MHz with a clock jitter of 65fs. The ADC has a SHA-less 4b front-end and includes digital calibration and dither to improve small-signal linearity. The ADC consumes 385mW from a 1.8V supply.

Conclusion 5:15 PM

POTPOURRI: PLL, OPTICAL, DSL

Session Chair: Larry DeVito, Analog Devices, Wilmington, MA
Associate Chair: Miki Moyal, Intel, Haifa, Israel

5.1 A 7.1mW 10GHz All-Digital Frequency Synthesizer with Dynamically Reconfigurable Digital Loop Filter in 90nm CMOS

1:30 PM

S-Y. Yang, W-Z. Chen
National Chiao Tung University, Hsinchu, Taiwan

A 10GHz all-digital frequency synthesizer with dynamic loop filter is presented. With less than 6.9µs locking time, the measured rms jitter from a 9.92GHz carrier is 0.9ps. A skew-compensated phase accumulator is proposed for high-speed and low-power operation. The core circuits consume 7.1mW. Fabricated in 90nm CMOS, the chip occupies 0.902mm^2.

5.2 Subharmonically Injection-Locked PLLs for Ultra-Low-Noise Clock Generation

2:00 PM

J. Lee[1], H. Wang[1], W-T. Chen[2], Y-P. Lee[2]
[1]National Taiwan University, Taipei, Taiwan
[2]Industrial Technology Research Institute, Hsinchu, Taiwan

A complete analysis of subharmonically injection-locked PLLs explains the noise-shaping phenomenon, and provides a model to predict the output phase noise. Two 20GHz PLLs based on the proposed theory are designed and fabricated in 90nm CMOS. The first chip achieves 149fs$_{rms}$ jitter while consuming 38mW from a 1.3V supply. The second prototype exhibits 85fs$_{rms}$ jitter with a power dissipation of 105mW.

5.3 Bang-Bang Digital PLLs at 11 and 20GHz with sub-200fs Integrated Jitter for High-Speed Serial Communication Applications

2:30 PM

A. Rylyakov, J. Tierno, H. Ainspan, J-O. Plouchart, J. Bulzacchelli, Z. Toprak, D. Friedman
IBM T. J. Watson, Yorktown Heights, NY

Two digital PLLs, realized in 65nm CMOS, feature a low-latency low-gain proportional path control and dynamic DCO steps with half-integer spacing. Time-domain $\Delta\Sigma$ modulation of the reference clock enables control of bang-bang PFD gain and PLL bandwidth. LC-DCO tuning ranges are 8.1 to 11.8GHz and 16.4 to 22.4GHz. The rms jitter, integrated from $f_c/1667$ to $f_c/2$, is 140fs$_{rms}$ at 11GHz and 190fs at 20GHz.

5.4 0.9mW 7GHz and 1.6mW 60GHz Frequency Dividers with Locking-Range Enhancement in 0.13µm CMOS

2:45 PM

S. Rong, W. Ng, H. Luong
Hong Kong University of Science and Technology, Hong Kong, China

Two ILFDs are designed with locking-range enhancement while consuming low power without using extra inductors. Implemented in 0.13µm CMOS, with 0dBm input power, two prototypes achieve locking ranges of 6.02 to 8.45GHz and 59.6 to 66.96GHz, around 3× and 2× improvement over that of the conventional ILFDs while consuming 0.9 and 1.6mW from a 0.8V supply.

Break **3:00 PM**

5.5 A 5.4mW 0.0035mm^2 0.48ps$_{rms}$-Jitter 0.8-to-5GHz Non-PLL/DLL All-Digital Phase Generator/Rotator in 45nm SOI CMOS

3:15 PM

K-H. Kim[1], D. M. Dreps[2], F. D. Ferrailo[3], P. W. Coteus[1], S. Kim[1], S. V. Rylov[1], D. J. Friedman[1]
[1]IBM T. J. Watson, Yorktown Heights, NY
[2]IBM, Austin, TX; [3]IBM, Poughkeepsie, NY

A non-PLL/DLL all-digital phase generator/rotator is realized in 45nm SOI CMOS. The circuit accepts 2 input phases plus interpolator controls and produces 4 output phases; it also supports relative I/Q adjustment for CDR applications. The 0.0035mm^2 circuit operates with phase error within 5° over a 0.8-to-5GHz range. At 5GHz, jitter is 0.48ps$_{rms}$, and the chip consumes 5.4mW from a 0.9V supply excluding the I/O buffers.

5.6 A 14mW 5Gb/s CMOS TIA with Gain-Reuse Regulated Cascode Compensation for Parallel Optical Interconnects

3:30 PM

S. Goswami, J. Silver, T. Copani, W. Chen, B. Vermeire, H. J. Barnaby, S. Kiaei
Arizona State University, Tempe, AZ

Merging regulated cascode compensation with the common-source stage of a shunt feedback TIA overcomes the BW limit at the input due to large photodiode capacitance resulting in power- and area-efficient BW extension. The 0.13µm CMOS prototype tolerates up to 2pF and 1pF input capacitance at 4Gb/s and 5Gb/s, respectively.

5.7 A 4Gb/s Current-Mode Optical Transceiver in 0.18µm CMOS

3:45 PM

J. Yun, M. Seo, B. Choi, J. Han, S. Yun
Ewha Womans University, Seoul, Korea

A current-mode optical transceiver is realized in 0.18µm CMOS. The transmitter includes a 4Gb/s VCSEL driver with the PMOS-load array modulation control that alleviates the PWD problem. The receiver consists of a 4Gb/s TIA with current-mirror input configuration that effectively desensitizes the gain fluctuation against the PVT variations, and a limiting amplifier with negative capacitance scheme. The optical transceiver chip occupies 1.2×1.2mm^2 and dissipates 170mW from a 1.8V supply.

5.8 Jitter-Reduction and Pulse-Width-Distortion-Compensation Circuits for a 10Gb/s Burst-Mode CDR Circuit

4:15 PM

J. Terada[1], Y. Ohtomo[1], K. Nishimura[1], H. Katsurai[1], S. Kimura[2], N. Yoshimoto[2]
[1]NTT, Atsugi, Japan; [2]NTT, Chiba, Japan

Jitter-reduction and pulse-width-distortion-compensation circuits are designed for a burst-mode CDR circuit of 10G-EPON systems. These circuits are implemented in individual CDR circuits in a 0.25µm SiGe BiCMOS process. The input jitter is reduced by 3dB at a jitter frequency of 1GHz and pulse-width distortion of +0.22/-0.32UI is compensated within 0.1UI.

5.9 CMOS Optical 4-PAM VCSEL Driver with Modal-Dispersion Equalizer for 10Gb/s 500m MMF Transmission

4:30 PM

D. Watanabe, A. Ono, T. Okayasu
Advantest, Gunma, Japan

A 4-PAM driver for VCSEL is fabricated in a 90nm CMOS process. The driver circuit has an equalization scheme to compensate a bandwidth degradation caused by modal dispersion of MMF. A 10Gb/s 500m 4-PAM transmission is achieved using conventional graded index MMF having a BW limitation of 500MHz·km. The power consumption is <47mW (4.7mW/Gb/s).

5.10 A VDSL2 CPE AFE in 0.15µm CMOS with Integrated Line Driver

4:45 PM

G. Cesura[1], A. Bosi[1], F. Rezzi[1], R. Castello[2], J. Chan[3], S. Wong[3], C. Yung[3], O. Carnu[4], T. Cho[4]
[1]Marvell, Pavia, Italy; [2]University of Pavia, Pavia, Italy
[3]Marvell, Hong Kong, China; [4]Marvell, Santa Clara, CA

A 0.15µm triple-oxide CMOS AFE for VDSL2 CPE with on-chip line driver delivers 14.5dBm signal power on the line from a 7V supply using 1.2V devices. The transmitter achieves an MTPR in excess of 69dBc while the receiver features THD<-65dBc over the 30MHz signal bandwidth. The total power consumption is 1.25W.

Conclusion 5:15 PM

CELLULAR AND TUNER

Session Chair: George Chien, MediaTek, San Jose, CA
Associate Chair: Aarno Pärssinen, Nokia, Helsinki, Finland

6.1 An Integrated Closed-Loop Polar Transmitter with Saturation Prevention and Low-IF Receiver for Quad-Band GPRS/EDGE

1:30 PM

R. Pullela[1], S. Tadjpour[1], D. Rozenblit[1], W. Domino[1], T. Obkircher[1], M. El Said[1], B. Ramachandran[2], T. Sowlati[1], D. Agahi[1], W. Chen[1], D. Badillo[1], M. Kahrizi[1], J. Komaili[1], S. Wloczysiak[1], U. Seckin[1], Y-Y. Choi[1], H. Aykol[1], M. Vadkerti[1], A. Mahjoob[1], H. Firouzkouhi[1], D. Shum[1], R. Suhanthan[1], N. Vakilian[1], T. Valencia[1], C. Dantec[1], A. Paff[1], M. Ahooie[1]

[1]Skyworks Solutions, Irvine, CA; [2]Skyworks Solutions, Hyderabad, India

A 0.13µm CMOS GSM/GPRS/EDGE transceiver with closed-loop polar transmitter and saturation-prevention sub-system achieves 26% EDGE PA efficiency and output spectrum of -64dBc in 40kHz BW at 400kHz. The RF solution includes a low-IF receiver with dynamic gain and phase correction, and a DigRF interface. The transceiver occupies a die area of 11.5mm^2.

6.2 A SAW-Less Multiband WEDGE Receiver

2:00 PM

O. Gaborieau[1], S. Mattisson[2], N. Klemmer[3], B. Fahs[1], F. Braz[1], R. Gudmundsson[2], T. Mattsson[2], C. Lascaux[1], C. Trichereau[1], W. Suter[3], E. Westesson[2], A. Nydahl[2]

[1]ST-NXP Wireless, Caen, France; [2]Ericsson Mobile Platforms, Lund, Sweden
[3]Ericsson Mobile Platforms, Raleigh, NC

A (3+4)-band WEDGE zero-IF receiver, including a SAW-less front-end with a wideband tuned balun and BB filter consumes 92mW and features 2.2dB NF, >48dBm IIP2, and -8dBm IIP3. A transceiver module, in mass production, combines an 11mm^2 0.25µm BiCMOS die with a Si-carrier to achieve a 7×7mm^2 double-flip-chip SiP.

6.3 Single-Chip Multiband WCDMA/HSDPA/HSUPA/EGPRS Transceiver with Diversity Receiver and 3G DigRF Interface Without SAW Filters in Transmitter / 3G Receiver Paths

2:30 PM

T. Sowlati[1], B. Agarwal[1], J. Cho[1], T. Obkircher[1], M. El Said[1], J. Vasa[1], B. Ramachandran[1], M. Kahrizi[1], E. Dagher[1], W-H. Chen[1], M. Vadkerti[1], G. Taskov[1], Y. Choi[1], H. Firouzkouhi[1], B. Saeidi[1], H. Akyol[1], U. Seckin[2], A. Mahjoob[1], S. D'Souza[1], C-Y. Hsieh[1], D. Guss[1], D. Shum[1], D. Badillo[1], I. Ron[1], D. Ching[1], F. Shi[1], Y. he[1], J. Komaili[1], A. Loke[1], R. Pullela[1], E. Pehlivanouglu[1], H. Zarei[1], S. Tadjpour[1], D. Agahi[1], D. Rozenblit[1], W. Domino[1], G. Williams[1], N. Damavandi[1], S. Wloczysiak[1]

[1]Skyworks Solutions, Irvine, CA; [2]Spectra-Linear, Istanbul, Turkey

A 0.13µm transceiver with 3G DigRF interface supports 7 WCDMA bands and quad-band EGPRS in the main path and a quad-band diversity receive path, operating in low-IF in 2G, and in direct conversion in 3G without interstage SAW filter, with IIP2 exceeding +50dBm. The transmitter has a SAW-less direct upconversion architecture for 2G and 3G with closed-loop power control, achieving -164dBc/Hz noise at 20MHz offset in low-band.

Break 3:00 PM

6.4 Single-Chip RFCMOS UMTS/EGSM Transceiver with Integrated Receive Diversity and GPS

3:15 PM

A. Hadjichristos[1], M. Cassia[1], H. Kim[2], C. Park[2], K. Wang[1], W. Zhuo[1], B. Ahrari[2], R. Brockenbrough[2], J. Chen[2], C. Donovan[2], R. Jonnalagedda[2], J. Kim[2], J. Ko[2], H. Lee[2], S. Lee[2], E. Lei[2], T. Nguyen[2], T. Pan[2], R. Sridhara[1], W. Su[1], H. Yan[1], J. Yang[2], C. Conroy[2], C. Persico[1], K. Sahota[1], B. Kim[2]
[1]Qualcomm, San Diego, CA; [2]Qualcomm, Santa Clara, CA

A highly integrated multimode transceiver in 0.18µm RFCMOS technology achieves 65-to-69mA supply current and supports UMTS Bands 1 to 6 and 8 to 10, and quad-band GSM/EDGE. Integrated GPS and UMTS receive diversity share portions of the same receiver while high-C/N PLL and LO chains eliminate interstage SAW filters for GSM/EDGE and a number of UMTS bands. The transceiver occupies a die area of 5.6×5.6mm^2.

6.5 A 45nm Low-Power SAW-Less WCDMA Transmit Modulator Using Direct Quadrature Voltage Modulation

3:45 PM

X. He, J. van Sinderen
NXP Semiconductors, Eindhoven, Netherlands

A 22mW SAW-less WCDMA transmit modulator in 45nm CMOS employs direct quadrature voltage modulation via a passive voltage mixer driven by a 25%-duty-cycle LO to achieve -52dBc ACLR, -49dBc LO leakage and 0.97% EVM with improved power efficiency. At 1dBm output the transmit modulator achieves -159dBc/Hz noise floor at a frequency offset beyond 40MHz.

6.6 An Embedded 65nm CMOS Low-IF 48MHz-to-1GHz Dual Tuner for DOCSIS-3.0

4:15 PM

F. Gatta, R. Gomez, Y. Shin, T. Hayashi, H. Zou, J. Chang, L. Dauphinee, J. Xiao, D-H. Chang, T-H. Chih, M. Brandolini, D. Koh, B-J. Hung, T. Wu, M. Introini, G. Cusmai, E. Zencir, L. Tan, B. Currivan, L. He, P. Cangiane, K. Lai, J. Lin, D. Lakshminarasimhan, A. Hung, C. Dang, H. Vu, G. Zhong, P. Vorenkamp
Broadcom, Irvine, CA

An embedded 65nm CMOS dual tuner for DOCSIS-3.0 cable modem achieves 50dB QAM peak SNR and -73dBm 256-QAM sensitivity. A single tuner occupies 5mm^2 while consuming 750mW. Paired with an LNA chip, the tuners downconvert up to 10 Annex-B DOCSIS channels in two 32MHz bands, exceeding DOCSIS and SCTE-40 requirements over the 48MHz-to-1GHz CATV frequency range.

6.7 A 1.2V 67mW 4mm^2 Mobile ISDB-T Tuner in 0.13µm CMOS

4:45 PM

Y-T. Huang, C. Yang, S. Huang, H. Pan, H. Hung
MaxRise, Hsinchu, Taiwan

An ISDB-T 1-segment RF tuner covering the UHF band is designed to address power-consumption reduction, improved performance, and lower cost in mobile TV service worldwide. Using a noise-canceling LNA, the tuner achieves 3dB/3.4dB NF at 470/812MHz. The 4mm^2 IC, implemented in 0.13µm CMOS, consumes 67mW from a 1.2V supply.

Conclusion **5:15 PM**

SE3: **Will ADCs Overtake Binary Frontends in Backplane Signaling?**

Organizer: **Ali Sheikholeslami,** *University of Toronto, Toronto, Canada*
Co-Organizer: **Robert Payne**, *Texas Instruments, Dallas, TX*

Moderator: **Jerry Lin**, *Ralink Technology, Hsinchu, Taiwan*

Receivers with an ADC front-end are now competing against conventional receivers with a binary front-end, but they occupy larger silicon area and possibly consume more power. This session discusses the pros and cons and the design trade-offs between the two approaches in backplane electrical signaling. Each of our five panelists will predict whether or not the switchover to ADC-based designs will become inevitable.

Time	Topic
8:00	**ADCs Will Dominate at 20Gb/s and Beyond** **Ichiro Fujimori**, *Broadcom, Irvine, CA*
8:15	**Are Serdes as We Know Them Dead?** **Andrew Joy**, *Texas Instruments, Northampton, Northants, United Kingdom*
8:30	**Let the Market Decide** **Michael Sorna**, *IBM, East Fishkill, NY*
8:45	**History Repeats Itself: ADCs Will Dominate** **Hirotaka Tamura**, *Fujitsu Laboratories, Kawasaki, Kanagawa, Japan*
9:00	**Are They Really That Different?** **Jared Zerbe**, *Rambus, Los Altos, CA*
9:15	Panel Discussion

SE4: Highlights of IEDM 2008

Organizer: **Roland Thewes,** *Qimonda, Munich, Germany*

Chair: **Ralf Brederlow,** *Texas Instruments, Freising, Germany*

In this session, four outstanding papers from IEDM 2008 are presented to the ISSCC circuit design community. They cover the areas of advanced CMOS platforms with 32nm design rules enabling high-performance as well as low-power operation, recent achievements in multi-chip module assembly techniques allowing the combination of various technologies and functionalities, and ultra-high frequency RF transistors opening the way towards THz applications.

Time	Topic
8:00	**New Heterogeneous Multi-Chip Module Integration Technology Using Self-Assembly Method** **T. Fukushima,** *et al.* *Tohoku University, Sendai, Japan*
8:30	**32nm General Purpose Bulk CMOS Technology for High Performance Applications at Low Voltage** **F. Arnaud,** *et al.* *STMicroelectronics*
9:00	**30nm E-mode InAs PHEMTs for THz and future Logic Applications** **Dae-Hyun Kim and J. A. del Alamo** *MIT, Cambridge, MA*
9:30	**32nm Gate-First High-k/Metal-Gate Technology for High Performance Low Power Applications** **C. H. Diaz,** *et al.* *TSMC, Hsinchu, Taiwan*

E1: Forewarned is Four-Armed: Classic Analog Misteakes to Avoid

Organizer: **Jed Hurwitz,** *Gigle Semiconductor, Edinburgh, United Kingdom*

Moderator: **Chris Mangelsdorf**, *Analog Devices, Tokyo, Japan*

Analog is an area where experience is deemed to be valuable not only to help design performing circuits, but to avoid those mistakes that can cause projects to fail to deliver.

In what promises to be a memorable evening, we have assembled a panel of analog experts who will present and discuss some of the most common, amusing, debatable, subtlest and saddest errors made in this field. There will be an opportunity for the audience to participate, but be prepared to open those wounds and admit to your own mistakes - it may be worth your while.

Panelists:

Bob Blauschild, *Independent Design Consultant, Los Gatos, CA*
Paul Brokaw, *Analog Devices, Tucson, AZ*
Jim Williams, *Linear Technology, Milpitas, CA*
Kofi Makinwa, *Delft University of Technology, Delft, Netherlands*
Klaas Bult, *Broadcom, Bunnik, Netherlands*
Zhiliang Hong, *Fudan University, Shanghai, China*

SE5: Things All RFIC Designers Should Know (But are Afraid to Ask)

Co-Organizers/Co-Chairs: **David Su,** *Atheros, Santa Clara, CA*
Arya Behzad, *Broadcom, San Diego, CA*

Much of the attention at conferences, such as ISSCC, has been focused on the design of wireless SoCs. However, bringing a wireless SoC to market requires significant technical knowledge beyond IC design. The objective of this evening session is to provide an introduction on topics that are typically not well understood by RF IC designers, in part, because they are not sufficiently emphasized in most college curricula, yet are critically important to the successful productization of wireless systems.

Time	Topic
8:00	**ESD Design Challenges for SoC and RF** **Charvaka Duvvury,** *Texas Instruments, Dallas, TX*
8:25	**Antennas: From Fundamental Limitations to Design** **Nicolaos G. Alexopoulos,** *Broadcom, Irvine, CA*
8:50	**Packaging Options for Wireless SoCs** **Lawrence Larson,** *University of California, San Diego, CA*
9:15	**CAD for RFIC/SoC: What You Don't Know CAN Really Hurt You** **Ravi Subramanian,** *Berkeley Design Automation, Santa Clara, CA*
9:40	**Wireless SoC Production Test Concepts for RFIC Designers** **Joe Kelly,** *Verigy, Neptune City, NJ*

DRAM

Session Chair: Kazuhiko Kajigaya, Elpida Memory, Sagamihara, Japan
Associate Chair: Heinz Hoenigschmid, Qimonda, Neubiberg, Germany

7.1 1.2V 1.6Gb/s 56nm 6F² 4Gb DDR3 SDRAM with Hybrid-I/O Sense Amplifier and Segmented Sub-Array Architecture

8:30 AM

Y. Moon, Y-H. Cho, H-B. Lee, B-H. Jeong, S-H. Hyun, B-C. Kim, I-C. Jeong, S-Y. Seo, J-H. Shin, S-W. Choi, H-S. Song, J-H. Choi, K-H. Kyung, Y-H. Jun, K. Kim
Samsung Electronics, Hwasung, Korea

A 4Gb DDR3 SDRAM at 1.2V and 1.6Gb/s/pin bandwidth is implemented in a 3M 56nm (2Cu1Al) process with 173.82mm² die area. For low-voltage low-power and high-frequency operation, half-frequency read-latency control, hybrid IOSA, and segmented sub-array architecture are developed. Standby currents are reduced by 63% and operating currents are reduced by 54% with t_{RCD} of 9.8ns and t_{AA} of 10.4ns.

7.2 8Gb 3D DDR3 DRAM Using Through-Silicon-Via Technology

9:00 AM

U. Kang, H-J. Chung, S. Heo, S-H. Ahn, H. Lee, S-H. Cha, J. Ahn, D. Kwon, J-H. Kim, J-W. Lee, H-S. Joo, W-S. Kim, H-K. Kim, E-M. Lee, S-R. Kim, K-H. Ma, D-H. Jang, N-S. Kim, M-S. Choi, S-J. Oh, J-B. Lee, T-K. Jung, J-H. Yoo, C. Kim
Samsung Electronics, Hwasung, Korea

An 8Gb 4-stack 3D DDR3 DRAM with through-silicon-via (TSV) is presented that decreases the standby power by 50% and active power by 25%, and increases the I/O speed to 1600Mb/s. The TSV check and repair scheme increases the assembly yield from 15% to 98%. By providing extra power pads, power noise is reduced to 100mV even if all 4 ranks are refreshed.

7.3 A 1.35V 4.3GB/s 1Gb LPDDR2 DRAM with Controllable Repeater and On-the-Fly Power-Cut Scheme for Low-Power and High-Speed Mobile Application

9:30 AM

B-H. Jeong, J. Lee, Y-J. Lee, T-J. Kang, J-H. Lee, D-H. Hong, J-H. Kim, E-R. Lee, M-C. Kim, K-H. Lee, S-I. Park, J-H. Son, S-K. Lee, T-W. Kwon, J-H. Ahn, Y-T. Kim
Hynix Semiconductor, Icheon, Korea

A 1.35V 4.3GB/s 1Gb LPDDR2 DRAM with controllable repeater and on-the-fly power-cut scheme is fabricated in a 66nm process. The DRAM is targeted for low-power and high-speed mobile applications. The global I/O lines are optimized with a GIO repeater scheme to overcome the high loading. The data bandwidth is 1066Mb/s/pin with associated maximum power consumption of 110mW.

Break 10:00 AM

7.4 A 75nm 7Gb/s/pin 1Gb GDDR5 Graphics Memory Device with Bandwidth-Improvement Techniques

10:15 AM

R. Kho, D. Boursin, M. Brox, P. Gregorius, H. Hoenigschmid, B. Kho, S. Kieser, D. Kehrer, M. Kuzmenka, U. Moeller, P. Petkov, M. Plan, M. Richter, I. Russell, K. Schiller, R. Schneider, K. Swaminathan, B. Weber, J. Weber, I. Bormann, F. Funfrock, W. Spirkl, H. Steffens, J. Weller, T. Hein, M. Gjukic
Qimonda, Neubiberg, Germany

A 1Gb GDDR5 DRAM is fabricated in a conventional 75nm DRAM process. To improve existing data transfer rates, we implement a boosting transmitter to open the data eye by 100mV, and a high-speed multiple-domain internal V_{INT} power-generator system to limit on-chip power noise in critical blocks to 10mV. A data-transfer rate of 7Gb/s/pin is achieved with a 1.5V supply.

7.5 Single-Ended Transceiver Design Techniques for 5.33Gb/s Graphics Applications

10:45 AM

H. Partovi[1], K. Gopalakrishnan[1], L. Ravezzi[1], O. Schumacher[2], R. Homer[1], R. Unterricker[2], W. Kederer[2]
[1]Qimonda, San Jose, CA; [2]Qimonda, Neubiberg, Germany

Circuit techniques for reliable single-ended signaling at 5.33Gb/s are described. With an incoming eye closure of 0.5UI, a capacitively balanced receiver has an input sensitivity of ±50mV. An integrated self-resetting 2:1 serializer/level-shifter consumes 3mW, and is insensitive to voltage difference between core and I/O voltage domains. The transmitter uses capacitive pre-emphasis to compensate for a band-limited channel and improves ISI by 32%.

7.6 A 6Gb/s/pin Pseudo-Differential Signaling Using Common-Mode Noise Rejection Techniques Without Reference Signal for DRAM Interfaces

11:15 AM

K-S. Ha[1], L-S. Kim[1], S-J. Bae[2], K-I. Park[2], J. Choi[2], Y-H. Jun[2], K. Kim[2]
[1]KAIST, Daejeon, Korea; [2]Samsung Electronics, Hwasung, Korea

A 6Gb/s/pin transceiver for DRAM interfaces is implemented in a 0.13µm CMOS process. To remove the reference signal, which increases the BER in single-ended signaling, pseudo-differential signaling encoding schemes are used to increase the eye width by 65ps and the eye-opening at a 10^{-12} BER by 235mUI. The transceiver dissipates 242.5mW and its active area is 1.0×0.3mm^2.

7.7 A 1.6V 3.3Gb/s 1Gb GDDR3 DRAM with Dual-Mode Phase- and Delay-Locked Loop Using Power-Noise Management with Unregulated Power Supply in 54nm CMOS

11:45 AM

H-W. Lee, W-J. Yun, Y-K. Choi, H-H. Choi, J-J. Lee, K-H. Kim, S-D. Kang, J-Y. Yang, J-S. Kang, H-O. Lee, D-U. Lee, S. Sim, Y-J. Kim, W-J. Choi, K-S. Song, S-H. Shin, H-W. Moon, S-W. Kwack, J-W. Lee, N-K. Park, K-W. Kim, Y-J. Choi, J-H. Ahn, B-T. Chung
Hynix Semiconductor, Icheon, Korea

A phase- and delay-locked loop is manufactured in 54nm CMOS. It has a DLL for phase compensation and PLL for jitter reduction. The charge-pump-type PLL has dual-K_{VCO}, self mode-shifting scheme and uses an unregulated power supply for a wide operating range. To reduce the V_{DD} noise due to low V_{PP} pumping efficiency, a new V_{PP} control is used and applied to a pseudo-rank architecture.

7.8 Low-V_t Small-Offset Gated Preamplifier for Sub-1V Gigabit DRAM Arrays

12:00 PM

S. Akiyama, T. Sekiguchi, R. Takemura, A. Kotabe, K. Itoh
Hitachi, Kokubunji, Japan

A low-V_t gated preamplifier (LGA) with fast sensing and local I/O driving capability even for low-voltage mid-point sensing is designed. A 70nm 128Mb DRAM core based on this LGA demonstrates 16.4ns row access (t_{RCD}) and 14.3ns read access (t_{AA}) at an array supply of 0.9V. The LGA is targeted for future sub-1V Gigabit DRAMs because the offset voltage of sense amplifiers is almost halved.

Conclusion 12:15 PM

MULTIMEDIA PROCESSORS

Session Chair: Fumio Arakawa, Hitachi, Tokyo, Japan
Associate Chair: Thomas Tomazin, MediaTek, Austin, TX

8.1 An Ultra-Low-Energy/Frame Multi-Standard JPEG Co-Processor in 65nm CMOS with Sub/Near-Threshold Power Supply

8:30 AM

Y. Pu[1,2], J. Pineda de Gyvez[1,2], H. Corporaal[2], Y. Ha[3]
[1]NXP Semiconductors, Eindhoven, Netherlands
[2]Eindhoven University of Technology, Eindhoven, Netherlands
[3]National University of Singapore, Singapore

SubJPEG is a state-of-the-art multistandard 65nm CMOS JPEG encoding 1.4×1.4mm^2 co-processor that enables ultra-wide V_{DD} scaling. With a 0.4V power supply, it delivers 15fps 640×480 VGA performance with 200nJ/frame energy consumption. This extreme low-power performance is well-suited for digital camera, portable wireless, and medical imaging applications.

8.2 A Versatile Recognition Processor Employing Haar-Like Feature and Cascaded Classifier

9:00 AM

Y. Hanai, Y. Hori, J. Nishimura, T. Kuroda
Keio University, Yokohama, Japan

A versatile recognition processor performs detection and recognition of image, video, sound and acceleration signals. It contains 2.1M transistors and occupies 0.89mm^2 in 90nm CMOS, and consumes 0.15μW/fps to 0.47mW/fps from a 0.9V supply at an operating frequency of 54MHz. The versatility and low-power dissipation are attributed to an optimized VLSI design employing Haar-like feature and cascaded classifier.

8.3 A 201.4GOPS 496mW Real-Time Multi-Object Recognition Processor with Bio-Inspired Neural Perception Engine

9:30 AM

J-Y. Kim, M. Kim, S. Lee, J. Oh, K. Kim, S. Oh, J-H. Woo, D. Kim, H-J. Yoo
KAIST, Daejeon, Korea

A 201.4GOPS recognition processor with multicastable 400MHz network-on-chip (NoC) integrates 128 200MHz processing elements and bio-inspired neural perception engine (NPE) to achieve 60fps recognition for VGA images with up to 10 salient objects in a frame. The 49mm^2 die in 0.13μm CMOS reduces power consumption to 496mW at 1.2V core with workload-aware power management and IP-level clock gating.

Break 10:00 AM

8.4 A Multi-Format Blu-ray Player SoC in 90nm CMOS

10:15 AM

C-C. Ju, T-M. Liu, C-C. Yang, S-H. Lin, K-P. Lan, C-H. Wu, T-H. Wei, C-C. Lien, J-Y. Wu, C-H. Hsiao, T-W. Chen, Y-L. Chu, G-Y. Lin, Y-C. Chang, K-S. Lin, C-M. Wang, H-M. Lin, C-Y. Cheng, C-C. Chen, C-H. Lin, Y-T. Lin, S-M. Lee, Y-C. Yang, Y-L. Cheng, C-C. Lee, M-S. Lai, W-H. Wu, T. Hu, C-W. Tseng, C-Y. Hsiao, W-L. Lee, B-J. Chen, P-C. Chiu, S-P. Chen, K-H. Li, K-H. Chao, C-M. Chen, C-C. Hsiao, J. Ju, W-H. Huang, C-H. Wang, H-S. Li, E. Su, J. Chen
MediaTek, Hsinchu, Taiwan

A Blu-ray Disc (BD) player SoC supporting diverse processing formats occupies in 7.9×7.9mm^2 in 90nm CMOS. Cost-effective techniques in decryption, decode and display modules are realized to lower cost. A 60fps H.264 video playback with HD/SD overlay display and HDMI-1.3 12b deep-color-mode output is achieved at 200MHz, 148.5MHz, and 222.5MHz clock frequency, respectively, and 1.605W power dissipation.

8.5 A 212MPixels/s 4096×2160p Multiview Video Encoder Chip for 3D/Quad HDTV Applications

10:45 AM

L-F. Ding, W-Y. Chen, P-K. Tsung, T-D. Chuang, H-K. Chiu, Y-H. Chen, P-H. Hsiao, S-Y. Chien, T-C. Chen, C-Y. Chang, W-L. Chen, P-C. Lin, L-G. Chen
National Taiwan Univeristy, Taipei, Taiwan

A 4096×2160p 280MHz multiview video encoder chip is implemented on a 11.46mm^2 die in 90nm CMOS. An 8-stage macroblock pipelined architecture with cache-based prediction core achieves 212Mpixel/s throughput, which is 3.4× to 7.7× higher than the previous works. A 407Mpixel/W power efficiency is achieved at 1.2V, and 94% on-chip SRAM size and 79% external memory bandwidth are saved.

8.6 A 45nm Single-Chip Application-and-Baseband Processor Using an Intermittent Operation Technique

11:15 AM

M. Shirasaki, Y. Miyazaki, M. Hoshaku, H. Yamamoto, S. Ogawa, T. Arimura, H. Hirai, Y. Iizuka, T. Sekibe, Y. Nishida, T. Ishioka, J. Michiyama
Panasonic, Yokohama, Japan

An intermittent operation technique is used to reduce the power consumption in audio playback. To reduce leakage current, four power-management mechanisms are utilized: power-gating, V_{DD} control, V_{BB} control and V_{SS} control. The 486MHz application processor and 245MHz baseband processor utilize 280M transistors and 25Mb SRAM on a 8.05×8.18mm^2 die in 45nm CMOS. In audio playback, it dissipates 9.6mW, while total power consumption is 15.3mW at 1.2V.

8.7 A 342mW Mobile Application Processor with Full-HD Multi-Standard Video Codec

11:45 AM

K. Iwata, T. Irita, S. Mochizuki, H. Ueda, M. Ehama, M. Kimura, J. Takemura, K. Matsumoto, E. Yamamoto, T. Teranuma, K. Takakubo, H. Watanabe, S. Yoshioka, T. Hattori
Renesas Technology, Tokyo, Japan

A full HD (1080p30) 500MHz mobile application processor with an H.264 HP/MPEG-2/MPEG-4 video codec is integrated on a 6.4×6.5mm^2 die in 65nm CMOS. With two parallel pipelines for macroblock processing and tile-based address translation circuits, the processor consumes 342mW in real-time playback of a full-HD H.264 stream from a 64b width low-power DDR-SDRAM at an operating frequency of 166MHz at 1.2V.

Conclusion 12:15 PM

DATA CONVERTER TECHNIQUES

Session Chair: Bernhard Boser, University of California, Berkeley, CA
Associate Chair: Aaron Buchwald, Mobius Semiconductor, Irvine, CA

9.1 A 130mW 100MS/s Pipelined ADC with 69dB SNDR Enabled by Digital Harmonic Distortion Correction

8:30 AM

A. Panigada, I. Galton
University of California, San Diego, CA

A 100MS/s pipelined ADC with on-chip digital background correction of residue amplifier nonlinearity and capacitor mismatch and with on-chip reference generators achieves a peak SNR of 70dB, a -1dBFS SFDR of 85dB, and an FOM of 0.52pJ/conversion-step. The 90nm CMOS IC consumes 130mW from 1.2V and 1.0V analog and digital power supplies, respectively.

9.2 A 50MS/s 9.9mW Pipelined ADC with 58dB SNDR in 0.18µm CMOS Using Capacitive Charge-Pumps

9:00 AM

I. Ahmed[1], J. Mulder[2], D. A. Johns[1]
[1]University of Toronto, Toronto, Canada
[2]Broadcom, Bunik, Netherlands

In order to achieve stage gain in a pipelined ADC, a capacitive charge-pump is combined with a source follower rather than opamps using feedback, resulting in a very-low-power topology. The 10b 50MS/s ADC in 1.8V 0.18µm CMOS achieves a peak SNDR/SFDR of 58.2/66dB, while consuming 3.9mW for all active circuits and 6mW for all clocking circuits.

9.3 A 12b 50MS/s Fully Differential Zero-Crossing-Based ADC Without CMFB

9:30 AM

L. G. Brooks, H. Lee
Massachusetts Institute of Technology, Cambridge, MA

An offset-compensated fully differential zero-crossing-based 12b 50MS/s pipelined ADC requiring no CMFB is implemented in 90nm CMOS. The power consumption is 4.5mW. The FOM is 88fJ/conversion-step.

Break 10:00 AM

9.4 A 9b 14µW 0.06mm^2 PPM ADC in 90nm Digital CMOS

10:15 AM

S. Naraghi[1], M. Courcy[2], M. P. Flynn[1]
[1]University of Michigan, Ann Arbor, MI
[2]National Semiconductor, Salem, NH

A PPM-based ADC architecture that exploits the time-domain resolution of nanometer CMOS is reported. The input signal is compared to a voltage ramp, producing non-uniform samples of the input. An iterative recovery algorithm generates uniform samples. The ADC occupies 0.06mm^2 in 90nm CMOS, achieves an ENOB of 7.9b over a 300kHz input bandwidth, and dissipates 14µW.

9.5 A 0.13µm CMOS 78dB SNDR 87mW 20MHz BW CT ΔΣ ADC with VCO-Based Integrator and Quantizer

10:45 AM

M. Park[1], M. H. Perrott[2]
[1]Massachusetts Institute of Technology, Cambridge, MA
[2]SiTime, Sunnyvale, CA

This work demonstrates a 4th-order CT ΔΣ ADC architecture that leverages a VCO to perform CT integration and quantization. For a 900MHz sample rate and a 4b quantizer/DAC, the ADC achieves a resolution of 12.7 ENOB in a 20MHz input signal bandwidth, consumes 87mW from a 1.5V supply, occupies an active area of 0.45mm^2 and is fabricated in a 0.13µm CMOS process.

9.6 A 1.2V 2MHz BW 0.084mm^2 CT ΔΣ ADC with -97.7dBc THD and 80dB DR Using Low-Latency DEM

11:15 AM

S-J. Huang, Y-Y. Lin
MediaTek, Hsinchu, Taiwan

A 3rd-order 3b CT ΔΣ ADC achieves 80dB DR and 79.1/79.07dB peak SNR/SNDR in 2MHz BW when clocked at 128MHz. A switch matrix lowers the quantizer-to-DAC delay, improves stability and relaxes the OTA BW requirement. A feedback DAC and a current tracking OTA are used to achieve -97.7dBc THD. The ADC uses 0.084mm^2 in 65nm CMOS, consumes 4.52mW from a 1.2V supply, and its FOM is 0.153pJ/conv.

9.7 A 20MHz BW 68dB DR CT ΔΣ ADC Based on a Multi-Bit Time-Domain Quantizer and Feedback Element

11:45 AM

V. Dhanasekaran[1,2], M. Gambhir[1], M. M. Elsayed[1], E. Sánchez-Sinencio[1], J. Silva-Martinez[1], C. Mishra[1], L. Chen[1], E. Pankratz[1]
[1]Texas A&M University, College Station, TX
[2]Qualcomm, San Diego, CA

A 3rd-order CT ΔΣ ADC that replaces the multi-bit quantizer and feedback DAC by a PWM generator and TDC is implemented in 65nm CMOS. The TDC provides a 50-level binary code and a time-quantized feedback pulse with 11b linearity while measuring 60×90µm^2. The modulator achieves 68dB DR in 20MHz BW, consumes 10.5mW and occupies 0.15mm^2.

9.8 A Multirate 3.4-to-6.8mW 85-to-66dB DR GSM/Bluetooth/UMTS Cascade DT ΔΣM in 90nm Digital CMOS

12:00 PM

L. Bos[1,2], G. Vandersteen[2], J. Ryckaert[1], P. Rombouts[3], Y. Rolain[2], G. van der Plas[1]
[1]IMEC, Leuven, Belgium
[2]Vrije Universiteit Brussel, Brussels, Belgium
[3]Ghent University, Ghent, Belgium

A multimode multirate 2-1 cascade ΔΣ ADC achieves a dynamic range of 66/77/85dB for UMTS/Bluetooth/GSM with 6.8/3.7/3.4mW. An optimal power/performance trade-off is obtained by relaxing the sampling speed of the 1st stage and appropriately increasing that of the 2nd stage. Implemented in 1.2V 90nm CMOS with an area of 0.076mm^2, the energy per conversion-step is 1.7/1.4/6.6pJ.

Conclusion **12:15 PM**

MULTI-Gb/s SERIAL LINKS AND BUILDING BLOCKS

Session Chair: Hui Pan, Broadcom, Irvine, CA
Associate Chair: Daniel Friedman, IBM T. J. Watson, Yorktown Heights, NY

10.1 A Scalable 3.6-to-5.2mW 5-to-10Gb/s 4-Tap DFE in 32nm CMOS

8:30 AM

L. Chen, X. Zhang, F. Spagna
Intel, Santa Clara, CA

A power-scalable multi-data-rate 4-tap DFE is implemented in 32nm CMOS. High data rate and low power dissipation are achieved by using a 1:2 demuxed current-integrating summer, sense-amplifier latched decision feedback, and fully differential current-recycled DAC. Occupying 120×53μm^2, the DFE consumes 3.6mW at 5Gb/s, 4.6mW at 8Gb/s, and 5.2mW at 10Gb/s from a 0.95V supply, and demonstrates BER<4.2×10^{-15} at 10Gb/s over a channel with -10dB loss.

10.2 A 10Gb/s Compact Low-Power Serial I/O with DFE-IIR Equalization in 65nm CMOS

9:00 AM

Y. Liu[1], B. Kim[2], T. O. Dickson[1], J. F. Bulzacchelli[1], D. Friedman[1]
[1]IBM T. J. Watson, Yorktown Heights, NY
[2]Massachusetts Institute of Technology, Cambridge, MA

A serial I/O targeting dense silicon carrier interconnects is reported. Based on expected channel characteristics, a low-power DFE-IIR RX is proposed. An 8.9Gb/s 1.8mW/Gb/s TX-RX pair operates over a 40mm on-chip wire designed to emulate a silicon carrier channel. The RX also equalizes 10Gb/s data over conventional chip-to-chip and backplane links with >20dB loss.

10.3 A 650Mb/s-to-8Gb/s Referenceless CDR Circuit with Automatic Acquisition of Data Rate

9:30 AM

S-K. Lee, Y-S. Kim, H. Ha, Y. Seo, H-J. Park, J-Y. Sim
Pohang University of Science and Technology, Pohang, Korea

A 650Mb/s-to-8Gb/s referenceless CDR circuit is described with automatic tracking of data rate. For frequency acquisition, a DLL-based loop is used with a simple phase/frequency detector. Implemented in 65nm CMOS, the CDR shows a BER of <10^{-12}. The 0.108mm^2 CDR consumes 20.6mW and 88.6mW at 650Mb/s and 8Gb/s, respectively.

Break 10:00 AM

10.4 A 10Gb/s Receiver with Track-and-Hold-Type Linear Phase Detector and Charge-Redistribution 1st-order $\Delta\Sigma$ Modulator

10:15 AM

K. Fukuda, H. Yamashita, F. Yuki, G. Ono, R. Nemoto, E. Suzuki, T. Takemoto, T. Saito
Hitachi, Tokyo, Japan

A 10Gb/s receiver with a digital CDR uses a track-and-hold-type linear phase detector (LPD) and charge-redistribution 1st-order $\Delta\Sigma$. It has low quantization error and high loop bandwidth due to the use of the LPD and maintains the advantages of a digital CDR such as low power consumption, small area, fast locking time, and a low-jitter recovery clock because no internal VCO is needed. The CDR tracking bandwidth is 20MHz and high-frequency jitter tolerance is 0.42UI$_{pp}$ at 10^{-12} BER. Power consumption of the LPD is 2.6mW while the entire receiver consumes 65mW.

10.5 A 4-Channel 10.3Gb/s Backplane Transceiver Macro with 35dB Equalizer and Sign-Based Zero-Forcing Adaptive Control

10:45 AM

Y. Hidaka[1], W. Gai[1], T. Horie[2], J. H. Jiang[1], Y. Koyanagi[2], H. Osone[1]
[1]Fujitsu Laboratories of America, Sunnyvale, CA
[2]Fujitsu Laboratories, Kawasaki, Japan

A 10.3Gb/s transceiver macro uses an adaptive analog linear equalizer (LE), a 1-tap DFE RX, and a fixed 3-tap pre-emphasis TX to cancel 15.7-to-35.8dB loss at $f_s/2$ for transmission over 2-to-30-inch FR4 backplanes. The LE and DFE are adapted by the sign-based zero-forcing scheme. Fabricated in 90nm CMOS, the TX/RX occupies 0.380mm^2 and consumes 260mW from a 1.2V supply at 10.3Gb/s per channel.

10.6 A 250Mb/s-to-3.4Gb/s HDMI Receiver with Adaptive Loop Updating Frequencies and an Adaptive Equalizer

11:15 AM

Y-B. Luo, P. Chen, Q-T. Chen, C-Y. Wang, C-H. Chang, S-J. Fu, C-M. Chen, H-S. Li
MediaTek, Hsinchu, Taiwan

A digital-phase-interpolator CDR circuit automatically adjusts the loop updating frequency by monitoring the input clock frequency to enlarge the CDR loop bandwidth without degrading high-frequency jitter tolerance. Additionally, the digital-phase-interpolator receiver with adaptive equalizer automatically adjusts to cable loss to achieve 3.4Gb/s transmission rate over a 25m HDMI cable. The core area with 3 channel receivers and TMDS PLL occupies 0.17mm^2 in 55nm CMOS.

10.7 A 2Gb/s Clock-Embedded Interface for Full-HD 10b 120Hz LCD Drivers with 1/5-Rate Noise-Tolerant Phase and Frequency Recovery

11:45 AM

K. Yamaguchi[1], Y. Hori[2], K. Nakajima[2], K. Suzuki[1], M. Mizuno[1], H. Hayama[2]
[1]NEC, Sagamihara, Japan
[2]NEC Electronics, Kawasaki, Japan

A 2Gb/s clock-embedded interface for LCD drivers is presented for high-speed data transfer and reduced area in transmission media. One pair of differential signals is needed to control the LCD driver and to display images. A 1/5-rate phase and frequency detector helps achieve a 25% power reduction. A 4B5B-based interface protocol is developed for noise-tolerant clock recovery. The CDR circuit consumes 93mW from a 3V supply. The rms jitter in the recovered clock is 11ps when a PRBS7 pattern is used.

Conclusion **12:15 PM**

TD: TRENDS IN WIRELESS COMMUNICATIONS

Session Chair: Hoi-Jun Yoo, KAIST, Daejeon, Korea
Associate Chair: Siva Narendra, Tyfone, Portland, OR

11.1 A GHz Spintronic-Based RF Oscillator

8:30 AM

P. Vincent[1], M. Cyrille[1], B. Viala[1], B. Delaet[1], J. Michel[1], P. Villard[1], J. Prouvée[1], D. Houssamedine[2], U. Ebels[2], J. Katine[3], D. Mauri[3], S. Florez[3], O. Ozaty[3], L. Folks[3], B. Terris[3], F. Badets[4]
[1]CEA-LETI-Minatec, Grenoble, France; [2]CEA-Spintec, Grenoble, France
[3]Hitachi, San Jose, CA; [4]STMicroelectronics, Grenoble, France

An ultra-high-density broadband magnetic tunnel junction (MTJ) spin torque oscillator (STO) is presented. A 200×200nm^2 STO operates from 4 to 10GHz and provides an output power of -45dBm. The STO is co-integrated with a high-impedance broadband amplifier and an injection-lock ring oscillator (ILO) on a 65nm CMOS technology to reach RF application specifications.

11.2 A Remote-Powered RFID Tag with 10Mb/s UWB Uplink and -18.5dBm Sensitivity UHF Downlink in 0.18µm CMOS

9:00 AM

M. Baghaei-Nejad[1,2], D. Sarmiento Mendoza[1], Z. Zou[1], S. Radiom[3], G. Gielen[3], L-R. Zheng[1], H. Tenhunen[1]
[1]Royal Institute of Technology, Stockholm, Sweden
[2]Tarbiat Moallem University of Sabzevar, Sabzevar, Iran
[3]KU Leuven, Leuven, Belgium

A remote-powered UWB RFID tag in 0.18µm CMOS employs asymmetric communication links, i.e., UWB uplink and UHF downlink in order to achieve extremely low power, high data rate and accurate positioning. Measurement shows the tag can operate up to 10Mb/s with minimum input power of 14.1µW, corresponding to 13.9m of operation range.

11.3 A Pulsed UWB Receiver SoC for Insect Motion Control

9:30 AM

D. C. Daly[1], P. P. Mercier[1], M. Bhardwaj[1], A. L. Stone[2], J. Voldman[1], R. B. Levine[2], J. G. Hildebrand[2], A. P. Chandrakasan[1]
[1]Massachusetts Institute of Technology, Cambridge, MA
[2]University of Arizona, Tucson, AZ

A 1g, 2.5mW wireless motion control system for cyborg moths is presented, consisting of a 3-to-5GHz non-coherent pulsed UWB RX SoC with an integrated 4-channel PWM stimulator mounted on a 1.5×2.6cm^2 PCB. The highly duty-cycled RX requires 0.5 to 1.4nJ/b. A multistage tuned inverter-based RF front-end and differential signal chain allow for robust, low energy operation.

Break **10:00 AM**

11.4 Towards Terahertz Operation of CMOS

10:15 AM

S. Sankaran[1,2], C. Mao[1], E. Seok[1,2], D. Shim[1], C. Cao[1,3], R. Han[1], C-M. Hung[2], K. K. O[1]
[1]University of Florida, Gainesville, FL; [2]Texas Instruments, Dallas, TX
[3]NXP Semiconductors, Austin, TX

A 250GHz modulated signal generator and Schottky diode detector, a 110-to-140GHz Schottky diode frequency doubler, a 41GHz oscillator and a 2THz cut-off frequency polysilicon-gate separated Schottky diode fabricated in CMOS, and the design activities for 800GHz CMOS PLL suggest the possibility of 1THz CMOS operation.

11.5 A 2.75mW Wideband Correlation-Based Transceiver for Body-Coupled Communication

10:45 AM

A. Fazzi, S. Ouzounov, J. van den Homberg
Philips Research, Eindhoven, Netherlands

A transceiver architecture for body-coupled communication uses the frequency band from 1 to 30MHz and achieves data rates of up to 8.5Mb/s with capacitively coupled digital signals. The receiver uses correlation for synchronization and data detection. The sensitivity is 350μV_{pp} at 10^{-3} BER. The transceiver occupies 0.19mm^2 in 0.13µm CMOS and consumes 2.75mW with 1.2V supply.

11.6 A 128b Organic RFID Transponder Chip, including Manchester Encoding and ALOHA Anti-Collision Protocol, Operating with a Data Rate of 1529b/s

11:15 AM

K. Myny[1,2], M. J. Beenhakkers[3], N. A. van Aerle[3], G. H. Gelinck[4], J. Genoe[1,2], W. Dehaene[5], P. Heremans[1,5]
[1]IMEC, Leuven, Belgium; [2]KHLim, Diepenbeek, Belgium
[3]Polymer Vision, Eindhoven, Netherlands
[4]TNO Science and Industry, Eindhoven, Netherlands; [5]KU Leuven, Leuven, Belgium

A 128b organic RFID transponder chip is demonstrated. The digital logic foil comprises 1286 pentacene transistors and is fully operational at a supply voltage of 24V. It yields a data rate of 1529b/s. Additional functionality is included, such as Manchester encoding and a basic ALOHA anti-collision protocol. WORM memory is also demonstrated with an 8b plastic transponder chip.

11.7 Organic CMOS Circuits for RFID Applications

11:30 AM

R. Blache, J. Krumm, W. Fix
PolyIC, Fuerth, Germany

A 4b organic CMOS RFID transponder operating at a carrier frequency of 13.56MHz is presented. The integrated digital CMOS circuit is based on soluble organic p- and n-type semiconductors. At V_{DD}=-20V the circuit operates at a clock frequency of 196Hz. After 3 months storage at ambient no vital degradation in signal is found.

11.8 Silicon-Resonator-Based 3µA Real-Time Clock with ±5ppm Frequency Accuracy

11:45 AM

D. Ruffieux[1], F. Krummenacher[2]
[1]CSEM, Neuchatel, Switzerland; [2]EPFL, Lausanne, Switzerland

A 3µA ultra-low-power, thermally compensated 32768Hz RTC is realized from a piezoelectric-driven silicon resonator in the MHz range. The linear and quadratic TCFs as well as fabrication tolerance of the resonator are compensated by temperature-dependent fractional division and the on/off duty cycling of part of the resonator load capacitance. A digital temperature sensor implemented as a RC-controlled ring oscillator with a strong temperature dependency achieves a resolution of 0.02°C.

11.9 A 500µW Neural Tag with 2μV_{rms} AFE and Frequency-Multiplying MICS/ISM FSK Transmitter

12:00 PM

S. Rai, J. H. Holleman, J. N. Pandey, F. Zhang, B. P. Otis
University of Washington, Seattle, WA

A 500µW neural-spike streaming system designed in 0.13µm CMOS is presented. The MICS/ISM transmitter uses an edge-combining frequency-multiplying PA to allow the TX to operate 9X below the carrier. The analog front-end achieves NEF of 2.48 with 2μV_{rms} input-referred noise. The analog receiver with an 8b SAR ADC allows continuous transmission of spike data with a range of 15m.

Conclusion 12:15 PM

RF BUILDING BLOCKS

Session Chair: Hooman Darabi, Broadcom, Irvine, CA
Associate Chair: Nikolaus Klemmer, Ericsson Mobile Platforms, Raleigh, NC

12.1 A Low-Noise Active Balun with IM2 Cancellation for Multiband Portable DVB-H Receivers

8:30 AM

D. Mastantuono, D. Manstretta
University of Pavia, Pavia, Italy

A low-noise active balun achieves broadband impedance matching, low noise and high IIP2 at the same time by introducing a low-noise IM2-cancellation feedback. The measured minimum IIP2 is 28dBm, showing an improvement of 9dB. The circuit achieves IIP3 of 2.5dBm and NF of 3.5 to 4.5dB, while consuming 7.8mW from a 1.2V supply.

12.2 A 3.6mW Differential Common-Gate CMOS LNA with Positive-Negative Feedback

9:00 AM

S. Woo[1], W. Kim[1], C-H. Lee[2], K. Lim[1], J. Laskar[1]
[1]Georgia Institute of Technology, Atlanta, GA
[2]Samsung RFIC Design Center, Atlanta, GA

A differential common-gate 0.18µm CMOS LNA is designed with both positive and negative feedback to boost gain, partially cancel noise, and consume low power without sacrificing the bandwidth and linearity advantages of a CG topology. The measurement results show 21dB voltage gain, 2dB minimum NF, and -3.2dB IIP3 while drawing 2mA from a 1.8V supply.

12.3 A Compact Low-Noise Weighted Distributed Amplifier in CMOS

9:15 AM

Y-J. Wang, A. Hajimiri
California Institute of Technology, Pasadena, CA

The finite impulse response of a weighted distributed amplifier is used to selectively suppress noise at predetermined frequencies and integrate ESD protection. A 0.13µm CMOS 1-to-10.6GHz LNA with a minimum NF of 2.5dB and a power gain of 11 to 13dB, consuming 17mW of power and occupying 0.43mm^2 is demonstrated.

12.4 A 0.2-to-2.0GHz 65nm CMOS Receiver Without LNA Achieving >11dBm IIP3 and <6.5dB NF

9:30 AM

M. C. Soer, E. A. Klumperink, Z. Ru, F. E. van Vliet, B. Nauta
University of Twente, Enschede, Netherlands

A direct-conversion receiver with SFDR of 79dB in 1MHz is realized by optimizing a 4-phase one-quarter-duty-cycle passive mixer for conversion loss and noise folding, while realizing the gain via IF amplifiers linearized by resistive negative feedback. The 65nm CMOS chip consumes 67mW while achieving a gain>19dB, IIP3>11dBm and NF<6.5dB over a 0.2-to-2GHz bandwidth.

12.5 A 0.6V 380µW -14dBm LO-Input 2.4GHz Double-Balanced Current-Reusing Single-Gate CMOS Mixer with Cyclic Passive Combiner

9:45 AM

J. Deguchi, D. Miyashita, M. Hamada
Toshiba, Kawasaki, Japan

A 0.6V 380µW 2.4GHz CMOS down-conversion mixer fabricated in 90nm CMOS employs a single-gate mixer topology enhanced by a current-reuse architecture, a cyclic passive combiner and a linearity-enhancement biasing circuit. With LO input of -14dBm, conversion gain is 12.7dB, IIP3 is -6.0dBm and DSB NF at 1MHz is 11.8dB. FOM is 20.8dB.

Break 10:00 AM

12.6 A 4.75GHz Fractional Frequency Divider with Digital Spur Calibration in 45nm CMOS

10:15 AM

S. Pellerano[1], P. Madoglio[2], Y. Palaskas[1]
[1]Intel, Hillsboro, OR; [2]Milan Polytechnic University, Milan, Italy

A 4.75GHz fractional divider for WiFi/WiMax LO generation is implemented in 45nm CMOS. The digital calibration uses a sub-ps-resolution stochastic TDC to correct phase mismatch and suppress fractional spurs. After calibration, fractional spurs are on average below -50dBc/-59dBc ($\sigma \approx 2$dBc) with a 3.8/2.5GHz output frequency.

12.7 A 0.75V 325µW 40dB-SFDR Frequency-Hopping Synthesizer for Wireless Sensor Networks in 90nm CMOS

10:45 AM

E. Lopelli[1], J. D. van der Tang[2], K. Philips[3], A. H. van Roermund[1], B. Gyselinckx[3]
[1]Eindhoven University of Technology, Eindhoven, Netherlands
[2]Broadcom, Bunnik, Netherlands; [3]Holst Centre, Eindhoven, Netherlands

A 0.75V baseband I/Q frequency-hopping synthesizer in 90nm CMOS uses single-sideband mixing schemes, programmable dividers, Walsh-shaping and I/Q programmable notch filters to generate 56 channels with SFDR >40dB. Lowering the power an order of magnitude to 350µW, compared to existing solutions, enables new fast-hopping sub-mW transceiver architectures for wireless sensor networks.

12.8 A Software-Defined-Radio Receiver Architecture Robust to Out-of-Band Interference

11:15 AM

Z. Ru, E. Klumperink, G. Wienk, B. Nauta
University of Twente, Enschede, Netherlands

A 2-stage polyphase harmonic-rejection mixer robust to gain error achieves 2nd-to-6th HR of more than 60dB for 40 samples without calibration. Voltage gain is realized at IF with low-pass filtering to mitigate blockers and out-of-band IM distortion. A prototype 0.4-to-0.9GHz zero-IF receiver in 65nm CMOS has 34dB gain, 4dB NF, +3.5dBm IIP3 and +47dBm IIP2 while drawing 50mA from 1.2V.

12.9 A 400-to-900MHz Receiver with Dual-Domain Harmonic Rejection Exploiting Adaptive Interference Cancellation

11:45 AM

N. A. Moseley, Z. Ru, E. A. Klumperink, B. Nauta
University of Twente, Enschede, Netherlands

An HR downconverter uses adaptive interference cancellation in the digital domain to enhance the HR of a mixer in the RF domain. Analog mismatch limits HR to about 40dB, which is improved to >80dB for 3rd- and 5th-order HR. The RF part is realized in 65nm CMOS with 27dB gain, 4dB NF, 6dBm IIP3 and 52dBm IIP2 while consuming 28mA from a 1.2V supply. The digital part is implemented in software.

Conclusion 12:00 PM

FLASH MEMORY

Session Chair: Mark Bauer, Numonyx, Folsom, CA
Associate Chair: Dae-Seok Byeon, Samsung Electronics, Hwasung, Korea

13.1 A 172mm^2 32Gb MLC NAND Flash Memory in 34nm CMOS

1:30 PM

R. W. Zeng[1], M. Taub[1], T. Tanaka[2], N. Chalagalla[1], D. Chu[1], D. Elmhurst[1], M. Goldman[1], C. Haid[1], A. Huq[1], T. Ichikawa[2], J. Jorgensen[1], O. Jungroth[1], N. Kajla[1], R. Kajley[1], K. Kawai[2], J. Kishimoto[2], A. Madraswala[1], T. Manabe[2], V. Mehta[1], M. Morooka[2], K. Nguyen[1], Y. Oikawa[2], B. Pathak[1], R. Rozman[1], T. Ryan[1], A. Sendrowksi[1], W. Sheung[1], M. Szwarc[1], Y. Takashima[2], S. Tamada[2], T. Tanzawa[2], D. Udeshi[1], S. Yamada[1], H. Yokoyama[2]
[1]Intel, Folsom, CA
[2]Micron, Tokyo, Japan

A 3.3V 32Gb NAND Flash memory is fabricated in 34nm CMOS. The MLC device delivers 50µs t_{READ}, 900µs t_{PROG} and 9MB/s write throughput with in-silicon optimization of disturb mechanisms. The MLC NAND uses a center-page buffer architecture that is shared between the upper and lower half of the plane. A 33-cell string minimizes edge WL effects such as state inhibit, endurance and coupling.

13.2 A 1.8V 30nJ Adaptive Program-Voltage (20V) Generator for 3D-Integrated NAND Flash SSD

2:00 PM

K. Ishida[1], T. Yasufuku[1], S. Miyamoto[2], H. Nakai[2], M. Takamiya[1], T. Sakurai[1], K. Takeuchi[1]
[1]University of Tokyo, Tokyo, Japan
[2]Toshiba, Yokohama, Japan

A boost-converter-based adaptive voltage generator for 3D-integrated SSD is demonstrated. Frequency and duty cycle are dynamically optimized for various V_{PGM}. The power consumption reduces by 88%, rise-time reduces by 73% and circuit area of the voltage generator decreases by 85%. The total power consumption of a NAND Flash memory reduces by 68%.

13.3 A 48nm 32Gb 8-Level NAND Flash Memory with 5.5MB/s Program Throughput

2:30 PM

S. Chang, S. Park, S. Lee, M. Jung, J. Han, K. Lim, J. Lee, J. Kim, W. Kang, T. Kang, H. Byun, I. Wang, Y. Noh, L. Kwon, B. Koo, J. Yang, Y. Koh
Hynix Semiconductor, Icheon, Korea

A 48nm 32Gb 8-level NAND Flash memory is fabricated in a total area of 201mm^2. To get high-speed program throughput, a pass-bit detector is developed. It achieves approximately 30% increases in program throughput to 5.5MB/s compared to that of the conventional scheme.

Break 3:00 PM

13.4 A 113mm² 32Gb 3b/cell NAND Flash Memory

3:15 PM

T. Futatsuyama[1], N. Fujita[1], N. Tokiwa[1], Y. Shindo[1], T. Edahiro[1], T. Kamei[2], H. Nasu[2], M. Iwai[1], K. Kato[1], Y. Fukuda[1], N. Kanagawa[1], N. Abiko[1], M. Matsumoto[2], T. Himeno[1], T. Hashimoto[1], Y-C. Liu[2], H. Chibvongodze[2], T. Hori[2], M. Sakai[2], H. Ding[2], Y. Takeuchi[1], H. Shiga[1], N. Kajimura[1], Y. Kajitani[1], K. Sakurai[1], K. Yanagidaira[1], T. Suzuki[1], Y. Namiki[1], T. Fujimura[1], M. Mui[2], H. Nguyen[2], S. Lee[2], A. Mak[2], J. Lutze[2], T. Maruyama[1], T. Watanabe[1], T. Hara[1], S. Ohshima[1]

[1]Toshiba, Yokohama, Japan

[2]SanDisk, Milpitas, CA

A 113mm² 32Gb 3b/cell (8-levels) NAND Flash memory using sub-35nm CMOS technology is developed. This 32Gb Flash die is sufficiently small to fit the microSD memory card format widely adopted in cell phones. This is achieved by a combination of 3b/cell technology and feature-size scaling.

13.5 A 2Gb/s 15pJ/b/chip Inductive-Coupling Programmable Bus for NAND Flash Memory Stacking

3:45 PM

Y. Sugimori[1], Y. Kohama[1], M. Saito[1], Y. Yoshida[1], N. Miura[1], H. Ishikuro[1], T. Sakurai[2], T. Kuroda[1]

[1]Keio University, Yokohama, Japan

[2]University of Tokyo, Tokyo, Japan

An inductive-coupling programmable bus is designed in 0.18µm CMOS. Compared to a conventional SSD, this wireless interface using relayed transmission reduces power consumption by 2×, I/O circuit-layout area by 40×, and achieves a data rate of 2Gb/s. In addition, since it enables one package to contain 64 chips, it reduces the number of packages by 8×.

13.6 A 5.6MB/s 64Gb 4b/cell NAND Flash Memory in 43nm CMOS

4:15 PM

C. Trinh[1], N. Shibata[2], T. Nakano[2], M. Ogawa[2], J. Sato[2], Y. Takeyama[2], K. Isobe[2], B. Le[1], F. Moogat[1], N. Mokhlesi[1], K. Kozakai[1], P. Hong[1], T. Kamei[1], K. Iwasa[2], J. Nakai[2], T. Shimizu[2], M. Honma[2], S. Sakai[2], T. Kawaai[2], S. Hoshi[2], J. Yuh[1], C. Hsu[1], T. Tseng[1], J. Li[1], J. Hu[1], M. Liu[1], S. Skalid[1], J. Chen[1], M. Watanabe[1], H. Lin[1], J. Yang[1], K. McKay[1], K. Nguyen[1], T. Pham[1], Y. Matsuda[2], K. Nakamura[2], K. Kanebako[2], S. Yoshikawa[2], W. Igarashi[2], A. Inoue[2], T. Takahashi[2], Y. Komatsu[2], C. Suzuki[2], K. Kanazawa[2], M. Higashitani[1], S. Lee[1], T. Murai[1], K. Nguyen[1], J. Lan[1], S. Huynh[1], M. Murin[1], M. Shlick[1], M. Lasser[1], R. Cernea[1], M. Mofidi[1], K. Schuegraf[1], K. Quader[1]

[1]SanDisk, Milpitas, CA

[2]Toshiba, Yokohama, Japan

A 64Gb 16-level (16LC) NAND flash memory in 43nm CMOS technology is developed. In addition to reducing cost per bit with 4b/cell and improving memory density, 5.6MB/s write performance is achieved using a three-step programming method, ABL sensing, and a sequential-sense concept for read and verify.

Conclusion **4:45 PM**

DIGITAL WIRELESS AND RECONFIGURABILITY

Session Chair: Kees van Berkel, ST-NXP Wireless, Eindhoven, Netherlands
Associate Chair: Pascal Urard, STMicroelectronics, Crolles, France

14.1 A Reconfigurable 0.13µm CMOS 110pJ/pulse Fully Integrated IR-UWB Receiver for Communication and Sub-cm Ranging

1:30 PM

M. K. Verhelst, N. van Helleputte, G. Gielen, W. Dehaene
KU Leuven, Leuven, Belgium

A reconfigurable fully integrated IR-UWB receiver implements a complete analog front-end and digital back-end with algorithms for data reception, synchronization and precise ranging. The IC achieves an energy consumption of 110pJ/pulse. A wireless link in excess of 10m is demonstrated. Sub-cm accuracy is achieved with 660nJ/ranging operation.

14.2 A 0.55V 16Mb/s 1.6mW Non-Coherent IR-UWB Digital Baseband with ±1ns Synchronization Accuracy

2:00 PM

P. P. Mercier, M. Bhardwaj, D. C. Daly, A. P. Chandrakasan
Massachusetts Institute of Technology, Cambridge, MA

A highly parallel non-coherent digital baseband uses modified synchronization codes and quadratic correlators in place of matched filters to achieve a ±1ns synchronization accuracy with an integration period of 31.2ns. This reduces synchronization time by 11× compared with previous results. Implemented in a 90nm CMOS process, it draws 1.6mW at 0.55V during acquisition.

14.3 A 110nm RFCMOS GPS SoC with 34mW -165dBm Tracking Sensitivity

2:30 PM

J-M. Wei[1], A. Lu[1], C-F. Kuo[1], C-N. Chen[1], C-C. Liu[1], H-C. Chiu[1], H-C. Yeh[1], J-H. Shieh[1], K-T. Chen[1], K-S. Huang[1], K-I. Li[1], M-J. Wu[2], M-H. Li[1], S-H. Chou[1], W-L. Lien[2], W-G. Yau[1], W-Z. Ge[1], W-C. Lai[1], W-H. Ting[1], Y-C. Yen[1], Y-J. Tsai[1], Y-C. Yeh[1]
[1]MediaTek, Hsinchu, Taiwan
[2]MediaTek, Singapore

A 17.3mm^2 GPS SoC supports location applications in the L1-band at 1575.42MHz. It integrates an RF front-end, GPS baseband, ARM processor, peripheral controllers and PMU. The baseband architecture is optimized for correlation efficiency and power consumption and offers the best reported TTFF. Power consumption is 34mW during tracking and 45mW during acquisition.

Break 3:00 PM

14.4 A 0.13µm CMOS 655Mb/s 4×4 64-QAM K-Best MIMO Detector

3:15 PM

M. Shabany, G. Gulak
University of Toronto, Toronto, Canada

A scalable, pipelined K-Best 4×4 MIMO Detector for K=10 occupies a core area of 0.9mm^2 and supports an SNR-independent data throughput rate of 655Mb/s with a 270MHz clock and 1.3V supply while dissipating 126mW. The architecture expands and visits the intermediate nodes of the search tree on-demand while having a fixed-length critical path independent of constellation order or the number of antennas.

14.5 A 1GHz Digital Channel Multiplexer for Satellite Outdoor Unit Based on a 65nm CMOS Transceiver

3:45 PM

P. Busson[1], N. Chawla[2], J. Bach[1], S. Le Tual[1], H. Singh[2], V. Gupta[2], P. Urard[1]
[1]STMicroelectronics, Crolles, France
[2]STMicroelectronics, Noida, India

A digital channel multiplexer for satellite outdoor unit running at 1GHz clock frequency is implemented in a mixed-oxide dual-voltage 65nm CMOS technology. This transceiver, based on a 1GS/s DSP approach with 500MHz input and output bandwidth, embeds two 8b 1GS/s ADCs and two 8b 1GS/s DACs. It consumes less that 1022mW at ambient temperature while achieving noise rejection up to 42.5dB on a single tone and >37dB on modulated satellite channels.

14.6 A 300mV 494GOPS/W Reconfigurable Dual-Supply 4-Way SIMD Vector Processing Accelerator in 45nm CMOS

4:15 PM

H. Kaul, M. A. Anders, S. K. Mathew, S. K. Hsu, A. Agarwal, R. K. Krishnamurthy, S. Borkar
Intel, Hillsboro, OR

A 4-way SIMD accelerator for power-constrained microprocessors fabricated in 1.1V, 45nm CMOS occupies 0.081mm^2. Signed 32b multiply using reconfigurable 16b multipliers and adder circuits and voltage hopping with dual-supplies enables mode-dependent power savings while achieving wide operating range (1.3V to 230mV) with 2.3GHz, 161mW operation at 1.1V and peak SIMD energy efficiency of 494GOPS/W at 300mV, 50°C.

Conclusion **4:45 PM**

DISPLAY AND IMAGER ELECTRONICS

Session Chair: Iliana Fujimori-Chen, Analog Devices, Wilmington, MA
Associate Chair: Oh-Kyong Kwon, Hanyang University, Seoul, Korea

15.1 A Piecewise-Linear 10b DAC Architecture with Drain-Current Modulation for Compact AMLCD Driver ICs

1:30 PM

Y-J. Jeon[1], H-M. Lee[1], S-W. Lee[1], G-H. Cho[1], H. Kim[2], Y-K. Choi[2], M. Lee[2]
[1]KAIST, Daejeon, Korea; [2]Samsung Electronics, Yongin, Korea

A piecewise-linear 10b DAC for an AMLCD data driver with interpolation by drain-current modulation is reported. The DAC achieves a DNL of 0.37 LSB and INL of 1.71 LSB. Output voltage mean and standard deviation of 6.35mV and 0.54mV are achieved. Each DAC occupies 14×473μm^2 in 0.10μm CMOS and total chip power consumption is 9.4mW.

15.2 A 10b Column Driver with Variable-Current-Control Interpolation for Mobile Active-Matrix LCDs

2:00 PM

H-M. Lee[1], Y-J. Jeon[1], S-W. Lee[1], G-H. Cho[1], H-R. Kim[2], Y-K. Choi[2], M. Lee[2],
[1]KAIST, Daejeon, Korea
[2]Samsung Electronics, Yongin, Korea

A 10b column driver for mobile AMLCDs uses variable-current-control interpolation in buffer amplifiers. Bias-current steering improves the interpolation accuracy. The INL and DNL are 0.7 LSB and 0.4 LSB, respectively. A total chip size of 20.18×1.68mm^2 is obtained in a 0.10μm 1.5V/5V CMOS process. The total power consumption is 20mW.

15.3 A 0.1e$^-$ Vertical FPN 4.7e$^-$ Read Noise 71dB DR CMOS Image Sensor with 13b Column-Parallel Single-Ended Cyclic ADCs

2:15 PM

J. Park[1], S. Aoyama[1], T. Watanabe[1], T. Akahori[1], T. Kosugi[1], K. Isobe[1], Y. Kaneko[1], Z. Liu[1], K. Muramatsu[1], T. Matsuyama[1], S. Kawahito[2]
[1]Brookman Lab, Hamamatsu, Japan; [2]Shizuoka University, Hamamatsu, Japan

A CIS with 13b column-parallel cyclic ADCs is presented. A single-ended architecture with low read noise increases DR up to 71dB. A vertical FPN of 0.1e$^-_{rms}$ is attained using digital CDS, which performs A/D conversion twice in a horizontal scan period of 6.83μs. The imager has 7.07V/lx·s sensitivity, 5.6μm ADC pitch, 61μV/e$^-$ conversion gain, 4.7e$^-_{rms}$ read noise and <0.5 LSB DNL.

15.4 A Digital Driving Technique for an 8b QVGA AMOLED Display Using ΔΣ Modulation

2:30 PM

J. Jang[1], M. Kwon[1], E. Tjandranegara[1], K. Lee[2], B. Jung[1]
[1]Purdue University, West Lafayette, IN; [2]LG Electronics, Seoul, Korea

A digital driving technique for an AMOLED display using ΔΣ modulation that mitigates the TFT V_t–shift issue with a 2TFT-1C pixel structure is reported. It also solves the false-contour problem while achieving the same or better resolution and relaxed gate scan time compared with PWM. The system is implemented using a 2.2-inch QVGA AMOLED panel and FPGA.

Break 3:00 PM

HIGH-SPEED AND mm-WAVE CIRCUITS

Session Chair: Kumar Lakshmikumar, Conexant Systems, Red Bank, NJ
Associate Chair: Jae-Yoon Sim, Pohang University of Science and Technology, Pohang, Korea

16.1 An 18Gb/s Duobinary Receiver with a CDR-Assisted DFE

3:15 PM

K. Sunaga, H. Sugita, K. Yamaguchi, K. Suzuki
NEC, Sagamihara, Japan

A 90nm CMOS DFE achieves 18Gb/s over 25cm low-ε PCB trace. Binary signals from the transmitter are equalized to duobinary waveforms. The ISI is suppressed without the need for DFE tap feedback within a symbol interval. The symbol-rate CDR generates accurate sampling clocks for both data and edge. The overall circuit area is 480×420μm^2, and the receiver consumes 100.2mW from a 1.2V supply when operating at 18Gb/s.

16.2 A 43.7mW 96GHz PLL in 65nm CMOS

3:45 PM

K-H. Tsai, S-I. Liu
National Taiwan University, Taipei, Taiwan

A 96GHz PLL is fabricated in a 65nm CMOS process. The VCO circuit is designed by optimizing active and passive devices to achieve a low power consumption of 43.7mW from a 1.2V supply. The PLL locks from 95.1 to 96.5GHz. The reference spur is less than -50dBc.

16.3 An Array of 4 Complementary LC-VCOs with 51.4% W-Band Coverage in 32nm SOI CMOS

4:15 PM

D. Kim[1], J. Kim[2], C. Cho[1], J-O. Plouchart[3], M. Kumar[1], W-H. Lee[1], K. Rim[1]
[1]IBM, Hopewell Junction, NY; [2]Qualcomm, San Diego, CA
[3]IBM T. J. Watson, Yorktown Heights, NY

An array of 4 complementary LC-VCOs is implemented in 32nm SOI CMOS technology for wide-band tuning. The VCOs tune from 83.2 to 96.7GHz and from 100.1 to 104.3GHz, covering 51.4% of W-band. The VCOs occupy 40×35μm^2 and are scalable for an array implementation in nanometer SoC. The array of parallel VCOs aims to overcome process variation and to improve yield.

16.4 A mm-Wave CMOS Multimode Frequency Divider

4:30 PM

H-K. Chen[1], H-J. Chen[2], D-C. Chang[3], Y-Z. Juang[3], Y-C. Yang[1], S-S. Lu[1]
[1]National Taiwan Univeristy, Taipei, Taiwan; [2]Faraday Technology, Hsinchu, Taiwan
[3]Chip Implementation Center, Hsinchu, Taiwan

A multiband multi-mode ILFD operates at 38 and 57GHz. A conventional divide-by-2 ILFD is extended to include the function of divide-by-3. The chip is implemented in a 0.13μm CMOS and consumes 3.12mW from a 1V supply. The core occupies 0.023mm^2.

16.5 A 128.24-to-137.00GHz Injection-Locked Frequency Divider in 65nm CMOS

4:45 PM

B-Y. Lin, K-H. Tsai, S-I. Liu
National Taiwan Univeristy, Taipei, Taiwan

A 65nm CMOS ILFD uses split injection and split cross-coupled pair and has a locking range of 128.24 to 137.00GHz. It consumes 5.5mW from a 1.1V supply excluding the biasing circuit and buffers. The core area is 0.32×0.16mm^2.

Conclusion **5:00 PM**

TD: ENERGY-AWARE SENSOR SYSTEMS

Session Chair: Alison Burdett, Toumaz Technology, Abingdon, United Kingdom
Associate Chair: Shuichi Tahara, NEC, Tsukuba, Japan

17.1 A Robust Wireless Sensor Node for In-Tire-Pressure Monitoring

1:30 PM

M. Flatscher[1], M. Dielacher[1], T. Herndl[1], T. Lentsch[1], R. Matischek[1], J. Prainsack[1], W. Pribyl[2], H. Theuss[3], W. Weber[4]
[1]Infineon Technologies, Graz, Austria
[2]Graz University of Technology, Graz, Austria
[3]Infineon Technologies, Regensburg, Germany
[4]Infineon Technologies, Munich, Germany

A self-sufficient tire-mounted wireless sensor node integrates a BAW-based low-power FSK 2.11GHz transceiver, an energy-scavenger-based low-volume and low-weight power supply, and a 3D vertical chip stack for compactness, low volume, and robustness for pressure, inertia, and temperature sensing.

17.2 A Release-on-Demand Wireless CMOS Drug Delivery SoC Based on Electrothermal Activation Technique

2:00 PM

Y-J. Huang, H-H. Liao, Y-J. J. Yang, T. Wang, P-L. Huang, C-W. Lin, Y-H. Wang, S-S. Lu
National Taiwan University, Taipei, Taiwan

An implantable release-on-demand drug delivery SoC in CMOS technology monolithically integrates wireless circuitry and 8 addressable 100nL reservoirs fabricated by CMOS-compatible post-IC processing. Upon receiving wireless commands, the reservoir content can be released due to the rupture of membranes by electro-thermal heating.

17.3 A 5.2mW Self-Configured Wearable Body Sensor Network Controller and a 12μW 54.9% Efficiency Wirelessly Powered Sensor for Continuous Health Monitoring System

2:30 PM

J. Yoo, L. Yan, S. Lee, Y. Kim, H. Kim, B. Kim, H-J. Yoo
KAIST, Daejeon, Korea

A 0.18μm CMOS 4.8mm^2 sensor chip harvests its power by an adaptive threshold rectifier with 54.9% efficiency, and consumes 12μW at 120kb/s data rate with an ECG AFE. The 0.18μm CMOS 15.0mm^2 network controller locates the sensor positions, wirelessly provides power to and transacts data with only the selected sensors, while dissipating 5.2mW at 1.8V.

Break 3:00 PM

17.4 An Integrated Power Supply System for Low-Power 3.3V Electronics Using On-Chip Polymer Electrolyte Membrane (PEM) Fuel Cells

3:15 PM

M. Frank[1], M. Kuhl[1], G. Erdler[2], I. Freund[2], Y. Manoli[1], C. Müller[1], H. Reinecke[1]
[1]University of Freiburg - IMTEK, Freiburg, Germany
[2]Micronas, Freiburg, Germany

A stabilized power supply is realized by monolithically integrated micro fuel cells within an extended CMOS process. The fuel cell system delivers a maximum power output of 450μW/cm^2. The control circuitry consists of an LDO, an on-chip oscillator and a programmable timing network and consumes an average power of 435nW. The system reaches an efficiency of up to 89% and provides a constant output of 3.3V.

17.5 A mm-Sized Implantable Power Receiver with Adaptive Link Compensation

3:45 PM

S. O'Driscoll[1], A. S. Poon[2], T. H. Meng[1]
[1]Stanford University, Stanford, CA; [2]University of Illinois, Urbana-Champaign, IL

A wireless power transfer system for implanted medical devices uses an antenna area 100× smaller than previous designs. Adaptive simultaneous conjugate matching and a high efficiency rectifier and regulator in 0.13µm CMOS together with a 4mm^2 antenna delivers 140µW at 1.2VDC from a 4cm^2 transmit antenna and a 0.25W 915MHz source through 15mm of tissue.

17.6 An Efficient Piezoelectric Energy-Harvesting Interface Circuit Using a Bias-Flip Rectifier and Shared Inductor

4:15 PM

Y. K. Ramadass, A. Chandrakasan
Massachusetts Institute of Technology, Cambridge, MA

A bias-flip rectifier that can improve the power-extraction capability from piezoelectric harvesters over conventional full-bridge rectifiers by 4.2× is implemented in 0.35µm CMOS. An efficient control circuit regulates the output voltage of the rectifier and recharges a storage capacitor. The inductor used within the bias-flip rectifier is shared efficiently with switching DC-DC converters reducing the overall component count.

17.7 An Energy-Aware Multiple-Input Power Supply with Charge Recovery for Energy-Harvesting Applications

4:30 PM

N. J. Guilar[1,2], R. Amirtharajah[1], P. J. Hurst[1], S. H. Lewis[1]
[1]University of California, Davis, CA; [2]Agilent Technologies, Santa Clara, CA

A multiple-input power-management IC for energy-harvesting systems, incorporating an energy-aware switched-capacitor AC-DC converter and a highly flexible charge recycling DC-DC converter, is fabricated in 0.25µm CMOS. The measured AC-DC conversion efficiency is 84% while delivering 74µW and occupies 0.15mm^2.

17.8 Integrated Capacitive Power-Management Circuit for Thermal Harvesters with Output Power 10 to 1000µW

4:45 PM

I. Doms[1,2], P. Merken[1,3], R. P. Mertens[1,2], C. van Hoof[1,2]
[1]IMEC, Leuven, Belgium ; [2]KU Leuven, Leuven, Belgium
[3]R.M.A., Brussels, Belgium

An efficient and compact power-management circuit for thermoelectric generators as a power supply for on-the-body wireless sensor nodes is implemented in 0.35µm CMOS. The circuit can handle input power levels from 10µW to 1000µW. The control circuit consumes 2 to 7µW depending on the input power level. The control algorithm leads to a system efficiency up to 70%.

17.9 An Optically Programmable SoC for an Autonomous mm^3-Sized Microrobot

5:00 PM

R. Casanova Mohr, A. Dieguez, A. Arbat, O. Alonso, A. Sanuy, J. Canals, J. Samitier
University of Barcelona, Barcelona, Spain

An SoC fabricated in ultra-low-leakage 0.13µm CMOS is used in an autonomous microrobot. The SoC integrates into 2.6×2.6mm^2 the electronics required to manage all the required microrobot functions. The architecture is centered on an embedded 8051 microprocessor and exploits the event-driven nature of the robot tasks to maintain power consumption below 1.5mW.

Conclusion **5:15 PM**

Sunday, February 8th — ISSCC 2009 TUTORIALS

8:00 AM & 10:00 AM	**T1:** Continuous-Time Filters **T2:** Adaptive Power Management **T3:** Displays: Turning Bits Into Pictures **T4:** Digitally-Assisted RF **T5:** Displays with Organic Transistors	12:30 PM & 2:30 PM	**T6:** SAR ADCs **T7:** Adaptive Design Techniques **T8:** Variation-Tolerant SRAM **T9:** Linearity in Radio Front-Ends **T10:** High-Speed Wireline Transceivers

ISSCC 2009 FORUMS

8:00AM	**F1:** SSD, Memory Subsystem Innovation	**F2:** Medical Image Sensors	**F3:** GIRAFE: 4G RF Frontends	**F4:** Ultra-Low-Voltage Circuit Design
1:00 PM to 6:00 PM	**SF1:** Student Forum			

ISSCC 2009 EVENING SESSIONS

7:30PM	**SE1:** Healthy Radios: Radio and Microwave Devices for the Health Sciences		**SE2:** Is Fabless MEMS Fabulous?	

Monday, February 9th — ISSCC 2009 PAPER SESSIONS

8:15AM	**Session 1:** Plenary Session						
1:30PM	**Session 2:** Imagers	**Session 3:** Microprocessor Technologies	**Session 4:** High-Speed Data Converters	**Session 5:** Potpourri: PLL, Optical, DSL	**Session 6:** Cellular and Tuner		
5:15PM	Social Hour: Poster Session - DAC/ISSCC Student-Design-Contest Winners; Author Interviews						

ISSCC 2009 SESSIONS

8:00PM	**SE3:** Will ADCs Overtake Binary Frontends in Backplane Signaling	**SE4:** Highlights of IEDM2008	**E1:** Forewarned is Four-Armed:Classic Analog Misteakes to Avoid	**SE5:** Things all RFIC Designers Should Know (But are afraid to ask)

Tuesday, February 10th — ISSCC 2009 PAPER SESSIONS

8:30AM	**Session 7:** DRAM	**Session 8:** Multimedia Processors	**Session 9:** Data Converter Techniques	**Session 10:** Multi-Gb/s Serial Links and Building Blocks	**Session 11:** **TD:** Trends in Wireless Communications	**Session 12:** RF Building Blocks	
1:30PM	**Session 13:** Flash Memory	**Session 14:** Digital Wireless and Reconfigurability	**Session 15:** Display and Imager Electronics **Session 16:** High-Speed and mm-Wave Circuits		**Session: 17**: **TD:** Energy-Aware Sensor Systems	**Session 18:** Ranging and Gb/s Communication	**Session 19:** Analog Techniques
5:15PM	Poster Session - DAC/ISSCC Student-Design-Contest Winners; Author Interviews; University Alumni Events; Women's Networking Reception						

ISSCC 2009 EVENING SESSIONS

8:00PM	**SE6:** Interleaving ADCs - Exploiting the Parallelism	**SE7:** Next-Generation Energy-Scavenging System	**E2:** MID - "Scaled Down" PC or "Souped Up" Handheld?

Wednesday, February 11th — ISSCC 2009 PAPER SESSIONS

8:30PM	**Session 20:** Sensors and MEMS	**Session 21:** 10Gb/s-to-40Gb/s Transmitters and Receivers	**Session 22:** PA and Antenna Interface	**Session 23:** PLLs and Clocks	**Session 24:** Wireless Connectivity		
1:30PM	**Session 25:** Medical	**Session 26:** Switched-Mode Techniques	**Session 27:** SRAM and Emerging Memory	**Session 28:** **TD:** Directions in Computing and Signaling	**Session 29:** mm-Wave Circuits		
5:15 PM	Author Interviews						

Thursday, February 12th — ISSCC 2009 SHORT COURSE

8:00 AM & 10:00 AM	Low-Voltage Analog and Mixed-Signal CMOS Circuit Design

ISSCC 2009 FORUMS

8:00AM	**F5:** ATAC: High-Speed Interfaces	**F6:** Multi-Domain Processors	**F7:** Clock Synthesis Design	**F8:** Integrated Neural Interfaces

RANGING AND Gb/s COMMUNICATION

Session Chair: Didier Belot, STMicroelectronics, Crolles, France
Associate Chair: Yorgos Palaskas, Intel, Hillsboro, OR

18.1 A Fully Integrated 24GHz UWB Radar Sensor for Automotive Applications

1:30 PM

E. Ragonese[1], A. Scuderi[2], V. Giammello[1], E. Messina[2], G. Palmisano[1]
[1]University of Catania, Catania, Italy
[2]STMicroelectronics, Catania, Italy

A fully integrated 24GHz UWB radar sensor implemented in a 0.13µm SiGe BiCMOS process adopts an analog correlation receiver and is able to transmit UWB pulses of 0.5ns and 1ns. The PSD of the transmitted signal is compliant with the maximum allowed EIRP defined by the ETSI mask.

18.2 A Single-Chip Dual-Band 22-to-29GHz/77-to-81GHz BiCMOS Transceiver for Automotive Radar

2:00 PM

V. Jain, F. Tzeng, L. Zhou, P. Heydari
University of California, Irvine, CA

A dual-band mm-wave transceiver operating in the 22-to-29GHz and 77-to-81GHz short-range automotive radar bands is fabricated in a 0.18µm BiCMOS technology. The 3.9×1.9mm^2 circuit achieves 35/31dB gain, 4.5/8dB NF and -30dB isolation between the two bands in the receive mode, and an output P_{1dB} of 14.5/10.5dBm in the transmit mode while consuming 0.54/0.615W in the two bands.

18.3 A 77GHz Transceiver in Standard 90nm CMOS

2:30 PM

Y. Kawano, T. Suzuki, M. Sato, T. Hirose, K. Joshin
Fujitsu Laboratories, Atsugi, Japan

A 90nm CMOS 77GHz transceiver for automotive radar applications is comprised of signal generator, transmitter and receiver. The transmitter output power is 3.3 to 6.3dBm in the frequency range from 73.5 to 77.1GHz, SSB phase noise is -83dBc/Hz at 1MHz offset, and receiver conversion gain is 2±1.5dB in the RF input frequency range from 76 to 77GHz. The 2.4×1.2mm^2 chip consumes 920mW.

Break 3:00 PM

18.4 A 1.1nJ/b 802.15.4a-Compliant Fully Integrated UWB Transceiver in 0.13µm CMOS

3:15 PM

D. Lachartre, B. Denis, D. Morche, L. Ouvry, M. Pezzin, B. Piaget, J. Prouvée, P. Vincent
CEA-LETI-Minatec, Grenoble, France

A 1.1nJ/b 0.13µm CMOS monolithic transceiver for UWB impulse radio, developed for the 4-to-5GHz band, performs ranging with 30cm accuracy and communication up to 31Mb/s. The transceiver includes a dual-mode, coherent and non-coherent front-end aiming at IEEE 802.15.4a compliance. In addition, the chip integrates a complete DBPSK-compliant digital baseband modem.

18.5 A 90nm CMOS Low-Power 60GHz Transceiver with Integrated Baseband Circuitry

3:45 PM

C. Marcu, D. Chowdhury, C. Thakkar, L. Kong, M. Tabesh, J. Park, Y. Wang, B. Afshar, A. Gupta, A. Arbabian, S. Gambini, R. Zamani, A. M. Niknejad, E. Alon
University of California, Berkeley, CA

A low-power 90nm CMOS 60GHz transceiver that includes RF, LO, PLL and BB integrated into a single chip is designed. With a 1.2V supply the chip consumes 170mW while transmitting 10dBm, and 138mW while receiving. Measured data transmission up to 5Gb/s on each of I and Q channels, and data reception over a 1m wireless link at 4Gb/s QPSK with less than 10^{-11} BER are demonstrated.

18.6 A Low-Power Fully Integrated 60GHz Transceiver System with OOK Modulation and On-Board Antenna Assembly

4:15 PM

J. Lee, Y. Huang, Y. Chen, H. Lu, C. Chang
National Taiwan University, Taipei, Taiwan

A fully integrated 60GHz transceiver system employs OOK modulation and on-board dipole antenna co-design to accomplish low-power short-distance data transmission. With solid front-end design, low-cost antenna, and efficient modulator/demodulator the system achieves BER<10^{-12} for 2.5Gb/s 2^{31}-1 PRBS over a distance of 4cm with a total power consumption of 286mW.

18.7 A 2.88Gb/s Digital-Hopping UWB Transceiver

4:45 PM

A. Tanaka, K. Numata, H. Kodama, H. Ishikawa, N. Oshima, H. Yano
NEC, Sagamihara, Japan

A digital-hopping UWB transceiver, in which LO frequency hopping is replaced by a frequency-hopping polyphase filter, is fabricated in 90nm CMOS, consuming 156mW in RX mode. A baseband width of 800MHz, with a passive LPF and a high-pass feedback VGA, help attain data rates up to 2.88Gb/s while maintaining compatibility with the current 480Mb/s data rate.

Conclusion **5:00 PM**

ANALOG TECHNIQUES

Session Chair: Doug Smith, SMSC, Austin, TX
Associate Chair: Yoshihisa Fujimoto, Sharp, Tenri, Japan

19.1 A Chopper Current-Feedback Instrumentation Amplifier with a 1mHz 1/f Noise Corner and an AC-Coupled Ripple Reduction Loop

1:30 PM

R. Wu, K. A. A. Makinwa, J. H. Huijsing
Delft University of Technology, Delft, Netherlands

A chopper current-feedback instrumentation amplifier uses a continuous-time AC-coupled ripple-reduction loop. The loop reduces the amplitude of the chopper ripple by 1100×, to levels below the amplifier input-referred noise. Other specifications include 5µV offset, >130dB CMRR, 230µA current drawn from a 5V supply, and an input noise spectral density of 15nV/√Hz that is flat down to 6mHz.

19.2 A 140dB-CMRR Current-Feedback Instrumentation Amplifier Employing Ping-Pong Auto-Zeroing and Chopping

2:00 PM

M. A. Pertijs, W. J. Kindt
National Semiconductor, Delft, Netherlands

A ping-pong auto-zeroed current-feedback instrumentation amplifier uses settling phases to reduce output ripple, and chopping at half the auto-zeroing frequency to eliminate the increased low-frequency noise associated with auto-zeroing. It achieves an input noise of 27nV/√Hz, an offset of 3µV, and a CMRR of 140dB in a common-mode voltage range that includes the negative supply.

19.3 A 150pW Program-and-Hold Timer for Ultra-Low-Power Sensor Platforms

2:30 PM

Y-S. Lin, D. Sylvester, D. Blaauw
University of Michigan, Ann Arbor, MI

A low-power timer is presented that uses a program-and-hold technique that consumes 150pW using an 11Hz current-starved oscillator. A temperature-insensitive current source is implemented by self-biasing of a resistor. Using a charge-holding technique, the active power is reduced by 200× as compared to the programming power. The 0.13µm CMOS design occupies 0.019mm^2 and has 5% cycle-time error when temperature varies from 0 to 90°C.

19.4 A 65nm CMOS Comparator with Modified Latch to Achieve 7GHz/1.3mW at 1.2V and 700MHz/47µW at 0.6V

2:45 PM

B. Goll, H. Zimmermann
Vienna University of Technology, Vienna, Austria

A comparator in a low-power CMOS technology ($V_t \approx 0.4V$) is presented, where a conventional latch consisting of two cross-coupled inverters is modified for fast operation even at a low supply voltage of 0.6V without needing static current. The sensitivity (BER of 10^{-9}) for 1.2V supply is 281mV at 7GHz and 27.2mV at 5GHz and for 0.6V supply is 90.2mV at 700MHz and 16mV at 500MHz.

Break 3:00 PM

19.5 A 25mA 0.13µm CMOS LDO Regulator with Power-Supply Rejection Better Than -56dB up to 10MHz Using a Feedforward Ripple-Cancellation Technique

3:15 PM

M. El-Nozahi, A. Amer, J. Torres, K. Entesari, E. Sánchez-Sinencio
Texas A&M University, College Station, TX

A feedforward ripple-cancellation technique is applied to an LDO regulator for achieving a high PSRR over a wide frequency range. The LDO is implemented in 0.13µm CMOS and supplies current up to 25mA with a minimum drop-out voltage of 0.15V. The measured PSRR shows a rejection better than -56dB up to 10MHz, while drawing a quiescent current of 50µA with a bandgap reference circuit included. Load regulation of 1.2mV for a 25mA step in load current is measured.

19.6 A sub-1V Bandgap Voltage Reference in 32nm FinFET Technology

3:30 PM

A-J. Annema[1], P. Veldhorst[1], G. Doornbos[2], B. Nauta[1]
[1]University of Twente, Enschede, Netherlands
[2]NXP Semiconductors, Leuven, Belgium

A sub-1V bandgap reference circuit is implemented in 32nm SOI FinFET technology, introducing an architecture that minimizes the total required resistor value. The circuit operates correctly for supply voltages above 0.9V with a supply current of 14µA at room temperature.

19.7 A 90nm CMOS CT BPF for Bluetooth Transceivers with DT 1b-Switched-Resistor Cutoff-Frequency Control

3:45 PM

H. Majima, M. Hamada
Toshiba, Kawasaki, Japan

A filter cutoff-frequency tuning scheme is presented. A 1b switched resistor operating at 200MHz is utilized. The effective RC time constant is controlled by the duty ratio of 1b signal. Compared to a conventional tuning scheme, finer frequency tuning and more linear control are achieved. $\Delta\Sigma$ modulation with dithering mitigates the spurious effect. The tuning scheme is applied to a channel-select BPF in a Bluetooth transceiver and achieves 6.3kHz-step cutoff-frequency control and less than 1.8kHz of differential linearity in a 1.2V 90nm CMOS design.

19.8 A 1.25mW 75dB-SFDR CT Filter with In-Band Noise Reduction

4:15 PM

A. Liscidini, A. Pirola, R. Castello
University of Pavia, Pavia, Italy

A filter technique based on cross-connected cascoded devices gives in-band highpass noise shaping and passive pre-filtering of out-of-band blockers. This results in both below kT/C in-band noise and out-of-band high IIP3. A 4^{th}-order LPF prototype in 90nm CMOS for WCDMA application has 32µV noise, integrated over the standard bandwidth, and +36dBm out-of band IIP3 that results in a 75dB SFDR with 1.25mW power consumption. Active die area is $0.5mm^2$.

Conclusion **4:45 PM**

SE6: Interleaving ADCs – Exploiting the Parallelism

Organizer: **Raf Roovers,** *NXP Semiconductors, Eindhoven, Netherlands*

Chair: **Kong-Pang Pun,** *Chinese University of Hong Kong, Hong Kong, China*

Why have interleaved ADCs become more and more popular in recent years? Are other ADC architectures running out of steam, and will interleaved ADCs become the standard in the near future just as multi-core microprocessors are replacing single core? Due to the shrinking area of a single converter, many slices can be integrated in parallel, resulting in a new degree of freedom for ADC designers, one providing higher speeds, better efficiency, and more flexibility. In this Session, an overview of recent developments in interleaving ADCs is provided.

Time	Topic
8:00	**Time Interleaved Analog-to-Digital Converters: An Algorithmic Melting Pot** **Kostas Doris,** *NXP Semiconductors, Eindhoven, Netherlands*
8:30	**Ultra-High-Speed Calibrated Time-Interleaved ADCs** **Pier Andrea Francese,** *National Semiconductor, Munich, Germany*
9:00	**Blind Identification Solves the Interleaving Problem** **Jan-Erik Eklund,** *SP Devices, Linköping, Sweden*
9:30	**Time-Interleaved ADCs, Past and Future** **Ken Poulton,** *Agilent Laboratories, Santa Clara, CA*

SE7: Next-Generation Energy-Scavenging Systems

Organizer: **Anantha Chandrakasan,** *MIT, Cambridge, MA*

Chair: **Uming Ko,** *Texas Instruments, Dallas, TX*
Christian Enz, *CSEM SA, Neuchâtel, Switzerland*

A decade of R&D in energy scavenging has resulted in micro-generators based on photovoltaic, vibration, and thermal mechanisms that produce 10's to 100's microwatts of power. These generators could power ultra-low-power portable devices from sensors and embedded processors to MP3 players, medical electronics, etc. More recently, there has also been a push towards wireless power transfer that can provide energy to higher-power portable equipment or appliances. The next step is to design 2nd-generation energy scavenging systems that optimize generators, conversion circuits, load electronics and energy storage that "buffers" the variations of scavenged energy. The challenges to achieve "fully autonomous operation" or "green portable" will be power efficiency, versatility, miniaturization, weight, and cost! The overall vision, advancement, and practical limits of various techniques will be discussed.

Time	Topic
8:00	**State-of-the-Art in Vibration and Thermo-Electric Generators, Circuits and Systems** **Chris Van Hoof,** *IMEC, Leuven, Belgium*
8:30	**Organic Photovoltaics and Solar Concentrators** **Marc Baldo,** *MIT, Cambridge, MA*
9:00	**Thermal Energy Scavenging Using Thin-Film TEG Devices** **Burkhard Habbe,** *Micropelt GmbH, Freiburg, Germany*
9:30	**Wireless Power** **Takayasu Sakurai,** *University of Tokyo, Tokyo, Japan*

E2: MID – 'Scaled Down' PC or 'Souped Up' Handheld?

Co-Organizers: **Yiwan Wong**, *Samsung, Yougin, Gyeonggi, Korea*
Raney Southerland, *ARM, Austin, TX*

Moderator: **Jan Rabaey**, University of *California, Berkeley, CA*

The new emerging Mobile Internet Device (MID) market has quite a few dynamics going on for what seems to be a promising driver for future consumer electronic equipment growth. This means that existing high-performance, personal-computer-focused, CPU architectures will need to reduce power consumption, and existing consumer-focused, low-power, embedded-core architectures will need to improve performance. Players in this space are not limited to the CPU core providers, but also platforms, consumer equipment makers, computer makers, software providers, etc. Discussion will include: how one or the other architectures is best fitted, strategies if appropriate, and how the eco system will all be tied together.

Panelists:
Shane Wall, *Intel, Santa Clara, CA*
Ian Drew, *ARM, Cambridge, United Kingdom*
Sampo Nurmentaus, *Movial, Helsinki, Finland*
Seshu Madhavapeddy, *Texas Instruments, Dallas, TX*
John Bruggeman, *Wind River, Alameda, CA*
Luis Pineda, *Qualcomm, San Diego, CA*

SENSORS AND MEMS

Session Chair: Christoph Hagleitner, IBM, Rüschlikon, Switzerland
Associate Chair: Kofi Makinwa, Delft University of Technology, Delft, Netherlands

20.1 A 1.05V 1.6mW 0.45°C 3σ-Resolution ΔΣ-Based Temperature Sensor with Parasitic-Resistance Compensation in 32nm CMOS

8:30 AM

Y. Li, H. Lakdawala, A. Raychowdhury, G. Taylor, K. Soumyanath
Intel, Hillsboro, OR

A temperature sensor in 32nm high-κ metal-gate digital CMOS is presented for microprocessor power and thermal management. The sensor comprises a front-end based on parasitic PNPs driven by chopped ratioed current sources and followed by a 2nd-order FB ΔΣ ADC. The sensor operates from -10 to 110°C, achieving a 3σ resolution of 0.45°C and <5°C inaccuracy without trimming.

20.2 A CMOS Smart Temperature Sensor with a Batch-Calibrated Inaccuracy of ±0.25°C (3σ) from -70 to 130°C

9:00 AM

A. L. Aita[1,2], M. A. Pertijs[3], K. A. A. Makinwa[1], J. H. Huijsing[1]
[1]Delft University of Technology, Delft, Netherlands
[2]Federal University of Santa Maria, Santa Maria, Brazil
[3]Holst Centre, Eindhoven, Netherlands

A 0.7µm CMOS smart temperature sensor has a batch-calibrated inaccuracy of ±0.25°C (3σ) from -70 to 130°C. This 2× improvement over the state-of-the-art is achieved at 3× lower power consumption. A PTAT clocking scheme reduces errors due to incomplete settling and leakage. Individual trimming reduces the sensor inaccuracy to ±0.1°C (3σ) over the military range from -55 to 125°C.

20.3 An Interface for a 300°/s Capacitive 2-Axis Micro-Gyroscope with Pseudo-CT Readout

9:30 AM

L. J. Aaltonen[1], T. Speeti[1], M. Saukoski[1,2], K. Halonen[1]
[1]Helsinki University of Technology, Espoo, Finland
[2]ELMOS Semiconductor, Dortmund, Germany

An interface for a capacitive 2-axis micro-gyroscope is implemented in 0.35µm HVCMOS with an active area of 2.5mm^2. The sensor start-up time is 0.4s and the x- and y-axis noise floors are 0.015°/s/√Hz and 0.041°/s/√Hz, respectively. The supply current for the on-chip charge pump, and drive and sense interfaces is 1.8mA. Area reduction is enabled by the pseudo-CT readout technique.

Break 10:00 AM

20.4 An Instrument-on-Chip for Impedance Measurements on Nanobiosensors with attoFarad Resolution

10:15 AM

F. Gozzini, G. Ferrari, M. Sampietro
Milan Polytechnic University, Milano, Italy

A high-resolution integrated impedance characterization system consists of a low-noise (3fA/√Hz up to 100kHz) current-to-voltage converter, a passive multiplier and a 20b ΔΣ ADC. With 50mV applied to the sample, it achieves a resolution of 1aF and is well-suited for measurements on nanobiodevices.

20.5 A Sub-pA ΔΣ Current Amplifier for Single-Molecule Nanosensors

10:45 AM

M. Bennati[1], F. Thei[1], M. Rossi[2], M. Crescentini[1], G. D'Avino[3], A. Baschirotto[3,4], M. Tartagni[1]
[1]University of Bologna, Cesena, Italy
[2]Silicon Biosystems, Cesena, Italy
[3]University of Salento, Lecce, Italy
[4]University of Milano-Bicocca, Lecce, Italy

A current-readout front-end for nanosensors based on a ΔΣ converter approach features an input-equivalent noise of 5fA/√Hz in a 1kHz bandwidth. The front-end detects ion-channel activity caused by single-molecule interactions. The device occupies 0.5mm^2 in 0.35µm 2P4M CMOS and consumes less than 23mW.

20.6 A Compact CMOS MEMS Microphone with 66dB SNR

11:00 AM

J. H-C. Citakovic[1,2], P. F. Høvesten[1], G. Rocca[1], A. Halteren[3], P. Rombach[1], L. J. Stenberg[1], P. Andreani[4], E. Bruun[2]
[1]Pulse, Roskilde, Denmark
[2]Technical University of Denmark, Lyngby, Denmark
[3]Pulse, Amsterdam, Netherlands
[4]Lund University, Lund, Sweden

A microphone system comprising 2 differentially operated MEMS microphones and a 0.18µm CMOS differential amplifier mounted on a common substrate die has a volume of 2.6×3.2×0.865mm^3 and an SNR of 66dBA over the 20Hz-to-20kHz audio band. Its sensitivity is -33.5dB (V_{rms}/Pa), its PSRR is >55dB, and its THD is <1% for sound pressure levels below 112dB. It consumes 120µA from a 1.8V supply.

20.7 A 2×32 Range-Finding Sensor Array with Pixel-Inherent Suppression of Ambient Light up to 120klx

11:15 AM

G. Zach, H. Zimmermann
Vienna University of Technology, Vienna, Austria

A 0.6µm BiCMOS correlation-based time-of-flight pixel circuit is reported that electronically suppresses up to 120klx of ambient light by using 2 memory capacitors. The fill factor is 58% with a 100×100µm^2 PIN-photodiode. Line sensor measurements for distances up to 3.2m are reported. The standard deviation is below 2cm for distances up to 1.2m with a measurement time of 50ms/point and 850nm LED illumination.

20.8 A 0.25µm Logarithmic CMOS Imager for Emissivity-Compensated Thermography

11:45 AM

F. X. Hutter, J. N. Burghartz
Institute for Microelectronics, Stuttgart, Germany

A 640×480-pixel 40fps device for a ratio-pyrometric thermal imaging camera includes pixel cells with a logarithmic response over a 140dB dynamic range. This allows ratio operations by subtracting signals from two neighboring pixels, one of which is covered by an IR filter, thus enabling the temperature measurements, independent of the object's emissivity.

Conclusion 12:15 PM

10Gb/s-to-40Gb/s TRANSMITTERS AND RECEIVERS

Session Chair: Naresh Shanbhag, University of Illinois at Urbana-Champaign, IL
Associate Chair: Takuji Yamamoto, Fujitsu Laboratories, Kawasaki, Japan

21.1 A 40Gb/s Multi-Data-Rate CMOS Transceiver Chipset with SFI-5 Interface for Optical Transmission Systems

8:30 AM

Y. Amamiya[1], S. Kaeriyama[2], H. Noguchi[1], Z. Yamazaki[1], T. Yamase[1], K. Hosoya[1], M. Okamoto[3], S. Tomari[4], H. Yamaguchi[4], H. Shoda[4], H. Ikeda[4], S. Tanaka[4], T. Takahashi[5], R. Ohhira[2], A. Noda[1], K. Hijioka[6], A. Tanabe[6], S. Fujita[1], N. Kawahara[5]
[1]NEC, Kawasaki, Japan
[2]NEC, Sagamihara, Japan
[3]NEC Engineering, Kawasaki, Japan
[4]NEC, Tokyo, Japan
[5]NEC, Chiba, Japan
[6]NEC Electronics, Sagamihara, Japan

A fully integrated 40Gb/s transmitter and receiver chipset is implemented in 65nm CMOS and packaged in plastic BGA. The full-rate transmitter with a 40GHz VCO and 40Gb/s retiming generates an output eye with rms jitter of 570fs to 900fs over the range of 39.8Gb/s to 44.6Gb/s at 2^{31}-1 PRBS. Power dissipation of each chip is 2.8W and die size is 4.9×5.2mm^2.

21.2 A Single-40Gb/s Dual-20Gb/s Serializer IC with SFI-5.2 Interface in 65nm CMOS

9:00 AM

K. Kanda[1], H. Tamura[1], T. Yamamoto[1], S. Matsubara[1], M. Kibune[1], Y. Doi[1], T. Shibasaki[1], S. Parikh[2], A. Kristensson[2], N. Tzartzanis[2], S. Ide[3], Y. Tsunoda[1], T. Yamabana[1], M. Sugawara[1], N. Kuwata[1], T. Ikeuchi[3], J. Ogawa[1], B. Walker[2]
[1]Fujitsu Laboratories, Kawasaki, Japan
[2]Fujitsu Laboratories of America, Sunnyvale, CA
[3]Fujitsu Limited, Kawasaki, Japan

A 40Gb/s serializer IC is implemented in 65nm CMOS. The IC has an SFI5.2-compliant 10Gb/s input interface and supports two different output modes, single 40Gb/s for OC-768 VSR and dual 20Gb/s for DQPSK. The IC is evaluated on a PCB and error-free operation is confirmed. The chip consumes 1.8W in the 40Gb/s mode, and 1.6W in the 20Gb/s mode from 1.2V and 3.3V supplies. The die size is 4.2×4.2mm^2.

21.3 A 40Gb/s Full-Rate 2:1 MUX in 0.18µm CMOS

9:30 AM

A. Yazdi, M. M. Green
University of California, Irvine, CA

A 40Gb/s 2:1 MUX is implemented in 0.18µm standard CMOS. Deterministic jitter is reduced from 600fs to 350fs via the use of a dynamic retimer clocked at 40GHz. The 40GHz clock is generated by a push-push VCO using two quadrature 20GHz oscillators. The transmitted single-ended data swing is 241mV$_{pp}$. A low-power distributed buffer is used to drive the 40Gb/s data to an off-chip 50Ω termination.

Break 10:00 AM

21.4 An 80mW 40Gb/s 7-Tap T/2-Spaced FFE in 65nm CMOS

10:15 AM

A. Momtaz[1,2], M. M. Green[1]
[1]University of California, Irvine, CA
[2]Broadcom, Irvine, CA

A 7-tap 40Gb/s FFE is implemented in a 65nm standard CMOS process. Tap-delay frequency-response variation is less than 1dB up to 20GHz and tap-to-tap delay variation is less than 2ps. More than 50% vertical and 70% horizontal eye opening from a closed input eye are observed. The FFE occupies 1mm^2 area and consumes 80mW from a 1V supply.

21.5 A 20Gb/s Full-Rate Linear CDR Circuit with Automatic Frequency Acquisition

10:45 AM

J. Lee, K-C. Wu
National Taiwan University, Taipei, Taiwan

A 20Gb/s full-rate CDR circuit is fabricated in 90nm CMOS and uses mixer-based linear phase detector and automatic frequency-locking technique without external reference. The recovered clock achieves a jitter of 407fs$_{rms}$ and 3.00ps$_{pp}$ on the recovered clock while consuming 154mW from a 1.5V supply. The die size is 0.97×0.88mm^2.

21.6 A 78mW 11.1Gb/s 5-Tap DFE Receiver with Digitally Calibrated Current–Integrating Summers in 65nm CMOS

11:15 AM

J. F. Bulzacchelli, T. O. Dickson, Z. Toprak Deniz, H. A. Ainspan, B. D. Parker, M. P. Beakes, S. V. Rylov, D. J. Friedman
IBM T. J. Watson, Yorktown Heights, NY

A 65nm CMOS 5-tap DFE receiver uses half-rate S/Hs and current-integrating summers to achieve 11.1Gb/s operation while consuming 78mW. RX logic calibrates the summer bias currents to stabilize their performance over process variations and different data rates. The receiver exhibits an input sensitivity of 38mV$_{pp\text{-}diff}$ at 8.5Gb/s. Equalization of a 30-inch PCB trace and a 16-inch Tyco backplane is demonstrated at 11.1 and 10Gb/s, respectively.

21.7 A 500mW Digitally Calibrated AFE in 65nm CMOS for 10Gb/s Serial Links over Backplane and Multimode Fibre

11:45 AM

J. Cao, B. Zhang, U. Singh, D. Cui, A. Vasani, A. Garg, W. Zhang, N. Kocaman, D. Pi, B. Raghavan, H. Pan, I. Fujimori, A. Momtaz
Broadcom, Irvine, CA

A DSP-based transceiver AFE is implemented in 65nm CMOS for 10Gb/s backplane/MMF applications. A 6b interleaved ADC in the receive-path is digitally calibrated and achieves 31.6dB SNDR and 39.0dB SFDR with a 5GHz input. The PLL uses a calibrated LC-VCO and the TX features a 3-tap FIR. The output exhibits 0.38ps$_{rms}$ RJ and 2.9ps$_{pp}$ ISI. The AFE occupies 3mm^2 and consumes 500mW from a 1V supply.

Conclusion 12:15 PM

PA AND ANTENNA INTERFACE

Session Chair: Michael Zybura, RFMD, Scotts Valley, CA
Associate Chair: Hiroyuki Sakai, Panasonic, Osaka, Japan

22.1 A 0.13µm CMOS Power Amplifier with Ultra-Wide Instantaneous Bandwidth for Imaging Applications

8:30 AM

J. Roderick, H. Hashemi
University of Southern California, Los Angeles, CA

A 0.13µm, 1.8×2.0mm^2 CMOS PA with an ultra-wide instantaneous bandwidth delivers a maximum class-A saturated output power of 21dBm with 3dB BW from 0.75 to 3.75GHz. The PA core is a 7-stage distributed amplifier with tapered characteristic impedance at the drain to eliminate the efficiency-degrading reverse-wave termination. The PA output is a 1-to-16 impedance transformer.

22.2 An Octave-Range Watt-Level Fully Integrated CMOS Switching Power Mixer Array for Linearization and Back-Off Efficiency Improvement

9:00 AM

S. Kousai[1,2], A. Hajimiri[1]
[1]California Institute of Technology, Pasadena, CA
[2]Toshiba, Kawasaki, Japan

A fully integrated octave-range 0.13µm CMOS power mixer occupies 2.6mm^2 with an output power of +31.3dBm into an external 50Ω load with a PAE of 42% at 1.8GHz and full-power gain compression of 0.4dB. The PAE with a non-constant-envelope 16QAM modulation is 19% with an average output power of +25.8dBm and an EVM of 5.2%.

22.3 A Single-Chip Highly Linear 2.4GHz 30dBm Power Amplifier in 90nm CMOS

9:30 AM

D. Chowdhury[1], C. Hull[2], O. Degani[2], P. Goyal[2], Y. Wang[1,2], A. M. Niknejad[1]
[1]University of California, Berkeley, CA
[2]Intel, Hillsboro, OR

A 90nm 2.4GHz CMOS linear PA uses a bypass network to ensure stability without sacrificing gain, achieving a saturated output power of 30.1dBm with 33% PAE and 28dB small-signal gain. Optimal biasing and capacitive compensation produce flat AM-to-AM and AM-to-PM response up to high power. With an OFDM modulated signal the PA has EVM better than -25dB at 22.7dBm average power.

Break 10:00 AM

22.4 A 60GHz-Band 1V 11.5dBm Power Amplifier with 11% PAE in 65nm CMOS

10:15 AM

W. L. Chan[1], J. R. Long[1], M. Spirito[1], J. J. Pekarik[2]
[1]Delft University of Technology, Delft, Netherlands
[2]IBM, Burlington, VT

A 65nm CMOS 60GHz three-stage differential PA uses transformers for input and output matching, and each gain stage uses a common-source amplifier with cross-connected neutralization capacitors to ensure stability. The 0.13×0.41mm^2 PA achieves a saturated output of 11.5dBm with 11% PAE from a 1V supply. Peak S_{21} is 15dB, with 10GHz 3dB bandwidth, and the S_{12} is better than -42dB.

22.5 50-to-67GHz ESD-Protected Power Amplifiers in Digital 45nm LP CMOS

10:45 AM

J. Raczkowski[1,2], W. De Raedt[2], B. Nauwelaers[1], P. Wambacq[2,3]
[1]KU Leuven, Leuven, Belgium
[2]IMEC, Heverlee, Belgium
[3]Vrije Universiteit Brussel, Brussels, Belgium

Two 60GHz power amplifiers in 45nm low-power digital CMOS achieve P_{1dB} of +8.4dBm and +10.6dBm and P_{sat}>+10.6dBm and +13.8dBm respectively with 1.1V supply. The output-power performance is maintained within the 50-to-67GHz range. The amplifiers have an ESD protection level of more than 5kV HBM.

22.6 A CMOS Adaptive Antenna-Impedance-Tuning IC Operating in the 850MHz-to-2GHz Band

11:15 AM

H. Song, B. Bakkaloglu, J. T. Aberle
Arizona State University, Tempe, AZ

A closed-loop adaptive antenna-impedance-tuning IC operating in the 850MHz-to-2GHz band performs a scan of 4096 antenna-matching-network states in 4.1ms, achieving an average return loss improvement of 15dB across the bandwidth and an average power savings of 370mW at 900MHz. The system uses a mixed-signal matching-state-search technique, replacing the need for an ADC.

22.7 A Tunable Integrated Duplexer with 50dB Isolation in 40nm CMOS

11:45 AM

M. Mikhemar[1], H. Darabi[1], A. Abidi[2]
[1]Broadcom, Irvine, CA
[2]University of California, Los Angeles, CA

A fully integrated 40nm CMOS tunable duplexer for full-duplex transceivers, based on a hybrid transformer and tuned for WCDMA band II, achieves 50dB isolation with 2.9dB receiver insertion loss and 1GHz tuning range, demonstrating comparable performance to that of external duplexers. The cascade of the duplexer and the LNA achieves a noise figure of 6.1dB, a gain of 23dB, and occupies an area of 0.2mm^2.

Conclusion **12:00 PM**

PLLs AND CLOCKs

Session Chair: Ivan Bietti, STMicroelectronics, Grenoble, France
Associate Chair: Changsik Yoo, Hanyang University, Seoul, Korea/ Silicon Image, Sunnyvale, CA

23.1 A 1MHz-Bandwidth Type-I ΔΣ Fractional-N Synthesizer for WiMAX Applications

8:30 AM

H. Hedayati[1], B. Bakkaloglu[1], W. Khalil[2]
[1]Arizona State University, Tempe, AZ; [2]Intel, Chandler, AZ

A 6GHz Type-I fractional-N PLL with a noise-cancelling discrete-time S/H loop-filter is presented. The 1MHz-BW PLL utilizes an inherently linear PFD and noise-cancelling charge-pump-DAC circuit to reduce quantization noise by more than 20dB. The chip is implemented in 0.18µm CMOS and has a core area of 2.7×1.2mm^2. With 26mA current draw from a 1.8V supply, the measured worst-case near-integer in-band spur is -61dBc and the integrated rms phase error is -42dBc.

23.2 A 2.2GHz 7.6mW Sub-Sampling PLL with -126dBc/Hz In-Band Phase Noise and 0.15ps$_{rms}$ Jitter in 0.18µm CMOS

9:00 AM

X. Gao[1], E. A. Klumperink[1], M. Bohsali[2], B. Nauta[1]
[1]University of Twente, Enschede, Netherlands
[2]National Semiconductor, Santa Clara, CA

A low-jitter 2.2GHz PLL exploits a phase detector that sub-samples the VCO output with the reference clock and requires no divider in locked state. It achieves an rms output jitter of 0.15ps (10kHz to 40MHz) and an in-band phase noise of -126dBc/Hz at 200kHz offset. The PLL draws 4.2mA from a 1.8V supply and occupies an active area of 0.4×0.45mm^2 in 0.18µm CMOS.

23.3 An Edge-Missing Compensator for Fast-Settling Wide-Locking-Range PLLs

9:30 AM

T-H. Chien[1], C-S. Lin[1], Y-Z. Juang[1], C-M. Huang[1], C-L. Wey[1,2]
[1]National Chip Implementation Center, Hsinchu, Taiwan
[2]National Central University, Jhongli, Taiwan

An edge-missing compensator (EMC) is proposed to approach the function of an ideal PD with ±512π linear range. A PLL implemented with a 9b EMC achieves 320MHz frequency hopping within 10µs logarithmically which is about 2.4× faster than conventional designs. The reference spur of the PLL is -48.7dBc and the phase noise is -88.31dBc/Hz at 10kHz offset.

Break 10:00 AM

23.4 A 975-to-1960MHz Fast-Locking Fractional-N Synthesizer with Adaptive Bandwidth Control and 4/4.5 Prescaler for Digital TV Tuners

10:15 AM

L. Lu[1,2], Z. Gong[1,2], Y. Liao[1], H. Min[2], Z. Tang[2]
[1]Ratio Microelectronics, Shanghai, China; [2]Fudan University, Shanghai, China

A 975-to-1960MHz fractional-N synthesizer for digital TV tuners is implemented in 0.18µm CMOS and its loop bandwidth is maintained across the wide tuning range. A fast AFC technique is proposed to reduce the residual fractional error. A 4/4.5 prescaler is designed to lower the phase noise. The measured bandwidth variation is less than 10.3%. The integrated rms phase error (100Hz to 40MHz) is from 0.6° to 1.05°. The locking time is 20µs with 6.4µs for AFC.

23.5 A 0.4-to-1.6GHz Low-OSR ΔΣ DLL with Self-Referenced Multiphase Generation

10:45 AM

X. Yu[1], W. Rhee[1], Z. Wang[1], J-B. Lee[2], C. Kim[2]
[1]Tsinghua University, Beijing, China; [2]Samsung Electronics, Hwasung, Korea

A 0.4-to-1.6GHz ΔΣ DLL enabling wide dynamic control range is implemented in 0.18µm CMOS. By using a frequency divider and a self-referenced multiphase generator, the ΔΣ modulator can operate at much lower frequency without causing false lock or glitch problems. To compensate for the reduced OSR due to frequency division in the DLL, a hybrid FIR filtering technique suppresses out-of-band quantization noise. The DLL has sub-ps resolution and has an integrated phase noise lower than $0.4ps_{rms}$ at 1.2GHz while consuming 5.27mW from a 1.8V supply.

23.6 A Leakage-Suppression Technique for Phase-Locked Systems in 65nm CMOS

11:15 AM

C-C. Hung, S-I. Liu
National Taiwan University, Taipei, Taiwan

An 800MHz PLL that incorporates a technique to compensate for the on-chip loop filter leakage is presented. The 65nm CMOS IC has an active area of $0.065mm^2$ and consumes 3.6mW from a 1.2V supply.

23.7 A Precision Relaxation Oscillator with a Self-Clocked Offset-Cancellation Scheme for Implantable Biomedical SoCs

11:30 AM

K. Choe[1], O. D. Bernal[1], D. Nuttman[2], M. Je[1]
[1]Institute of Microelectronics, Singapore; [2]Physical Logic, Bnei Brak, Israel

A 38µW 3.2MHz relaxation oscillator for implantable biomedical SoCs uses self-clocked offset-canceling comparators. While consuming 5µW more than the design without offset cancellation, it has 4dB lower Allan variance floor. Random-walk frequency modulation is observed at a gate-time interval of 10ms as compared to 1ms in conventional oscillators. The phase-noise corner frequency is lowered from 50kHz to 20kHz, and Gaussian regime is reduced. Thus the long-term frequency stability and close-in phase fluctuations are improved.

23.8 An On-Chip CMOS Relaxation Oscillator with Power Averaging Feedback Using a Reference Proportional to Supply Voltage

11:45 AM

Y. Tokunaga, S. Sakiyama, A. Matsumoto, S. Dosho
Matsushita Electric Industrial, Osaka, Japan

A power-averaging feedback (PAF) concept is presented that overcomes conventional relaxation oscillator problems such as sensitivity to comparator delay, aging, and flicker noise of current sources. A test-chip fabricated in 0.18µm CMOS measures frequency variations of ±0.16% when supply changes from 1.7 to 1.9V and ±0.19% when temperature changes from -40 to 125°C. The prototype draws 25µA from a 1.8V supply, occupies $0.04mm^2$, and achieves 7× reduction in accumulated jitter (at 1500^{th} cycle) as compared to a oscillator without PAF.

Conclusion 12:00 PM

WIRELESS CONNECTIVITY

Session Chair: Mototsugu Hamada, Toshiba, Kawasaki, Japan
Associate Chair: Mark Ingels, IMEC, Leuven , Belgium

24.1 A 2mm² 0.1-to-5GHz SDR Receiver in 45nm Digital CMOS

8:30 AM

V. Giannini[1], P. Nuzzo[1], C. Soens[1], K. Vengattaramane[1,2], M. Steyaert[2], J. Ryckaert[1], M. Goffioul[1], B. Debaillie[1], J. van Driessche[1], J. Craninckx[1], M. Ingels[1]
[1]IMEC, Leuven, Belgium ; [2]KU Leuven, Leuven, Belgium

A direct-conversion 0.1-to-5GHz SDR RX+LO is implemented in 45nm 1.1V CMOS with 2mm² core area, using resistive-feedback LNAs, a passive mixer with enhanced out-of-band IIP3 and a 5th-order low-area 0.5-to-20MHz baseband filter. The LO signal is generated from a dual VCO 4-to-10GHz fractional-N PLL. The receiver achieves NF down to 2.3dB, out-of-band IIP3 up to -3dBm, and total power consumption from 59 to 115mW.

24.2 A 65nm CMOS Inductorless Triple-Band-Group WiMedia UWB PHY

9:00 AM

D. Leenaerts[1], R. van de Beek[1], J. Bergervoet[1], H. Kundur[1], G. van der Weide[1], A. Kapoor[1], T. Pu[2], Y. Fang[2], Y. Wang[2], B. Mukkada[2], H. Lim[2], M. Kiran[2], C. Lim[2], S. Badiu[2], A. Chang[2]
[1]NXP Semiconductors, Eindhoven, Netherlands; [2]ST-NXP Wireless, Singapore

A 3.3×3.3mm² 65nm CMOS fully integrated inductorless WiMedia v1.2 UWB PHY SoC including radio plus digital baseband covers all TFC codes, using a single RF signal path to cover band groups 1, 3 and 6. EVM for 480MB/s is -24dB, sensitivity is -81dBm for 53Mb/s and IIP3 at maximum gain setting is >-4dBm. At 480Mb/s data rate the PHY draws 383mW and 312mW in RX and TX modes respectively from a 1.2V supply.

24.3 A Reconfigurable Demodulator with 3-to-5GHz Agile Synthesizer for 9-band WiMedia UWB in 65nm CMOS

9:30 AM

A. Mazzanti[1], M. B. Vahidfar[2], M. Sosio[2], F. Svelto[2]
[1]University of Modena and Reggio Emilia, Modena, Italy
[2]University of Pavia, Pavia, Italy

A 65nm CMOS demodulator, reconfigurable between fundamental and sub-harmonic operation modes, requires a reference frequency covering less than 1/3 of the RF bandwidth. The realized chip, tailored to UWB band groups 1, 3 and 4, includes a 4-phase ring oscillator injection locked by LC PLLs, and quadrature mixers followed by transimpedance amplifiers. The synthesizer consumes 43mW.

24.4 A Highly Integrated Low-Power 2.4GHz Transceiver Using a Direct-Conversion Diversity Receiver in 0.18µm CMOS for IEEE802.15.4 WPAN

9:45 AM

G. Retz[1], H. Shanan[1], K. Mulvaney[1], S. O'Mahony[1], M. Chanca[2], P. Crowley[3], C. Billon[1], K. Khan[1], P. Quinlan[1]
[1]Analog Devices, Cork, Ireland; [2]Analog Devices, Valencia, Spain
[3]Analog Devices, Limerick, Ireland

A 0.18µm CMOS RF sensor-network transceiver based on the 802.15.4-2.4GHz WPAN standard integrates a radio controller, a direct-conversion diversity receiver and a transmitter based on direct VCO modulation. The 5.85mm² IC draws 16.8mA from 1.8V in receive mode and 18mA at 3dBm output power. The receiver achieves 9.5dB NF, -96dBm sensitivity and -18dBm IIP3, with 54dB of IR at ±5MHz offset.

Break 10:00 AM

24.5 A Fully Integrated 2×2 MIMO Dual-Band Dual-Mode Direct-Conversion CMOS Transceiver for WiMAX/WLAN Applications

10:15 AM

L. Lin, N. Wongkomet, D. Yu, C-H. Lin, M. He, B. Nissim, S. Lyuee, P. Yu, T. Sepke, S. Shekarchian, L. Tee, P. Muller, J. Tam, T. Cho
Marvell, Santa Clara, CA

A 2×2 MIMO dual-band dual-mode direct-conversion transceiver is implemented in 90nm CMOS, occupying 12.4mm^2. The RX chain has 3.5dB NF and IIP3 of -11dBm and +12dBm in high- and low-gain modes respectively. A TX EVM of -35dB is achieved at +5dBm output power, and remains below -35dB over a 60dB range of output power.

24.6 A 1.1V 5-to-6GHz Reduced-Component Direct-Conversion Transmit Signal Path in 45nm CMOS

10:45 AM

J. C. Rudell[1,2], P. Goyal[1], C. D. Hull[1], S. Ravid[3], A. Kidwai[1]
[1]Intel, Hillsboro, OR; [2]University of Washington, Seattle, WA; [3]Intel, Haifa, Israel

A 5-to-6GHz 1.1V highly linear 45nm CMOS transmit signal path has P_{sat} of 14.9dBm, P_{1dB} of 12.2dBm and consumes 108mA. The TX realizes a combined filter pole, VGA and linear mixer transconductor using a single opamp. EVM of -37dB at 9.2dB backoff from P_{1dB}, and TX noise of -143dBm/Hz and -146dBm/Hz at 100MHz and 300MHz offset from the carrier, respectively, enable use in multistandard co-existing radios.

24.7 A 2.4GHz 2Mb/s Versatile PLL-Based Transmitter Using Digital Pre-Emphasis and Auto Calibration in 0.18µm CMOS for WPAN

11:15 AM

H. Shanan, G. Retz, K. Mulvaney, P. Quinlan
Analog Devices, Cork, Ireland

As part of a 2.4GHz WPAN RF SoC in 0.18µm CMOS, a 2Mb/s transmitter at 2.4835GHz based on a $\Delta\Sigma$ fractional-N PLL and digital pre-emphasis filter consumes 18mA from a 1.8V supply at 3dBm output power. The circuit maintains a worst-case rms phase error of 8.4° for GMSK signals and an rms EVM of 2% for IEEE802.15.4-compliant signals over a ±50% variation in the PLL BW.

24.8 A 7.2mW Quadrature GPS Receiver in 0.13µm CMOS

11:30 AM

K-W. Cheng, K. Natarajan, D. J. Allstot
University of Washington, Seattle, WA

The integrated RF front-end of a low-IF GPS receiver uses a gate-modulated quadrature VCO and a stacked quadrature-LNA-mixer-VCO cell that provides 42.5dB gain with 1mW power consumption. A continuous-time $\Delta\Sigma$ ADC achieves 65dB DR and dissipates 5mW using polyphase filters, resistor DACs and continuous-time comparators. The NF is 6.5dB and total power dissipation is 7.2mW.

24.9 A 10.8mW Body-Channel-Communication/MICS Dual-Band Transceiver for a Unified Body-Sensor-Network Controller

11:45 AM

N. Cho, J. Bae, H-J. Yoo
KAIST, Daejeon, Korea

A 10.8mW 0.18µm CMOS transceiver supporting 30-to-70MHz body-channel communication and 402-to-405MHz medical-implant communication achieves -65dBm/35μV_{rms} sensitivity and -32/-25dBm P_{1dB}. The LNA provides constant 23dB gain in the dual bands and attenuates out-of-band interferers by >10dB. The front-end reduces the energy consumption of the transceiver by 30%.

Conclusion **12:15 PM**

MEDICAL

Session Chair: Albrecht Rothermel, University of Ulm, Ulm, Germany
Associate Chair: Timothy Denison, Medtronic, Minneapolis, MN

25.1 A Wireless and Batteryless 130mg 300µW 10b Implantable Blood-Pressure-Sensing Microsystem for Real-Time Genetically Engineered Mice Monitoring

1:30 PM

P. Cong, N. Chaimanonart, W. H. Ko, D. J. Young
Case Western Reserve University, Cleveland, OH

A wireless and batteryless minimally invasive implantable blood-pressure-sensing microsystem for real-time monitoring of genetically engineered mice is presented. The sensor features automatic offset cancelation, wireless data telemetry, and adaptive RF powering capability. Evaluation of the microsystem implanted inside an untethered laboratory mouse demonstrates a blood-pressure-sensing resolution of 1mmHg with 60dB dynamic range.

25.2 A Wireless IC for Time-Share Chemical and Electrical Neural Recording

2:00 PM

M. Roham[1], P. A. Garris[2], P. Mohseni[1]
[1]Case Western Reserve University, Cleveland, OH
[2]Illinois State University, Normal, IL

A 1.1mW 4-channel IC is presented that wirelessly monitors brain dopamine release and its postsynaptic bioelectrical response at the same recording site. The 5mm^2 IC is fabricated in a 0.5µm 2P3M CMOS process and uses a configurable 3rd-order CT-$\Delta\Sigma$M that yields *in vivo* measurement results of 3.5µV_{rms} input-referred noise in 4kHz BW, and 79pA in 5kHz BW for electrical and fast-scan voltammetric chemical neurosensing, respectively.

25.3 A Flexible Clockless 32-Channel Simultaneous Wireless Neural Recording System with Adjustable Resolution

2:30 PM

M. Yin[1], M. Ghovanloo[2]
[1]North Carolina State University, Raleigh, NC
[2]Georgia Institute of Technology, Atlanta, GA

A clockless 32-channel simultaneous wireless implantable neural recording SoC is described, in which a flexible PWM-TDM-based architecture provides a tradeoff between BW, resolution, DR, and number of active channels. The 0.5µm CMOS SoC includes 4 additional signals for supply, reference, and temperature monitoring. Signals are sampled at 640kS/s and the SoC consumes 5.6mW.

Break 3:00 PM

25.4 A Biomedical Multiprocessor SoC for Closed-Loop Neuroprosthetic Applications

3:15 PM

T-C. Chen[1,2], K. Chen[2], W. Liu[2], L-G. Chen[1]
[1]National Taiwan Univeristy, Taipei, Taiwan
[2]University of California, Santa Cruz, CA

A biomedical multiprocessor SoC that processes and translates multichannel neural signals into stimulation currents in real time is implemented on a software-programmable and hardware-accelerated platform for implantable closed-loop neuroprostheses. The 28.3mm^2 chip in 0.35µm CMOS consumes 4.1, 3.5 and 2.9mW for 16-channel spike sorting, epilepsy implant and eye-blink reanimation, respectively.

25.5 A CMOS Fluorescent-Based Biosensor Microarray

3:45 PM

B. Jang, P. Cao, A. Chevalier, A. Ellington, A. Hassibi
University of Texas, Austin, TX

A fully integrated 7×8 fluorescent-based biosensor array for DNA detection is reported. The 0.35µm CMOS readout circuitry includes an in-pixel capacitive TIA and ADC. The emission thin-film fluorescent long-pass filter and capturing probe layer are fabricated on top of the chip. A detection DR exceeding 5 orders of magnitude is achieved with a minimum sensitivity of <10 DNA fluorophores/µm^2.

25.6 A Frequency-Shift CMOS Magnetic Biosensor Array with Single-Bead Sensitivity and No External Magnet

4:15 PM

H. Wang, Y. Chen, A. Scherer, A. Hajimiri
California Institute of Technology, Pasadena, CA

An ultra-sensitive frequency-shift-based magnetic particle sensor array is integrated in 0.13µm CMOS with no need for external permanent or electro-magnets. With a frequency resolution under 0.2ppm, the sensor successfully detects both a single magnetic bead (D=2.4µm) and 1nanomolar magnetic-nanoparticle-labeled DNA samples.

Conclusion **4:45 PM**

SWITCHED-MODE TECHNIQUES

Session Chair: Francesco Rezzi, Marvell Semiconductor, Pavia, Italy
Associate Chair: Philip K.T. Mok, Hong Kong University of Science and Technology, Hong Kong, China

26.1 Multiple-Output Step-Up/Down Switching DC-DC Converter with Vestigial Current Control

1:30 PM

K-S. Seol[1], Y-J. Woo[1], G-H. Cho[1], G-H. Cho[2], J-W. Lee[2], S-I. Kim[3]
[1]KAIST, Daejeon, Korea
[2]JDA Technology, Daejeon, Korea
[3]LG Electronics, Kyunggi, Korea

A single-chip multiple-output DC-DC converter that uses vestigial-current-control method is implemented in 0.5µm BiCMOS occupying 3.6mm^2. It consists of 3 step-up/down outputs, 2 step-up outputs, and 1 auxiliary output, and operates stably under wide load variation with simple control loop compensation. The measured efficiency is higher than 83% while delivering load power of 1.5W.

26.2 Single-Inductor Dual-Input Dual-Output Buck-Boost Fuel-Cell-Li-Ion Charging DC-DC Converter Supply

2:00 PM

S. Kim, G. A. Rincon-Mora
Georgia Institute of Technology, Atlanta, GA

A micro fuel cell energizes a wireless microsensor for extended operation time while a Li-ion microscale battery provides peak transmission power. A 1V±25mV 2MHz single-inductor fuel-cell-Li-ion charger-supply CMOS IC capable of supplying 1mA and adjusting to 0.1-to-1mA load dumps within 30µs (with output regulation of ±50mV during mode transitions) is presented.

26.3 Digitally Assisted Quasi-V^2 Hysteretic Buck Converter with Fixed Frequency and without Using Large-ESR Capacitor

2:30 PM

F. Su, W-H. Ki
Hong Kong University of Science and Technology, Hong Kong, China

A quasi-V^2 hysteretic buck converter in 0.35µm CMOS senses the inductor current ripple through an on-chip RC filter across the inductor, relaxing the need for an output capacitor with large ESR. A digital adaptive delay compensator is used to fix the switching frequency at 3MHz, with 3.3% variation across the overall operating range. The output capacitor is 4.4µF with ESR below 30mΩ. At V_o=0.9V, the load transient recovery time is 2.4µs for a 50 to 500mA step, and is 2.8µs for a 500 to 50mA step. The overshoot and undershoot voltages are 38mV and 45mV, respectively.

Break 3:00 PM

26.4 A 20W/channel Class-D Amplifier with Significantly Reduced Common-Mode Radiated Emissions

3:15 PM

P. Siniscalchi, R. Hester
Texas Instruments, Dallas, TX

A Class-D audio amplifier that uses a modified power stage enabling 3 level PWM with a single power supply is presented. Common-mode EMI is eliminated making filter-less operation possible. The device is fabricated in a high-voltage 0.25µm BCD process and delivers up to 20W/channel and passes the FCC Class-B standard for radiated emissions. THD+N is 0.2% at 5W. Efficiency is 90% at 10W.

26.5 Two Class-D Audio Amplifiers with 89/90% Efficiency and 0.02/0.03% THD+N Consuming Less than 1mW of Quiescent Power

3:45 PM

M. Rojas-Gonzalez, E. Sánchez-Sinencio
Texas A&M University, College Station, TX

Two Class-D audio amplifiers with linearity, efficiency, and PSRR performance comparable to recently published works but consuming less than 10× quiescent power are presented. Both designs, fabricated in 0.5µm CMOS with a 2.7V single supply, are based on a hysteretic nonlinear controller that avoids the complex task of generating a highly linear triangle carrier signal.

26.6 A 460W Class-D Output Stage with Adaptive Gate Drive

4:15 PM

M. Berkhout
NXP Semiconductors, Nijmegen, Netherlands

A Class-D output stage operating from an 85V supply is realized in an SOI-based BCD process. The output stage uses an adaptive gate driver that adjusts the speed of charging and discharging of the gates of the power MOSFETs depending on their terminal voltages. Measurements show smooth transitions at high output currents and output power is 460W at 10% THD.

Conclusion **4:45 PM**

SRAM AND EMERGING MEMORY

Session Chair: Peter Rickert, Texas Instruments, Richardson, TX
Associate Chair: Hideaki Kurata, Hitachi, Kokubunji, Japan

27.1 A 4.0GHz 291Mb Voltage-Scalable SRAM in 32nm High-κ Metal-Gate CMOS with Integrated Power Management

1:30 PM

Y. Wang, U. Bhattacharya, F. Hamzaoglu, P. Kolar, Y. Ng, L. Wei, Y. Zhang, K. Zhang, M. Bohr
Intel, Hillsboro, OR

A voltage-scalable 291Mb SRAM in 32nm high-κ metal-gate logic CMOS features a 0.171μm^2 6T cell. The 128kb SRAM subarray consumes 5mW leakage power at 1V. The SRAM operates at 4GHz at 1.0V and 2GHz at 0.8V. Integrated power management featuring close-loop array-leakage control, floating-bitline and wordline-driver sleep, enables 58% reduction in leakage power.

27.2 A Process-Variation-Tolerant Dual-Power-Supply SRAM with 0.179μm^2 Cell in 40nm CMOS Using Level-Programmable Wordline Driver

2:00 PM

O. Hirabayashi, A. Kawasumi, A. Suzuki, Y. Takeyama, K. Kushida, T. Sasaki, A. Katayama, G. Fukano, Y. Fujimura, T. Nakazato, Y. Shizuki, N. Kushiyama, T. Yabe
Toshiba Semiconductor, Kawasaki, Japan

A dual-power-supply 40nm CMOS SRAM with 0.179μm^2 cell is 10% smaller than the SRAM scaling trend. To improve the cell stability, the design uses a level-programmable wordline driver and dynamic array-supply control. The cell failure rate is reduced by more than three orders of magnitude.

27.3 A 2ns-Read-Latency 4Mb Embedded Floating Body Memory Macro in 45nm SOI Technology

2:30 PM

A. P. Singh[1], M. K. Ciraula[2], D. R. Weiss[2], J. J. Wuu[2], P. Bauser[1], P. de Champs[1], H. Daghighian[1], D. Fisch[1], P. Graber[1], M. Bron[1]
[1]Innovative Silicon, Lausanne, Switzerland
[2]AMD, Fort Collins, CO

An embedded memory macro is developed for high-performance microprocessors, using a single-transistor floating-body cell. Eight 4Mb macros are incorporated on a test-chip fabricated in a 45nm SOI logic process. Silicon measurements confirm 2ns read latency with a memory-macro operating window of 0.5V.

Break 3:00 PM

27.4 A 90nm 12ns 32Mb 2T1MTJ MRAM

3:15 PM

R. Nebashi[1], N. Sakimura[1], H. Honjo[1], S. Saito[1], Y. Ito[2], S. Miura[1], Y. Kato[1], K. Mori[1], Y. Ozaki[2], Y. Kobayashi[2], N. Ohshima[1], K. Kinoshita[1], T. Suzuki[1], K. Nagahara[1], N. Ishiwata[1], K. Suemitsu[1], S. Fukami[1], H. Hada[1], T. Sugibayashi[1], N. Kasai[1]
[1]NEC, Sagamihara, Japan
[2]NEC Electronics, Sagamihara, Japan

A 32Mb MRAM with a 2 transistors and 1 magnetic tunnel junction (2T1MTJ) cell attains a 12ns access time. The 91mm^2 die is fabricated in 90nm CMOS. A 63% area efficiency is obtained using a spontaneous write-current assistant. The memory cell area is reduced by half using the boosted wordline technique.

27.5 A 1.6GB/s DDR2 128Mb Chain FeRAM with Scalable Octal Bitline and Sensing Schemes

3:45 PM

H. Shiga, D. Takashima, S. Shiratake, K. Hoya, T. Miyakawa, R. Ogiwara, R. Fukuda, R. Takizawa, K. Hatsuda, F. Matsuoka, Y. Nagadomi, D. Hashimoto, H. Nishimura, T. Hioka, S. M. Doumae, S. Shimizu, M. Kawano, T. Taguchi, Y. Watanabe, S. Fujii, T. Ozaki, H. Kanaya, Y. Kumura, Y. Shimojo, Y. Yamada, Y. Minami, S. Shuto, K. Yamakawa, S. Yamazaki, I. Kunishima, T. Hamamoto, A. Nitayama, T. Furuyama
Toshiba Semiconductor, Yokohama, Japan

A 1.6GB/s nonvolatile 128Mb chain FeRAM in 0.13µm CMOS is demonstrated. The 87.7mm^2 die uses 0.252µm^2 cell with a cell sensing signal of 200mV, an octal bitline architecture, low-parasitic-capacitance sensing, and dual-metal platelines. Power-supply bounce due to the 400MHz clock is suppressed to 50mV by event-driven current suppliers.

Conclusion 4:15 PM

TD: DIRECTIONS IN COMPUTING AND SIGNALING

Session Chair: Ali Keshavarzi, TSMC, San Jose, CA
Associate Chair: Satoshi Shigematsu, NTT, Atsugi, Japan

28.1 Optical I/O Technology in Tera-Scale Computing

1:30 PM

I. Young, E. Mohammed, J. Liao, A. Kern, S. Palermo, B. Block, M. Reshotko, P. Chang
Intel, Hillsboro, OR

An optical I/O architecture with 90nm CMOS circuits, 1×12 VCSEL/detector arrays and polymer waveguides achieves packaged 10Gb/s/channel at 11pJ/b, while a pre-emphasis TX enables potential 18Gb/s at 9.6pJ/b link efficiency. Increased optical CMOS I/O integration with ring resonator modulators and Ge detectors projects to near 1pJ/b with current 20Gb/s performance.

28.2 Wireless DC Voltage Transmission Using Inductive-Coupling Channel for Highly-Parallel Wafer-Level Testing

2:00 PM

Y. Yoshida[1], K. Nose[2], Y. Nakagawa[2], K. Noguchi[2], Y. Morita[2], M. Tago[2], T. Kuroda[1], M. Mizuno[2]
[1]Keio University, Kanagawa, Japan
[2]NEC, Sagamihara, Japan

An inductive-coupling DC-voltage transceiver realizes a low-cost, highly-parallel screening test on wafer. It can output a DC voltage with 6b resolution without any area-consuming digital or synchronization circuits, and corrects the output voltage error without needing calibration circuits on the die-under-test. All the circuits for DC tests are implemented into the area of a 100×100μm^2 inductor.

28.3 A Stretchable EMI Measurement Sheet with 8×8 Coil Array, 2V Organic CMOS Decoder, and -70dBm EMI Detection Circuits in 0.18μm CMOS

2:30 PM

K. Ishida[1], N. Masunaga[1], Z. Zhou[1], T. Yasufuku[1], T. Sekitani[1], U. Zschieschang[2], H. Klauk[2], M. Takamiya[1], T. Someya[1], T. Sakurai[1]
[1]University of Tokyo, Tokyo, Japan
[2]Max Planck Institute for Solid State Research, Stuttgart, Germany

A stretchable 12×12cm^2 EMI measurement sheet is developed to enable the measurement of the EMI distribution on the surface of the electronic devices by wrapping the devices in the sheet. The sheet includes 8×8 coil array, 2V organic CMOS decoder, 40% stretchable interconnects with carbon nanotubes, and -70dBm EMI detection circuits in 0.18μm CMOS.

Break 3:00 PM

28.4 Field-Coupled Nanomagnets for Interconnect-Free Nonvolatile Computing

3:15 PM

M. Becherer[1], G. Csaba[1], R. Emling[1], W. Porod[2], P. Lugli[1], D. Schmitt-Landsiedel[1]
[1]Technical University Munich, Munich, Germany
[2]University of Notre Dame, South Bend, IN

This paper presents the potential of programmable ferromagnetic computing devices composed of thin focused ion beam patterned Co/Pt films with 2.2×10^9 devices/cm^2 and nonvolatile behavior. They offer rad-hard and parallel information processing at 300K and can be accessed by electrical input and output. These logic devices offer ~$5x10^{-18}$J energy per switching event and overcome the shortcomings of electrical wiring by a contactless clocking scheme.

28.5 Chip-Scale Camera Module (CSCM) Using Through-Silicon-Via (TSV)

3:45 PM

H. Yoshikawa, A. Kawasaki, T. Iizuka, Y. Nishimura, K. Tanida, K. Akiyama, M. Sekiguchi, M. Matsuo, S. Fukuchi, K. Takahashi
Toshiba Semiconductor, Yokohama, Japan

TSV technology is applied to a CMOS image sensor module and a size reduction of 55% in volume and 36% in footprint is achieved. Optimization of TSV parasitic circuits achieves electrical performance comparable with the conventional product that uses bonding wires. The saving of passive components and their related assembly allows a cost reduction of 25% when employing TSV technology.

28.6 A Subjective-Contour Generation LSI System with Expandable Pixel-Parallel Architecture for Vision Systems

4:15 PM

T. Morie, Y. Kim
Kyushu Institute of Technology, Kitakyushu, Japan

A 0.25µm CMOS LSI containing 35×35pixel units executes a directional (anisotropic) diffusion algorithm that consists of a simple cellular-neural-network-based updating rule, and generates analog ridge-like diffusion states by propagating the internal state of pixel units in the given direction. Experimental results are shown for subjective contour generation.

28.7 An Inductive-Coupling Link for 3D Integration of a 90nm CMOS Processor and a 65nm CMOS SRAM

4:45 PM

K. Niitsu[1], Y. Shimazaki[1,2], Y. Sugimori[1], Y. Kohama[1], K. Kasuga[1], I. Nonomura[2], M. Saen[3], S. Komatsu[3], K. Osada[3], N. Irie[3], T. Hattori[2], A. Hasegawa[2], T. Kuroda[1]
[1]Keio University, Yokohama, Japan
[2]Renesas Technology, Tokyo, Japan
[3]Hitachi, Tokyo, Japan

A 90nm CMOS 8-core processor is mounted face down on a package by C4 bump and a 65nm CMOS 1MB SRAM is glued on it face up. The two chips operating with different supply voltages are AC-coupled by inductive coupling that provides 19.2Gb/s data link. Measured power and area efficiency of the link is 1pJ/b and 0.15mm^2/Gb/s, which is 1/30 and 1/3 in comparison with the DDR2 interface, respectively.

Conclusion **5:00 PM**

mm-WAVE CIRCUITS

Session Chair: Francesco Svelto, University of Pavia, Pavia, Italy
Associate Chair: Pietro Andreani, Lund University, Lund, Sweden

29.1 A 1.1V 150GHz Amplifier with 8dB Gain and +6dBm Saturated Output Power in Standard Digital 65nm CMOS Using Dummy-Prefilled Microstrip Lines

1:30 PM

M. Seo[1], B. Jagannathan[2], C. Carta[1], J. J. Pekarik[3], L. Chen[1], P. Yue[1], M. Rodwell[1]
[1]University of California, Santa Barbara, CA
[2]IBM, Burlington, VT
[3]IBM, Crolles, France

A 150GHz 3-stage amplifier in digital 65nm CMOS occupies 0.41mm^2. Transistor layout is optimized to yield 4.8dB of maximum stable gain at 150GHz. Dummy-prefilled microstrip lines are used. Shunt-stub tuning and radial stubs reduce matching loss. Measurement shows 8.3dB gain, 6.3dBm P_{sat}, 1.5dBm P_{1dB} and 27GHz 3dB BW while consuming 25.5mW at 1.1V.

29.2 W-Band CMOS Amplifiers Achieving +10dBm Saturated Output Power and 7.5dB NF

2:00 PM

D. Sandström, M. Varonen, M. Kärkkäinen, K. A. Halonen
Helsinki University of Technology, Espoo, Finland

Two W-band amplifiers are implemented in 65nm CMOS. The slow-wave CPW-based amplifier achieves +10dBm output power, 7.5dB NF,and 13dB gain at 100GHz with a 72mA current consumption at 1.2V. Chip size of the implemented slow-wave amplifier is 0.33mm^2. Substrate shielding of the passives improves performance when compared to the other amplifier which uses unshielded passives.

29.3 A 26dB-Gain 100GHz Si/SiGe Cascaded Constructive-Wave Amplifier

2:30 PM

J. F. Buckwalter, J. Kim
University of California, San Diego, CA

A 0.12µm SiGe BiCMOS 82mW wideband mm-wave amplifier topology, based on cascaded traveling-wave stages constructively add forward traveling waves while canceling backward traveling waves. It achieves 26dB gain at 99GHz with a 14GHz 3dB bandwidth, for overall 290GHz GBW. The input and output return losses are greater than 15dB and 12dB, respectively. The output-referred P_{1dB} is -0.1dBm.

Break 3:00 PM

29.4 A Dual-Mode Architecture for a Phased-Array Receiver Based on Injection Locking in 0.13µm CMOS

3:15 PM

S. Patnaik, N. Lanka, R. Harjani
University of Minnesota, Minneapolis, MN

A dual-mode architecture for phased-array receivers based on injection locking is reported. A four-channel prototype in 0.13µm CMOS occupies 1.44mm^2 of active area, operates at 2.4GHz and draws 42mW from a 1.55V supply. Each oscillator injection-locks to a common signal to generate the required phase.

29.5 A Digitally Controlled Compact 57-to-66GHz Front-End in 45nm Digital CMOS

3:45 PM

J. Borremans[1], J. Raczkowski[1,2], P. Wambacq[1,3]
[1]IMEC, Leuven, Belgium
[2]KU Leuven, Leuven, Belgium
[3]Vrije Universiteit Brussel, Brussels, Belgium

A 57-to-66GHz direct-downconversion front-end in 45nm digital CMOS achieves a minimum NF of 6dB and 26dB gain, consuming 19mA from a 1.1V supply. Low flicker noise, a large-area bondpad with optional ESD protection, chip area of 0.023mm^2, and all-digital control make this frontend practical for phased-array systems.

29.6 A 57-to-66GHz Quadrature PLL in 45nm Digital CMOS

4:15 PM

K. Scheir[1,2], G. Vandersteen[2], Y. Rolain[2], P. Wambacq[1,2]
[1]IMEC, Heverlee, Belgium
[2]Vrije Universiteit Brussel, Brussels, Belgium

A 57-to-66GHz quadrature PLL in low-power 45nm digital CMOS achieves a large tuning range with 2 QVCOs and a tunable injection-locked prescaler. The circuit has quadrature outputs, consumes 78mW from a 1.1V supply, achieves a phase noise of -82dBc/Hz at 3MHz offset around 61.6GHz, and has a reference spur level of -42dBc.

29.7 A 59GHz Push-Push VCO with 13.9GHz Tuning Range Using Loop-Ground Transmission Line for a Full-Band 60GHz Transceiver

4:45 PM

T. Nakamura, T. Masuda, K. Washio, H. Kondoh
Hitachi, Kokubunji, Japan

A 59GHz push-push VCO for a full-band 60GHz transceiver in 0.18µm SiGe BiCMOS achieves 13.9GHz tuning range, 1.2dBm output power, and phase noise of -108dBc/Hz at 1MHz offset. A second-harmonic output technique, using a loop-ground transmission line, contributes to achieving the wide tuning range. The VCO achieves an FOM_T of -189.6dB when tuning range is included.

Conclusion **5:00 PM**

Low-Voltage Analog and Mixed-Signal CMOS Circuit Design

Organizer: **Ian Galton**, *University of California, San Diego, CA*

Instructors: **Lucien Breems**, *NXP Semiconductors, Eindhoven, Netherlands*
Klaas Bult, *Broadcom, Bunnik, Netherlands*
Behzad Razavi, *University of California, Los Angeles, CA*
Willy Sansen, *KU Leuven, Leuven, Belgium*

OVERVIEW:

The relentless scaling of supply voltage that has accompanied advances in CMOS technology has been great for digital circuits but has made high-performance analog and mixed-signal circuits increasingly challenging to design. Nevertheless, market pressures continue to dictate high levels of integration in mass-market communication and entertainment devices to minimize product cost and size. Increasingly, this necessitates the inclusion of low-noise amplifiers, mixers, filters, and data converters, along with large amounts of digital circuitry in highly-scaled CMOS technology at analog supply voltages of 1.2V or less. Unfortunately, traditional topologies for these analog blocks are not compatible with such low supply voltages, so innovative new techniques for low-voltage analog and mixed-signal CMOS design are required. This short course provides a detailed view of the problems associated with low-voltage analog and mixed-signal design and describes techniques for overcoming these problems. It is intended for both entry-level and experienced analog and mixed-signal circuit designers.

To Register, please use the ISSCC 2009 Registration Form on the Advance Program Centerfold. **Sign-in** is at the San Francisco Marriott Hotel, Level B-2, beginning at 7:00AM on Thursday, February 12, 2009.

The Short Course will be offered twice on Thursday, February 12: The first offering is scheduled for **8:00AM to 4:30PM**. The second offering is scheduled for **10:00AM to 6:30PM**.

DVD of the Short Course & Selected Referenced Papers: A DVD of the Short-Course may be purchased at registration time, or at the on-site registration desk. A substantial price reduction is offered to those who attend the course. The DVD will be mailed approximately four months after the end of the conference. The DVD will include: (1) The visuals of the four Short-Course presentations in PDF format; (2) Audio recordings of the presentations along with written transcriptions; (3) Bibliographies of background papers for all four presentations; and (4) PDF copies of selected relevant background material and important papers in the field (10 to 20 papers per presentation).

OUTLINE:

Low-Power Low-Voltage Opamp Design

This presentation explores the limits in terms of speed, noise and power consumption for opamps at the lowest supply voltages. Operational amplifiers require compensation capacitances if two or more stages are used. As a result, the power consumption is increased. A design plan is developed to optimize the power reduction of two- and three-stage Miller operational amplifiers. The maximum gain-bandwidth product of such amplifiers in future nanometer CMOS technologies can then easily be estimated. Other important specifications are discussed as well, such as the noise performance, the common-mode input range, the output impedance, the slew-rate, etc. Then the symmetrical amplifier, the folded-cascode amplifier and the Miller OTA amplifier are compared in terms of speed, power consumption and noise. Finally, a large number of opamp configurations are discussed with special attention to those operating at supply voltages below 1V, down to even 0.5V. They are all fully differential and thus require common-mode feedback, the power consumption of which must be minimized as well.

Instructor: Willy Sansen received the PhD degree in Electronics from the University of California, Berkeley in 1972. He has been a full professor at the KU Leuven since 1980. Since 1984 he has headed the ESAT-MICAS laboratory on analog design, which includes about sixty members and which is mainly active in research projects with industry. He is a fellow of the IEEE. Prof. Sansen is a member of several editorial and program committees of journals and conferences. He is co-founder and organizer of the workshops on Advances in Analog Circuit Design (AACD) in Europe. He is a member of the executive and program committees of the IEEE ISSCC conference. He was program chair of the ISSCC-2002 conference. He is president of the IEEE Solid-State Circuits Society from January 2008 on. He has been involved in design automation and in numerous analog integrated circuit designs for telecommunications, consumer electronics, medical applications and sensors. He has been supervisor of sixty-five PhD theses in these fields. He has authored and coauthored more than 660 papers in international journals and conference proceedings and fifteen books the most recent being "Analog Design Essentials" (Springer 2006).

Low-Voltage Sigma-Delta A/D Converters

The demand for higher resolution and larger bandwidth Sigma-Delta ($\Delta\Sigma$) A/D converters is being driven by applications such as modern multi-standard communications receivers, high-precision audio, and future software-defined and multi-channel radios. New technology nodes, although offering speed advantages, have lower supply voltages and degraded transistor characteristics. This makes the design of low-voltage high-resolution $\Delta\Sigma$ A/D converters very challenging. Lucien Breems will present an overview of the $\Delta\Sigma$ playground including continuous-time and switched-capacitor $\Delta\Sigma$ converters and show architectural and circuit innovations for high-resolution and large-bandwidth $\Delta\Sigma$ ADC designs in low-voltage nanometer technologies.

Instructor: Lucien Breems received his MSc and PhD degrees in Electrical Engineering from the Delft University of Technology, Netherlands, in 1996 and 2001, respectively. In 2000, he joined the Mixed-Signal Circuits and Systems Department of Philips Research, Eindhoven, Netherlands. Since 2007, he has been with NXP Semiconductors where he leads a research group working on Sigma-Delta A/D converters. He is the author of the book "Continuous-Time Sigma-Delta Modulation for A/D Conversion in Radio Receivers" (Boston, MA: Kluwer, 2001) and his research interests include Sigma-Delta modulators and mixed-signal circuit design.

The Effect of Technology Scaling on Power Dissipation in Analog CMOS Circuits

It is often stated that technology scaling is unfavorably affecting analog CMOS circuits. Reality however is not that simple and straightforward. Taking power dissipation as the most dominating aspect of circuit design, a general approach for estimating power dissipation in analog CMOS circuits as a function of technology scaling is introduced. It is shown that while technology has progressed from multiple-micrometer to sub-100nm dimensions, matching-dominated circuits were able to achieve a reduction in power dissipation whereas noise-dominated circuits saw an increase. A literature review, ranging over more than a decade, in technology as well as publication dates confirms these conclusions. These findings are applied to ADC architectures, like flash and pipeline ADCs, and it is shown why pipeline ADCs benefit from high, thick-oxide supply voltages whereas flash ADCs benefit from the technology's thinner oxides. Various circuit techniques, published in the literature, are discussed that help to combat the specific challenges posed by the scaling of the technology. Specific threats in current and future technologies are also discussed.

Instructor: Klaas Bult received the MS and PhD degrees in Electrical Engineering, Twente University, Enschede, Netherlands. From 1988 to 1994 he was with Philips Research Laboratories, Eindhoven, Netherlands. From 1994 to 1996 he was an Associate Professor at UCLA, teaching and researching RF CMOS circuits and data converters. Since 1996 he has been with Broadcom Corporation where he started the Broadcom Analog and RF Microelectronics group in Irvine, CA, responsible for the analog part of all mixed-signal chips for application in digital communication systems. In 1999, he started the Broadcom Design Center in Bunnik, Netherlands. Klaas Bult was the recipient of the Lewis Winner Award for outstanding conference paper of ISSCC in 1990, 1992 and 1997 and a co-recipient of the Jan van Vessem Award for Best European Paper in 2004 from the same conference.

Sub-1V RF Design: Challenges and Techniques

The design of RF circuits, in technology nodes beyond 90nm, faces critical issues arising from both the nonidealities of the transistors and the reduction of the supply voltage. This presentation describes the low-voltage behavior of various RF building blocks and introduces techniques that better lend themselves to low-voltage operation. Examples include low-noise amplifiers, mixers, voltage-controlled oscillators, and power amplifiers. Noise-gain-linearity and phase-noise-headroom trade-offs are formulated and various topology candidates for relaxing these trade-offs are studied.

Instructor: Behzad Razavi received his PhD from Stanford University in 1992. He is Professor of Electrical Engineering at UCLA, where he conducts research on wireless transceivers, phase-locking phenomena, broadband data communications, and data converters. He has received awards at ISSCC, CICC, and ESSCIRC and published seven books. He is an IEEE Fellow, an IEEE Distinguished Lecturer and was recognized as one of the top ten authors in the 50-year history of ISSCC.

F5: ATAC: High-Speed Interfaces

Organizer: **John Stonick**, *Synopsys, Hillsboro, OR*

Committee: **Yuriy Greshishchev**, *Nortel, Ottawa, Canada*
Yusuke Ohtomo, *NTT, Atsugi, Kanagawa, Japan*
Doug Smith, *SMSC, Austin, TX*

The goal of this forum is to provide circuit designers with an opportunity to learn from leading experts about the design issues and system-level challenges that arise in the development of transceivers for a wide cross-section of application areas and associated standards. The transceivers for these different standards share some similarities but also marked differences. The audience will have an opportunity to not only learn about these similarities and differences but also develop an understanding as to why they exist how they arose. Additionally, the audience will be able garner insight into where these standards are heading and what challenges lie ahead in the future.

The first speaker, Gerry Talbot (AMD), will cover PCI-Express (PCIE), electrical signaling. He will provide an overview of PCIE including its evolution from 2.5 to 8Gb/s, covering key specification aspects and will describe the enabling technologies for this standard to work. The second speaker, Mike Pennell (SMSC), will provide a physical layer perspective for the latest universal serial bus (USB) interface, USB 3.0. He will focus on physical layer characteristics and challenges including power management, clocking, cable and connector, signaling, transmit and receive equalization, and compliance testing. The third speaker, Robert Elliott (HP), will cover transceivers for the serial attached SCSI (SAS) standard starting with the physical layer established in SAS-1 and then moving on to the physical layer of SAS-2 which includes a doubling of the physical link rate to 6Gb/s while supporting lossier, more challenging interconnects. The fourth speaker, Jon Rogers (Gennum), will address the transceiver challenges presented by the high-definition multimedia interface (HDMI) standard and the related Society of Motion Picture and Television Engineers (SMPTE) video transmission standard. The fifth speaker, George Zimmerman (Solarflare), will present insights into transceiver design for the IEEE 10GBASE-T standard. His talk will focus on design considerations to minimize power and maximize the utility of a single-chip 10GBASE-T solution. The sixth speaker, Ali Ghiasi (Broadcom), will discuss the evolution of IO technology for 10 gigabit ethernet (GbE) to the small form pluggable (SFP+) form factor which utilizes serializer/deserializer framer interface (SFI) for its electrical interface and leverages electronic dispersion compensation to compensate for both electrical as well as optical dispersions. Additionally he will discuss trends for higher speeds, 40GbE, 100GbE, as well as 17Gb/s fibre channel.

Finally, the forum will conclude with a panel discussion in which these experts can voice their opinions on cutting-edge design issues and the standards future that lies ahead.

Forum Agenda:

Time	Topic
8:00	Breakfast
8:45	**Introduction** **John Stonick**, *Synopsys, Hillsboro, OR*
9:00	**PCI Express Electrical Signaling** **Gerry Talbot**, *AMD, Boxborough, MA*
10:00	**Implementation of USB 3.0 technology—A Physical Layer Perspective** **Mike Pennell**, *SMSC, Phoenix, AZ*
11:00	Break
11:15	**Serial Attached SCSI (SAS)—6Gb/s and Beyond** **Robert Elliott**, *Hewlett Packard, Houston, TX*
12:15	Lunch
1:15	**Multimedia Connectivity: Transceiver Challenges in the Home and the Broadcast Studio** **Jon Rogers**, *Gennum, Toronto, Canada*
2:15	**Complexity, Utility and Energy Efficiency for Copper Ethernet at 10Gb/s and Beyond** **George Zimmerman**, *Solarflare Communications, Irvine, CA*
3:15	Break
3:30	**Optical and Electrical Tradeoffs for SFP+ Module/Host and Trends in Higher Speed Fibre Channel/Ethernet** **Ali Ghiasi**, *Broadcom, San Jose, CA*
4:30	Panel Discussion
5:00	Conclusion

F6: Multi-Domain Processors

Organizer: **Stefan Rusu,** *Intel, Santa Clara, CA*

Committee: **Sam Naffziger,** *AMD, Fort Collins, CO*
Lew Chua-Eoan, *Qualcomm, San Diego, CA*
Sonia Leon, *Sun Microsystems, Santa Clara, CA*
Suhwan Kim, *Seoul National University, Seoul, Korea*

Multiple clock and power domains are widely used to manage power in modern nanoscale designs. This Forum presents the latest design techniques in multiple-domain clock and power management for high-performance processors, as well as low-power systems-on-chip (SoC). Topics include clock and data synchronization, power gating, floorplan and layout implications, clock and power grids, test requirements, and modular design techniques. Practical examples are presented from both industry and academia.

The Forum starts with an introduction from **Stefan Rusu (Intel)** who summarizes the trends and challenges in using multiple clock and power domains in modern processors. **Phil Restle (IBM)** discusses several practical implementations that illustrate how the strong desire for more power and clock domains must in practice be tempered with the realities of design complexity, finite wiring resources and the critical importance of high-quality power and clock distributions. **Stephen Kosonocky (AMD)** focuses on low-V_{MIN} circuit-design methods (like 8T SRAM cells), power-gating techniques for high-performance systems, on-die regulation for cache design, proper start-up power sequencing and voltage translation for signals between voltage planes. **Elad Alon (UC Berkeley)** shows that the slow adoption of multi-supply designs is due to the impedance degradation caused by heavily partitioned package power planes. He also discusses possible approaches to alleviate the impedance degradation by using on-die noise suppression or active regulation to lower the impedance of each of the power grids. **Radu Marculescu (CMU)** addresses the energy optimization in multiprocessor systems-on-chip using voltage-frequency islands and a network-on-chip communication approach. A globally asynchronous, locally synchronous (GALS) design methodology achieves low power consumption and design modularity. **Masayuki Ito (Renesas)** presents a multi-power-domain implementation for a mobile WCDMA/GPRS processor. He covers isolation techniques, layout topology examples, power-on rush-current reduction, design flow for multi-power-domain, and CAD tool support. **Rob Aitken (ARM)** describes homogeneous- and heterogeneous-core systems, cache architectures and methods for voltage scaling. Silicon results for several design approaches at the 40nm node are compared and their implications for both hard- and soft-IP delivery are discussed.

The forum concludes with a 40-minute question and answer session with all seven of the presenters in a panel format with an opportunity to discuss the presented material. This all-day Forum encourages open exchange in a closed workshop. Attendance is limited and pre-registration is required. Coffee breaks and an in-room lunch are provided, to allow a chance for participants to interact with the Forum presenters.

Forum Agenda

Time	Topic
8:00	Breakfast
8:30	**Multi-Domain Design Overview** **Stefan Rusu**, *Intel, Santa Clara, CA*
9:20	**Multi-domain Design and Hardware Experiences** **Phil Restle,** *IBM, Yorktown Heights, NY*
10:10	Break
10:30	**Low-V_{MIN}-Circuit Design Techniques for Low Active and Standby Power: A Circuit and System Level Perspective** **Stephen Kosonocky,** *AMD, Fort Collins, CO*
11:20	**Supply Impedance Issues and Control in Multi-Supply Processors** **Elad Alon,** *University of California, Berkeley, CA*
12:10	Lunch
1:00	**milliJoules for 1000 Cores: Energy-Efficient Multiprocessor Systems-on-Chip Using Voltage-Frequency Islands** **Radu Marculescu,** *Carnegie Mellon University, Pittsburgh, PA*
1:50	**Multi-Power-Domain Mobile-Processor Design** **Masayuki Ito,** *Renesas, Toyko, Japan*
2:40	Break
3:00	**Adaptive Methods and Embedded IP –Architecture and Circuit Challenges** **Rob Aitken,** *ARM, Sunnyvale, CA*
3:50	Panel Discussion
4:30	Conclusion

F7: Clock Synthesis Design

Organizer/Chair: **Jan Craninckx,** *IMEC, Leuven, Belgium*

Committee: **Ivan Bietti,** *STMicroelectronics, Grenoble, France*
Michael Flynn, *University of Michigan, Ann Arbor, MI*
Kari Halonen, *Technical University of Helsinki, Helsinki, Finland*
Peter Kinget, *Columbia University, New York, NY*
Katsu Nakamura, *Analog Devices, Wilmington, MA*

One of the most critical and challenging functions present in almost every electronic system is clock or frequency generation. High-performance clocks or precise frequency references are needed in digital systems, data converters, serial data communications and wireless transceivers, to just name a few examples. The phase-locked loop (PLL) concept has been around for many decades and still forms the core of most frequency-synthesis and clock-generation solutions. Increased performance and functionality requirements are driving significant innovations to the basic PLL structure and implementation. Continued scaling of semiconductor devices are further leading toward more digitally oriented realizations with significant circuit and architectural innovations.

This forum will present recent developments in frequency synthesis and clock generation by leading experts in this field. First, advanced techniques for the design of fractional-N PLLs will be discussed, that allows phase modulation and accurate methods for spur and noise suppression. The next three talks will focus on all-digital PLLs, focusing on implementation of critical building blocks as well as on full system performance for wireless communication applications. The last two presentations will cover the challenge of low-jitter clock generation for data-converter applications.

The forum will conclude with a panel discussion where the attendees have the opportunity to ask questions and to share their views. Attendance is limited and pre-registration is required. This all-day forum encourages open information exchange. The targeted participants are circuit designers and system engineers who need to learn how the latest advances in high-performance clock generation and frequency synthesis will impact their future designs.

Forum Agenda:

Time	Topic
8:00	Breakfast
8:40	**Welcome and Introduction** **Jan Craninckx,** *IMEC, Leuven, Belgium*
8:45	**Calibration Tourniquets for Fractional-N Synthesizers** **Satoshi Tanaka,** *Renesas Technology, Komoro, Japan*
9:30	**Enhancement Techniques for Fractional-N PLLs** **Ian Galton,** *University of California, San Diego, CA*
10:15	Break
10:45	**High-Performance Time-to-Digital Conversion** **Mike Perrot,** *SiTime, Sunnyvale, CA*
11:30	**Fully Integrated All-Digital PLL Architectures for Wideband Fractional Frequency Synthesis** **Francesco Svelto,** *University of Pavia, Pavia, Italy*
12:15	Lunch
1:45	**Architecture Trends and Requirements of RF PLLs for Wireless** **Bogdan Staszewski,** *Texas Instruments, Dallas, TX*
2:30	**Clock Challenges for GHz ADCs** **Robert Neff,** *Agilent Technologies, Santa Clara, CA*
3:15	Break
3:45	**Analysis and Design of Low-Jitter Clocks for High-Resolution ADCs** **Ahmed M.A. Ali,** *Analog Devices, Greensboro, NC*
4:30	Panel Discussion
5:00	Conclusion

F8: Integrated Neural Interfaces

Organizer: **Reid Harrison,** *University of Utah, Salt Lake City, UT*

Committee: **Timothy Denison,** *Medtronic, Minneapolis, MN*
Roland Thewes, *Qimonda, Munich, Germany*
Albrecht Rothermel, *University of Ulm, Ulm, Germany*

While interfaces to the brain were recently confined to science fiction, cochlear implants and deep-brain stimulators are now becoming commonplace. This forum will cover circuit and material technology used to stimulate and record signals from the nervous system. Issues familiar to many circuit designers – low noise design, micropower design, partitioning between digital and analog circuits – will be recurring themes throughout this all-day forum.

Applications for integrated electronics in biomedical devices grow more numerous every year. This forum is designed to be accessible to circuit designers of any background; previous experience in biology or medical devices is not necessary. The speakers will present cutting-edge work from both industry and academia.

The forum will begin with an introduction to the burgeoning field of brain-machine interfaces. **Krishna Shenoy** (Stanford U) will describe state-of-the-art electrophysiological techniques and signal-processing algorithms used to extract control signals from the brain for guiding prosthetic devices.

The next talk, by **Stuart Cogan** (EIG Laboratories), explores the nature of electrodes used to record electrical activity from neural tissue. The properties of the electrode-tissue interface have important consequences on circuit design for both recording and stimulation applications. Conversely, circuit design for biomedical applications requires careful attention to safety issues. **Maurits Ortmanns** (U Ulm) will discuss the design of integrated circuits for the stimulation of the retina with a focus on safety considerations. The design of electronics for implantable medical devices poses many constraints (e.g., size, power dissipation, and telemetry bandwidth) for circuit designers. **Reid Harrison** (U Utah) will outline several prominent design trade-offs that result from these unique challenges, including the trade-off between power and noise in biosignal amplifiers, and the optimization of wireless inductive power links.

In addition to electrical recording and stimulation, modern microsystems are beginning to incorporate microfluidics for a complete electrochemical interface to the nervous system. **Ken Wise** (U Michigan) will describe recent advances in MEMS devices, integrated electronics, and biocompatible packaging for a wide range of therapeutic applications. Miniaturization may also be facilitated through the use of wafer-level integration. **Chris Van Hoof** (IMEC) will present packaging and integration technologies for wearable and implantable health-care devices, as well as ultra-low-power front-end electronics for microwatt biopotential recording.

While some neural interface technologies are still in the research and development stage, others are mature medical products that routinely improve the lives of thousands of people. **Timothy Denison** (Medtronic) will describe commercial deep-brain stimulation (DBS) technology that provides therapy for the treatment of movement disorders such as Parkinson's disease. While current clinical systems operate in a closed-loop manner, there is ongoing research to create a closed-loop system by add sensing capabilities and on-board algorithms to the stimulator, with the goal of helping physicians provide more optimized therapy. A survey of solutions being explored in early-stage research devices will be presented.

This all-day forum encourages open interchange and discussion. Attendance is limited and pre-registration is required. Breakfast, lunch, and coffee breaks will be provided to allow for a chance for participants to mingle and discuss the issues.

Forum Agenda

Time	Topic
8:00	Breakfast
8:30	**Welcome and Overview** **Reid Harrison,** *University of Utah, Salt Lake City, UT*
8:40	**High-Performance Cortically-Controlled Prosthesis Design** **Krishna Shenoy,** *Stanford University, Stanford, CA*
9:30	**Electrode and Electrode-Tissue Interface Properties Relevant to the Design of Implanted Microelectronic Devices** **Stuart Cogan,** *EIC Laboratories, Norwood, MA*
10:20	Break
10:35	**Safety Issues and Circuit Implementation for Retinal Stimulators** **Maurits Ortmanns,** *University of Ulm, Ulm, Germany*
11:25	**Wireless Neural Recording Systems: Design Trade-Offs at the Circuit and System Levels** **Reid Harrison,** *University of Utah, Salt Lake City, UT*
12:15	Lunch
1:30	**Wireless Implantable Microsystems: Electronic Interface to the Nervous System** **Ken Wise,** *University of Michigan, Ann Arbor, MI*
2:20	**Ultra-Low-Power Biopotential Circuits and Their Integration in Wearable and Implantable Interfaces** **Chris Van Hoof,** *IMEC, Leuven, Belgium*
3:10	Break
3:30	**Technology Considerations for Adaptive Neuromodulation Systems** **Timothy Denison,** *Medtronic, Minneapolis, MN*
4:20	Panel Discussion All speakers and committee members
4:50	Conclusion

HOW TO REGISTER FOR ISSCC

Advance Registration: ISSCC offers online advance registration. This is the fastest, most convenient way to register and will give you immediate email confirmation of whether or not you have a place in the events of your choice. If you register online, which requires a credit card, your registration is processed while you are online, and your email confirmation can be printed for your recordkeeping. To register online, go to the ISSCC website at www.isscc.org or go directly to the registration website at https://www.yesevents.com/isscc

You can also register in advance by fax or mail using the "2009 IEEE ISSCC Registration Form". All payments must be made in U.S. Dollars, by credit card or check. Checks must be made payable to "ISSCC 2009". It will take several days before you receive email confirmation when you register using the form. **Registration forms received without full payment will not be processed until payment is received at YesEvents.**

For those who wish to register by fax or mail, the Registration Form can be downloaded from the ISSCC website. Please read the explanations and instructions on the back of the form carefully.

The deadline for registering at the Early Registration rates is 11:59 pm Pacific Time **January 9, 2009.** After January 9th, and on or before 6:00 am Pacific Time January 26, 2009, registrations will be processed **only at the Late Registration rates. After January 26th, you must register onsite at the onsite rates.** Because of limited seating capacity in the meeting rooms and hotel fire regulations, **onsite registrations may be limited**. Therefore, you are urged to register early to ensure your participation in all aspects of ISSCC 2009.

Onsite Registration: The Onsite Registration and Advance Registration Pickup Desks at ISSCC 2009 will be located in the Yerba Buena Ballroom Foyer at the San Francisco Marriott. All participants, except as noted below, should register or pick up their registration materials at these desks as soon as possible. **Pre-registered Presenting Authors and all pre-registered members of the ISSCC Program Committee must go directly to Golden Gate A3 to collect their conference materials.**

REGISTRATION DESK HOURS:

Saturday,	February 8	4:00 PM to 7:00 PM
Sunday,	February 9	6:30 AM to 8:00 PM
Monday,	February 10	6:30 AM to 3:00 PM
Tuesday,	February 11	8:00 AM to 3:00 PM
Wednesday,	February 12	8:00 AM to 3:00 PM
Thursday,	February 13	7:00 AM to 1:00 PM

All students must present their Student ID at the Conference Registration Desk to receive the student rates. Those registering at the IEEE Member rate must provide their IEEE Membership number.

Payments by credit card will appear on your monthly statement as a charge from ISSCC.

Membership saves you on ISSCC registration

Take advantage of reduced ISSCC registration fees by using your IEEE membership number to activate the rate.

If you're an IEEE member and have forgotten your member number, simply phone IEEE at 1(800) 678-4333 and ask. IEEE membership staff will take about 2 minutes to look up your number for you. If you come to register onsite without your membership card, you can phone IEEE then, too. Or you can request a membership number look-up by email. Use the online form at: www.ieee.org/web/aboutus/help/member_technical.html

If you're not a member, consider joining before you register to save on your fees. Join online at www.ieee.org/join at any time day or night and you'll receive your member number by email confirmation.

Be involved all year long.

You come to ISSCC once a year to network and keep informed about your field. Stay informed all year by joining the IEEE Solid-State Circuits Society. SSCS brings you

- The inaugural Solid-State Circuits Magazine quarterly
- One free trial year of the new IEEE Nanotechnology Magazine

- Local Chapter meetings
- JSSC online each month in Xplore
- Four other conferences throughout the year and around the world
- Access to all the articles from those same four conferences in Xplore
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- The opportunity to subscribe to related co-sponsored publications on Computer Aided Design of ICs and Systems, Display Technology, Semiconductor Manufacturing, Sensors, Technology Management, VLSI Systems, and Applied Earth Observations

Society membership costs $24 with your IEEE membership. Use the onsite membership registration desk outside the Willow Room at the hotel to renew or join. This desk is staffed during the same hours as ISSCC registration from Saturday through Wednesday, but closes at 10 am on Thursday.

Cancellations/Adjustments: Prior to 6:00 am Pacific Time **January 26th, 2009,** conference registration can be cancelled and fees paid will be refunded (less a processing fee of $75). Registration category or credit card used can also be changed (for a processing fee of $35). Send an email to the registration contractor at ISSCCinfo@yesevents.com to cancel or make other adjustments. No refunds will be made after 6:00 am Pacific Time January 26th, 2009. Paid registrants who do not attend the conference will be sent all relevant conference materials.

HOW TO MAKE HOTEL RESERVATIONS

ISSCC participants are urged to make their hotel reservations at the San Francisco Marriott online. To do this, go to the conference website at www.isscc.org and click on the Hotel Reservation link to the San Francisco Marriott. **In order to receive the special group rates you will need to enter the following Group Codes: IEEIEEA for a single/double; IEEIEEB for a triple; IEEIEEC for a quad.** The special ISSCC group rates are $229/single; $229/double; $249/triple; and $269/quad (per night plus tax). In addition, we have negotiated that ISSCC attendees staying at the Marriott receive **in-room Internet access for free**. All online reservations require the use of a credit card. Online reservations are confirmed immediately, while you are online. You should print the page containing your confirmation number and reservation details and bring it with you when you travel to ISSCC.

For those who wish to make hotel reservations by fax or mail, the Hotel Reservation Form can be downloaded from the ISSCC website. Be sure to fill in your correct email address and fax number if you wish to receive a confirmation by email or fax. The reservation fax number is 415-486-8153.

For those who must make hotel reservations by telephone, call 888-575-8934 (US) or 415-896-1600 and ask for "Reservations." **You must also provide the appropriate Group Code listed above when making your reservation.**

Once made and confirmed, your reservation can be changed online or by calling the Marriott at 415-896-1600 (ask for "Reservations"); or by faxing your change to the Marriott at 415-486-8153. Have your hotel confirmation number ready.

Hotel Deadline: Reservations must be received at the San Francisco Marriott no later than January 16, 2009 to obtain the special ISSCC rates. A limited number of rooms are available at these rates. **Once this limit is reached or after January 16th, the group rate will no longer be available and reservation requests will be filled at the best available rate.**

IMPORTANT NOTICE FOR ALL 2009 ISSCC PARTICPANTS: It is vitally important that all 2009 ISSCC participants who do not live within driving distance of San Francisco make their hotel reservations at the San Francisco Marriott, which is the conference hotel and location of all conference activities. The room rates have been negotiated based upon our need to use all available meeting space in the hotel. If we do not fill our negotiated room block, ISSCC must pay huge fees for using all of the space. This will then result in unnecessary and unpopular increases in registration fees for ISSCC in future years. Please support the Executive Committee in their attempt to keep your ISSCC registration fees reasonable. Book your room at the San Francisco Marriott hotel for ISSCC 2009.

ITEMS INCLUDED IN REGISTRATION

Events:

Technical Sessions: Registration includes admission to all technical sessions and evening sessions starting Sunday evening and continuing throughout Monday, Tuesday and Wednesday.

Technical Book Display: A number of technical publishers will have collections of professional books and textbooks on display during the Conference. These books are available for sale or to order onsite. The Book Display is in Golden Gate Hall C, located one level above the ballroom. The Book Display will be open on Monday from 12:00Noon - 6:30PM; on Tuesday from 10:00AM to 6:30PM; and on Wednesday from 10:00AM to 2:00PM.

Poster Sessions: The recent ISSCC/DAC student contest winners will display their work in poster form outside Golden Gate C. All these students will be available to discuss their posters during the Social Hour on Monday evening.

Author Interviews: Author Interviews will be held in the Atrium of the hotel, located one level above the lobby, on Monday and Tuesday. On Wednesday, they will be located in the Foyer outside the Yerba Buena Ballroom.

Social Hour: Social Hour refreshments will be available starting at 5:15 pm on Monday in Golden Gate C and the Foyer surrounding the Book Display as well as in the Atrium with the Author Interviews.

University Events: Several universities are planning social events during the Conference. A link is provided during online registration that will take you to a list of universities hosting these events so that you can send an email to indicate your interest in attending. You can also reach this list directly by going to www.isscc.org and clicking on the "University Alumni Events" link.

Publications:

Full conference registration includes:

-The **Digest of Technical Papers** in both hard copy and on CD (available for pick-up onsite beginning on Sunday at 4 pm, and during registration hours on Monday through Wednesday).

-The **ISSCC 2009 DVD** that includes the Digest and Visuals Supplement (mailed in April). **Student registration does not include the ISSCC 2009 DVD, however the DVD is available for purchase at a reduced fee for students.**

Special note for ISSCC 2009: The 800+ page Visuals Supplement book has been discontinued. These visuals are included in the ISSCC 2009 DVD which is included with conference registration for non-students and available to students at a reduced fee.

OPTIONAL EVENTS

Educational Events: Many educational events are available at ISSCC 2009 for an additional fee. There are ten 90-minute Tutorials and four all-day Forums on Sunday. There are four additional all-day Forums on Thursday as well as an all-day Short Course. See the schedule for details of the topics and times.

ISSCC Student Forum: After the successful launch of the ISSCC Student Forum last year, ISSCC will continue and expand this student activity at ISSCC 2009. This year, the ISSCC Student Forum is scheduled on Sunday, February 8th at the San Francisco Marriott hotel from 1:00 pm to 6:00 pm. Audience attendance at the Student Forum is open to both students and others, but space is limited and registration is required.

The Forum consists of a succession of 5-minute presentations by graduate students (Masters and PhD candidates) from around the world, who have been selected on the basis of a short submission concerning their ongoing research. Selection is based on the potential novelty and coherence of their proposed presentation. Note that the work described is not intended to be complete or final.

For additional information on the ISSCC Student Forum, see www.isscc.org/studentforum

Women's Networking Reception: ISSCC will be sponsoring a networking event for women in solid-state circuits on **Tuesday evening**. It is an opportunity to get to know

other women in the profession and discuss a range of topics including leadership, work-life balance, and professional development. By registering and paying a nominal fee for this event, you will receive a ticket to the reception, a chance to build new friendships, and an opportunity to expand your professional network. Please indicate on your ISSCC registration form if you plan to attend this special event, open to women only.

OPTIONAL PUBLICATIONS

All Short Course and Tutorial DVDs contain audio and written transcripts synchronized with the presentation visuals. In addition, the Short Course DVDs contain a pdf file of the presentations suitable for printing, and pdf files of key reference material.

ISSCC 2009 Publications: The following ISSCC 2009 publications can be purchased in advance or onsite:

- Additional copies of the **Digest of Technical Papers** in book or CD format.
- Additional copies of the **ISSCC 2009 DVD (mailed in April 2009).**
- **ISSCC 2009 DVD** at the special student price **(mailed in April 2009).**
- **2009 Tutorials DVD**: All ten 90 minute Tutorials **(mailed in June 2009).**
- **2009 Short Course DVD**: "Low-Voltage Analog and Mixed-Signal CMOS Circuit Design" **(mailed in June 2009)**.

Earlier ISSCC Publications: Selected publications from ISSCC 2008 and earlier can still be purchased, but some have been removed from the registration form to save space. There are several ways to purchase this material:

-Items listed on the registration form can be purchased with registration and picked up onsite at the conference.

-Visit the ISSCC website at www.isscc.org and click on the link "Purchase ISSCC Conference Materials" where you can order online or download an order form to mail or fax. For a small shipping fee, this material will be sent to you immediately and you will not have to wait until you attend the conference to get it.

-Visit the new ISSCC Publications Desk. This desk is located in the registration area and has the same hours as does conference registration. With payment by cash, check or credit card, you can pick up your materials at this desk.
The following DVDs are available:

- 2008 Tutorials: All ten 90 minute Tutorials from ISSCC 2008
- 2008 Short Course: "Embedded Power Management for IC Designers"
- 2007 Tutorials: All ten 90 minute Tutorials from ISSCC 2007
- 2007 Short Course: "Analog, Mixed-Signal and RF Circuit Design in Nanometer CMOS"
- 2006 Short Course: "Analog-to-Digital Converters"
- 2005 Short Course: "RF CMOS Circuits"
- 2004 Short Course: "Deep-Submicron Analog and RF Circuit Design"

ISSCC Replay on Demand: ISSCC is again offering a Web Access service, called **ISSCC '09 Replay on Demand**. Those who purchase ISSCC '09 Replay on Demand will be sent a Logon ID and Password that allows them access to an ISSCC website where they can view the paper presentations from ISSCC 2009, 2008 and 2007. The papers from ISSCC 2007 and 2008 will be available as soon as you get your Login, and the papers from ISSCC 2009 will be added in June 2009, at which time notification will be sent to all users. Access expires on June 30, 2010. A sample of Replay is currently available for viewing at www.isscc.org. It includes a few selected papers. There you will find that the presentation for each paper consists of all presented visuals together with cursor overlay and audio recording of the speaker.

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Golden Gate Hall
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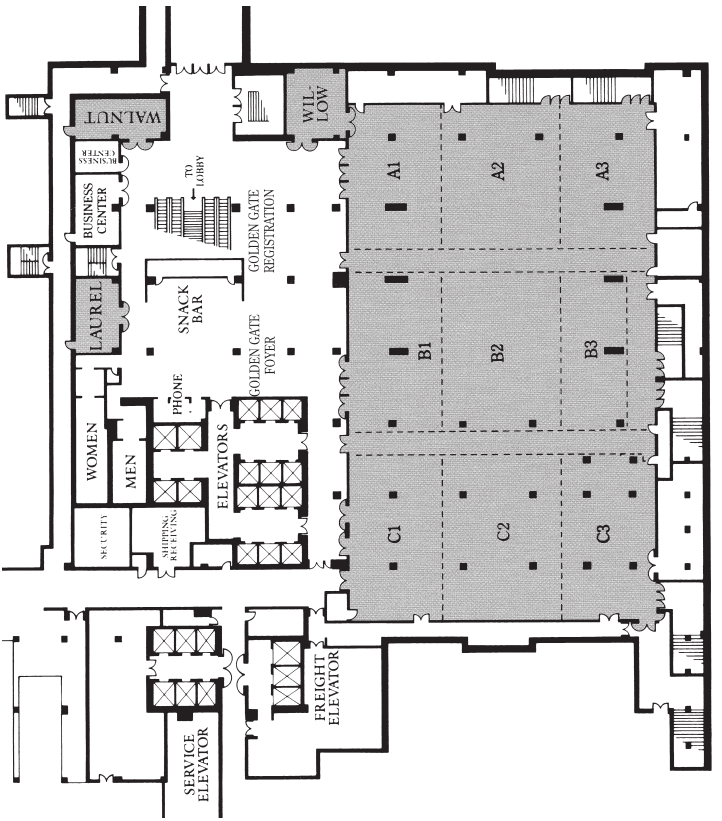

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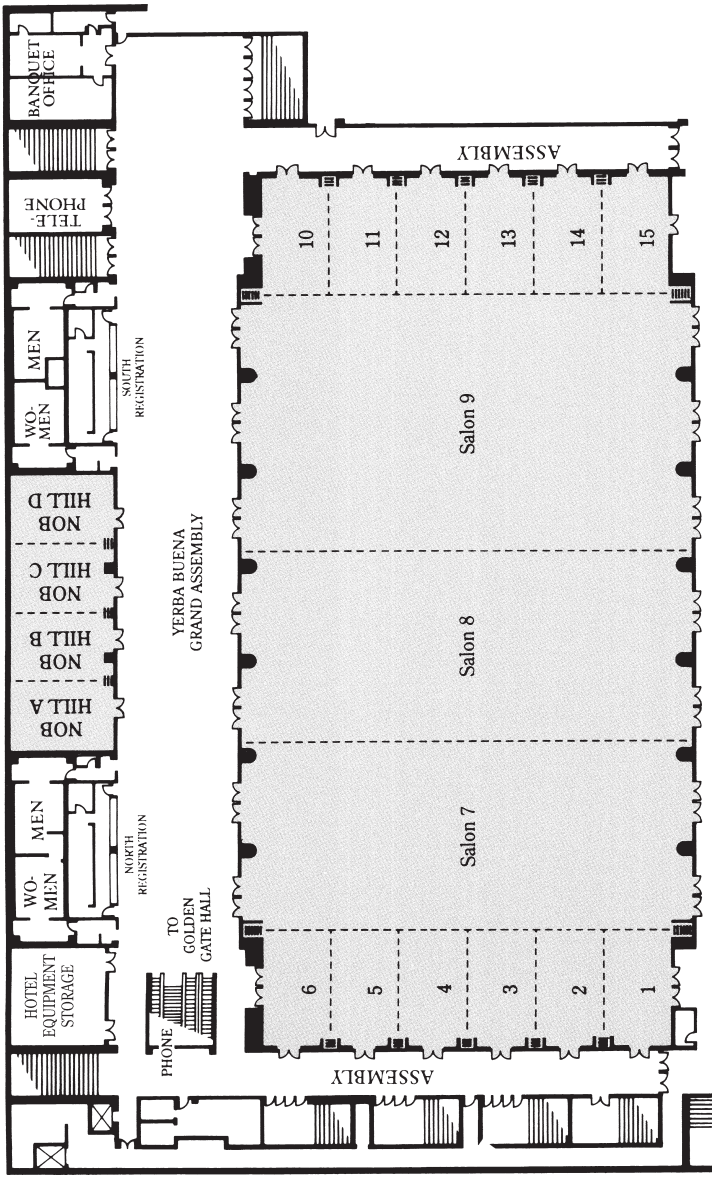

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